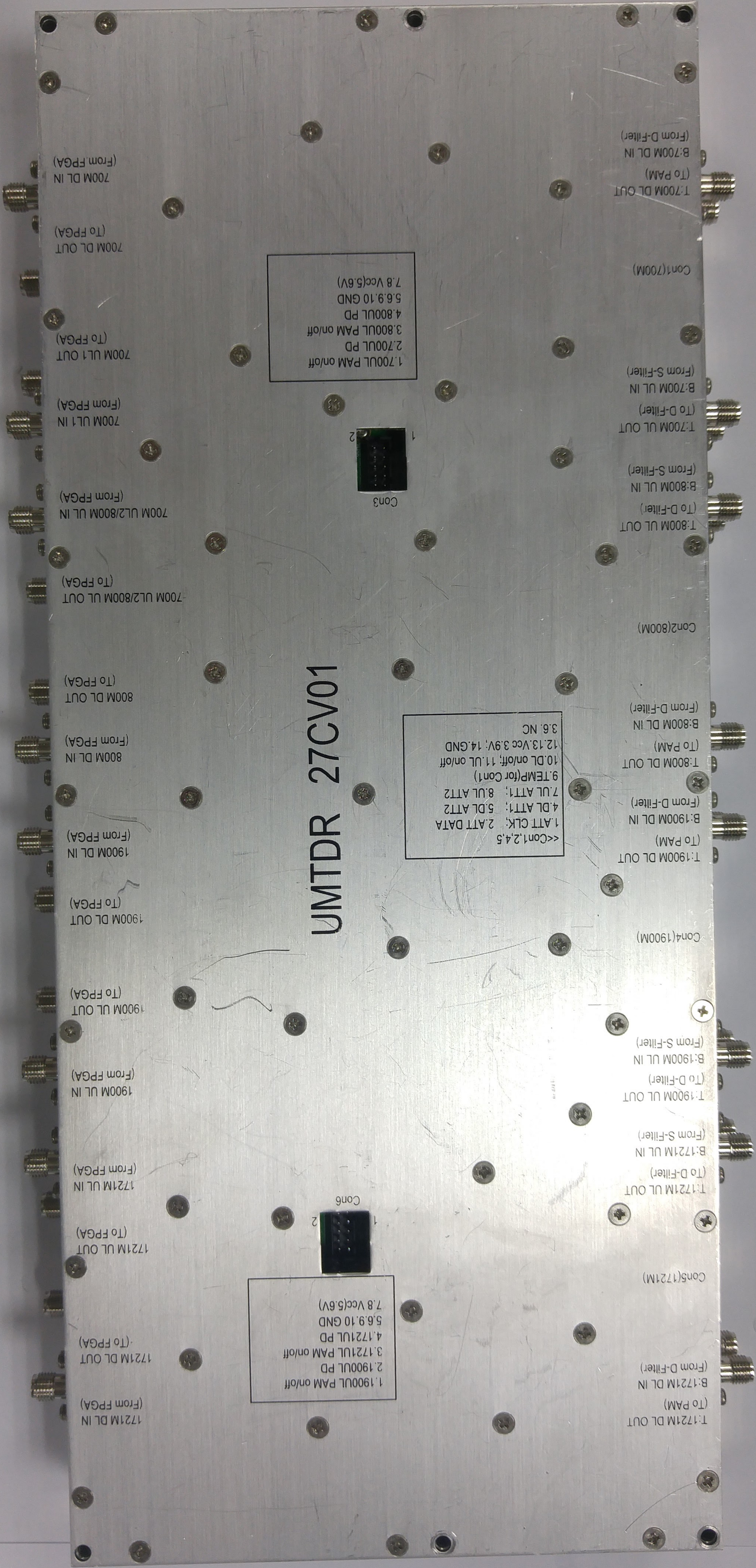




UMTDR 27CV01

1. 700UL PAM on/off
2. 700UL PD
3. 800UL PAM on/off
4. 800UL PD
5. 6.9, 10 GND
7.8 Vcc(5.6V)

Con3

<<Con1,2,4,5
1. ATT CLK; 2. ATT DATA
4. DL ATT1; 5. DL ATT2
7. UL ATT1; 8. UL ATT2
9. TEMP(for Con1)
10. DL on/off; 11. UL on/off
12. 13. Vcc 3.9V; 14. GND
3.6. NC

Con6

1. 1900UL PAM on/off
2. 1900UL PD
3. 1721UL PAM on/off
4. 1721UL PD
5. 6.9, 10 GND
7.8 Vcc(5.6V)

1. 700M DL OUT
(To PAM)
8. 700M DL IN
(From D-Filter)

Con1(700M)

1. 700M UL OUT
(To D-Filter)
8. 700M UL IN
(From S-Filter)
1. 800M UL OUT
(To D-Filter)
8. 800M UL IN
(From S-Filter)

Con2(800M)

1. 1900M DL OUT
(To PAM)
8. 1900M DL IN
(From D-Filter)
1. 800M DL OUT
(To PAM)
8. 800M DL IN
(From D-Filter)

Con4(1900M)

1. 1900M UL OUT
(To D-Filter)
8. 1900M UL IN
(From S-Filter)
1. 1721M UL OUT
(To D-Filter)
8. 1721M UL IN
(From S-Filter)

Con5(1721M)

1. 1721M DL OUT
(To PAM)
8. 1721M DL IN
(From D-Filter)

1. 700M DL OUT
(To FPGA)
8. 700M DL IN
(From FPGA)

1. 700M UL OUT
(To FPGA)
8. 700M UL IN
(From FPGA)

1. 700M UL2/800M UL OUT
(To FPGA)
8. 700M UL2/800M UL IN
(From FPGA)

1. 800M DL OUT
(To FPGA)
8. 800M DL IN
(From FPGA)

1. 1900M DL OUT
(To FPGA)
8. 1900M DL IN
(From FPGA)

1. 1900M UL OUT
(To FPGA)
8. 1900M UL IN
(From FPGA)

1. 1721M UL OUT
(To FPGA)
8. 1721M UL IN
(From FPGA)

1. 1721M DL IN
(From FPGA)
8. 1721M DL OUT
(To FPGA)

