



Annex C

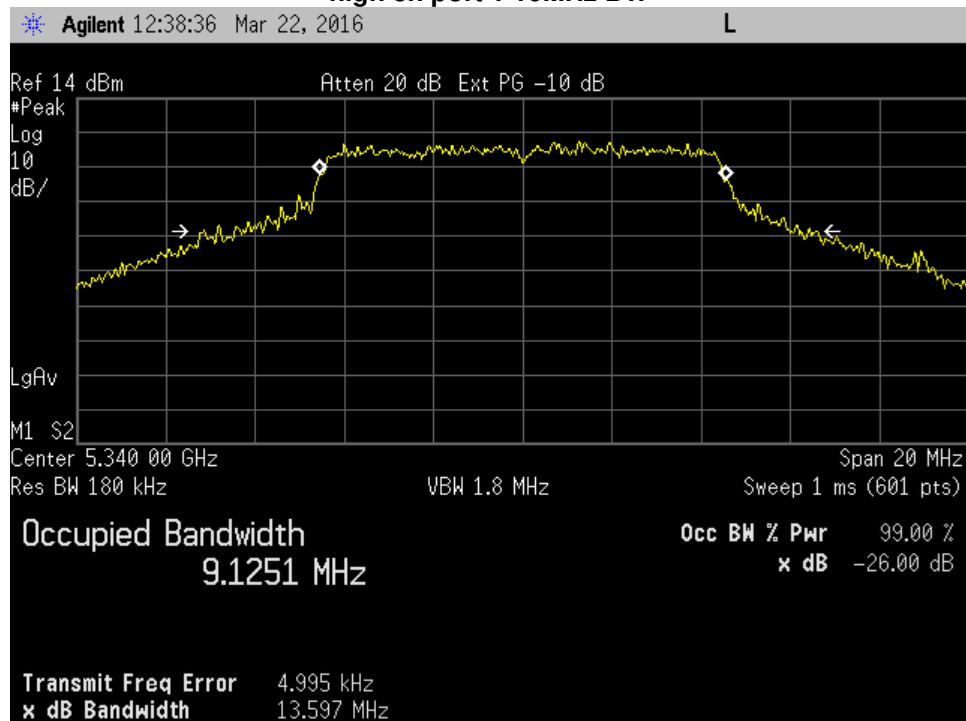
Occupied Bandwidth

UNII-2A and UNII-2C

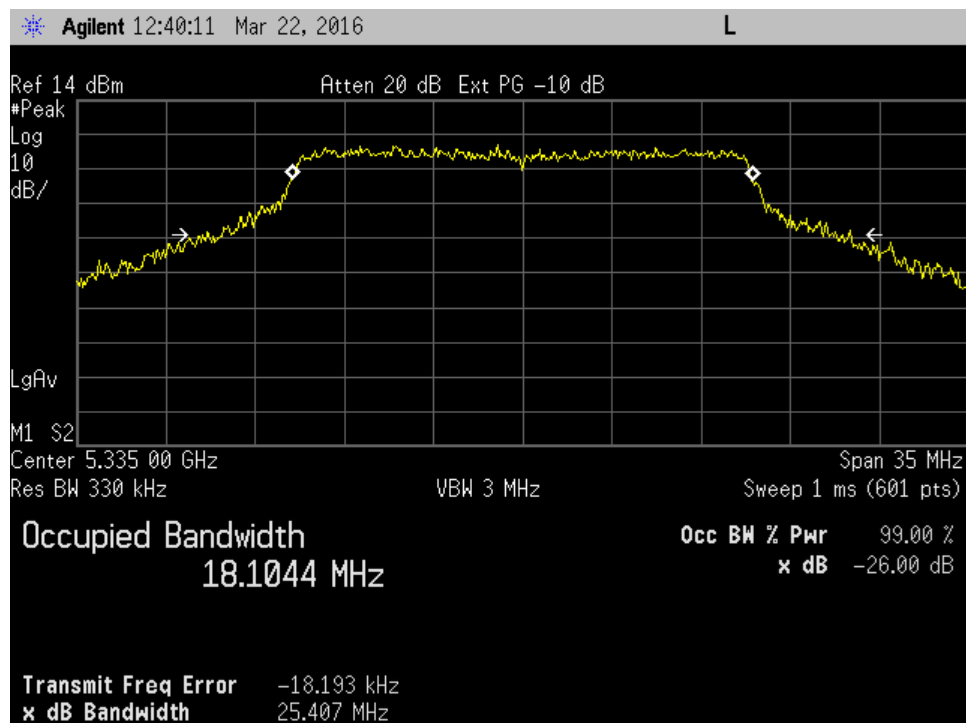


UNII-2A Occupied Bandwidth

high ch port 1 10MHz BW

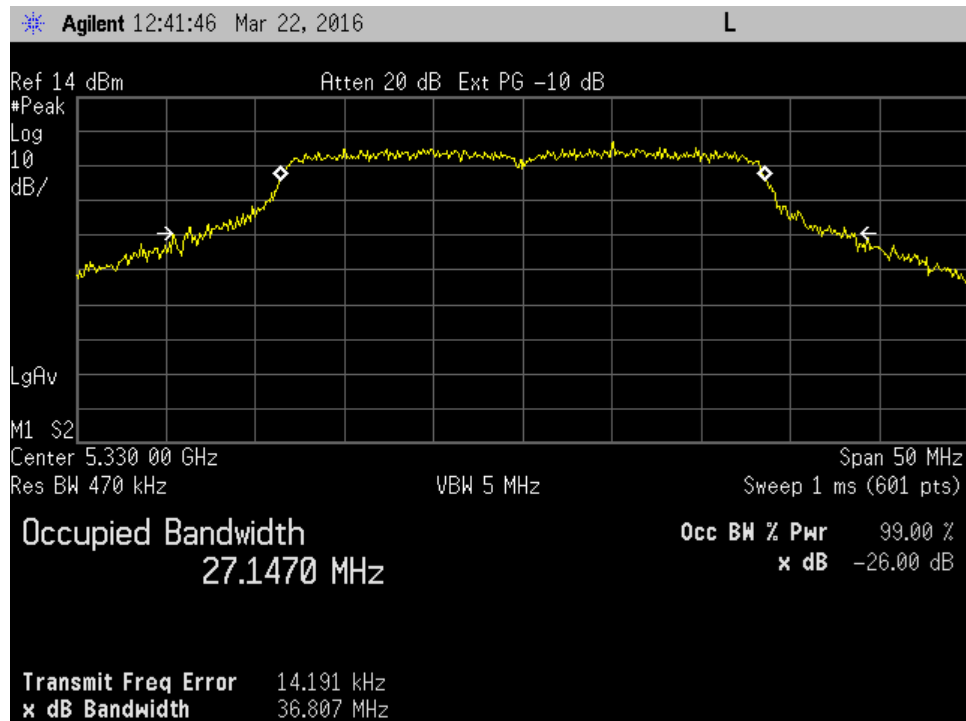


high ch port 1 20MHz BW

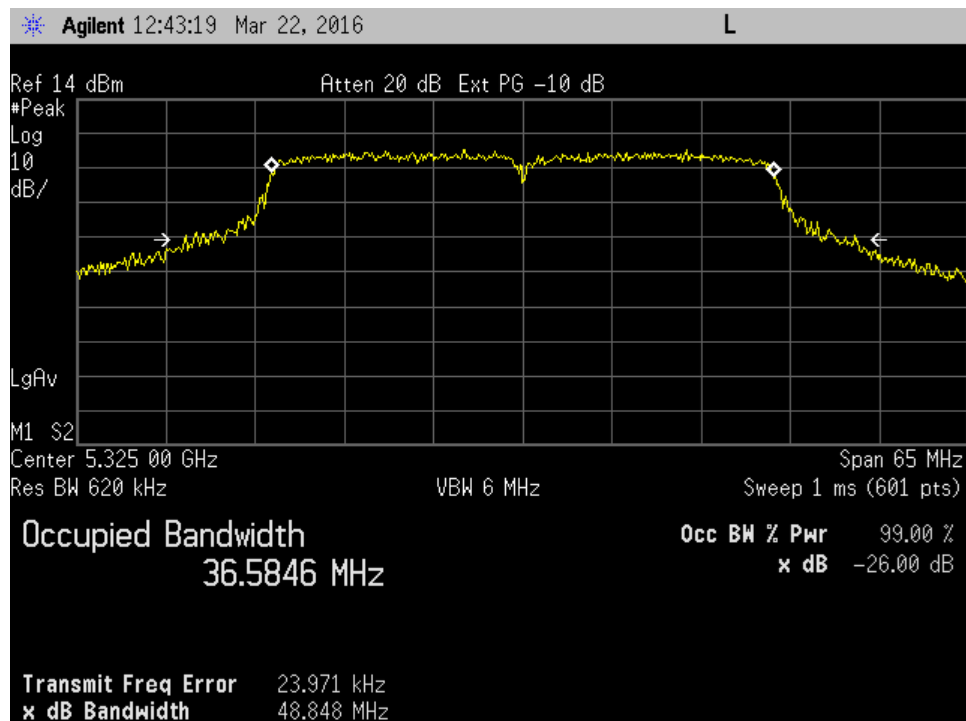




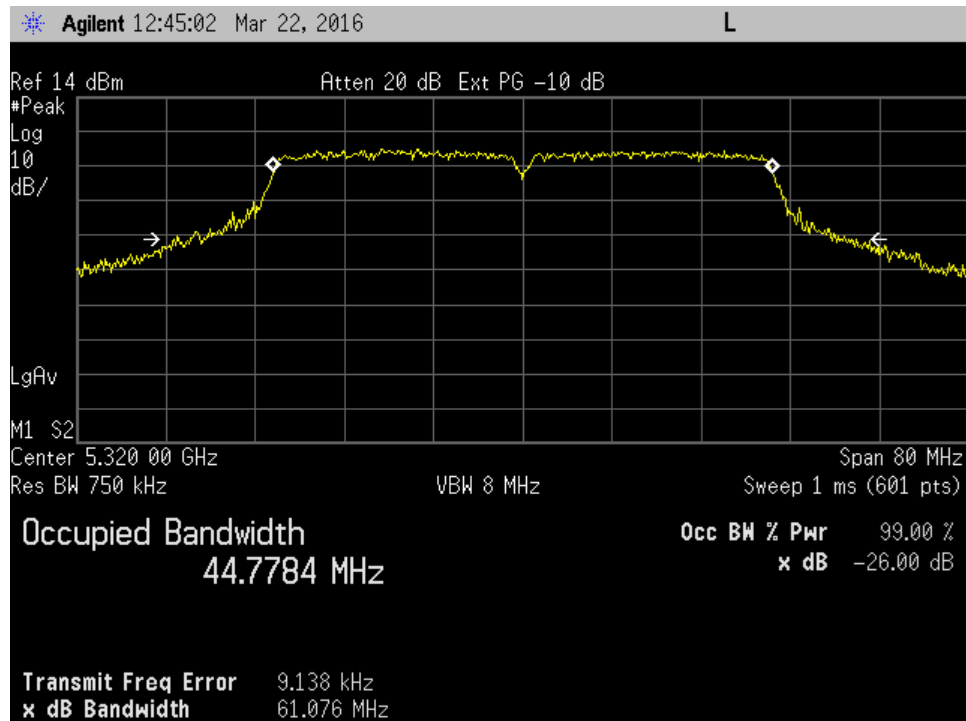
high ch port 1 30MHz BW



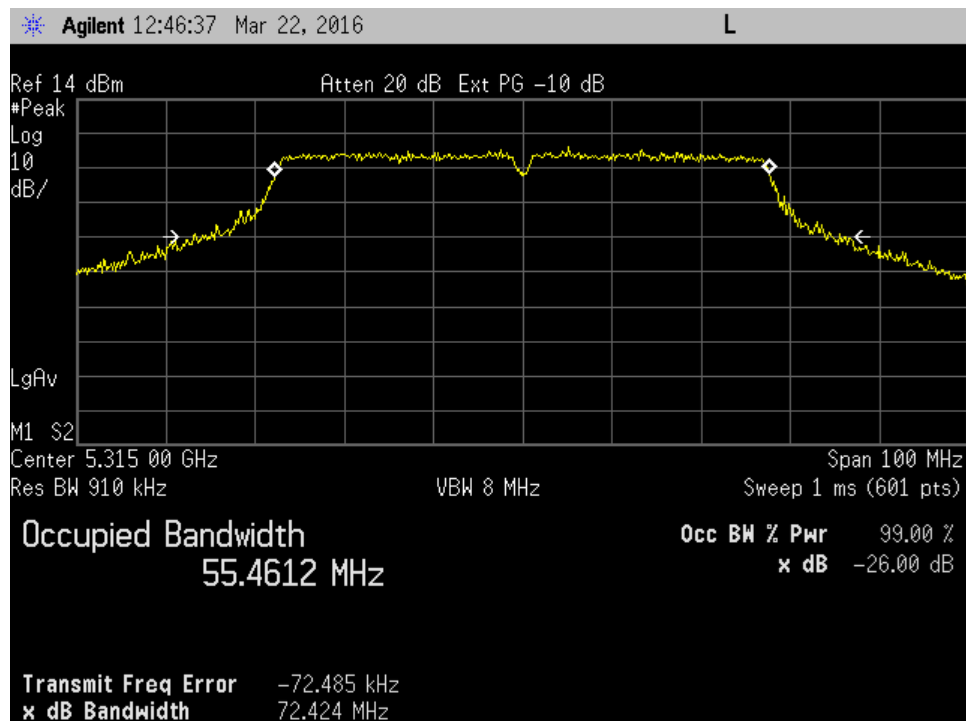
high ch port 1 40MHz BW



high ch port 1 50MHz BW

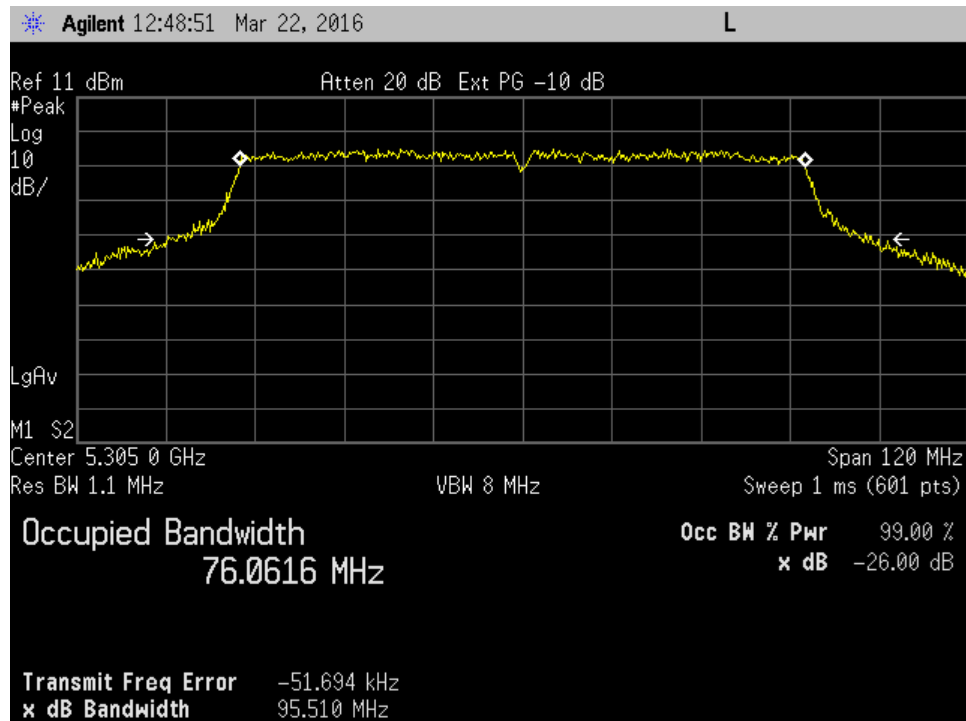


high ch port 1 60MHz BW

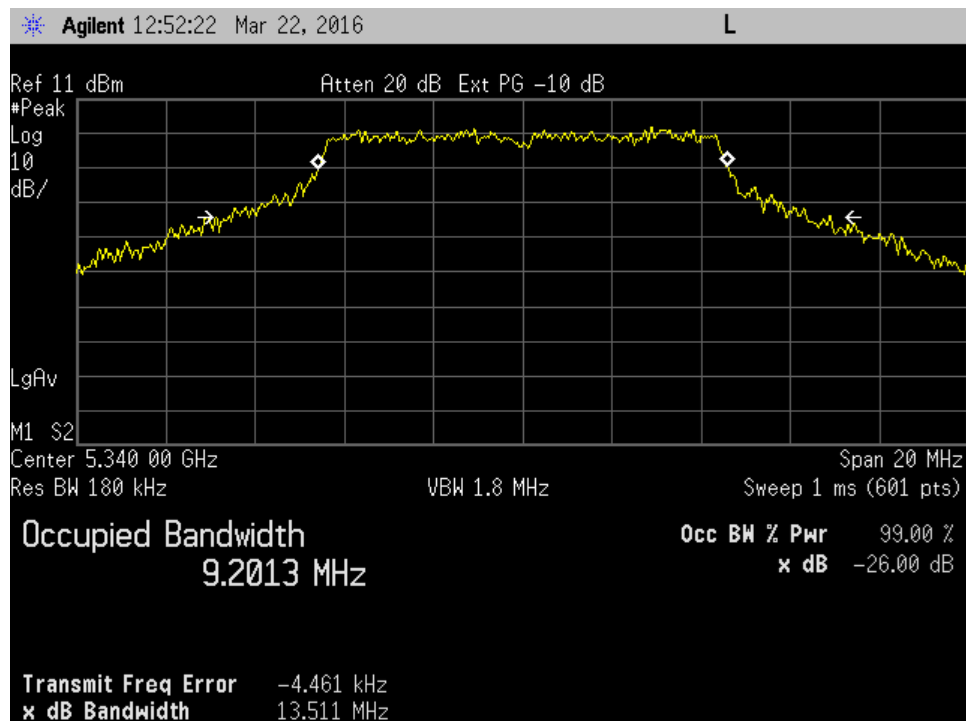




high ch port 1 80MHz BW

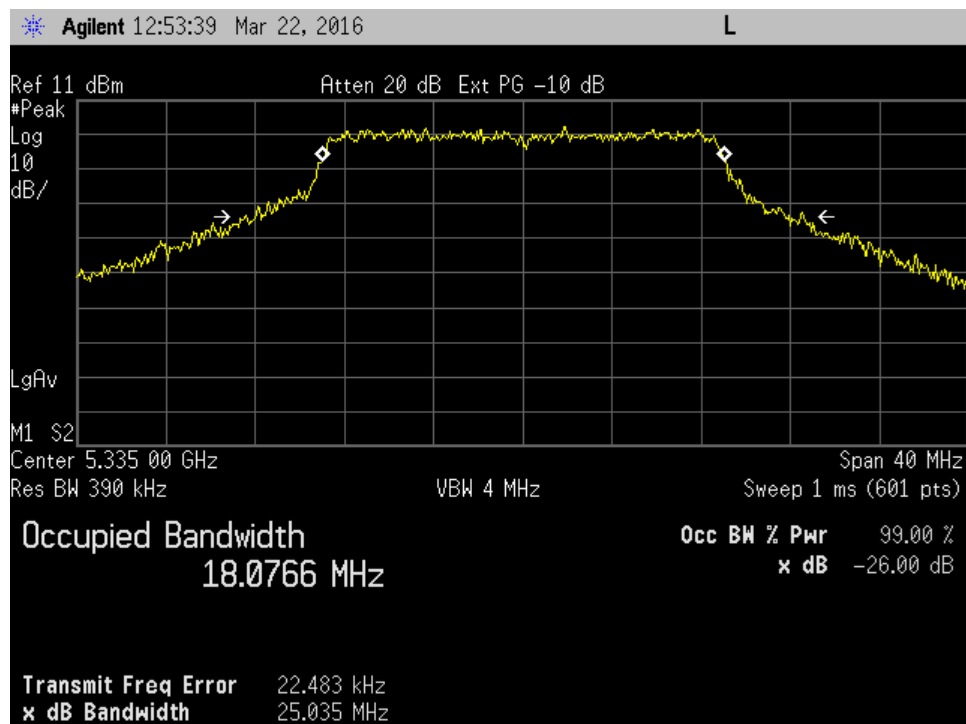


high ch port 2 10MHz BW

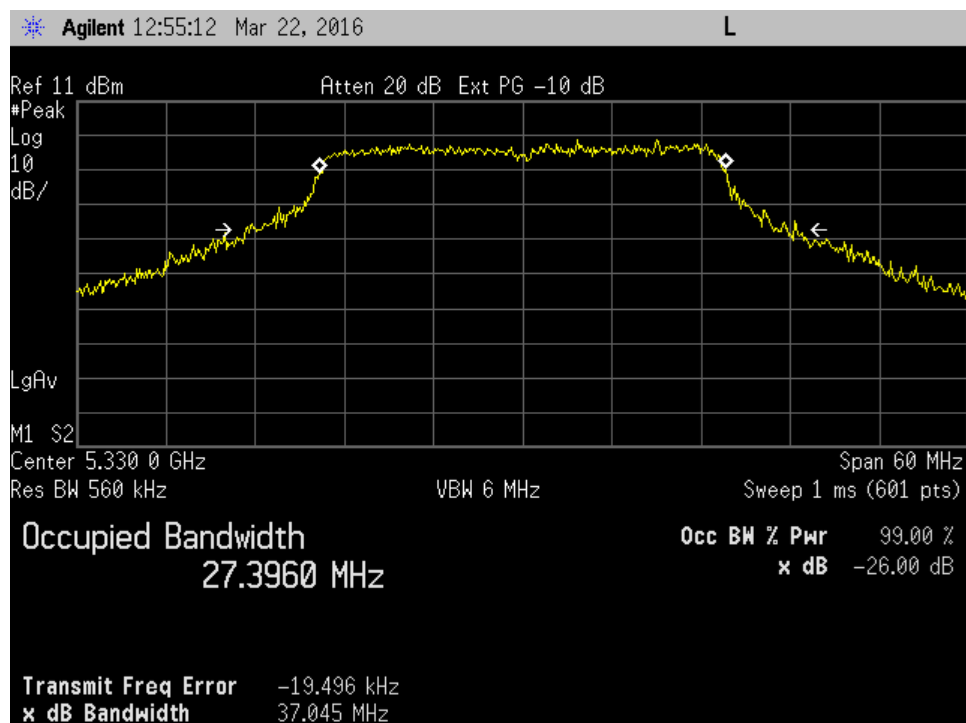




high ch port 2 20MHz BW

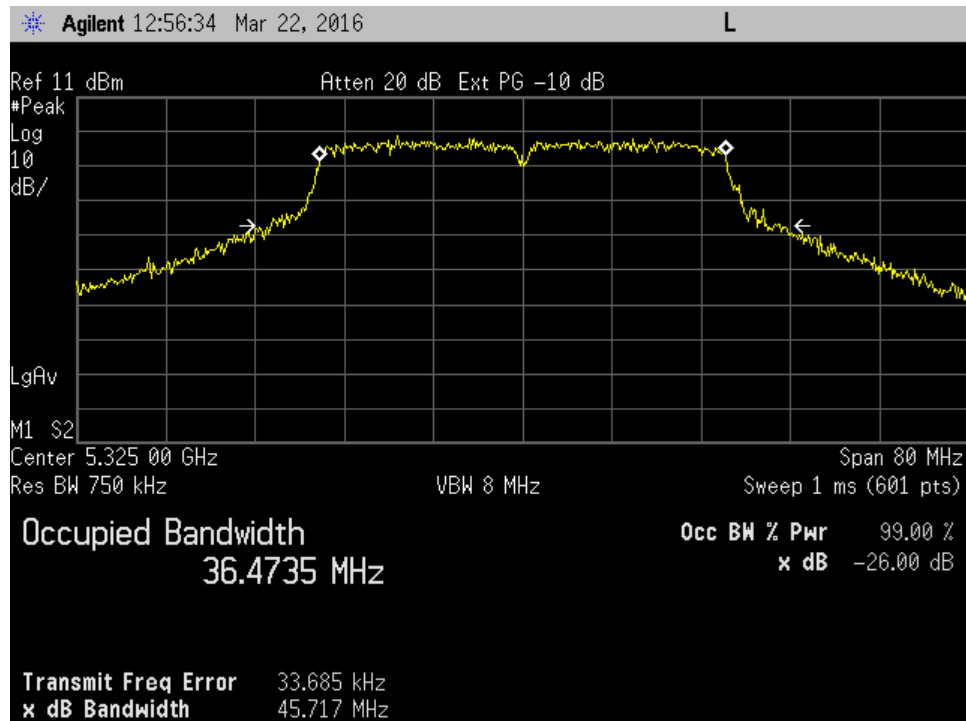


high ch port 2 30MHz BW

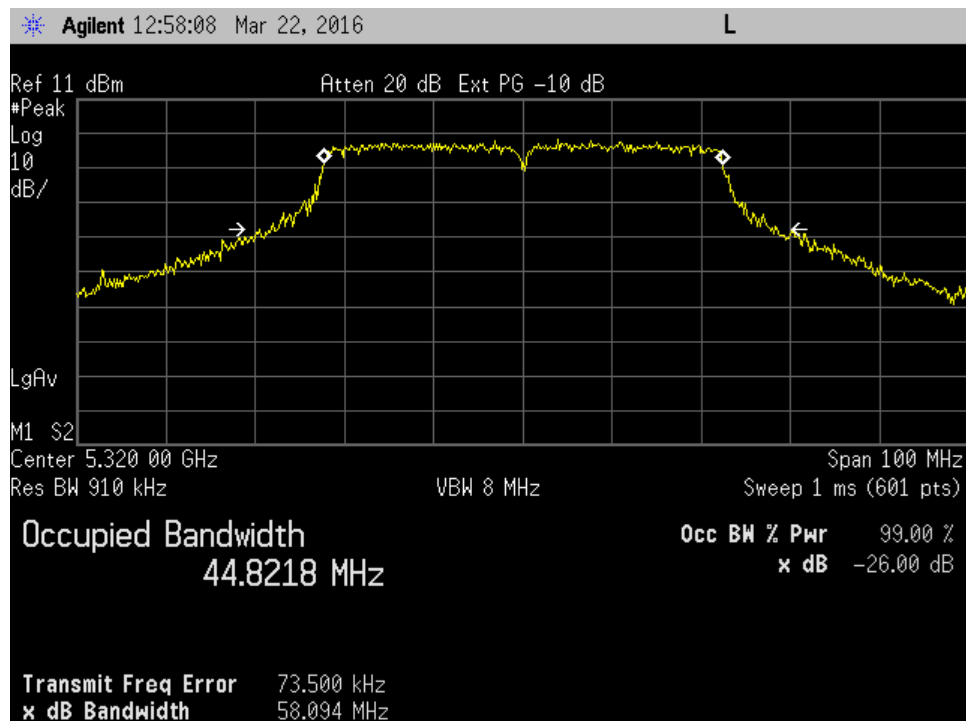




high ch port 2 40MHz BW

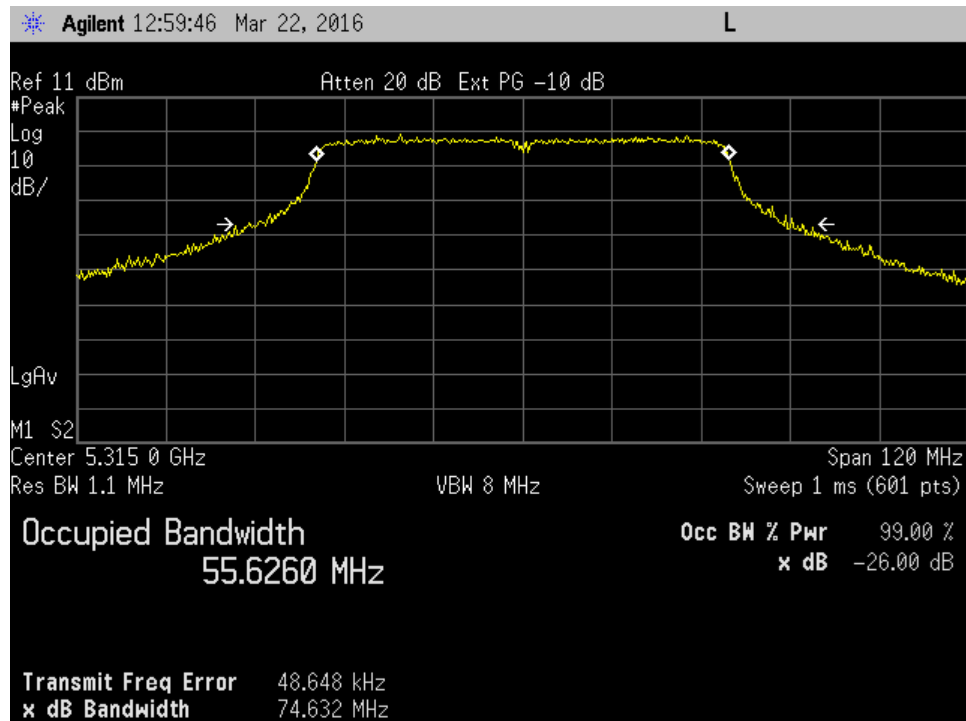


high ch port 2 50MHz BW

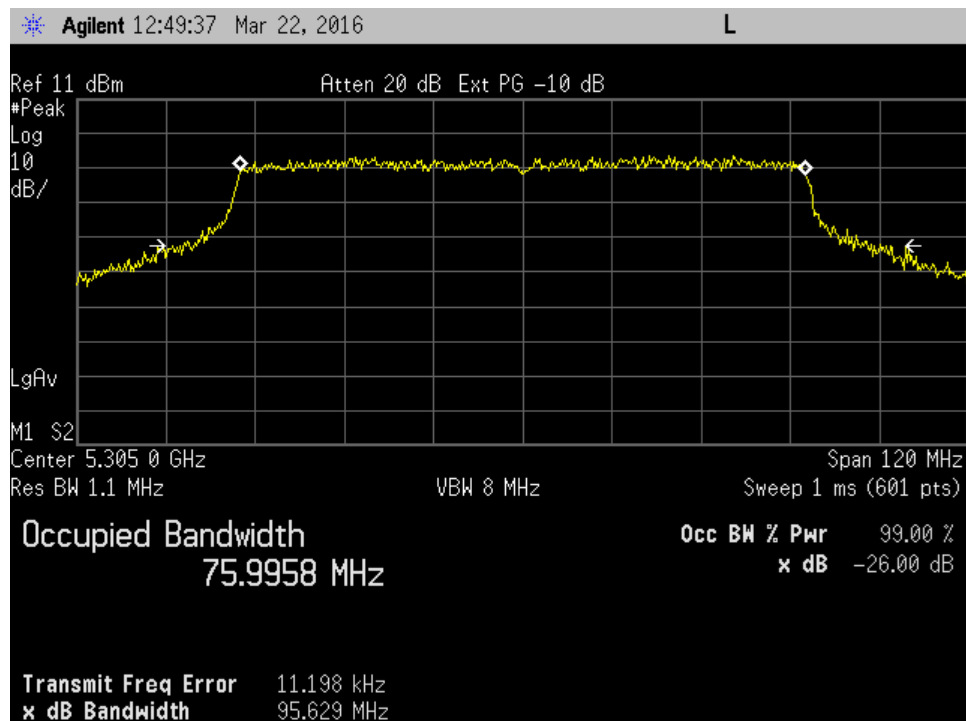




high ch port 2 60MHz BW

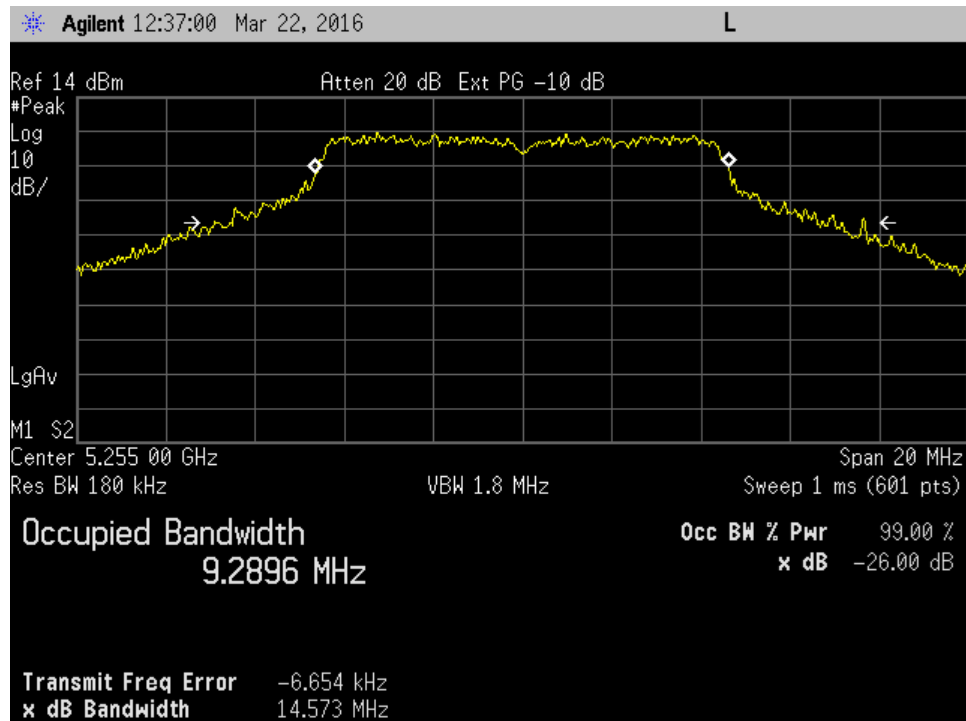


high ch port 2 80MHz BW

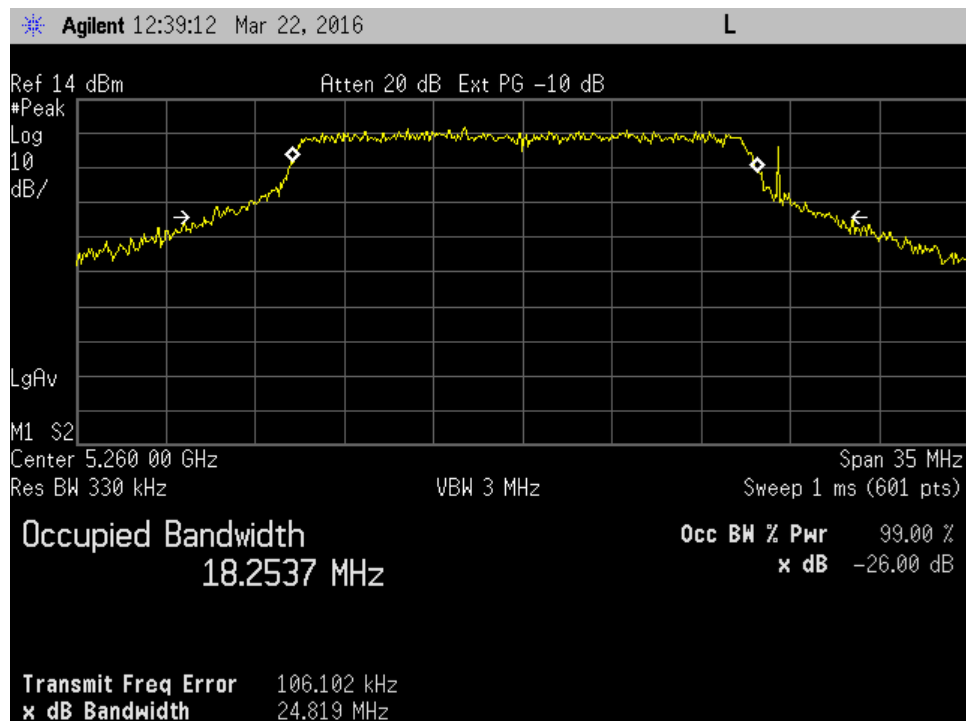




low ch port 1 10MHz BW

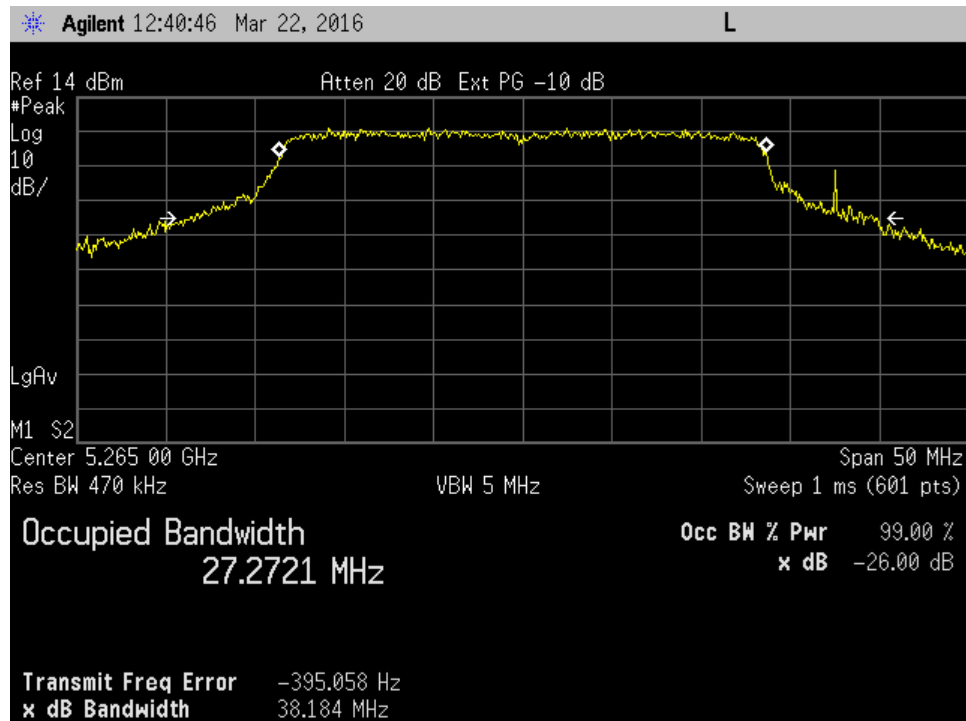


low ch port 1 20MHz BW

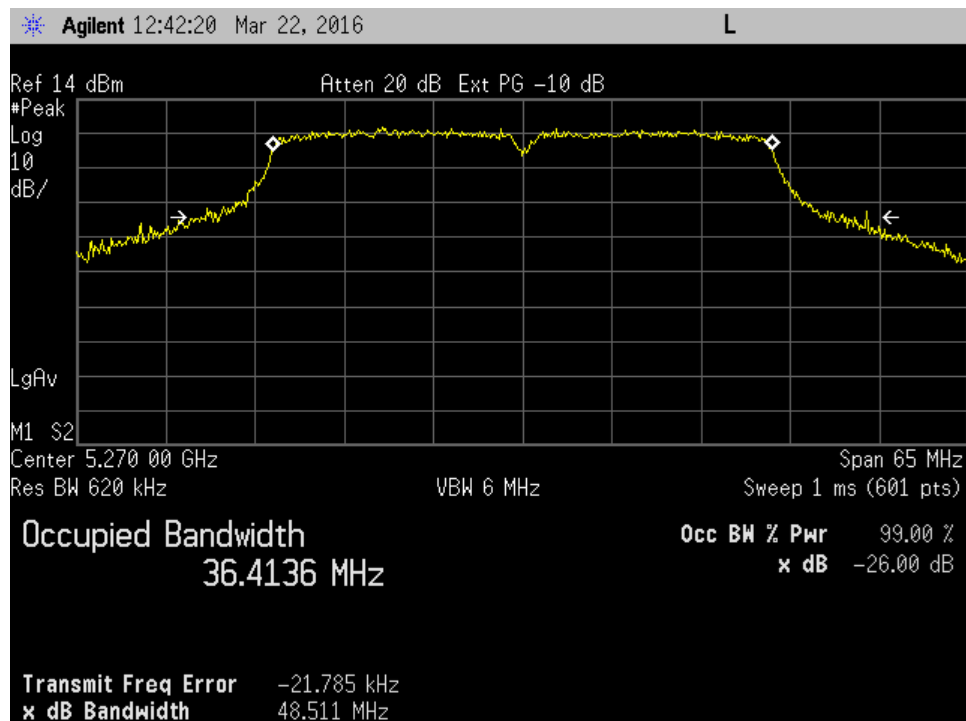




low ch port 1 30MHz BW

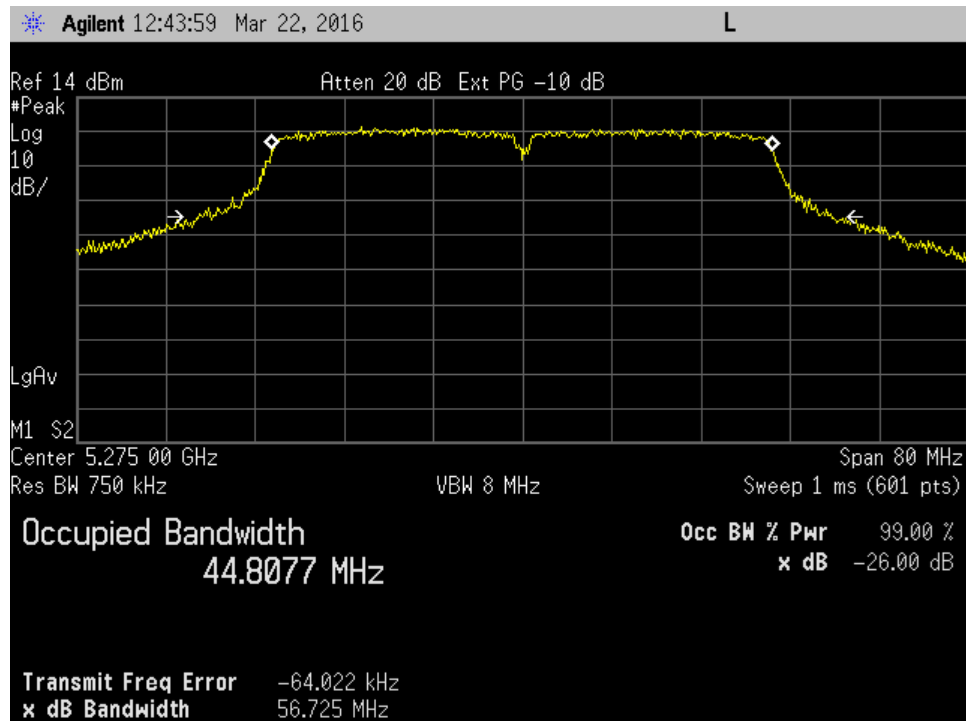


low ch port 1 40MHz BW

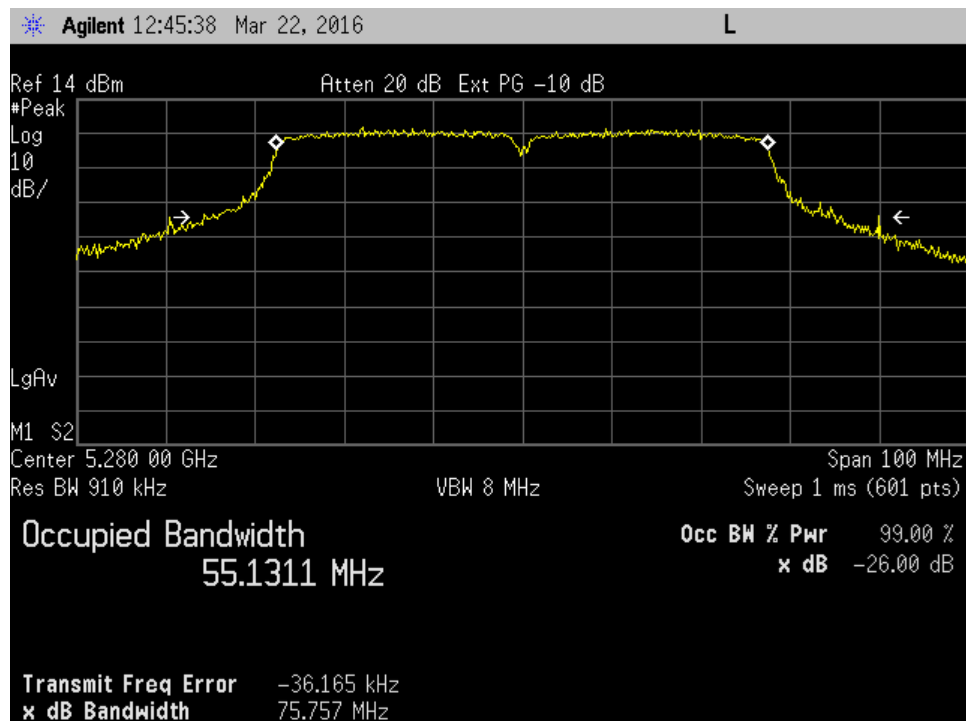




low ch port 1 50MHz BW

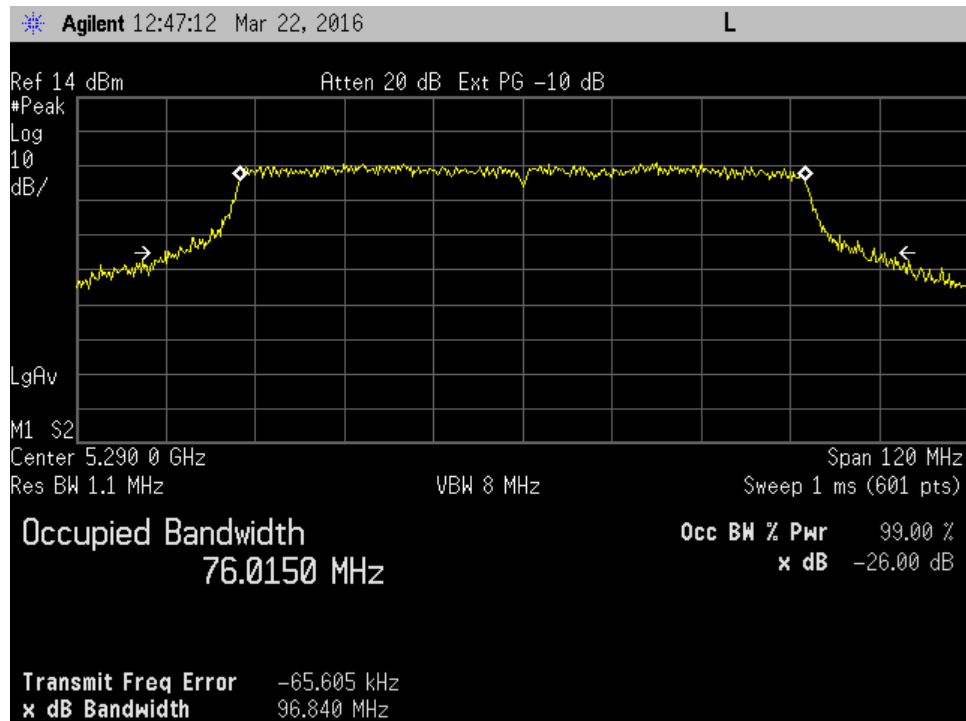


low ch port 1 60MHz BW

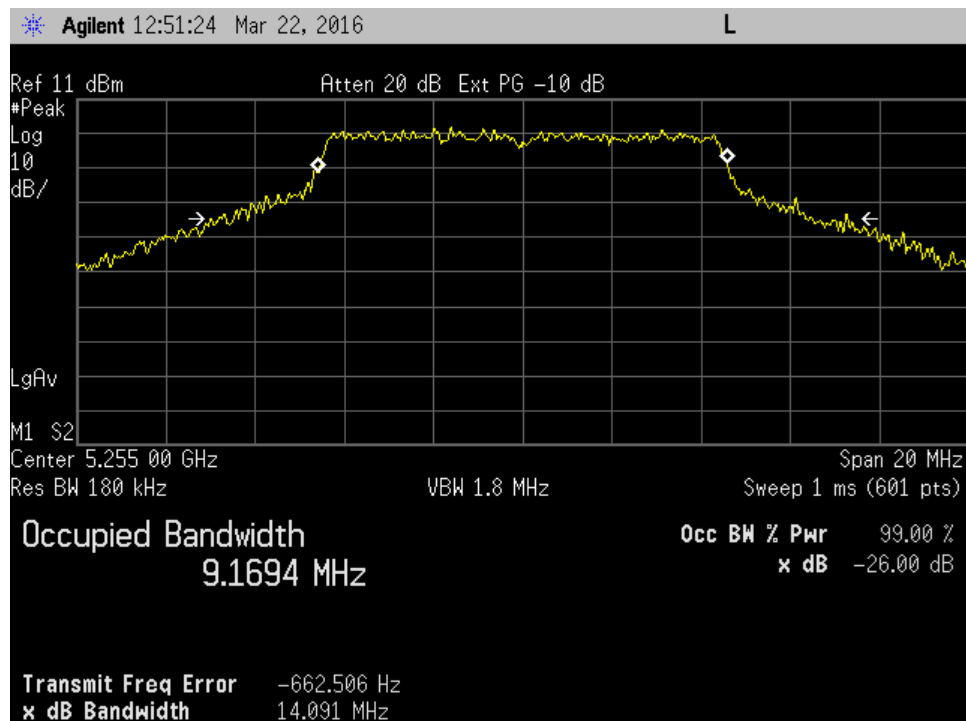




low ch port 1 80MHz BW

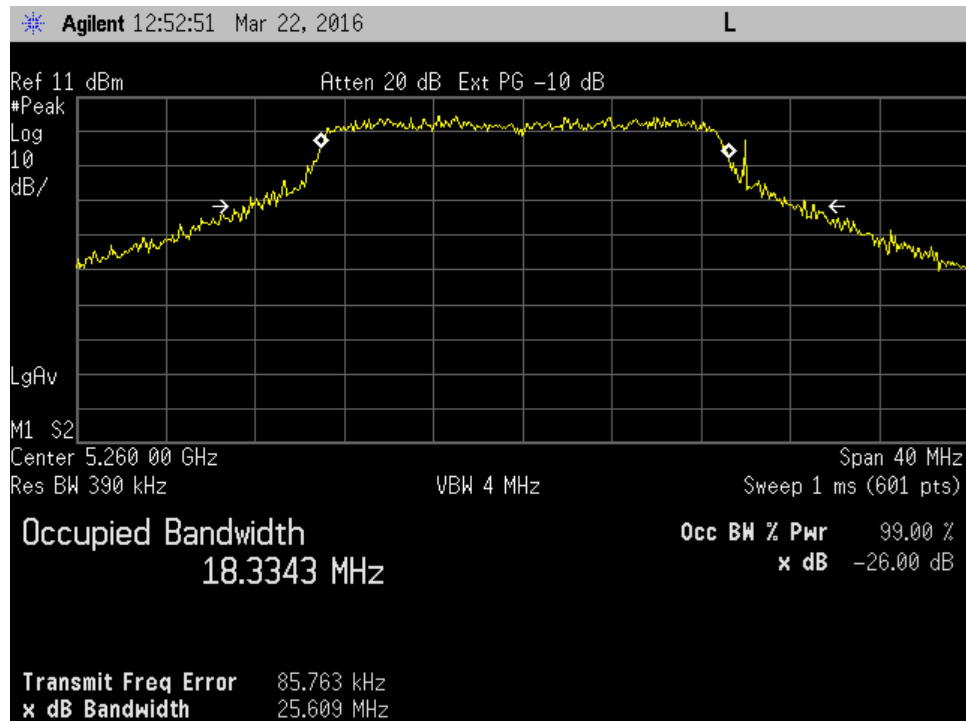


low ch port 2 10MHz BW

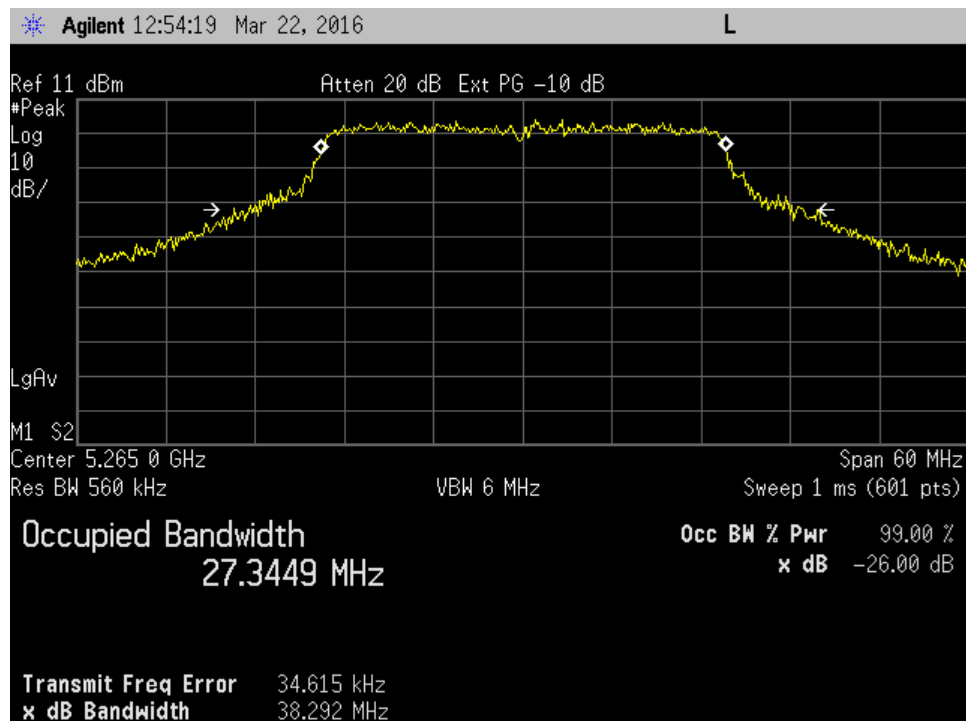




low ch port 2 20MHz BW

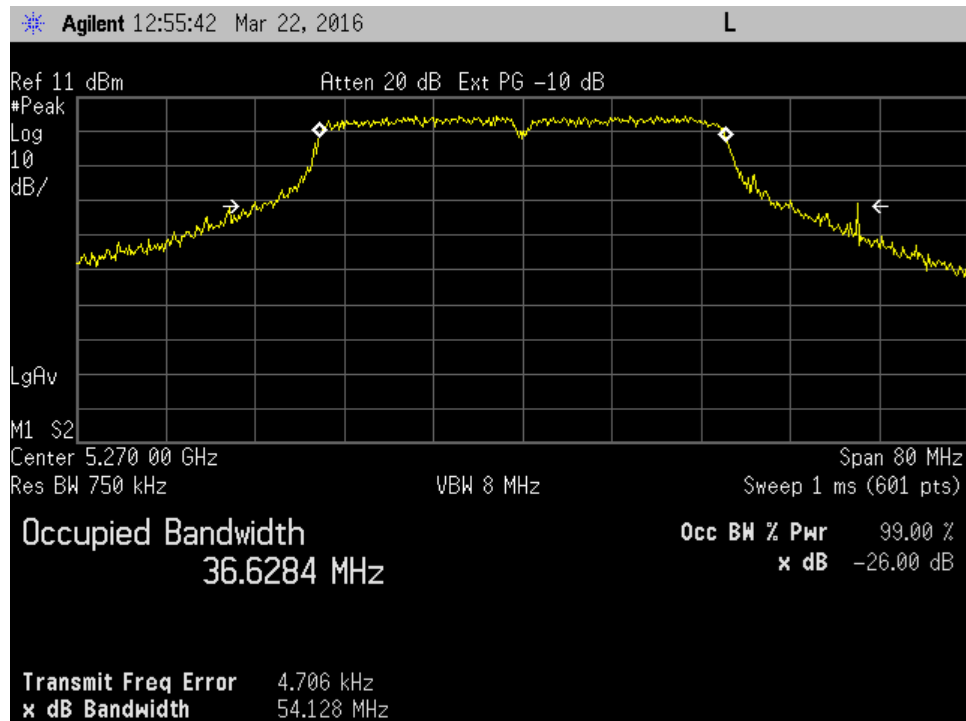


low ch port 2 30MHz BW

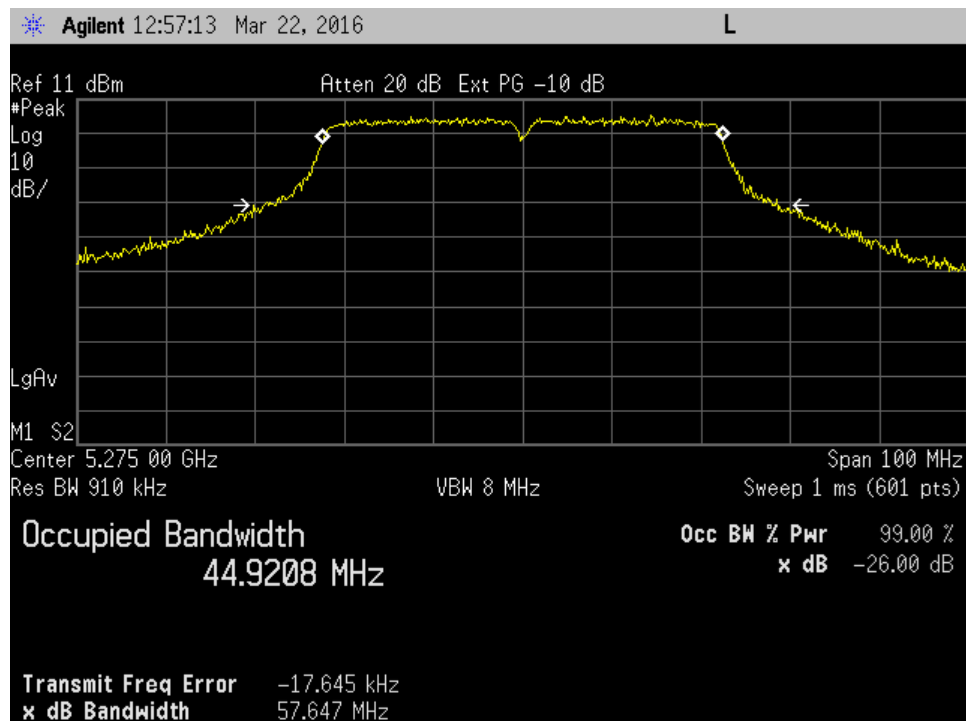




low ch port 2 40MHz BW

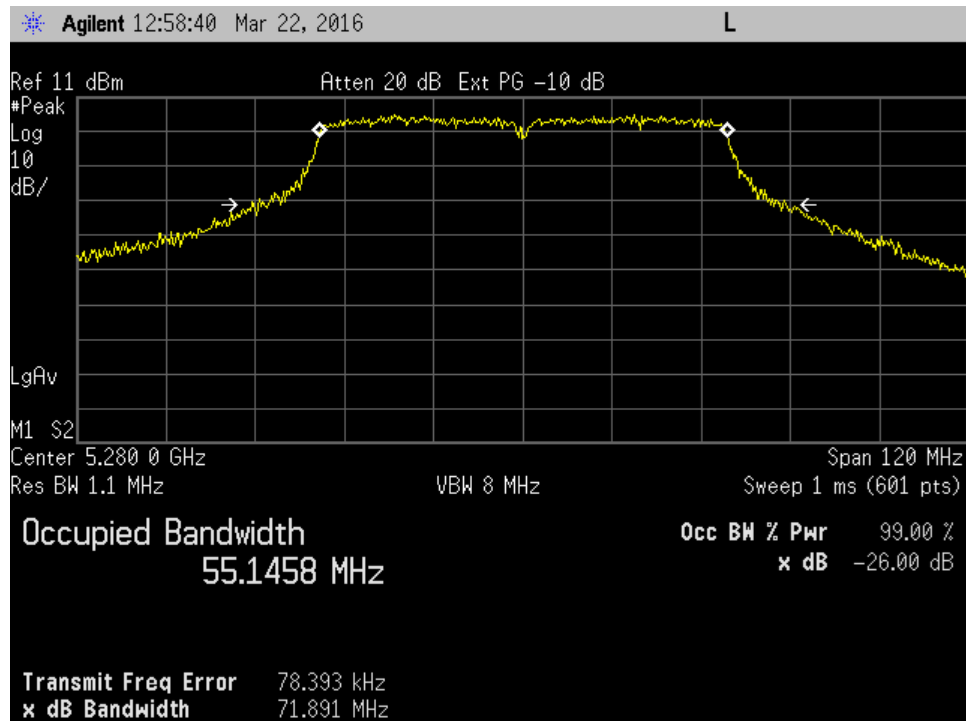


low ch port 2 50MHz BW

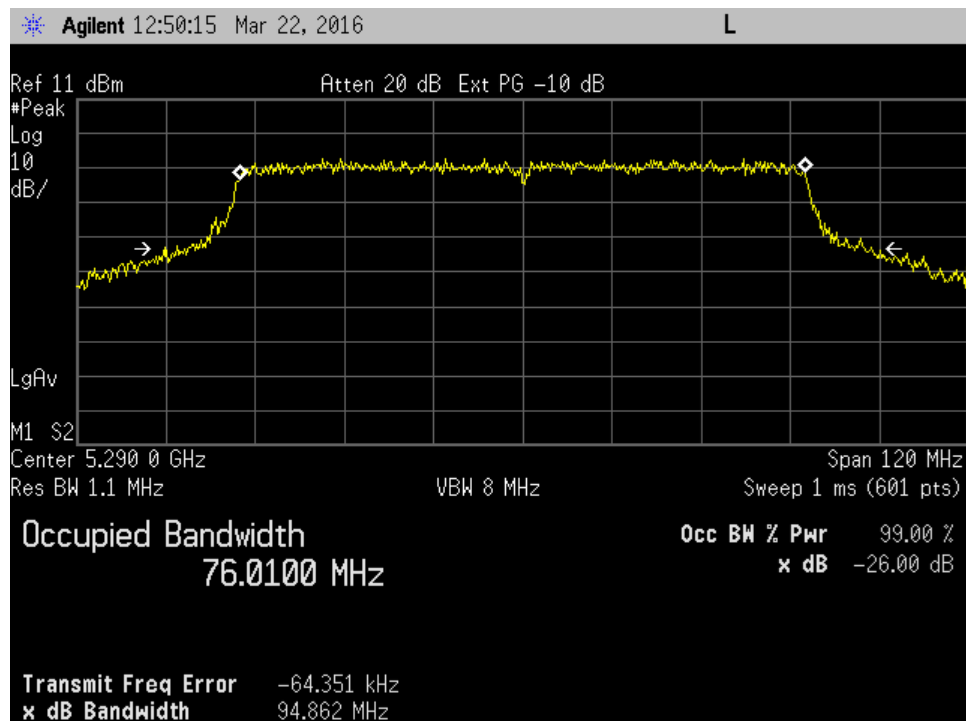




low ch port 2 60MHz BW

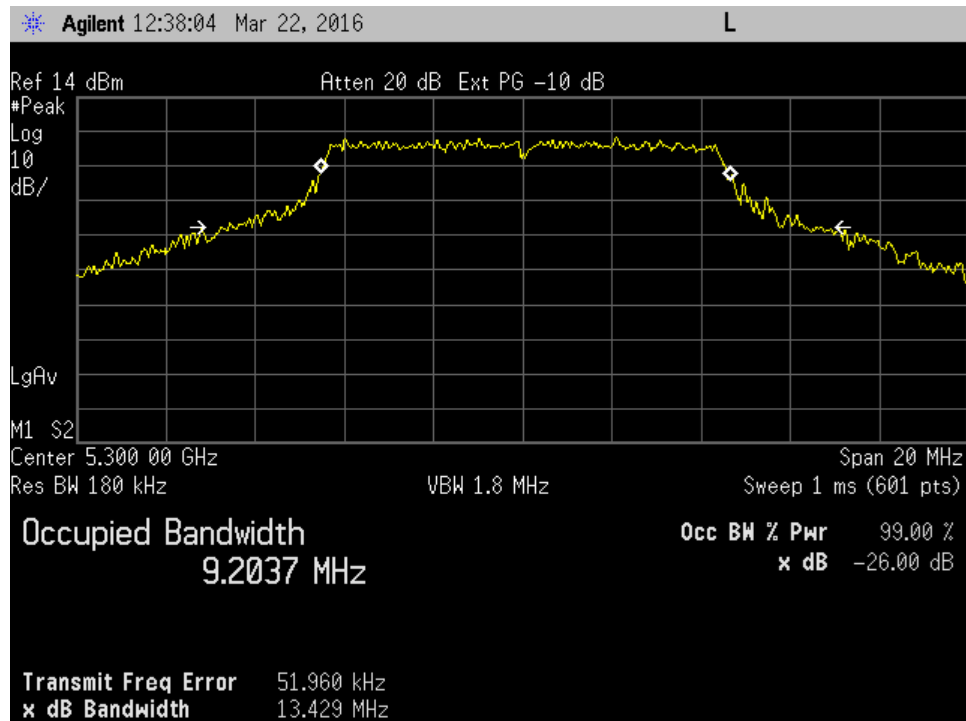


low ch port 2 80MHz BW

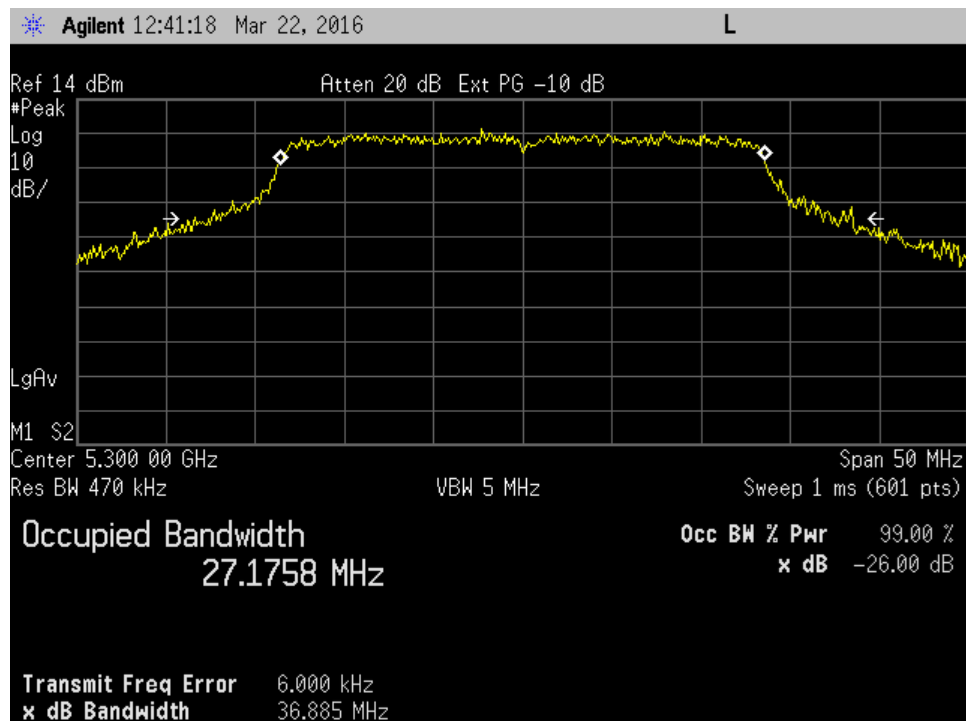




mid ch port 1 10MHz BW

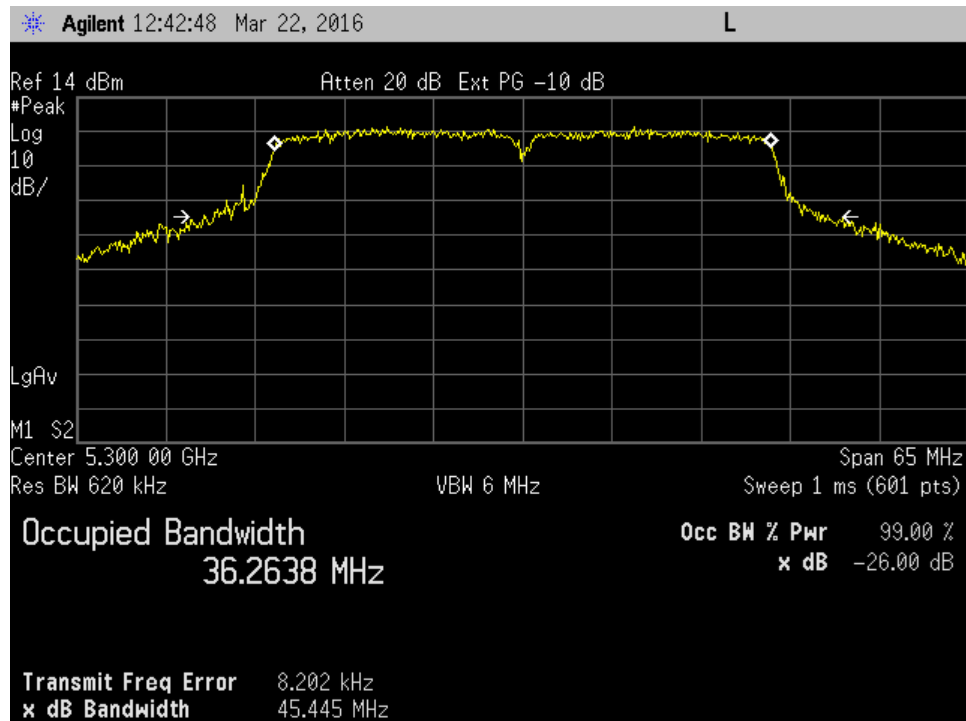


mid ch port 1 30MHz BW

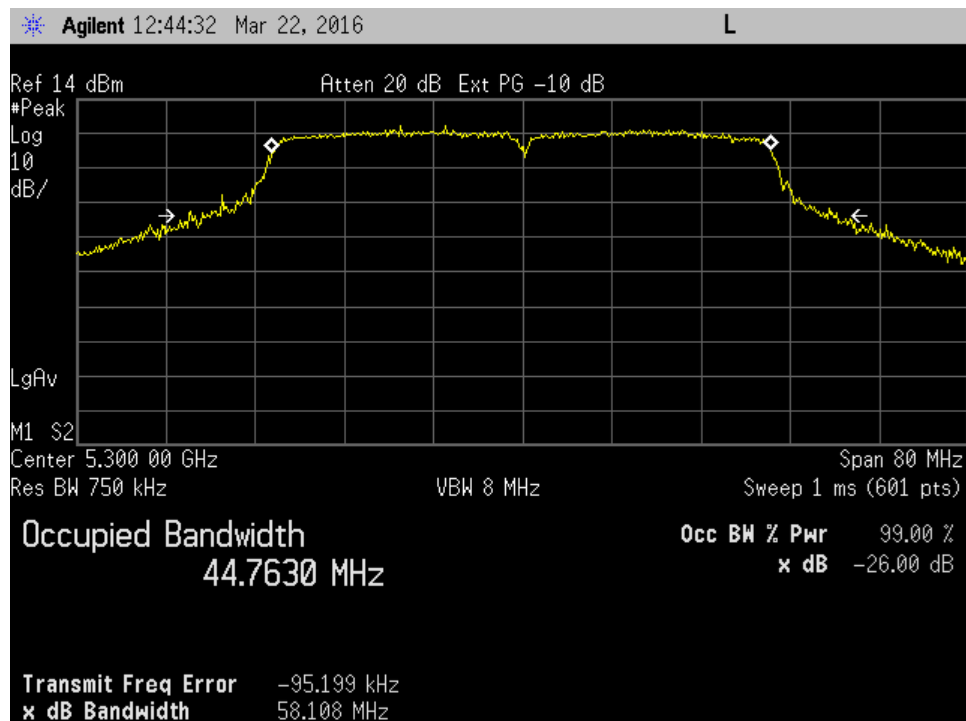




mid ch port 1 40MHz BW

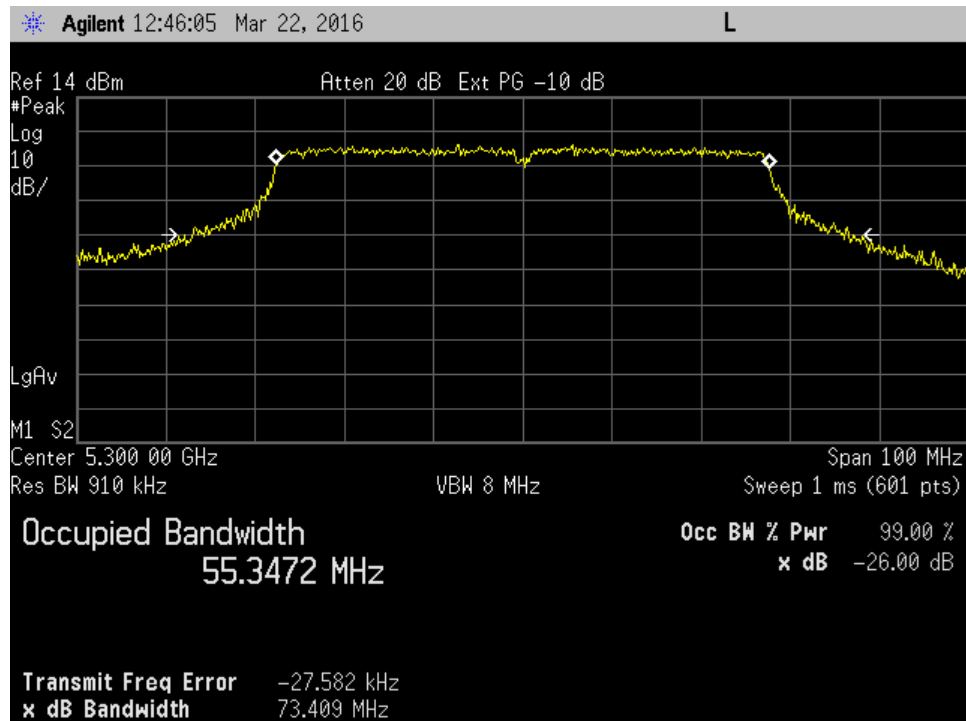


mid ch port 1 50MHz BW

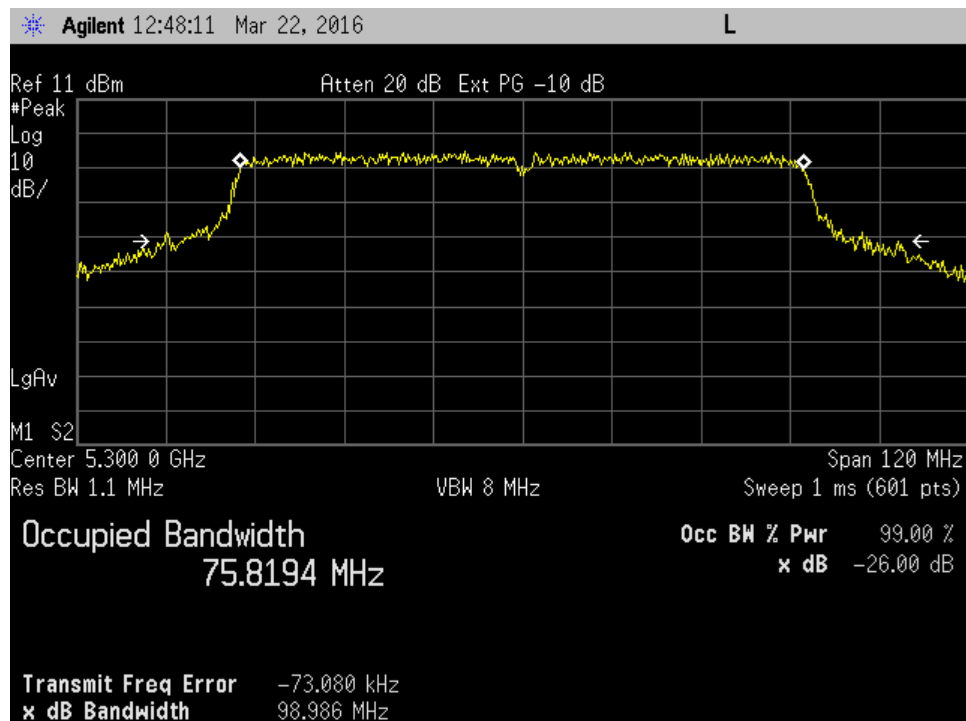




mid ch port 1 60MHz BW

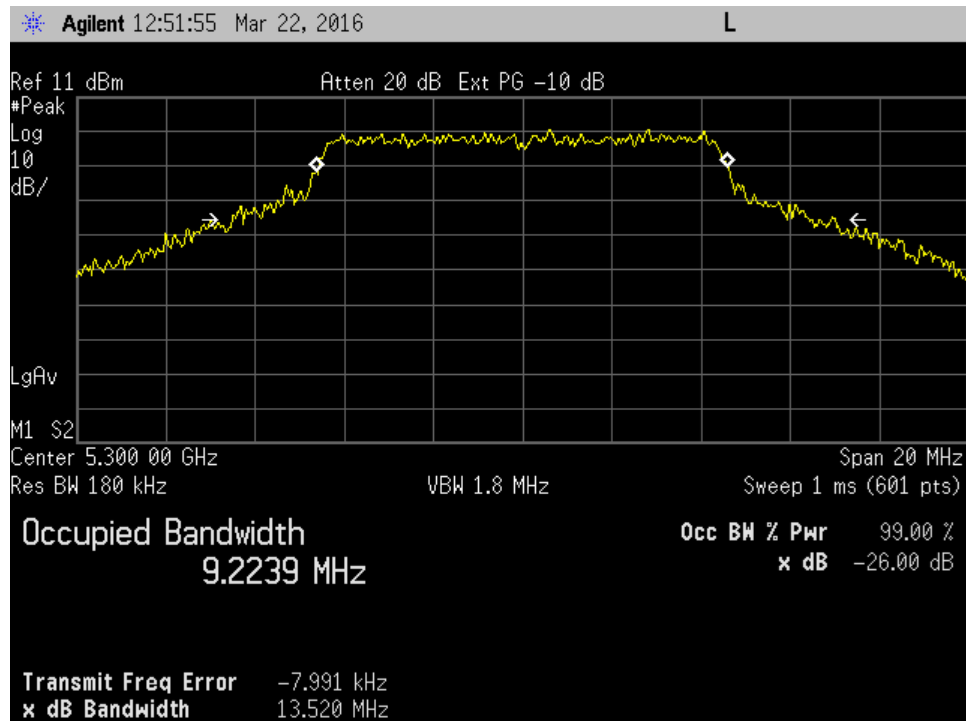


mid ch port 1 80MHz BW

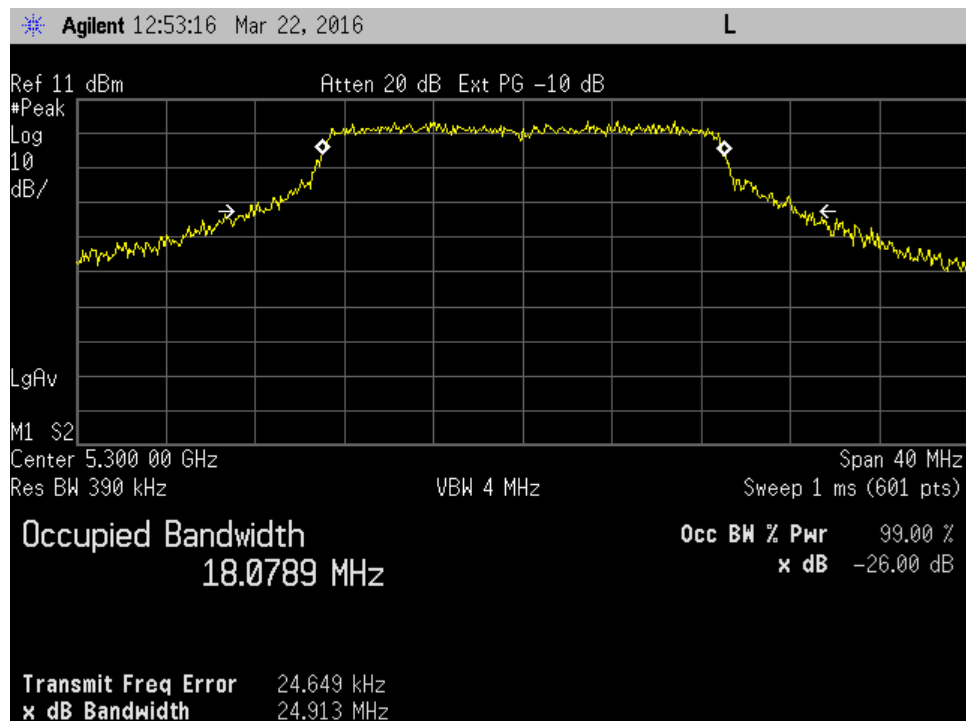




mid ch port 2 10MHz BW

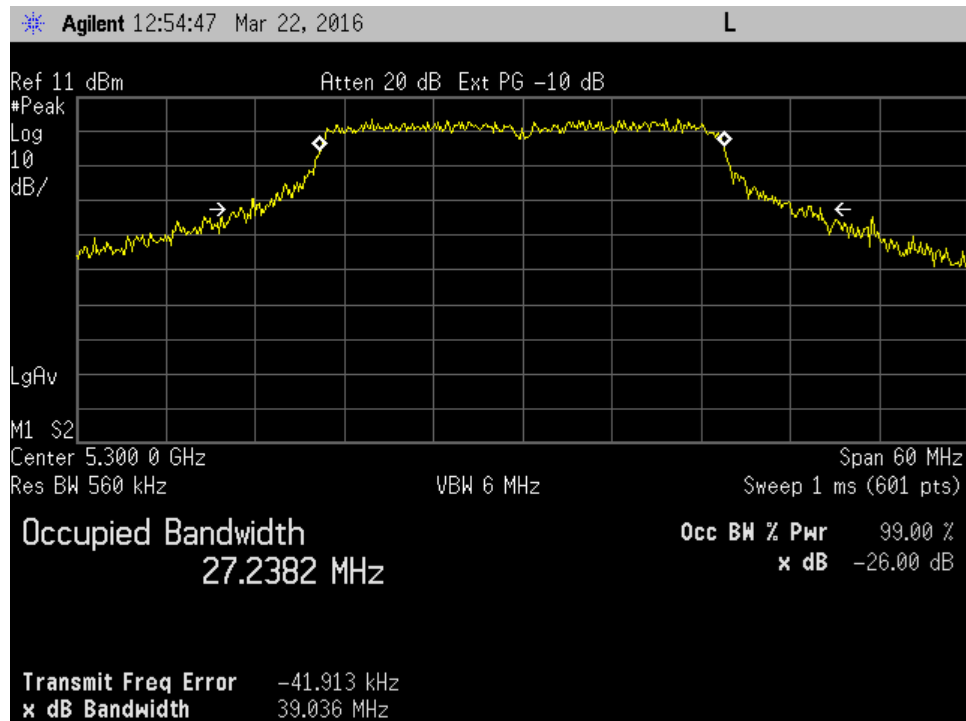


mid ch port 2 20MHz BW

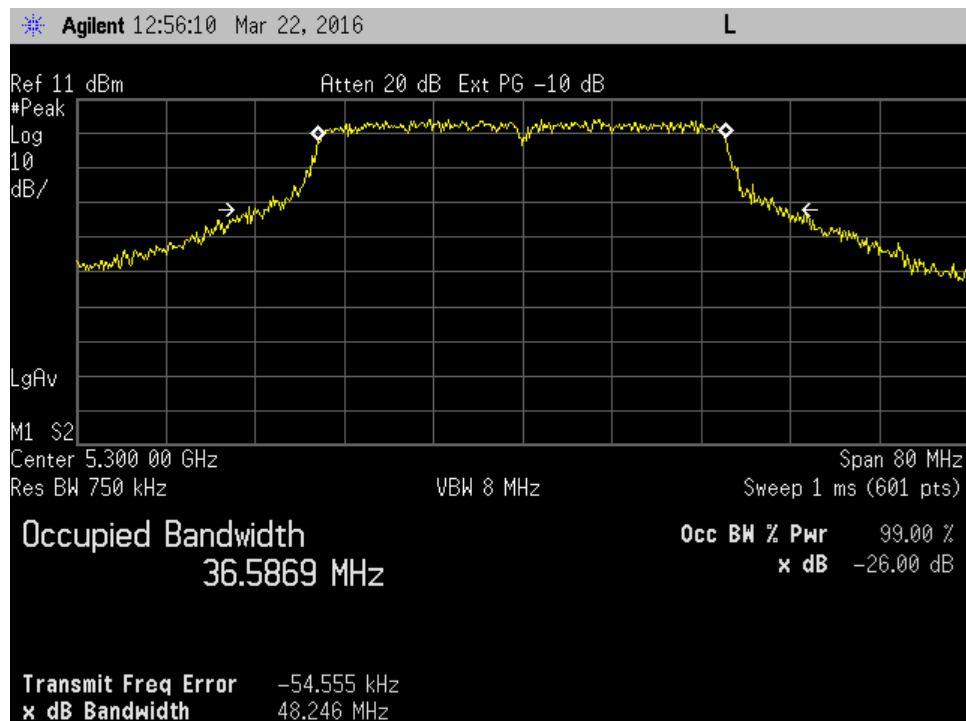




mid ch port 2 30MHz BW

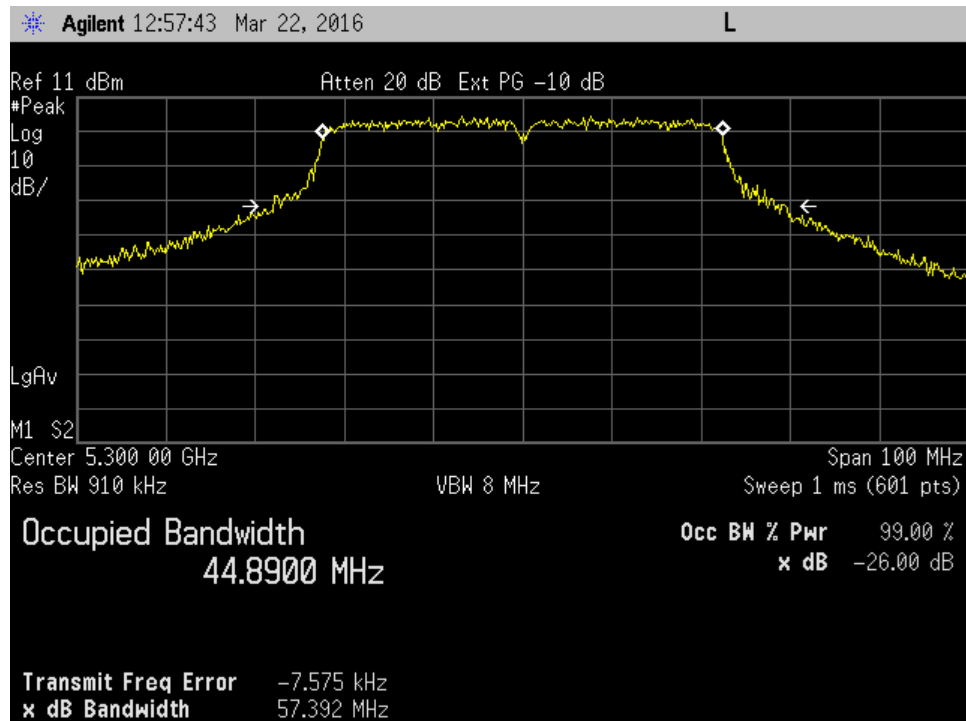


mid ch port 2 40MHz BW

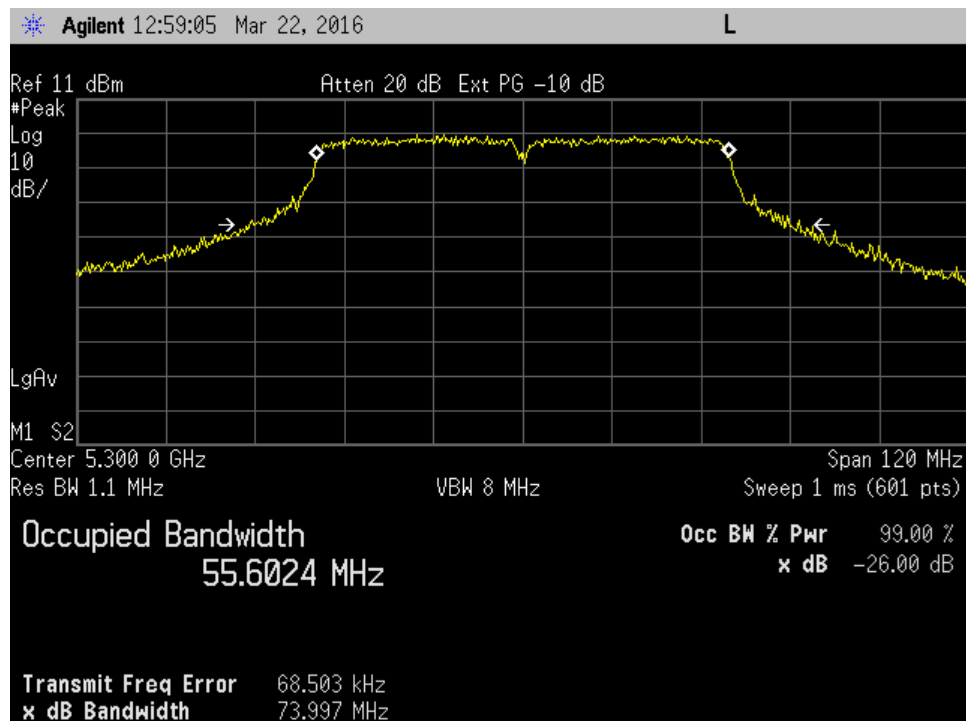




mid ch port 2 50MHz BW

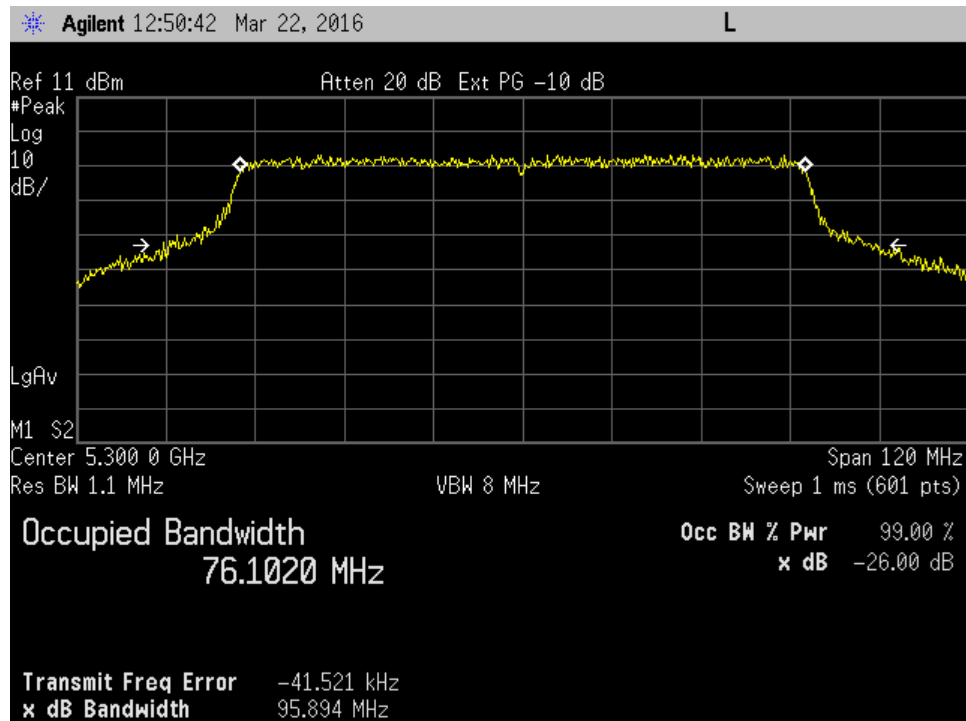


mid ch port 2 60MHz BW

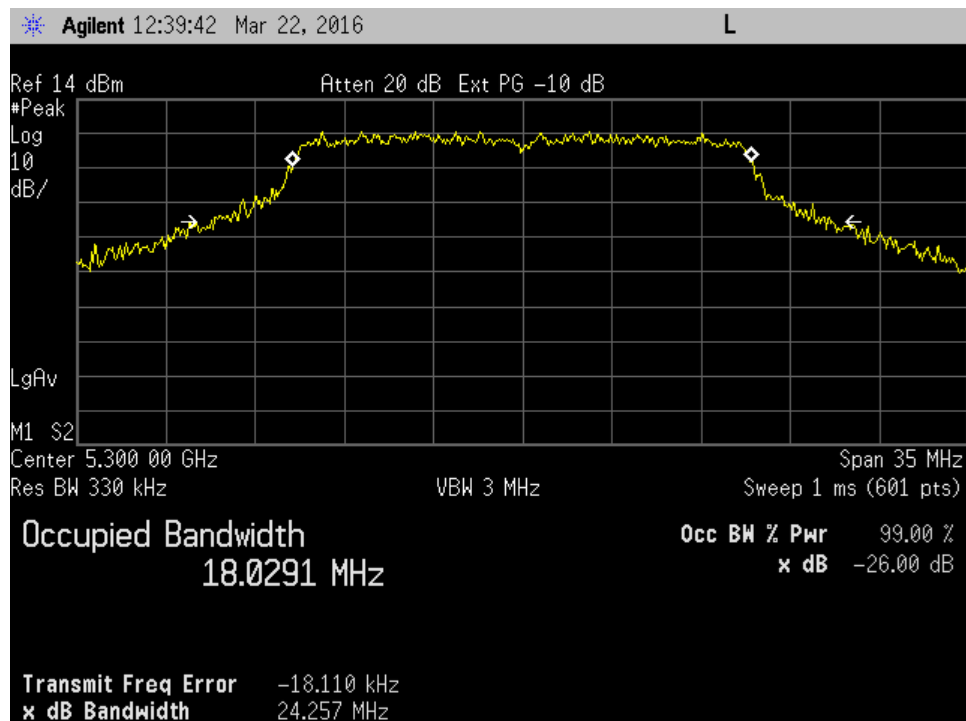




mid ch port 2 80MHz BW



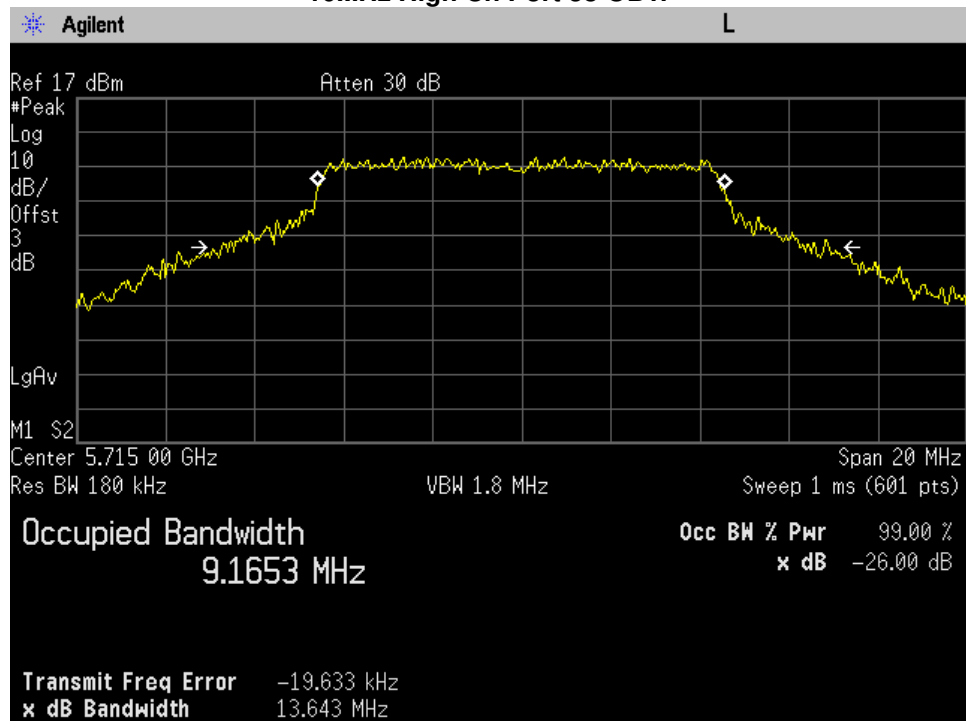
midw ch port 1 20MHz BW



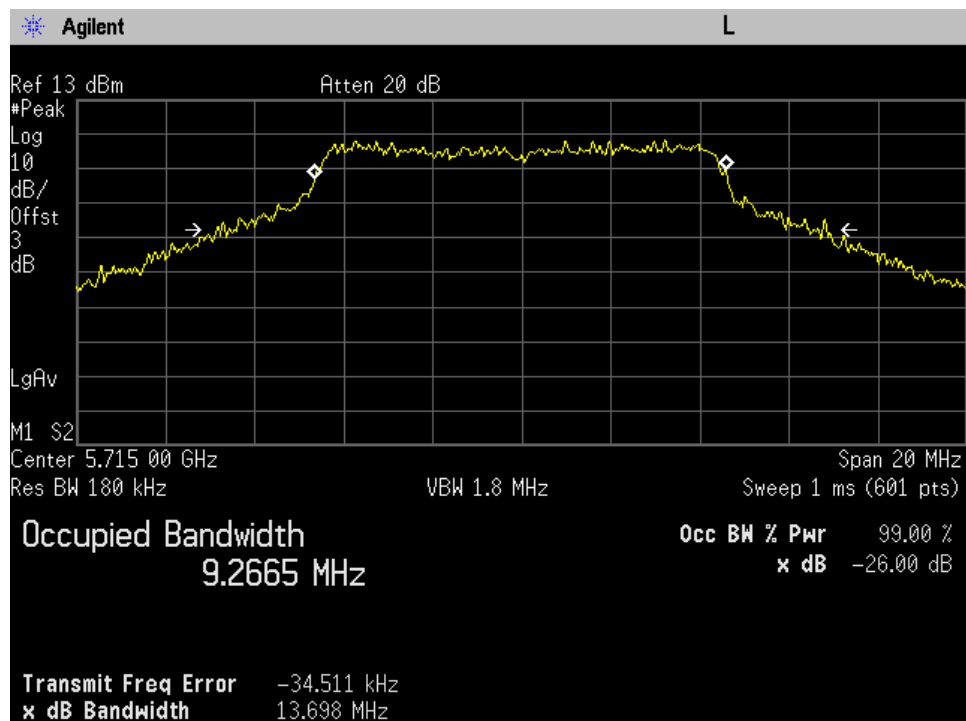


UNII-2C Occupied Bandwidth

10MHz High Ch Port J8 OBW

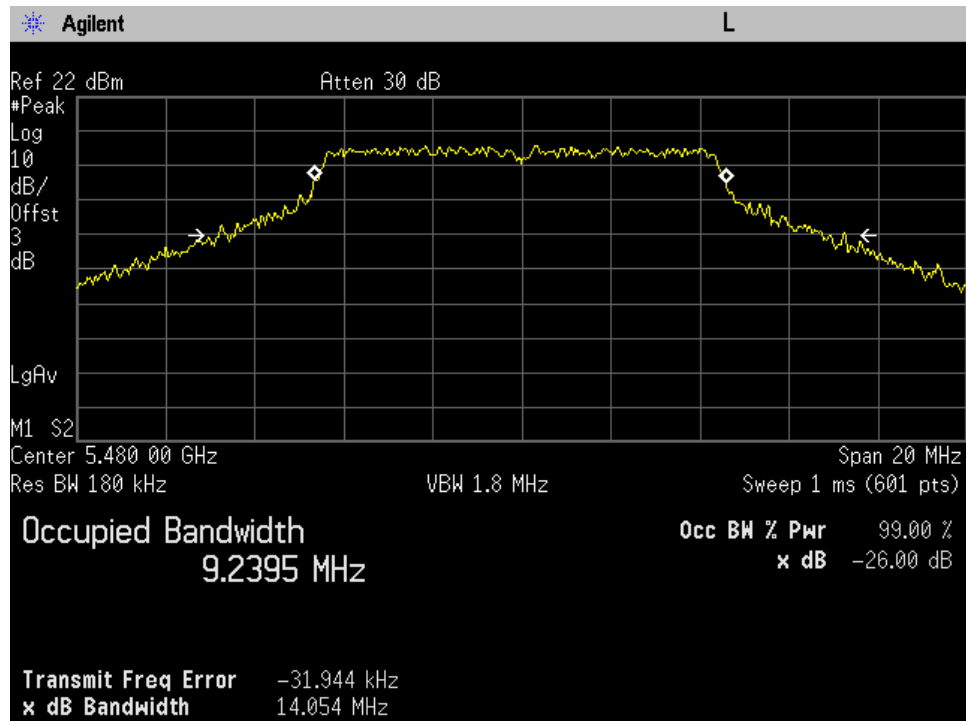


10MHz High Ch Port J7 OBW

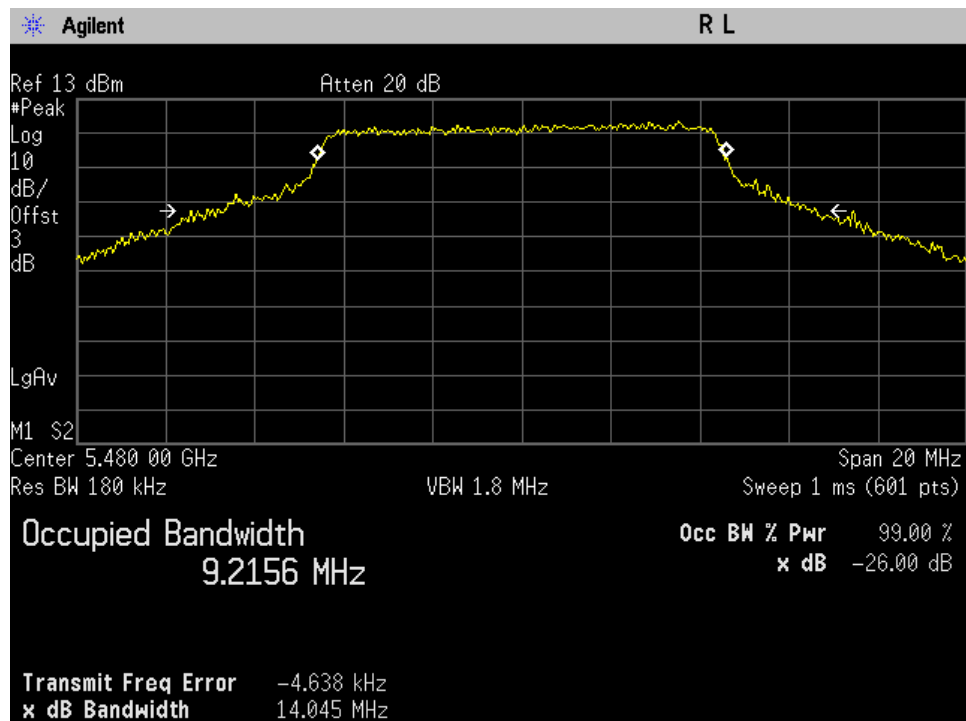




10MHz Low Ch Port J8 OBW

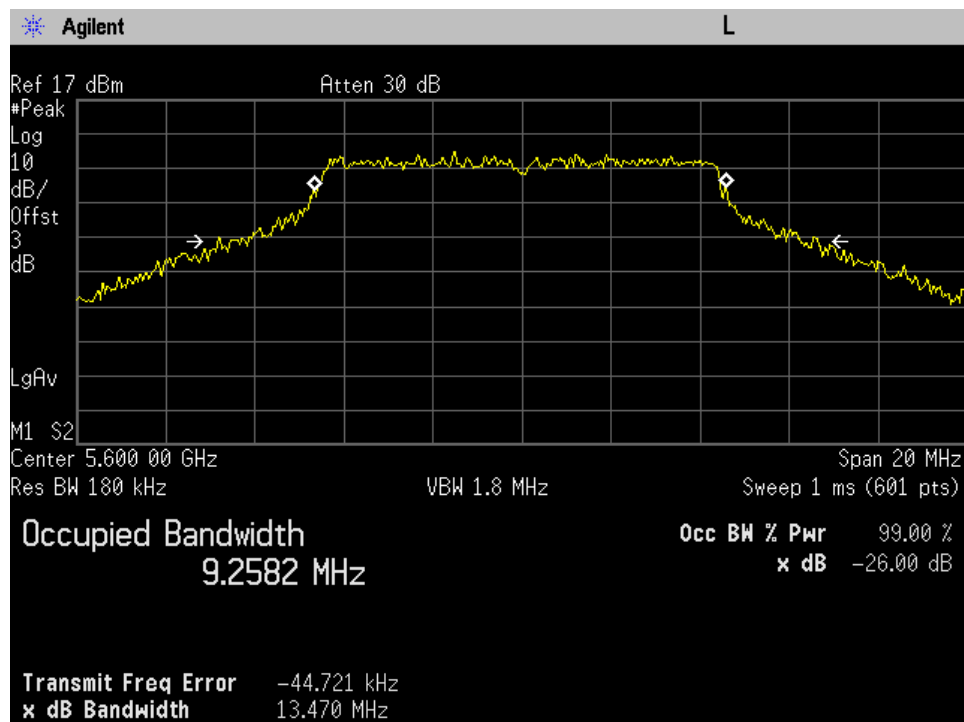


10MHz Low Ch Port J7 OBW

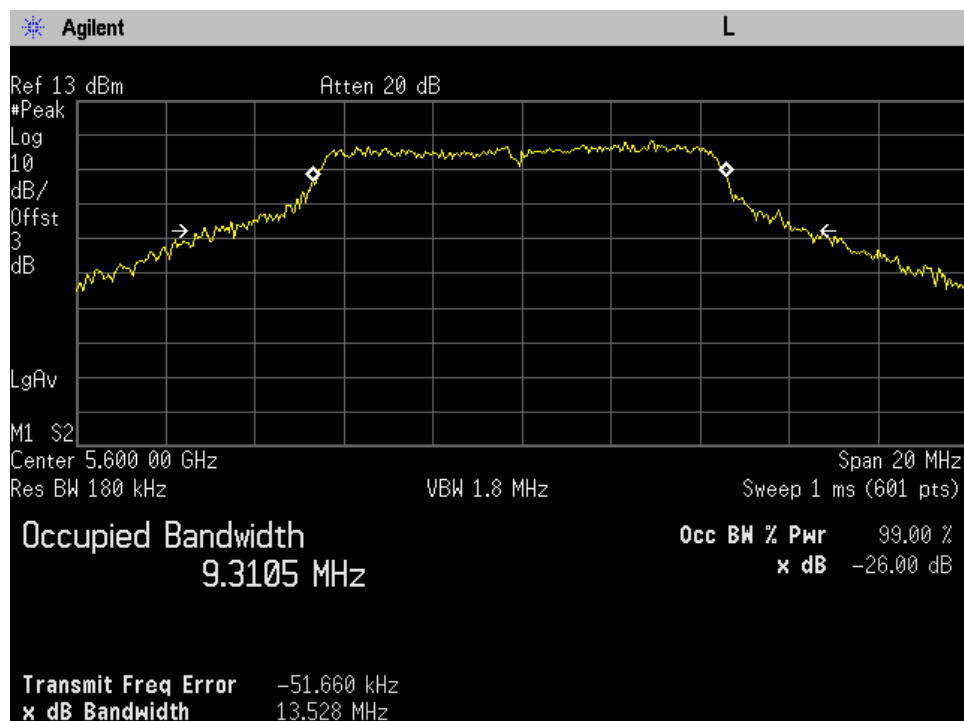




10MHz Mid Ch Port J8 OBW

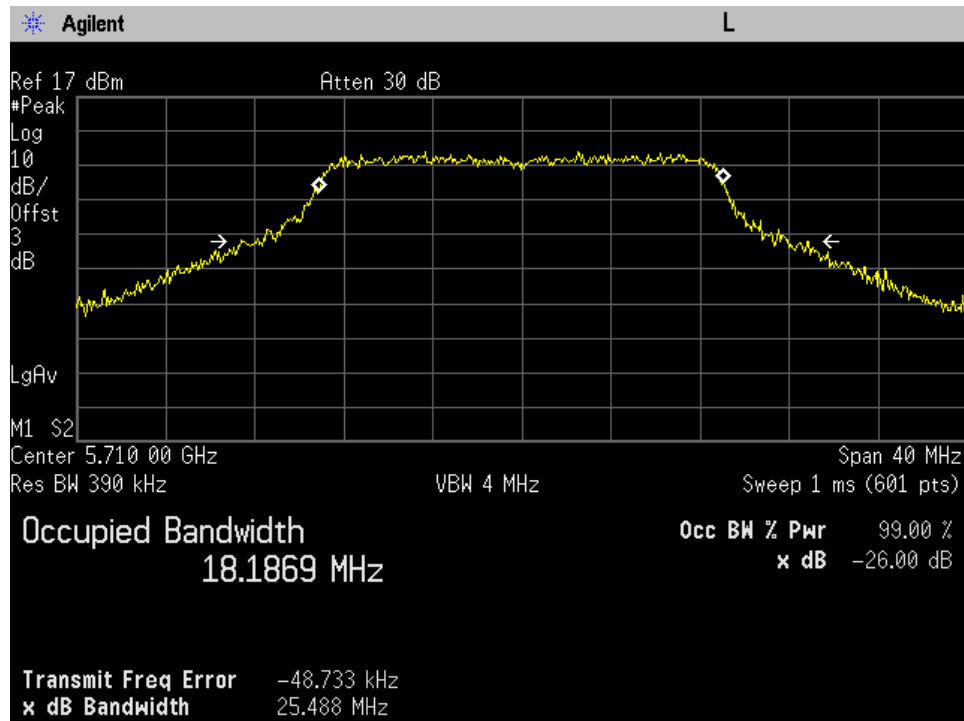


10MHz Mid Ch Port J7 OBW

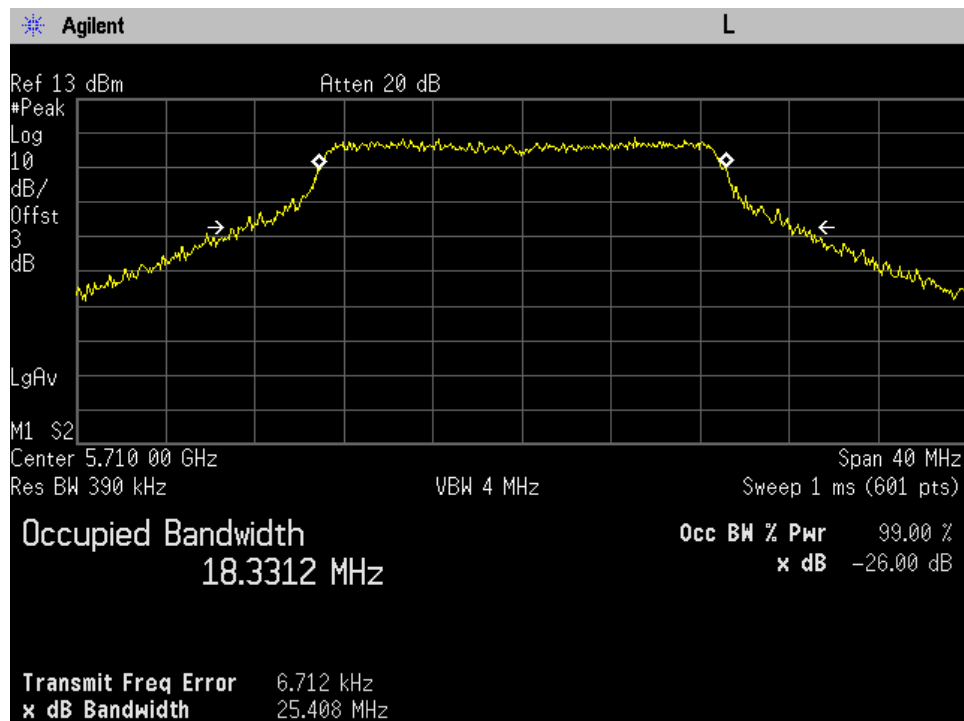




20MHz High Ch Port J8 OBW

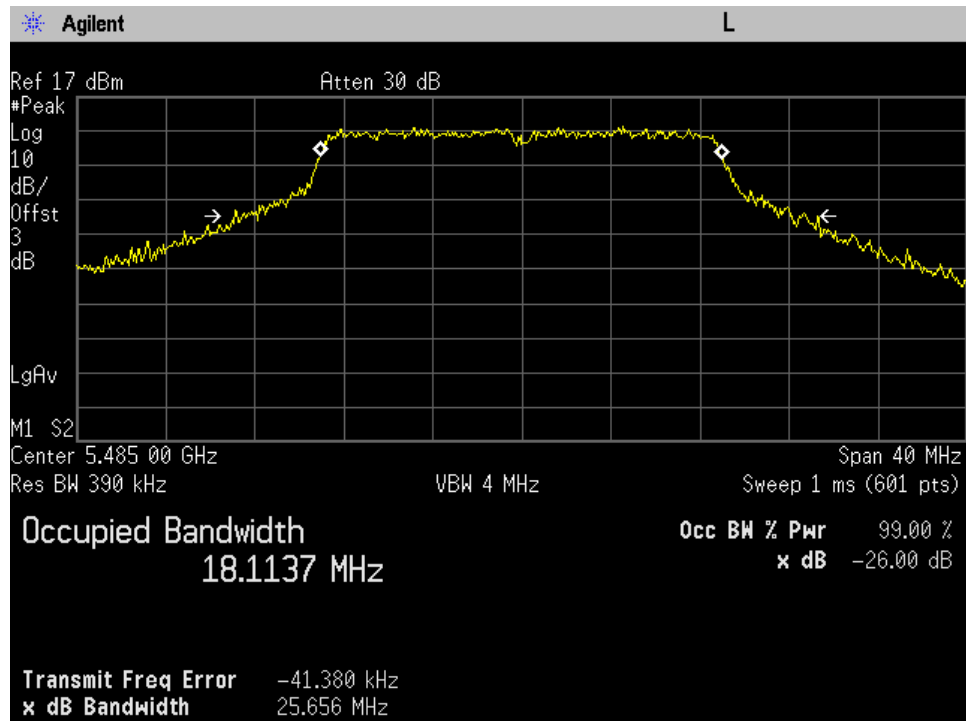


20MHz High Ch Port J7 OBW

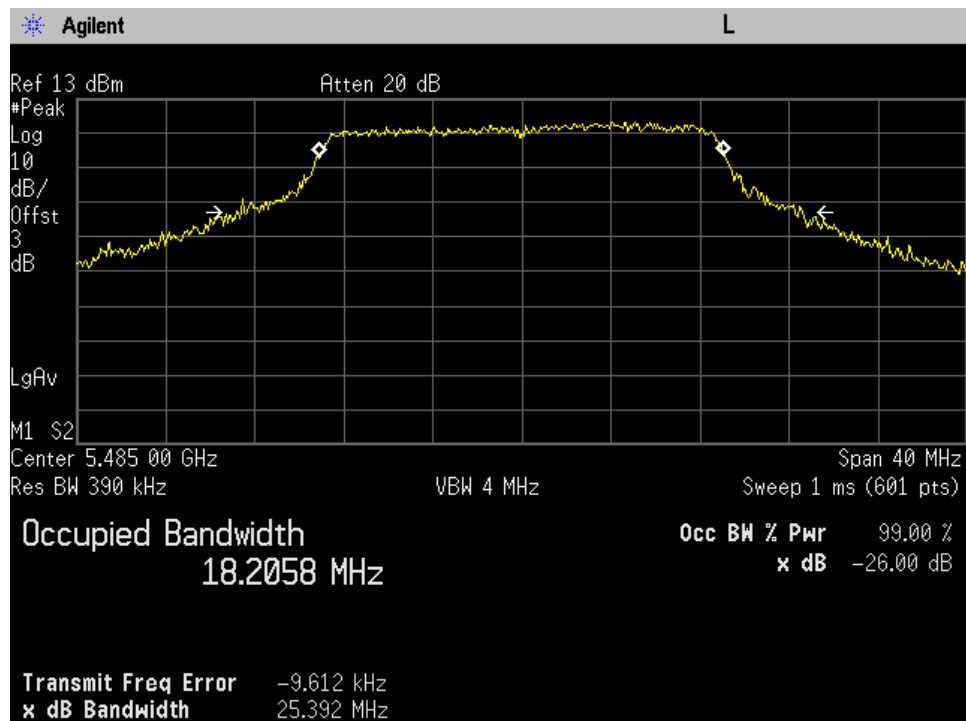




20MHz Low Ch Port J8 OBW

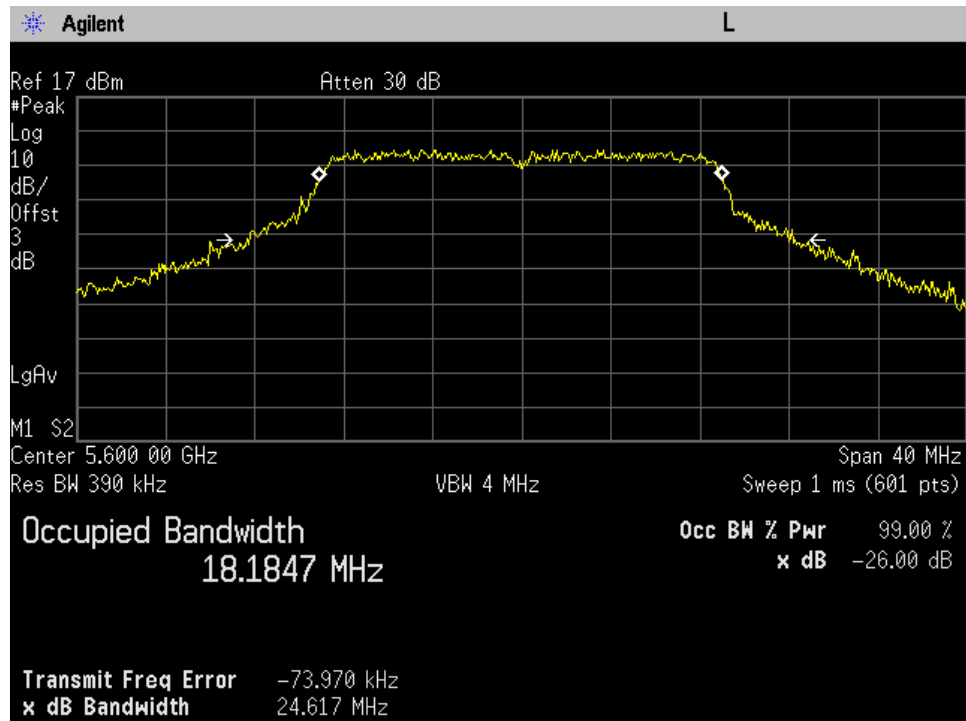


20MHz Low Ch Port J7 OBW

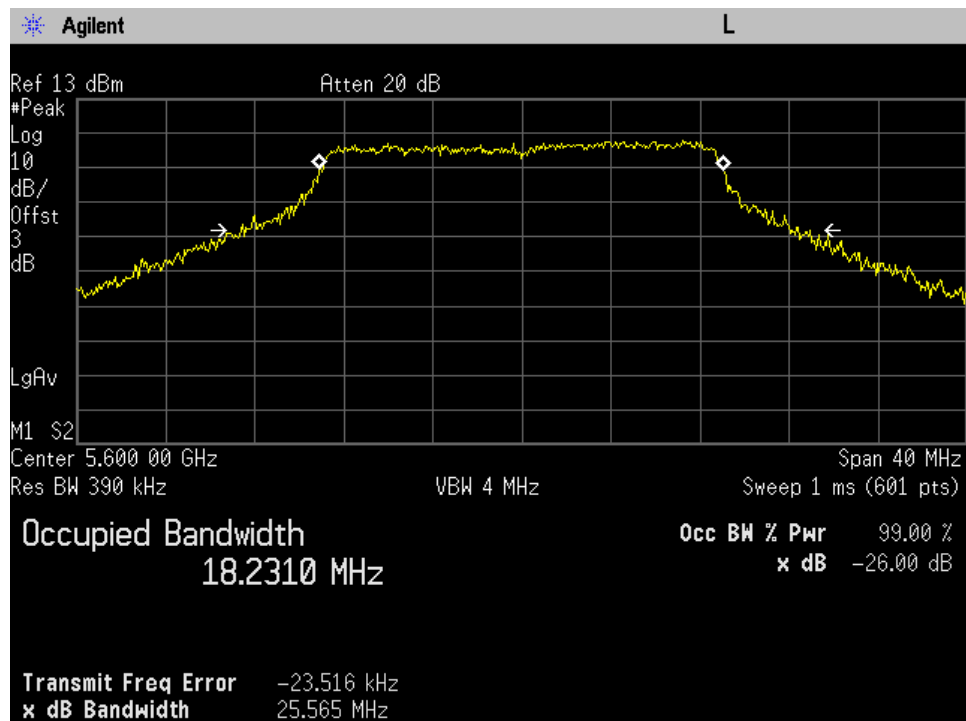




20MHz Mid Ch Port J8 OBW

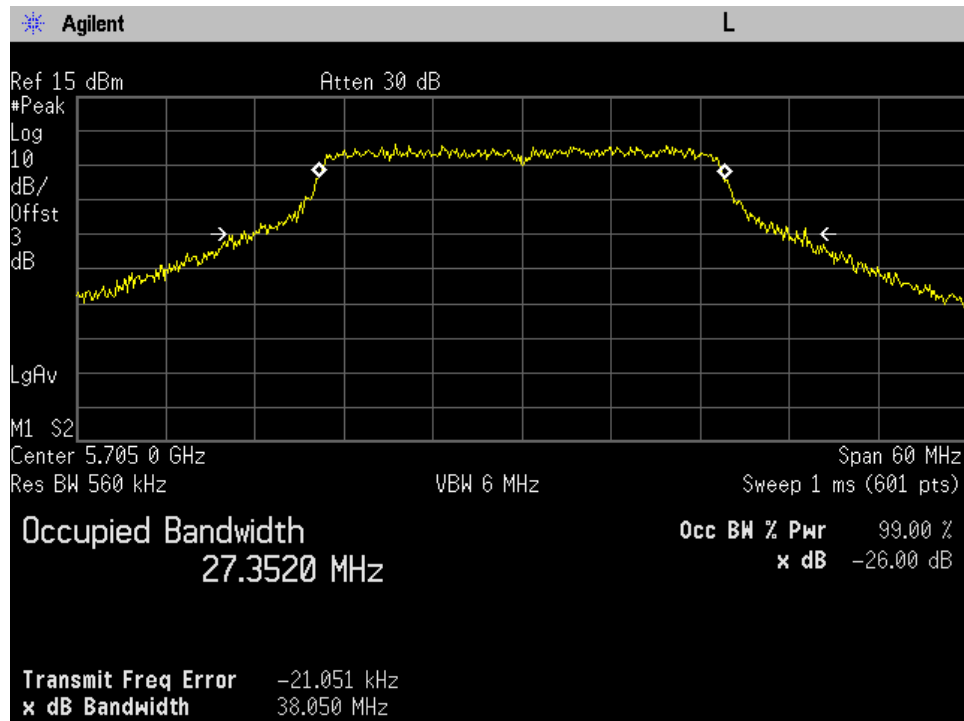


20MHz Mid Ch Port J7 OBW

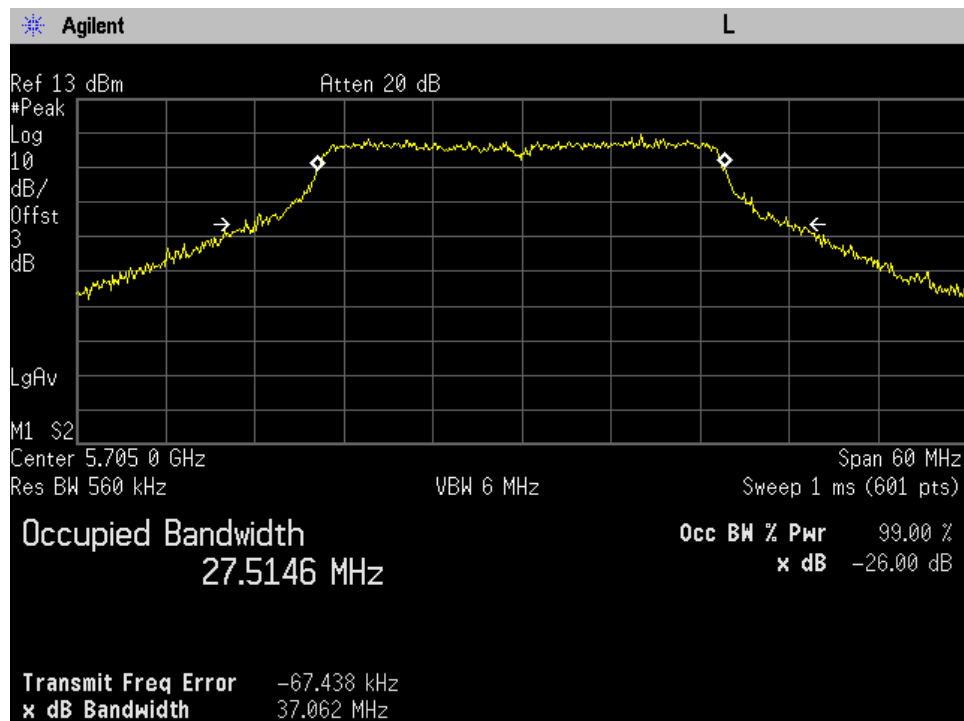




30MHz High Ch Port J8 OBW

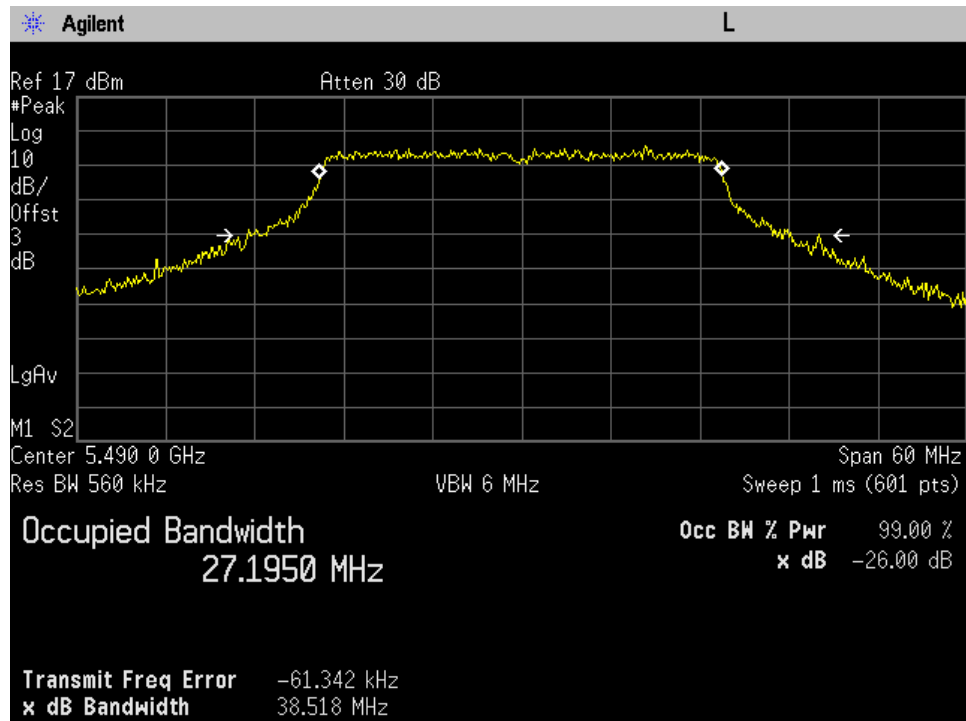


30MHz High Ch Port J7 OBW

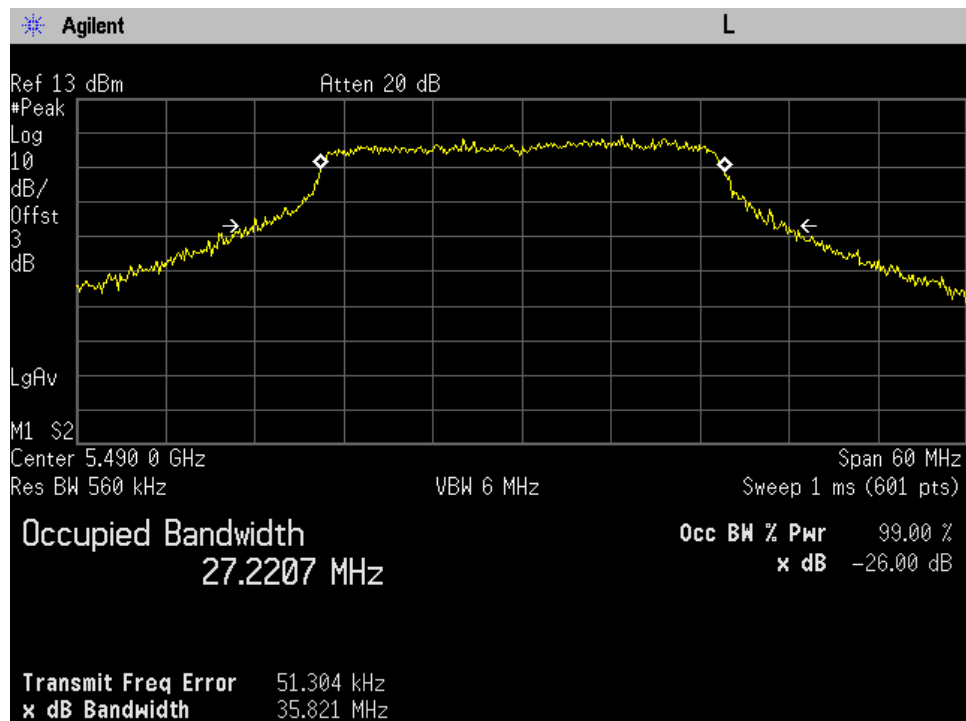




30MHz Low Ch Port J8 OBW

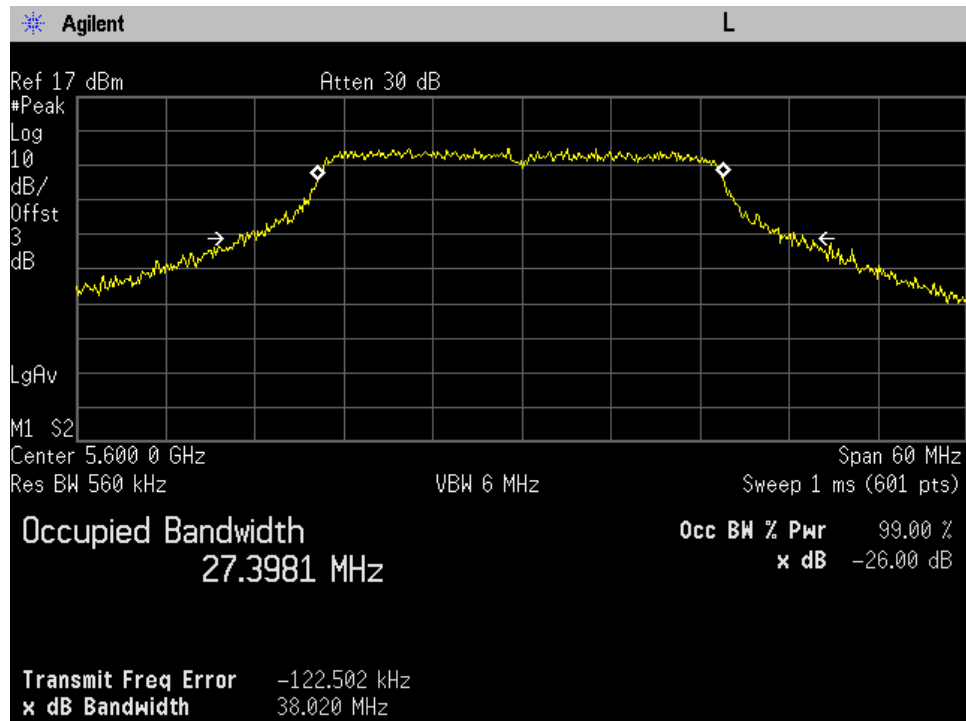


30MHz Low Ch Port J7 OBW

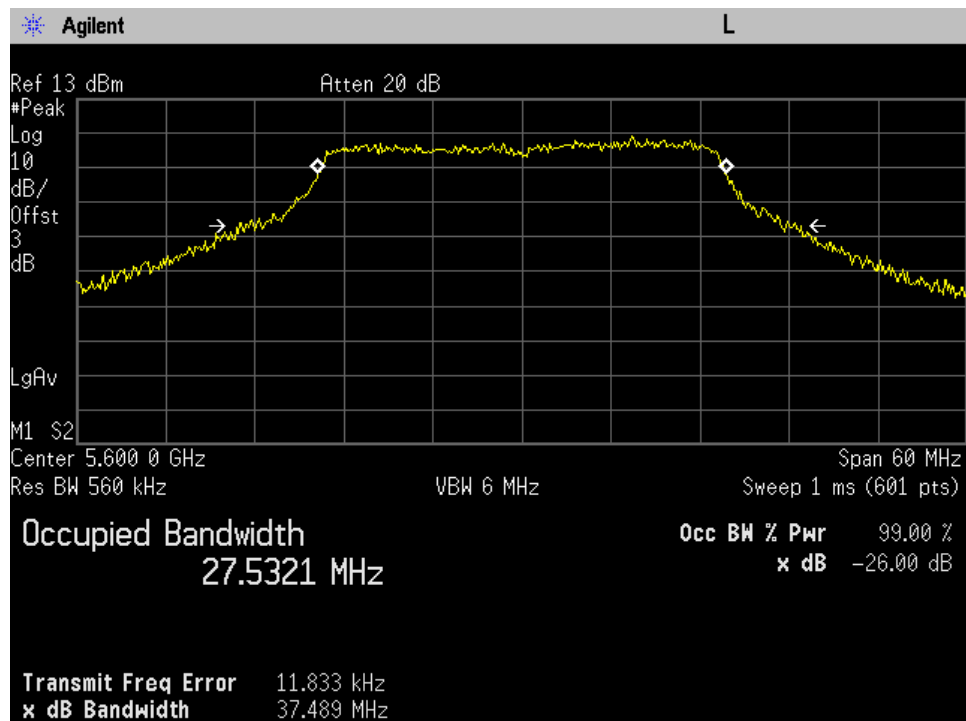




30MHz Mid Ch Port J8 OBW

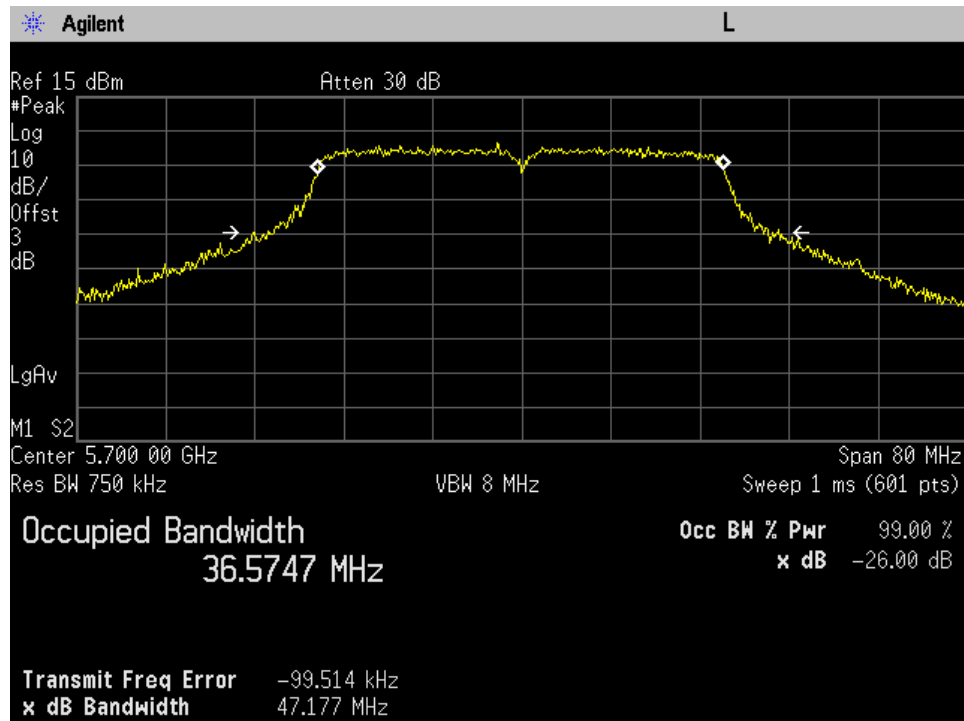


30MHz Mid Ch Port J7 OBW

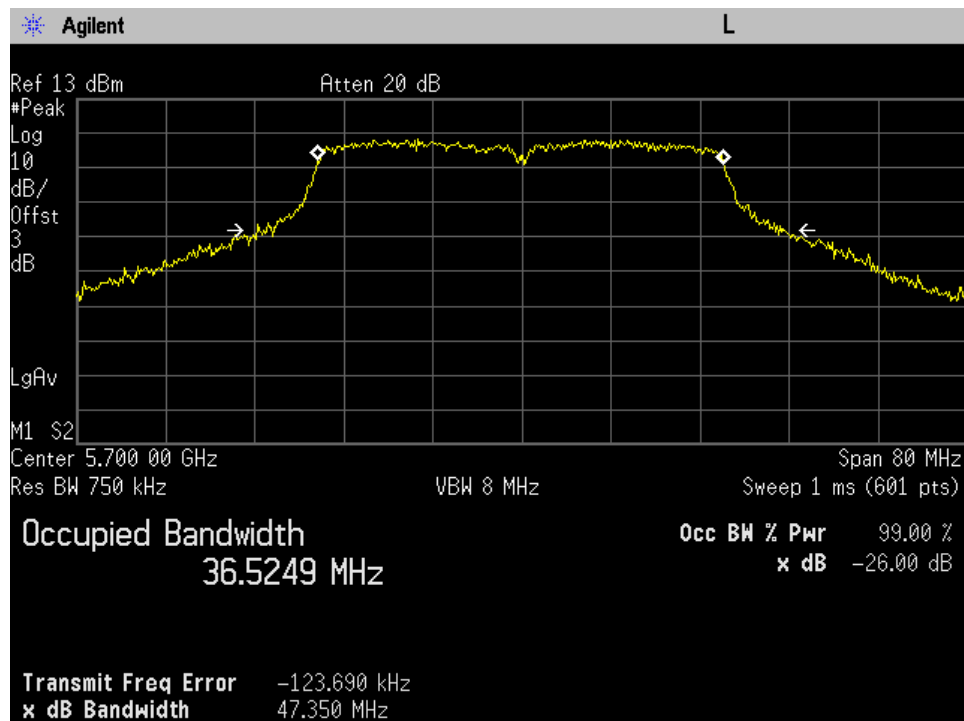




40MHz High Ch Port J8 OBW

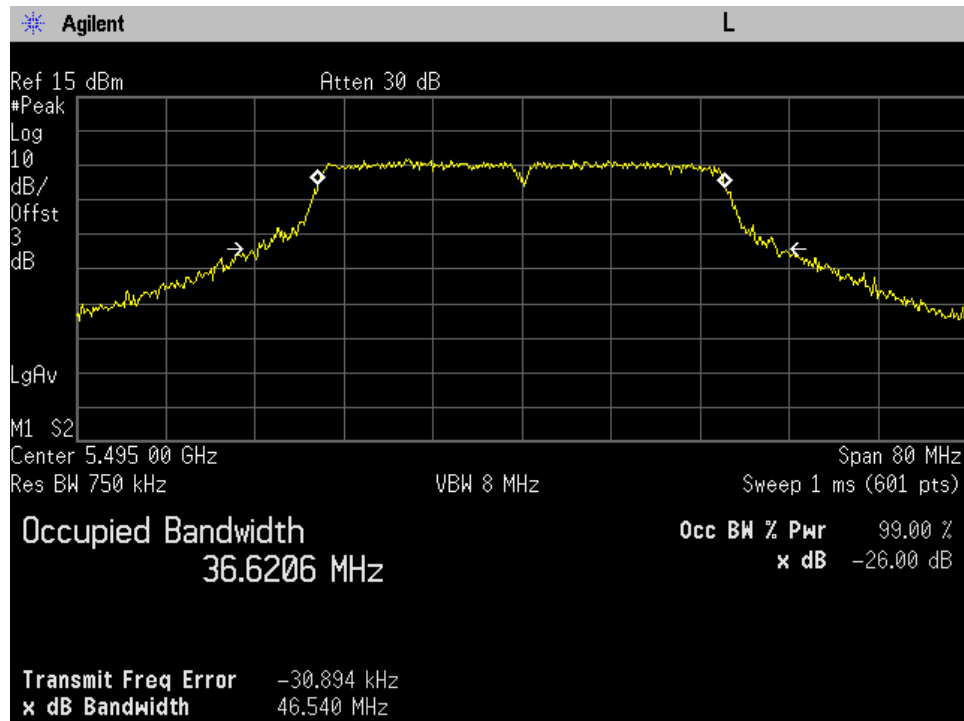


40MHz High Ch Port J7 OBW

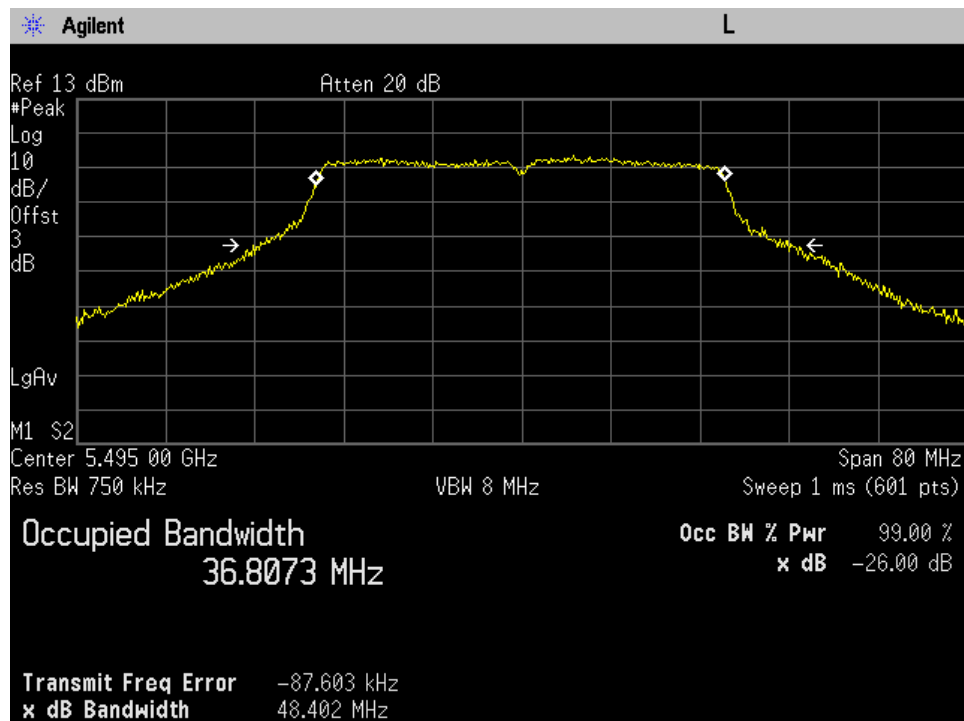




40MHz Low Ch Port J8 OBW

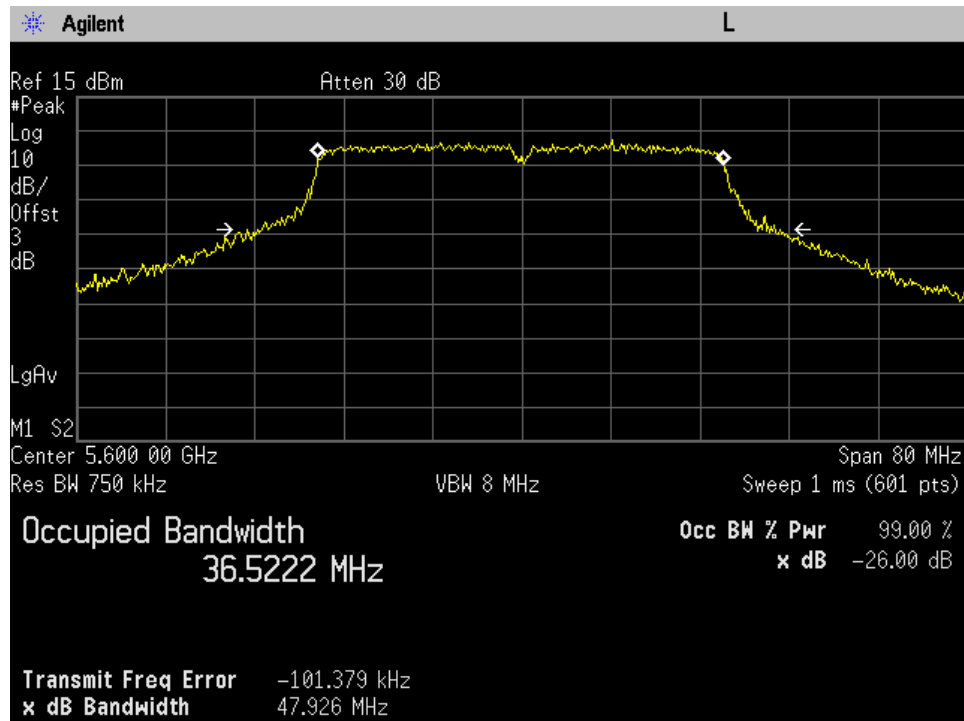


40MHz Low Ch Port J7 OBW

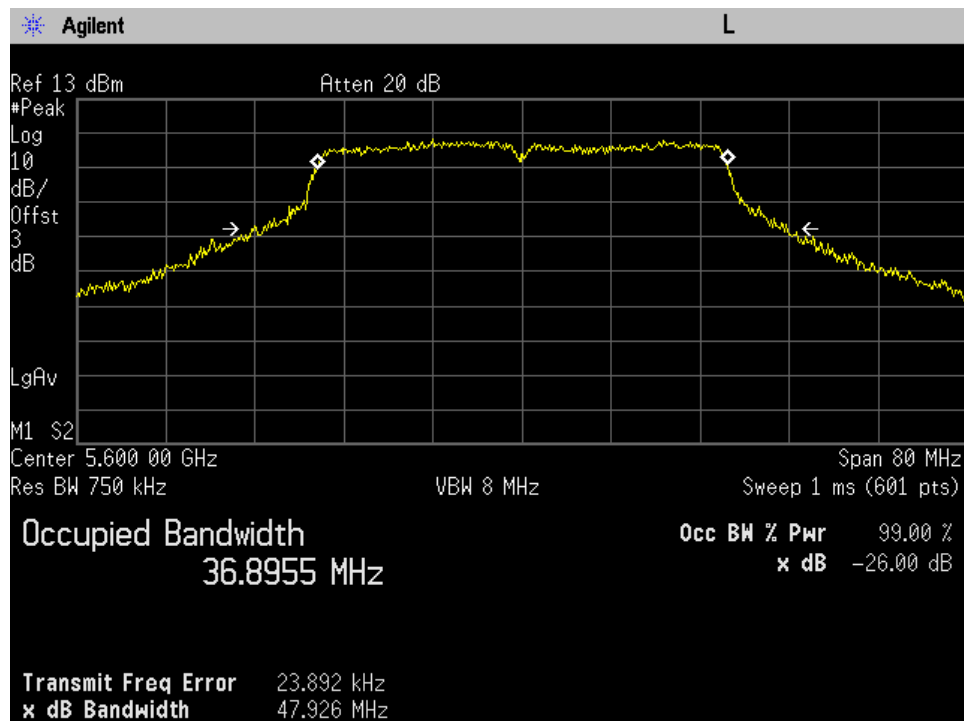




40MHz Mid Ch Port J8 OBW

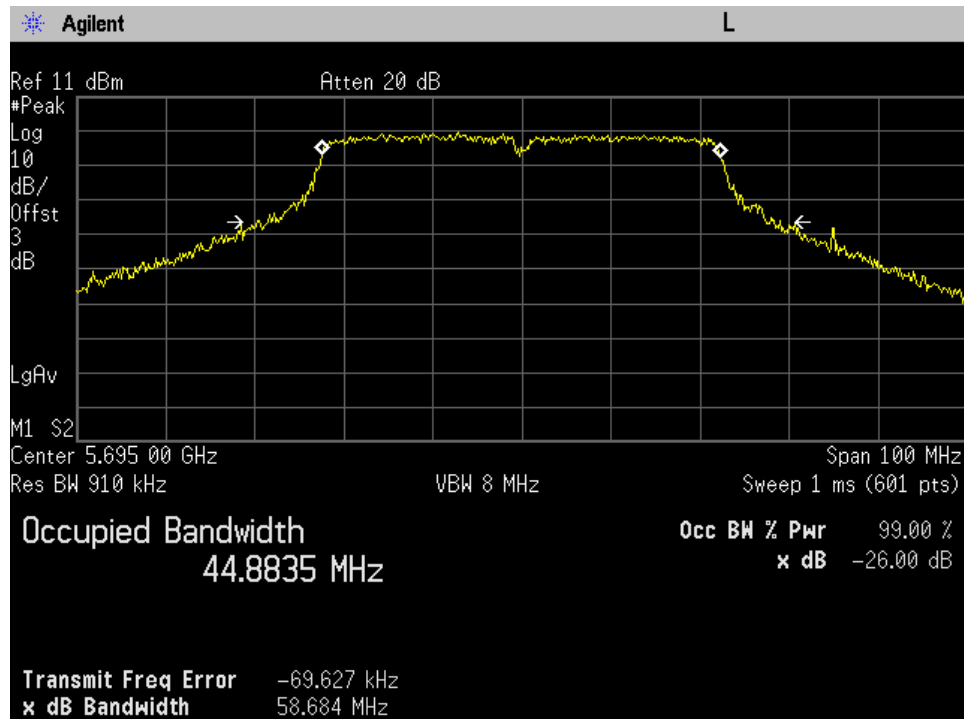


40MHz Mid Ch Port J7 OBW

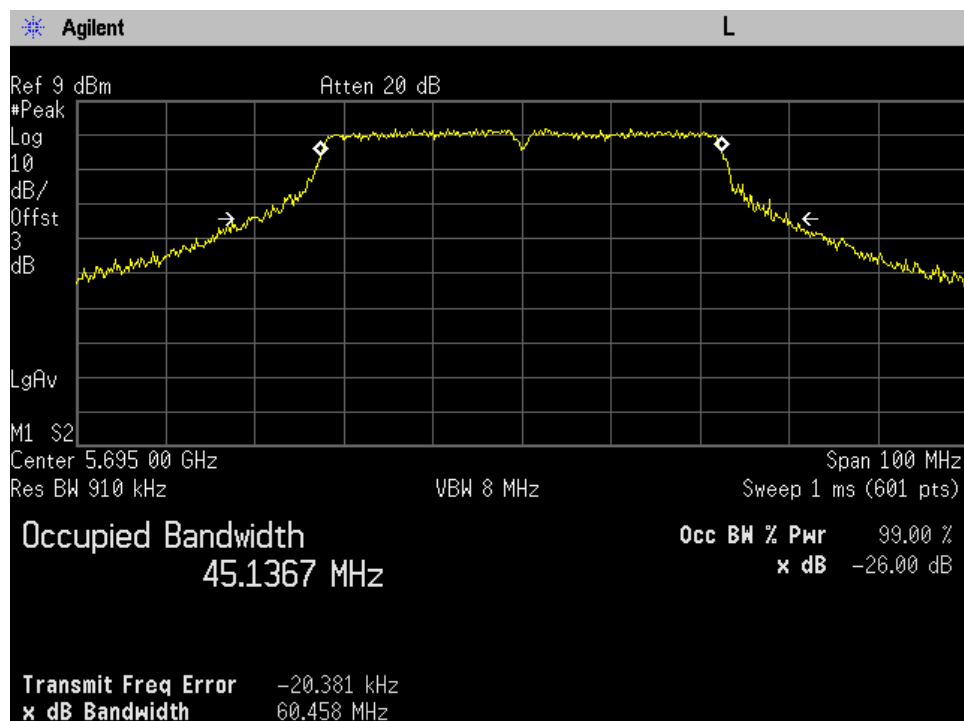




50MHz High Ch Port J8 OBW

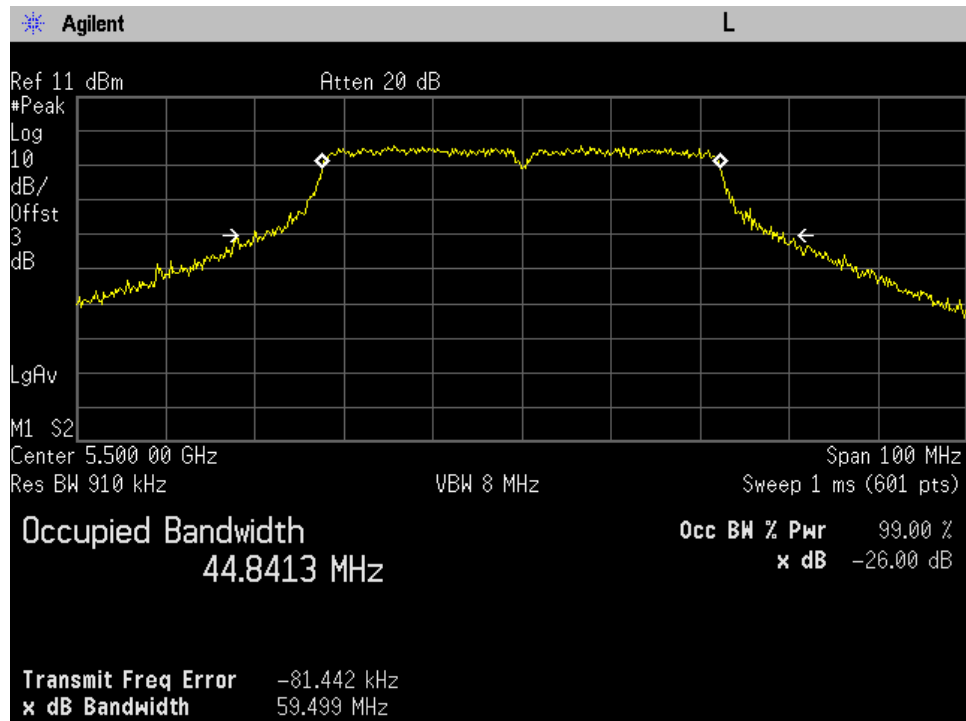


50MHz High Ch Port J7 OBW

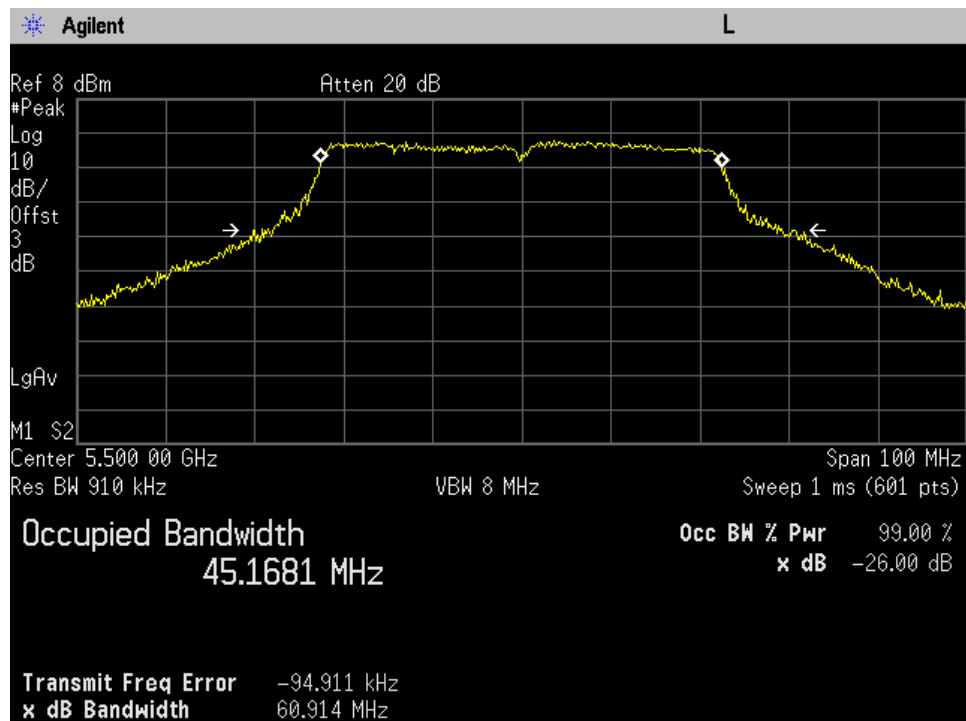




50MHz Low Ch Port J8 OBW

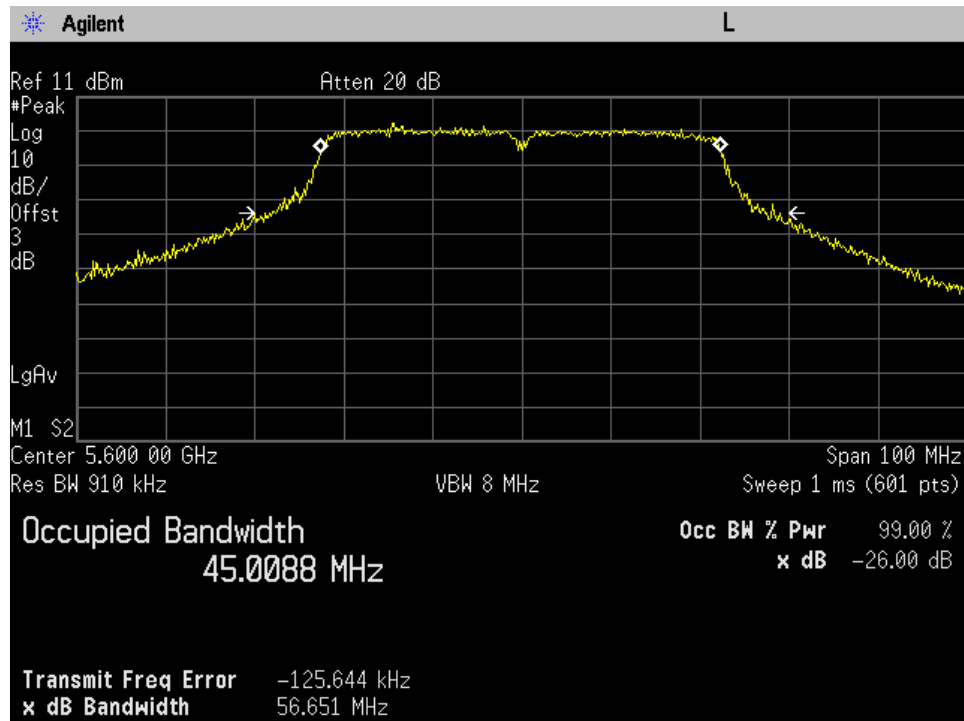


50MHz Low Ch Port J7 OBW

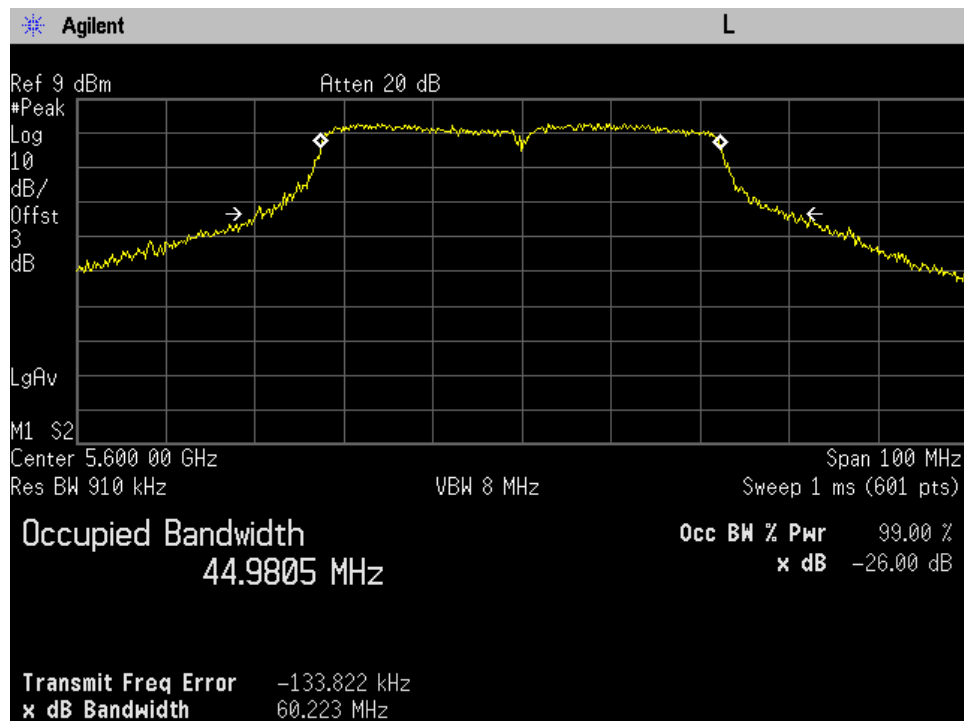




50MHz Mid Ch Port J8 OBW

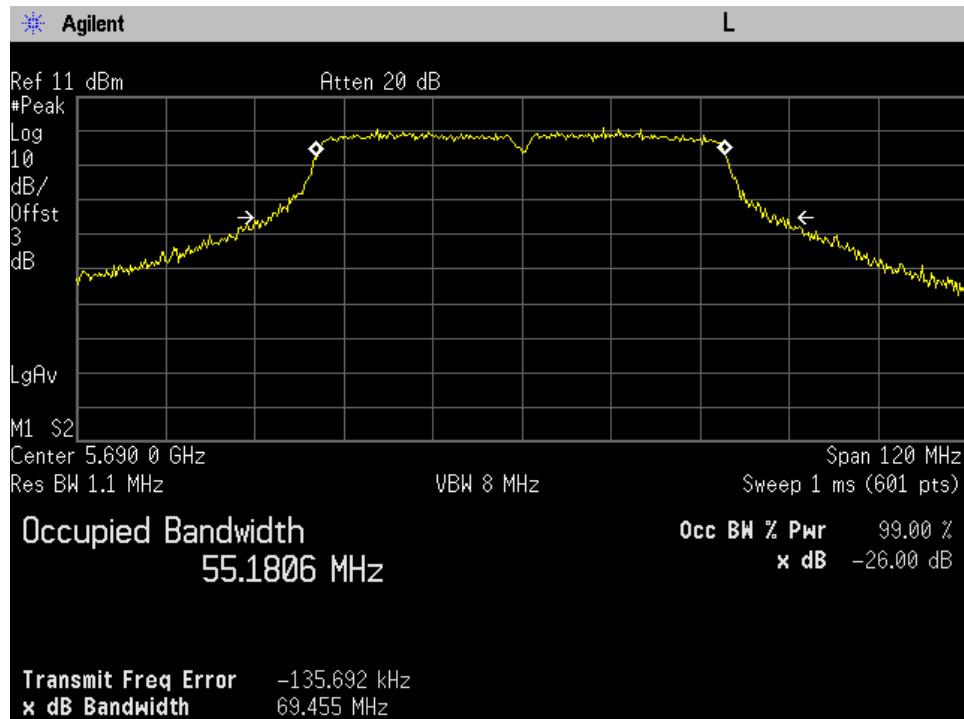


50MHz Mid Ch Port J7 OBW

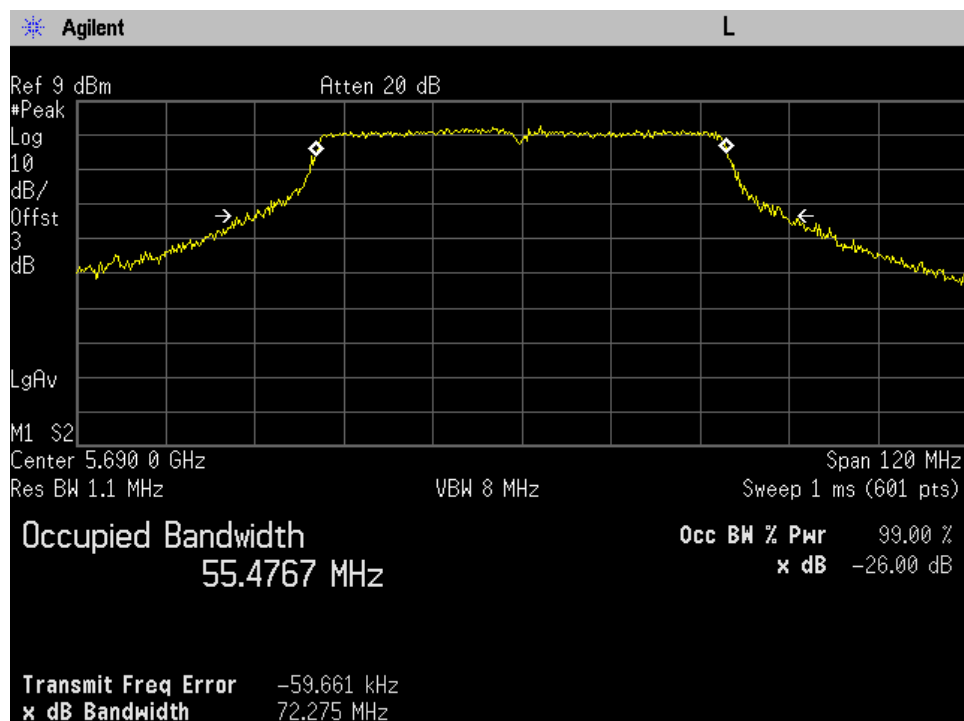




60MHz High Ch Port J8 OBW

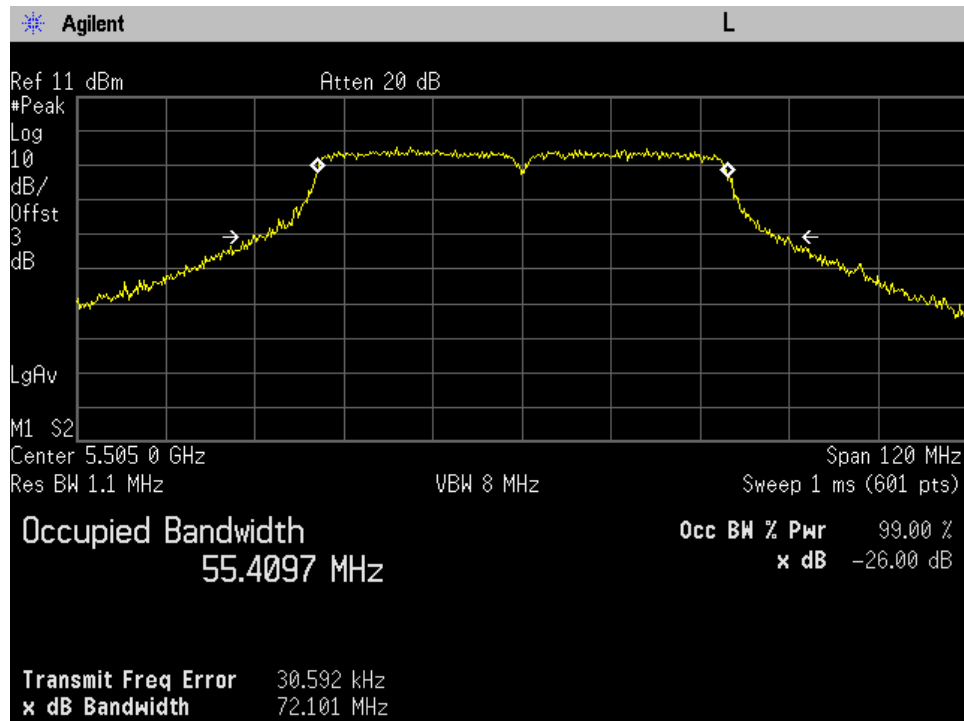


60MHz High Ch Port J7 OBW

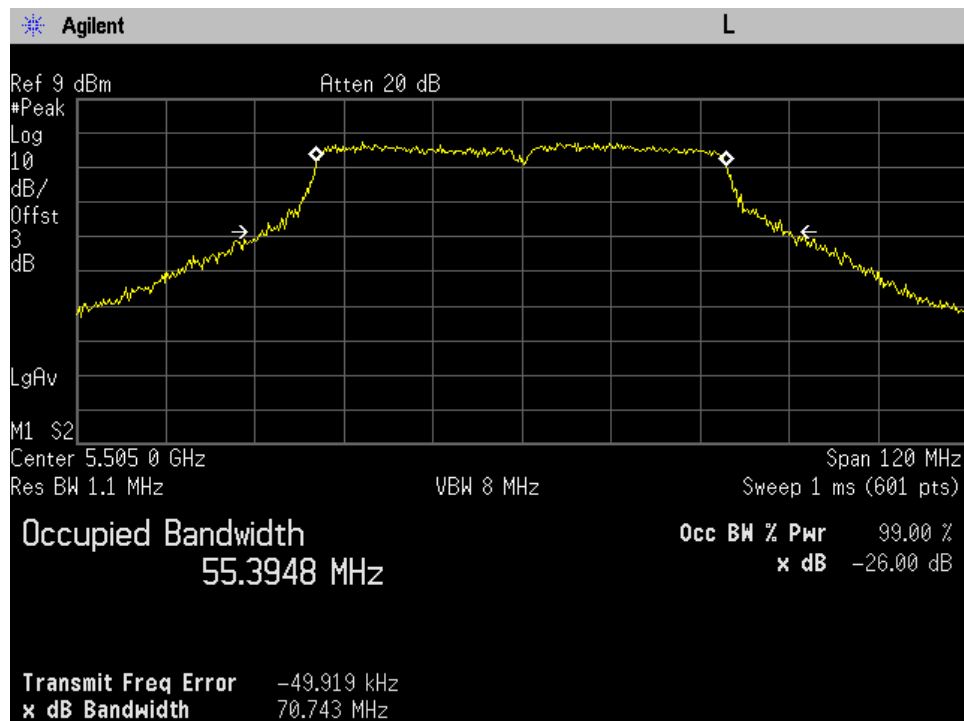




60MHz Low Ch Port J8 OBW

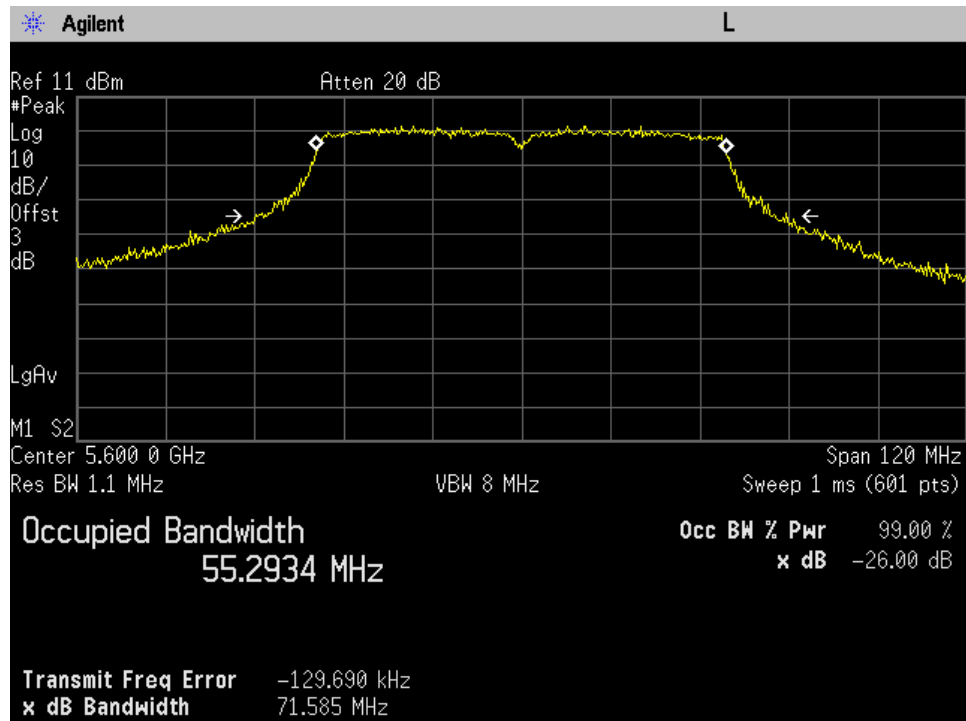


60MHz Low Ch Port J7 OBW

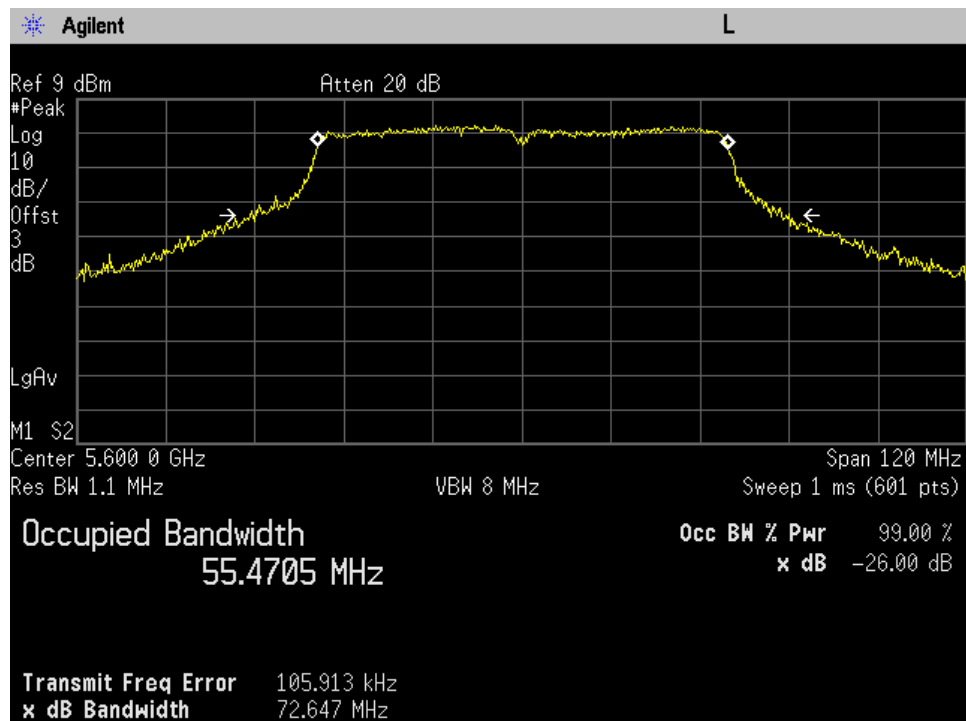




60MHz Mid Ch Port J8 OBW

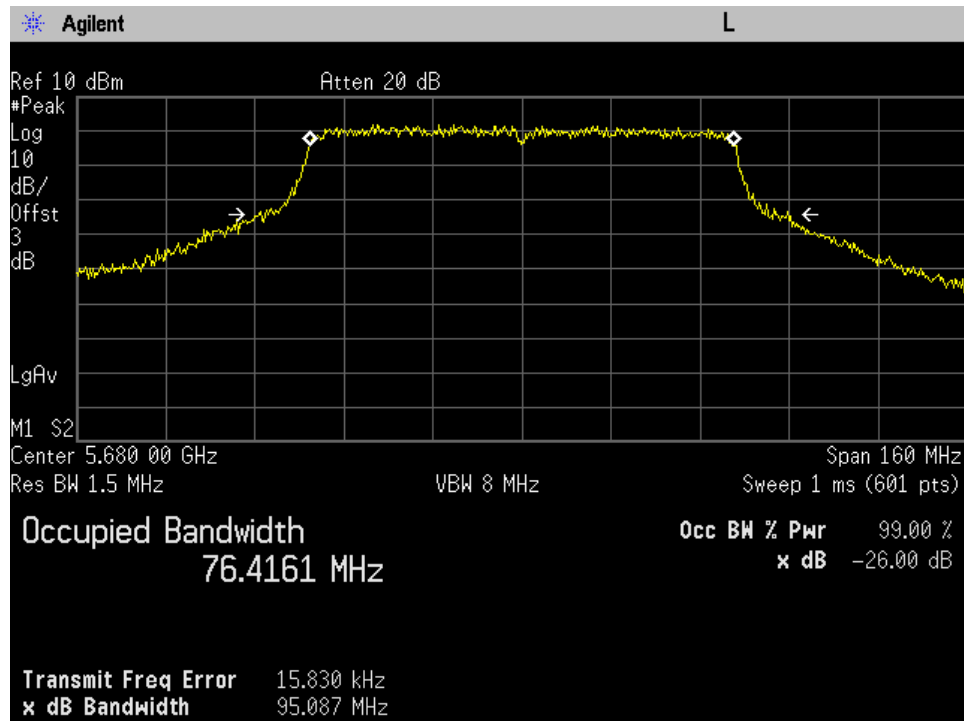


60MHz Mid Ch Port J7 OBW

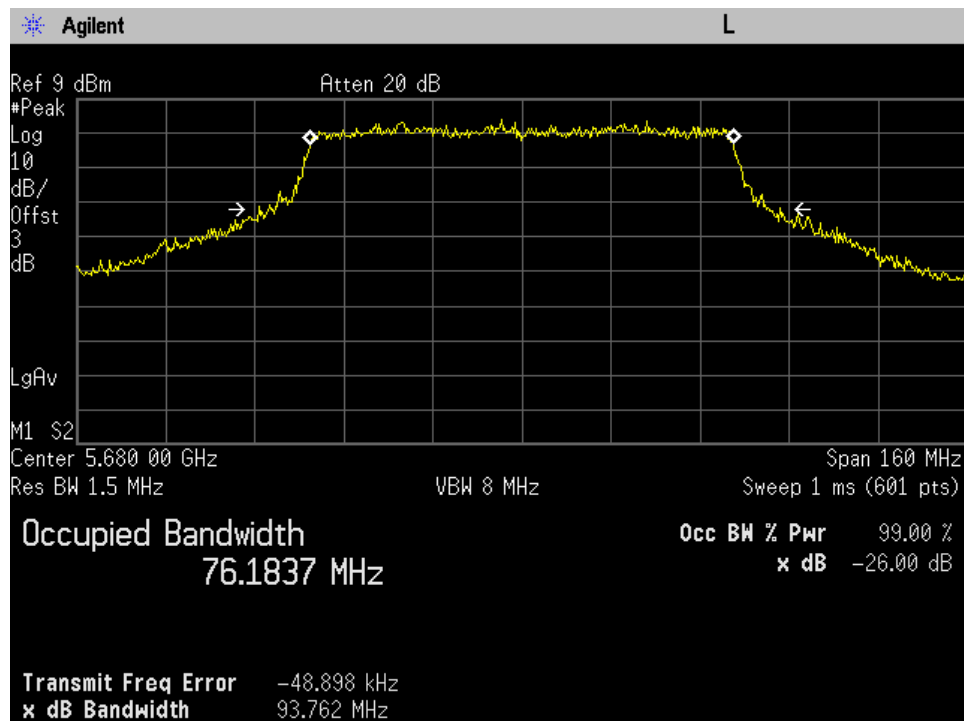




80MHz High Ch Port J8 OBW

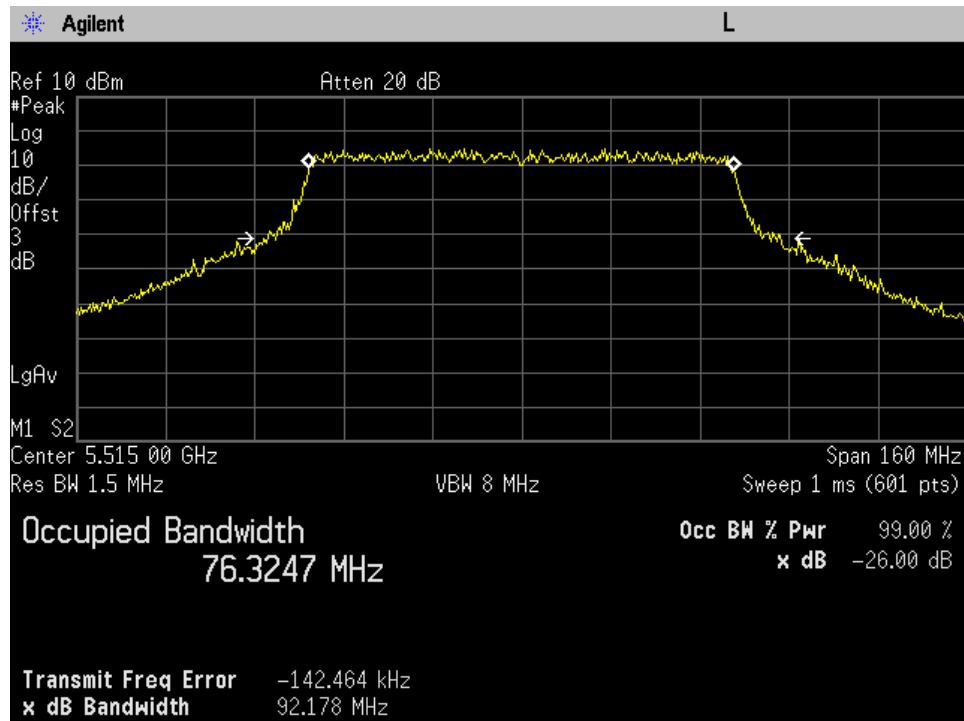


80MHz High Ch Port J7 OBW

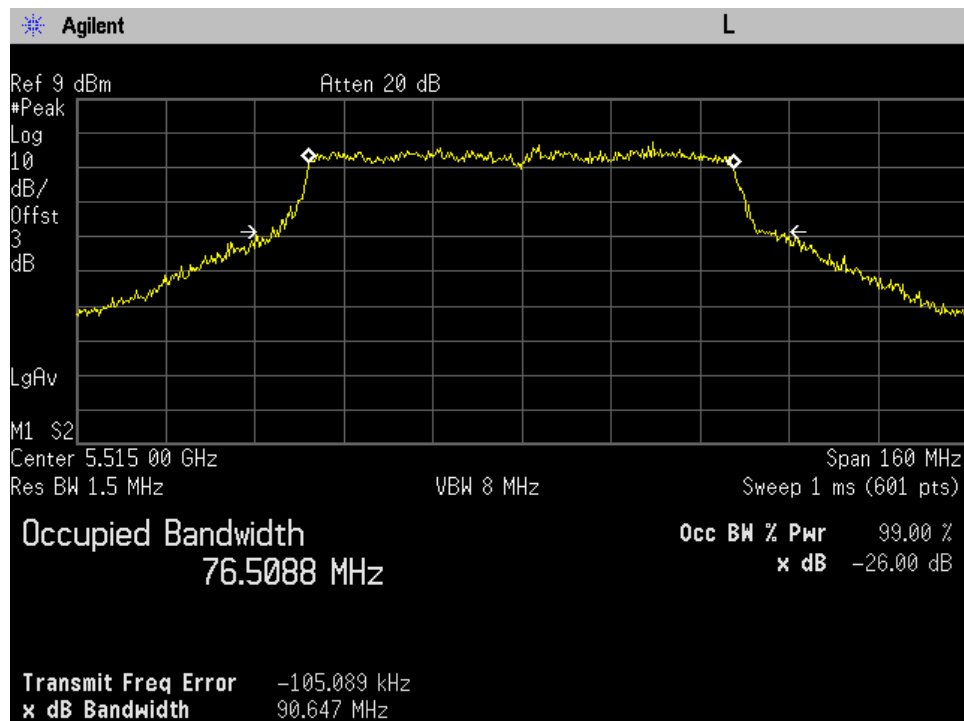




80MHz Low Ch Port J8 OBW

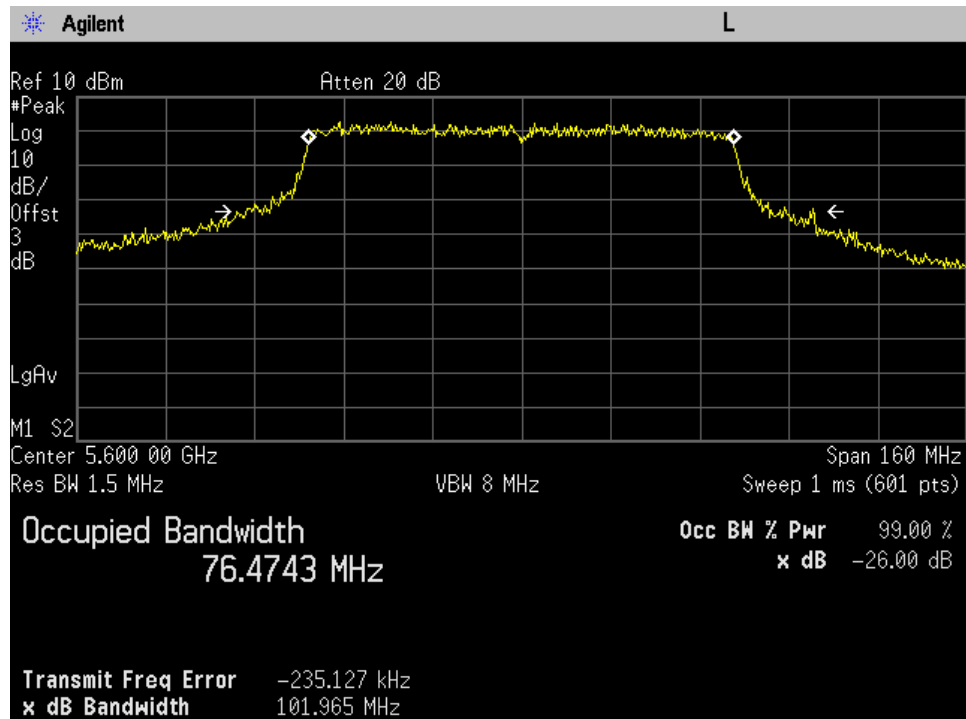


80MHz Low Ch Port J7 OBW





80MHz Mid Ch Port J8 OBW



80MHz Mid Ch Port J7 OBW

