Com WM RD

Dustin:

Datacard Variant
Hardware Specification

Status: Released/Reviewed

Document: 060928_Dustin_HW_Specification_datacard.doc

Version: 01/06

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Published by the
Com WM RD HW 1
Siemens AG
13629 Berlin
Germany

Released by:	Date / Sign
Roke Manor Research Limited	28 September 2006/ C Edwards

Document: Dustin_HW_Specification.doc
Archive Revision:

Authors: Chris Edwards, Rob Clifford, Michael Weyrauch
Date: 15.12.2004

Archive:

Revision History

Status	Date	Author	Reason for Change
01/01	02.08.2004	Chris Edwards	Created – based on Maja HW Spec
01/02	15.12.2004	Rob Clifford/Michael Weyrauch	Updated to latest Qualcomm architecture
01/03	01.06.2005	Russell Taylor	Minimum voltage changed to 3.1V
01/04	22.03.2006	Chris Edwards	Update
01/05	10.09.2006	Colin Drysdale	Remove references to the US build.
01/06	28.09.2006	Colin Drysdale	Updated the block diagrams and removed all references to Audio.

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1 Introduction

This document describes the hardware of the Dustin HSDPA PCMCIA Datacard. This document is split into the following sections:

- Reference Documents.
- Product Concept
- Circuit Concept
- Baseband Part
- RF Part
- Antenna
- Interfaces – Baseband to RF. Cardbus.
- Mechanical Construction
- PCB Construction

The Dustin data card will support;-

- GSM 850/900/1800/1900, GPRS Class 10
- EGPRS 850/900/1800/1900
- WCDMA 2100
- HSDPA (High Speed Downlink Packet Access)

HSDPA has been included into the latest releases (5 and above) of the 3GPP UE FDD specification /9/ and offers increased downlink performance with a focus on data communication such as file download, web browsing and audio/video streaming.

The Dustin card supports UE category 12 QPSK HSDPA that corresponds to 1.8MBits/Sec downlink rate. The theoretical peak data rate for HSDPA is 14MBits/sec. It can achieve this by changing the modulation scheme to 16-QAM. There are other techniques such as soft combing etc; however these techniques are outside of the scope of this document.

1.1 Dustin Router and PCC and Builds

There are two basic product variants as follows:-
Variant A:
Data Card HSDPA for usage in an UMTS Router (new product of key-customer) with audio interface, voice call functionality and SAT subset (device lock)
Variant B:
Data Card HSDPA for usage in a PC w/o audio interface, Embedded Firmware uploadable by End-User (EUU-End User Update)

THIS DOCUMENT COVERS VARIANT B ONLY. NO AUDIO FUNCTIONALITY IS INCLUDED IN THIS VARIANT.

ALSO NOTE THAT THE DATACARD VARIANT DOES NOT CONTAIN AN AUDIO HEADSET CONNECTOR.

1.2 Referenced Documents

/1/ ..\..\DesignData\Qualcomm\Reference_Schematics\Qualcomm_Baseband_MSM6275_Reference_Schematic_80-V8991-2_RevA.pdf

/2/ ..\..\DesignData\BoM\DataSheets\ComponentData\Qualcomm\Qualcomm_Polar6275_RF_Schematic80-V8991-1.pdf

/3/ ..\..\Test\Standards\3GPP TS 51.010-2 v5.9.0 [2004-07] R5 MS PICS (GSM & Edge).doc

/4/ ..\..\Test\Standards\ETSI TS 134 121 v5.3.1 [2004-04] R5 Terminal Conformance Specification Radio Tx & Rx (FDD).pdf

/5/ ..\..\DesignData\WorkingPapers\WP_0002 RF3164 evaluation working paper.doc

/6/ ..\..\DesignData\WorkingPapers\WP_0008 RFMD RF3163 850MHz WCDMA PA evaluation.doc

/7/ ..\..\DesignData\Mechanical\PCB Interface\040921 Dustin PCB Interface X72-LY-2246-006 IssM.pdf

/8/ ..\..\DesignData\Mechanical\Presentations\040720 Dustin Mechanical Concept.ppt

/9/ ..\..\Test\Standards\3GPP TS 25.101 v5.11.0 [2004-06] R5 UE Radio Tx & Rx (FDD).doc

/10/ ..\..\DesignData\WorkingPapers\WP_0009 Dustin SMPS selection for GSM PA.doc

/11/ ..\..\Test\Standards\PC Card Standard 8.0\PC Card Standard Vol2 Rel8.0 [2004-01] Electrical Specification.pdf

/12/ ..\..\DesignData\BoM\DataSheets\Qualcomm_MSM6275_Mobile_Station_Modem_80V-7955-1_RevB_DevSpec.pdf

/13/ Terms and Abbreviations

A/D	Analog-to-Digital Converter
AF	Audio Frequency
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AMR	Adaptive Multi Rate
ARP	Antenna Reference Point
ASIC	Application Specific Integrated Circuit
BB	Baseband
CPU	Central Processing Unit
CR	Change Request
CTR	Common Technical Regulation
DAI	Digital Audio Interface
/DCD	Data Carrier Detect
DFC	Digital Frequency Centering
DSB	Development Support Board
DSP	Digital Signal Processor
/DSR	Data Set Ready
/DTR	Data Terminal Ready
DTX	Discontinuous transmission
EFR	Enhanced Full Rate
EMC	Electro Magnetic Compatibility
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Equivalent Serial Resistance
ETS	European Telecommunication Standard
FE	Front-End
FFC	Flat Flexible Cable
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GSC	(Type of antenna connector)
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HW	Hardware
IC	Integrated Circuit
IF	Intermediate Frequency
IMEI	International Mobile Equipment Identity
I/O	Input/Output

ISO	International Standards Organization
ITU	International Telecommunications Union
LDO	Low Drop Out
LFBGA	Low-Profile Fine-Pitch Ball Grid Array
Li-Ion	Lithium-Ion
LNA	Low Noise Amplifier
LO	Local Oscillator
Mbps	Mbit per second
MMI	Man Machine Interface
MTBF	Mean Time Between Failures
NTC	Negative Temperature Coefficient
OC	Offset Compensation
OTP	One Time Programmable
PA(C)	Power Amplifier (Control)
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Power Down
PGC	Programmable Gain-Controlled Amplifier
PLL	Phase Locked Loop
PSU	Power Supply Unit
RAM	Random Access Memory
RF	Radio Frequency
/RING	Ring Indication
ROM	Read-Only Memory
RTC	Real Time Clock
/RXD	Receive direction
Rx	Receive direction
SAW	Surface Acoustical Wave Filter
SELV	Safety Extra Low Voltage
SIM	Subscriber Identification Module
SMS	Short Message Service
SRAM	Static Random Access Memory
SW	Software
TBR	Technical Based Regulation
TBD	To Be Defined
TBI	To Be Inserted
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
/TXD	Transmit direction

Tx	Transmit direction
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Quartz Oscillator
VSWR	Voltage Standing Wave Ratio

2 Compliance Documents

General documents:

- **99/05/EC** Directive of the European Parliament and of the council of 9 March 1999 on radio equipment and telecommunications terminal equipment and the mutual recognition of their conformity
- **89/336/EC** Directive on electromagnetic compatibility
- **73/23/EC** Directive on electrical equipment designed for use within certain voltage limits (Low Voltage Directive)
- **EN 301 489-1 v.1.2.1 (07-2000)** Electromagnetic compatibility and radio spectrum matters (ERM); Electromagnetic compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
- **EN 301 489-7 (09-2000)** Electromagnetic compatibility and radio spectrum matters (ERM); Electromagnetic compatibility (EMC) standard for radio equipment and services; Part 7:

  Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems (GSM and DCS)
- **EN 300 607-1** Digital cellular telecommunications system (Phase 2+); Mobile Station (MS) conformance specification; Part 1: Conformance specification (GSM 11.10-1 version 7.2.1 Release 1998)
  all tests according the up to date test spec: **3GPP TS 51.010-1 v.4.9.0** (formerly 11.10-1)
- **EN 301 511: v.7.0.1 (12-2000)** Global system for mobile communications (GSM); Harmonised standard for mobile stations in the GSM 900 and GSM 1800 bands covering essential requirements under Article 3(2) of the R & TTE Directive (1999/5/EC) (GSM 13.11 version 7.0.1)
- **EN 50 360 : 2001** Product standard to demonstrate the compliance of mobile phones with the basic restrictions related to human exposure to electromagnetic fields (300 MHz - 3 GHz)
- **ES 59005/ANSI/ IEEE C95.**1-1992 Considerations for evaluation of human exposure to Electromagnetic Fields (EMF) from Mobile Telecommunication Equipment (MTE) in the frequency range 30MHz-6GHz (relevant for applications)
- **92/59/EEC** Product Security
- **CISPR Pub. No I 16-1**
- **DIN 40839** (interference in automobiles)
- **CENELEC WGMTE** “Safety consideration for human exposure to e.m.f.s. from mobile telecommunication equipment (MTE) in the frequency range 30 MHz – 6 GHz”
- Internal Auxiliary Specification for VHF broadcasting range (-82 dBm) (due to interference to the FM frequency bands)
- **EN 55022** “Limits and methods of measurements of radio disturbance characteristics of information technology equipment”
- **DIN 54840** (plastic parts typify) (Remark: No toxic material like Cadmium of Tantalum in the mobile parts), CTR 31/32 (CTR: Common Technical Regulation)
- **IEC 60068** Environmental testing
- **DIN 40050** (climatic conditions & type of protection)
- **EN 60950 : 2000** Product safety according
- **EN 1811** Reference Test Procedure for Determining the Release of Nickel from Products that come into Direct and Prolonged Contact with the Skin
- **ISO/IEC 7816-3** Information Technology – Identification Cards – Identification Cards with contacts – Part 3: Electronic signals and transmission protocols
- **FCC 47 CFR Part 15, etc.**

3 Product Concept

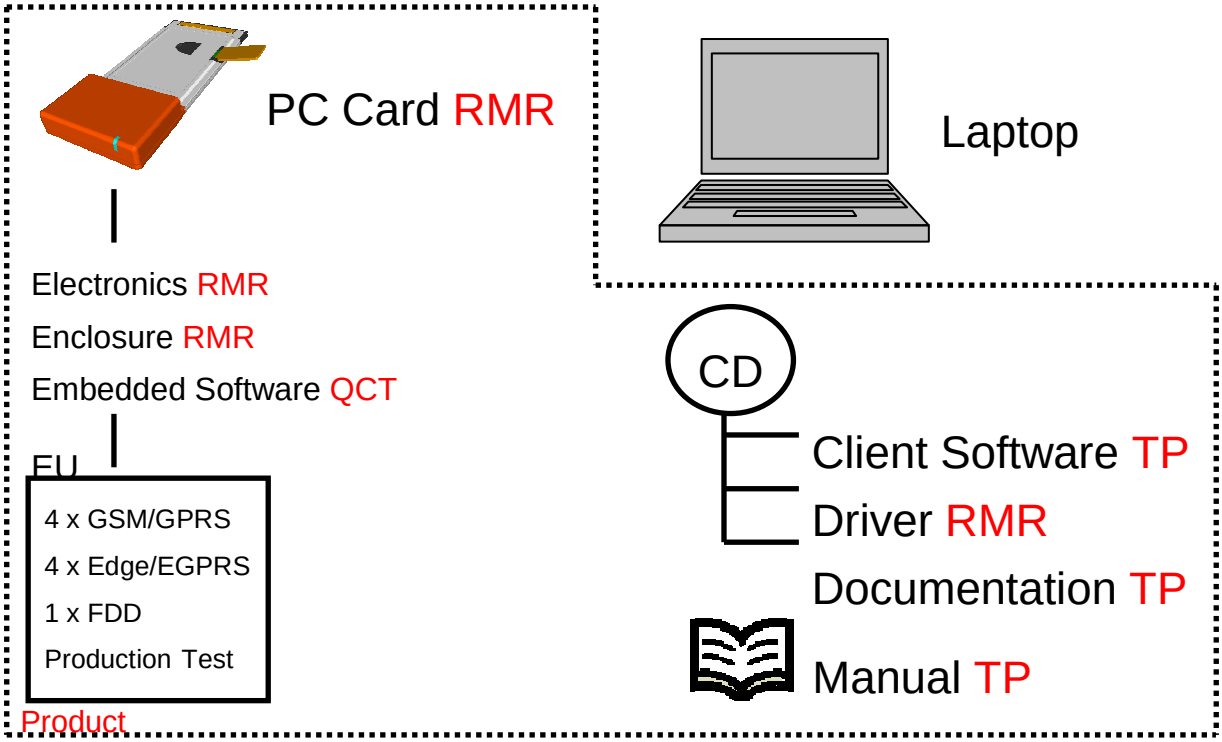
Dustin is a Dual Band WCDMA/QuadBand GSM/GPRS Cardbus Datacard and features high downlink speeds using HSDPA.

Dustin uses a Cardbus interface and will slot into a compatible Laptop personal computer so that data can be exchanged over mobile networks.

The main focus of HSDPA is Data communication, such as email, web browsing, data base retrieval, server access and audio and video streaming.

3.1 Block Diagram for Product Concept

The datacard connects to the laptop over the cardbus interface.



(TP = Third Party Client Developer)

Figure 3-1: Overview of product concept

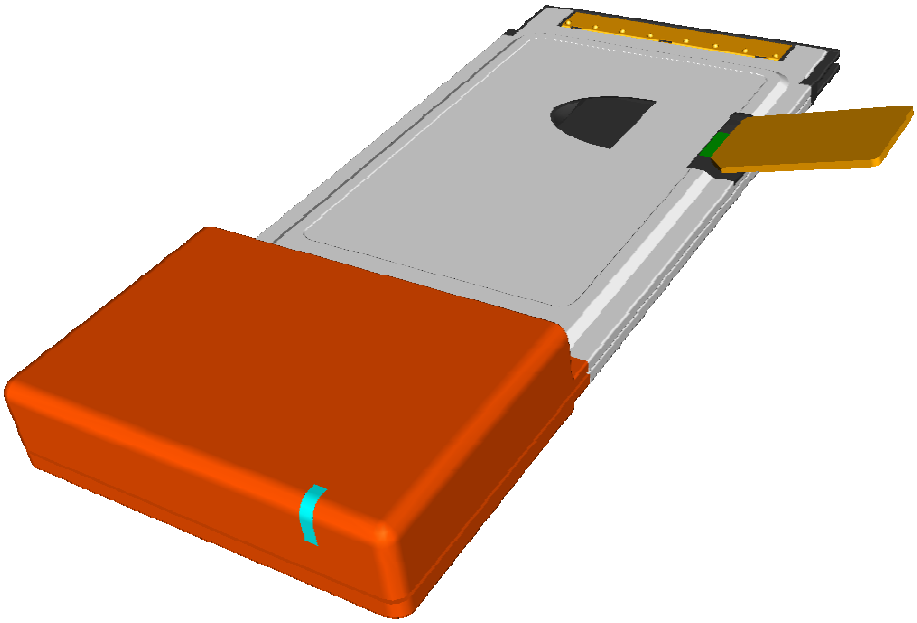


Figure 3-2 : Dustin Datacard

Figure 3-2 shows the datacard. The large red bulge at the bottom is a plastic cover for the antenna. The remainder of the card will slot into the laptop/PDA. The SIM card is shown as it slots into it's plastic holder.

4 Circuit Concept

The Circuit is based on the Qualcomm MSM6275 Chipset. This comprises Qualcomm Chips as follows;-

- MSM 6275 Baseband Chip
- PM 6650 Power Management
- RTR 6250 GSM Transceiver/WCDMA Transmitter
- RFL6202 WCDMA Low Noise Amplifier
- RFR6202 WCDMA Receiver

In order to interface to the Cardbus interface we are using a PCI to USB interface Chip from NEC

NEC UPD720101 Cardbus to USB Interface Chip

Power Amplifiers have been selected from RF MicroDevices and Anadigics for WCDMA and GSM/EDGE operation respectively.

4.1 Block Diagram for Circuit Concept

Figure 4-1 shows a block diagram of the Dustin datacard and illustrates the major functional components:

Baseband Block:

- WCDMA/GSM Controller MSM 6275 from Qualcomm
- Power supply (ASIC) PM6650 from Qualcomm
- Flash/SDRAM memory
- Cardbus to USB interface chip from NEC
- External Interface, 68-way connector cardbus interface

WCDMA/GSM RF:

- RF WCDMA Receiver (RFL6202 and RFR6202) from Qualcomm
- RF WCDMA Transmitter RTR 6250 from Qualcomm
- RF Power Amplifiers from RFMD and Anadigics.
- EPCOS receive SAWs (according to variant – see below)
- Skycross Antenna

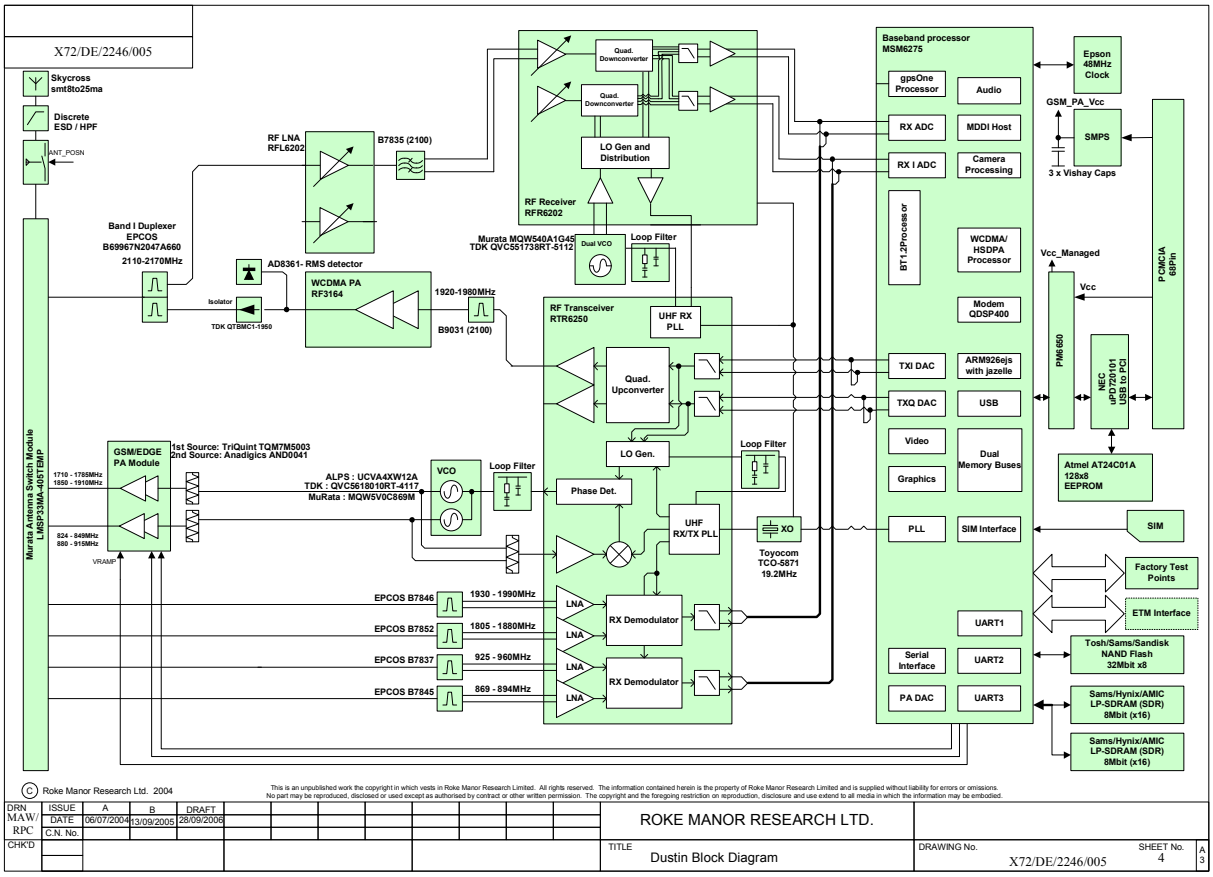


Figure 4-1: Block diagram for Dustin

4.2 Functional Units

4.2.1 Baseband Part

The baseband consists of the following parts:

- WCDMA/GSM Baseband Processor
- Power Supply (ASIC)
- Nand Flash memory
- SDRAM Memory
- PCI to USB interface

The RF interface and the various low-frequency analog audio and digital interfaces are integrated in the MSM6275 baseband IC. The operating software controls the entire signal processing on the module from MSM6275 and operates the interfaces.

In addition to complex data signals, the RF interface (in the block diagram Figure 4-1) also contains control signals for the RF part.

The power supply of Dustin, its activation, deactivation, reset generation and SIM voltage supply are handled by the PSU-ASIC PM 6650.

The SIM Interface is provided by MSM6275, which also supplies the control signal for switching the SIM supply voltage on/off.

4.2.2 RF Part

The RF part is designed for quad-band GSM use and Single Band WCDMA use and supports GSM850, EGSM900 DCS1800 and PCS1900 as well as WCDMA 2100. The key components of the RF part are the transceiver IC RTR6250 and WCDMA receiver IC RFL 6202/RFR6202 from Qualcomm. Beside these IC's the radio part comprises the following function blocks:

- PA's from RFMD and Anadigics
- EPCOS SAW filters and Duplexers.

A more detailed description of the RF part is given in chapter 6.

4.2.2.1 Internal Interfaces

- Internal interfaces: Baseband interface – RF part. Please see section 7.1.

4.2.2.2 External Interfaces

- Cardbus Interface

The datacard is supplied with power and interfaces with the Host (laptop) via the 68-way cardbus connector. The host controls the MSM6275 Baseband using USB but in order to do this a PCI to USB converter chip is incorporated in the device and the datacard is controlled over this interface

- SIM interface with additional ground connection CCGND and CCIN signal (ChipCard inserted).

- External RF connector for conducted measurements.

5 Baseband (BB) Part

5.1 Baseband Processor (MSM 6275)

5.1.1 Processor Core

The MSM6275 device integrates the ARM926EJ-S™ processor, offering the ARM® Jazelle™ Java® hardware accelerator, two low-power, high-performance QDSP4000™ digital signal processor (DSP) cores, hardware acceleration for video, imaging, and graphics, and a wideband stereo codec to support enhanced digital audio applications. The hardware acceleration eliminates the need for the multimedia companion processors normally required for video and audio-based applications that support MP3 music files, a MIDI synthesizer, video and still-image record and playback, and 2D/3D graphics functions.

The MSM6275 IC also integrates gpsOne® functionality, featuring enhancements by SnapTrack, Inc. to support assisted and standalone GPS. This enables a wide variety of location-based services and applications, including points of interest, personal navigation and friend finder.

Integrated into the MSM6275 chipset solution are Bluetooth® wireless connectivity and USB on-the-go (OTG) host controller functionality, allowing seamless communication directly with printers, digital cameras, keyboards, and other accessories.

The MSM6275 device includes support for the SecureMSM™ security solution:
It incorporates an unchangeable hardware ID unique to each MSM.
The result is a very robust platform securing OMA DRM v2.0 services, CPRM, and e-commerce transactions. IMEI freeze and SIM lock protection benefit from hardware security.

The MSM6275 device is offered in a 14 x 14 mm, 409-ball, 0.5 mm pitch, lead-free CSP package.

5.1.1.1 µC Section

Industry standard ARM926EJ-S embedded microprocessor subsystem

- 16 kB instruction and 16 kB data cache
- Instruction set compatible with ARM7TDMI
- ARM version 5TEJ instructions
- Higher performance 5 stage pipeline, Harvard cached architecture
- Higher internal CPU clock rate with on-chip cache
- Java hardware acceleration
- Enhanced memory support
- 75 MHz bus clock for SDRAM and PSRAM
- 32-bit SDRAM and PSRAM
- Dual memory buses separating the high-speed memory subsystem (EBI1) from low-speed
- peripherals (EBI2) such as LCD panels
- 1.8 V or 2.6 V memory interface support (excluding EBI1)
- Burst mode NOR FLASH or SRAM
- Burst mode is supported on all four EBI1 chip selects.
- NAND FLASH memory interface:
  - 8/16 bit data I/O width NAND FLASH support
  - 512-byte / 2 KB page-size support
  - Support up to two NAND Flash
  - Boot from NAND
- Internal watchdog and sleep timers, see chapter 5.1.9

5.1.2 Boot Mode Configuration

The MSM6275 is configured in the following way:

Pin	MSM6275 Pin no.	Description
BOOT_MODE3	AD1	Determines normal or trusted boot mode of the chip. Function 0: Normal boot **1**: Trusted boot (used on Dustin)
BOOT_MODE2	AE22	Determines NAND I/O configuration of the chip. Function 0 = 8-bit **1** =16-bit (used on Dustin)
BOOT_MODE	AE21	Determines NOR or NAND boot mode of the chip. Function 0: boot from NOR flash on EBI1 **1**: boot from NAND flash on EBI2 (used on Dustin)
MODE2	T21	Determines operating mode of the chip. MODE[2:0] Function **000** Native, ARM9 JTAG (used on Dustin) 001 Native, ARM9 JTAG, ETM 010 Native, MSM JTAG (BST) 011 Reserved 100 Reserved 101 Reserved 110 Reserved 111 Reserved
MODE1	U23	
MODE0	Y23	

Table 5-1: Boot Mode Configuration

5.1.3 HW-ID

There is a 4-bit HW-ID realized on Dustin. Via population/not-population of pull-up/down resistors HW-ID can be set. The following table shows the meaning of each HW-ID's bit.

Pin	MSM6275 Pin no.	Testpoint	Description
GPIO105	AD2	TP623	Reserved **0**: (pull-down R2036) 1: (pull-up R2033 to VREG_MSME)
GPIO104	AE3	TP622	Determines EU/US variant of Dustin. 0 = EU variant (pull-down R2032) 1 = US variant (pull-up R2031 to VREG_MSME)

GPIO27	N16	--	Reserved **0**: (pull-down R2038) 1: (pull-up R2035 to VREG_MSMP)
GPIO26	K21	--	Reserved **0**: (pull-down R2037) 1: (pull-up R2034 to VREG_MSMP)

Table 5-2: HW-ID

5.1.4 MSM6275 Power domains

The MSM6275 contains 4 separate power domains, P1, P2, P3, and P4. The following table shows the connections on Dustin. See chapter Overview of Supply Voltages for voltage values.

Power domain	Connected to Supply Voltage
P1	VREG_MSME
P2	VREG_MSME
P3	VREG_MSMP
P4	VREG_MSMP

Table 5-3: Power domains

5.1.5 Reset

The following figure shows Dustin's reset concept.

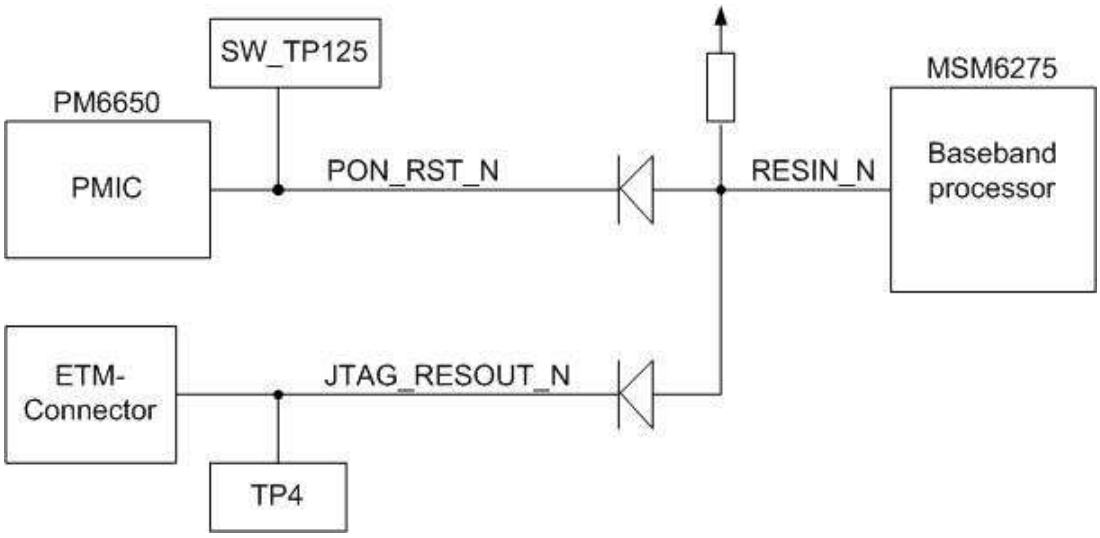


Figure 5-1: Reset concept

5.1.6 Peripherals

interfaces
- USB On-the-Go core, supports both slave and host functionality

- Three universal asynchronous receiver transmitter (UART) serial ports
- USIM controller (via UART), see chapter 5.1.8
- Integrated 4-bit secure digital (SD) controller for SD and Mini SD cards (not used in Dustin)
- Parallel LCD interface (not used in Dustin)
- General-purpose I/O pins
- High-speed, serial MDDI, which optimizes the interconnection cost between the MSM and LCD panel (not used in Dustin)

multimedia interfaces
- Two QDSP4000 DSPs
- Integrated Java and 2D/3D graphics accelerator with Sprite engine
- Integrated USB host controller functionality
- High-quality digital camera processing, supporting CCD or CMOS image sensors up to 4-megapixel

- Dedicated support for market-leading codecs such as MPEG-4, H.263, H.264
- Integrated stereo wideband CODEC for music/digital clips
    - 72-polyphony MIDI wave table synthesizer for high-quality music playback through the MSM6275 integrated wideband codec
- Video telephony services

- Location-based services
    - Integrated gpsOne processing
    - Standalone gpsOne mode in which the handset acts as a GPS receiver

- CMX (text, picture, and MIDI streaming)
    - 72 voices
    - 44 kHz sampling
    - 512 kB wave table
    - Morphing player and Free A.T.
    - PNG decoder
    - Pitch bend range support
    - MLZ decoder
    - Integrated PNG/SAF A.T.

5.1.7 NAND-FLASH + SD-RAM

An external Flash memory device is used as non-volatile, erasable and reprogrammable (software update) program memory for MSM6275 and for storing user data (parameter settings) and alignment data for the device.

	Dustin	
Parameter	**NAND-Flash, 256 Mbit (32Mx8)**	**SD-RAM, 2 x 256Mbit (2 x 4Mx16x4, organized as 4Mx32x4)**
Manufacturer	Samsung	Samsung
Order name	K9F5608Q0C-DIB0	K4M56163PE-BG1L
Package	63-Ball TBGA 0.8mm pitch (11 x 9)	54-Ball FBGA 0.8mm pitch (11 x 8)
Data bus	8-Bit	16-Bit
Product family	1.8V	1.8V
Boot block		n.a.
Erase Cycles per Block	100k	n.a.
Temperature Range	-40°C to +125°C (absolute maximum ratings)	-25°C to +85°C

Table 5-4: Memory outline, sample run A1/A2

	Dustin	
Parameter	**NAND-Flash, 256 Mbit (16Mx16)**	**SD-RAM, 512Mbit (4Mx32x4, organized as 16Mx32)**
Manufacturer	Samsung	Samsung
Order name	K9F5616Q0C-JIB0	K4M51323PC-DG1L
Package	63-Ball TBGA 0.8mm pitch (11 x 9)	90-Ball FBGA 0.8mm pitch (11 x 13)
Data bus	16-Bit	32-Bit
Product family	1.8V	1.8V
Boot block		n.a.
Erase Cycles per Block	100k	n.a.
Temperature Range	-40°C to +125°C (absolute maximum ratings)	-25°C to +85°C

Table 5-5: Memory outline, sample run B1

5.1.8 SIM – Interface

MSM6275 has an integrated SIM/USIM interface compatible with the ISO 7816 IC card standard (see /12/) . The signals “USIM_RST”, “USIM_CLK”, and “USIM_DATA” are routed through the power management IC in order to use its built-in level translators for interfacing the MSM6275 to the external SIM/USIM.

The power management IC provides a regulated SIM/USIM supply voltage “VREG_RUIM”, which is controlled by the MSM6275.

Signal	Description	MSM6275 pin no.
USIM_RESET	Chip card reset, provided by baseband processor MSM6275	G6
USIM_CLK	Chip card clock, various clock rates can be set in the baseband processor	F4
USIM_DATA	Serial data line, input and output.	E4
VREG_RUIM	SIM/USIM supply voltage (RUIM = Removable User Identity Module)	fed by PM6650
GND	Ground connection	-
VPP		TP24, TP618

Table 5-6: SIM card reader’s signals

The signals “USIM_RST”, “USIM_CLK”, and “USIM_DATA” are protected by an “EMIF03” EMI and ESD protection circuit (Z29). Additional spark gaps are implemented at signals “USIM_RST”, “USIM_CLK”, “USIM_DATA”, and “VDD”.

5.1.9 Watchdog Control

The MSM6275 contains an internal watchdog unit which can be disabled by either

- populating the 0-Ohm resistor R43 (schematic's page 11, 1D) or by
- providing GND-potential to production testpoint TP10 (schematic's page 11, A8)

R43 and TP10 are connected to Pin "WDOG_EN", AE17, internal pull-Up.

5.1.10 Clock Generation

5.1.10.1 TCXO

All required system clocks are derived from a 19.2MHz clock rate ("TCXO"), which is generated in the RF part and fed via the PM6650 into MSM6275.

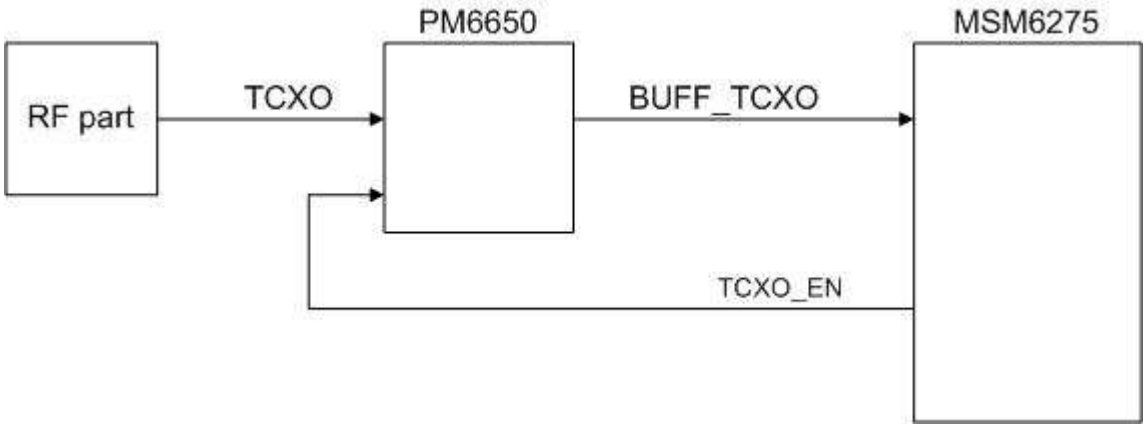


Figure 5-2: TCXO path

The signal "TCXO" is fed to the PM6650 via capacitive coupling.

5.1.10.2 Sleep Clock

A 32.768 kHz "SLEEP_CLK" signal is generated in the PM6650 and fed into the MSM6275.

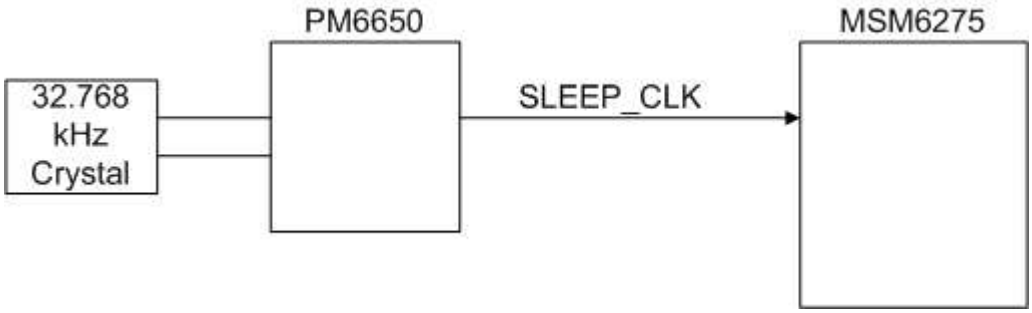


Figure 5-3: Sleep Clock path

5.1.10.3 48 MHz Clock

A 48 MHz crystal oscillator is used to generate the clocking for the CardBus-to-USB bridge's and the MSM6275's USB sections.

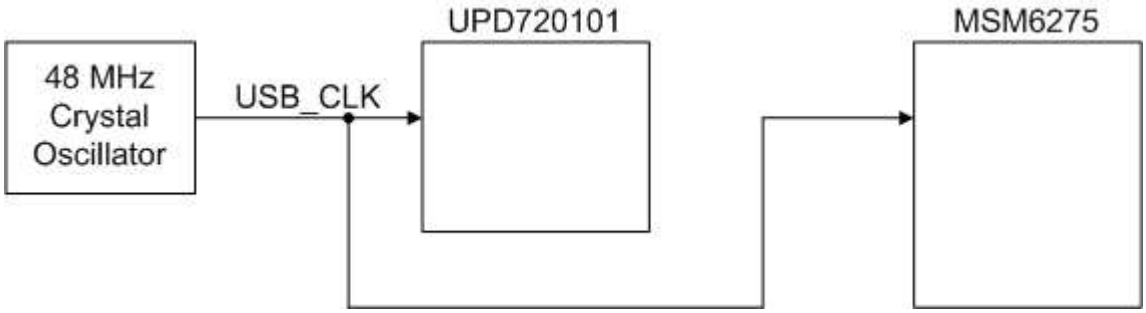


Figure 5-4: 48 MHz path

The signal "USB_CLK" is fed to the MSM6275 through a voltage divider and capacitive coupling.

5.1.11 Thermistors

At 3 dedicated positions the ambient/PCB temperature can be measured. 22k-Ohm thermistors are used as temperature sensors. With 47k-Ohm resistors they build voltage dividers which are connected to 3 HKADC input pins. The voltage dividers are fed by VREG_MSMA to achieve precise temperature measurements.
HKADC is the MSM6275's on-chip 8-bit analog-to-digital converter. The following table shows the connections to the ADC's multiplexed inputs.

Signal	MSM6275 Pin no.	Analog input	Testpoint	Position on PCB / measured temperature
MSM_THERM	Y21	HKAIN4	SW_TP17	Close to MSM6275, top side
PA_THERM	V19	HKAIN3	TP99	Under CDMA-PA, bottom side
RF_THERM	AA23	HKAIN1	TP98	Under 19.2MHz-VCTCXO, bottom side

Table 5-7: Thermistors

5.1.12 Serial Interface

The MSM6275 contains 3 universal asynchronous revceiver transmitter (UART) serial ports. One of them, UART1, is used on Dustin. The respective signals are connected to 4 production testpoints. The following table contains the details.

Signal	MSM6275 pin no.	Description	Testpoint
UART1_TXD	L26	UART transmit serial data, output at MSM6275	TP140
UART1_RXD	M23	UART receive serial data, input at MSM6275	TP139

UART1_CTS	P16	UART clear-to-send signal, input at MSM6275	TP141
UART1_RFR	P21	UART ready-for-receive signal, output at MSM6275	TP142

Table 5-8: UART1 signals

5.1.13 LEDs

Currently there is one double-LED in the design to illustrate Dustin's operating status.

The PMIC's built-in current sinks are used to drive the LEDs. The following table shows the connections, colors and currents of the LEDs.

LED	PMIC pin no.	PMIC pin name	Description
Blue (V722)	22	LCD_DRVn	max. 10mA LED current, driving PMIC current can be adjusted in 10mA steps.
Green (V722)	21	GP1_DRVn	max. 10mA LED current, driving PMIC current can be adjusted in 5mA steps.

Table 5-9: LEDs

The LED operates as follows:

- When searching for a network LED flashes green at 2Hz
- When registered with a GSM network, green LED goes steady
- When registered with a WCDMA network, blue LED goes steady
- During long periods of inactivity, the LEDs are extinguished

5.2 CardBus to USB Bridge

A CardBus to USB bridge from NEC (µPD720101) is chosen for interfacing Dustin to the host PC.

This integrated circuit complies with the Universal Serial Bus (USB) Specification Revision 2.0, Open Host Controller Interface (OHCI) Specification for full-/low-speed signaling, and Intel's Enhanced Host Controller Interface (EHCI) Specification for high-speed signaling. It works up to 480 Mbps.
3 host controller cores with PCI interface and USB2.0 transceivers are integrated into this single chip.

The bridge's system clock is derived from the 48 MHz crystal oscillator, see 5.1.10.3.

Only USB port 1 is used to let the host PC communicate with the baseband processor.

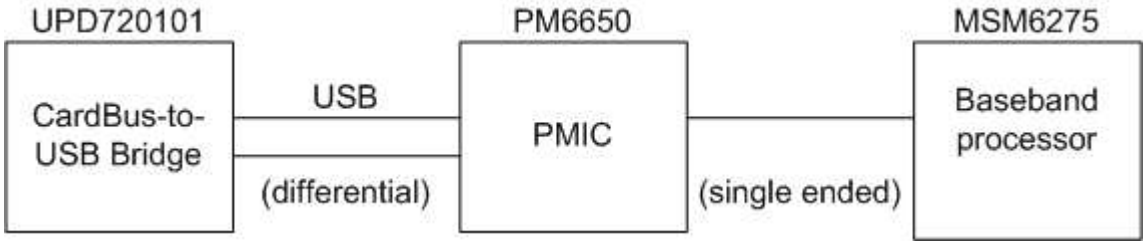


Figure 5-5 USB path

A 144-pin plastic, 0.8 mm pitch (12 x 12) FBGA package is used.

For storing the bridge's configuration data (Dustin's manufacturer ID, clock source, …) a serial I^2C-EEPROM (e.g. Atmel, AT24C01A) is used.

5.3 Power Supply

Dustin is power supplied by the host (Laptop, PC) via the 68-way CardBus connector X1515 (2 pins 3.3V and 4 pins GND).

As the CardBus standard allows a maximum current drawn from the host of about 1A Dustin is designed respectively.
In order to provide the required peak currents a SMPS (Switched-Mode Power Supply) has been incorporated into the design which boosts the GSM PA's supply voltage to 3.6V and limits the inrush current to less than 1A.

All power supply issues are handled by the Power Management IC ("PMIC") PM6650. This

device provides the following features:

- Stabilization of the baseband's supply voltages using low drop linear voltage regulators
- Generation of various supply voltages for the RF part
- USIM/SIM supply voltage
- Level translation for the MSM 6275's USIM/SIM interface signals

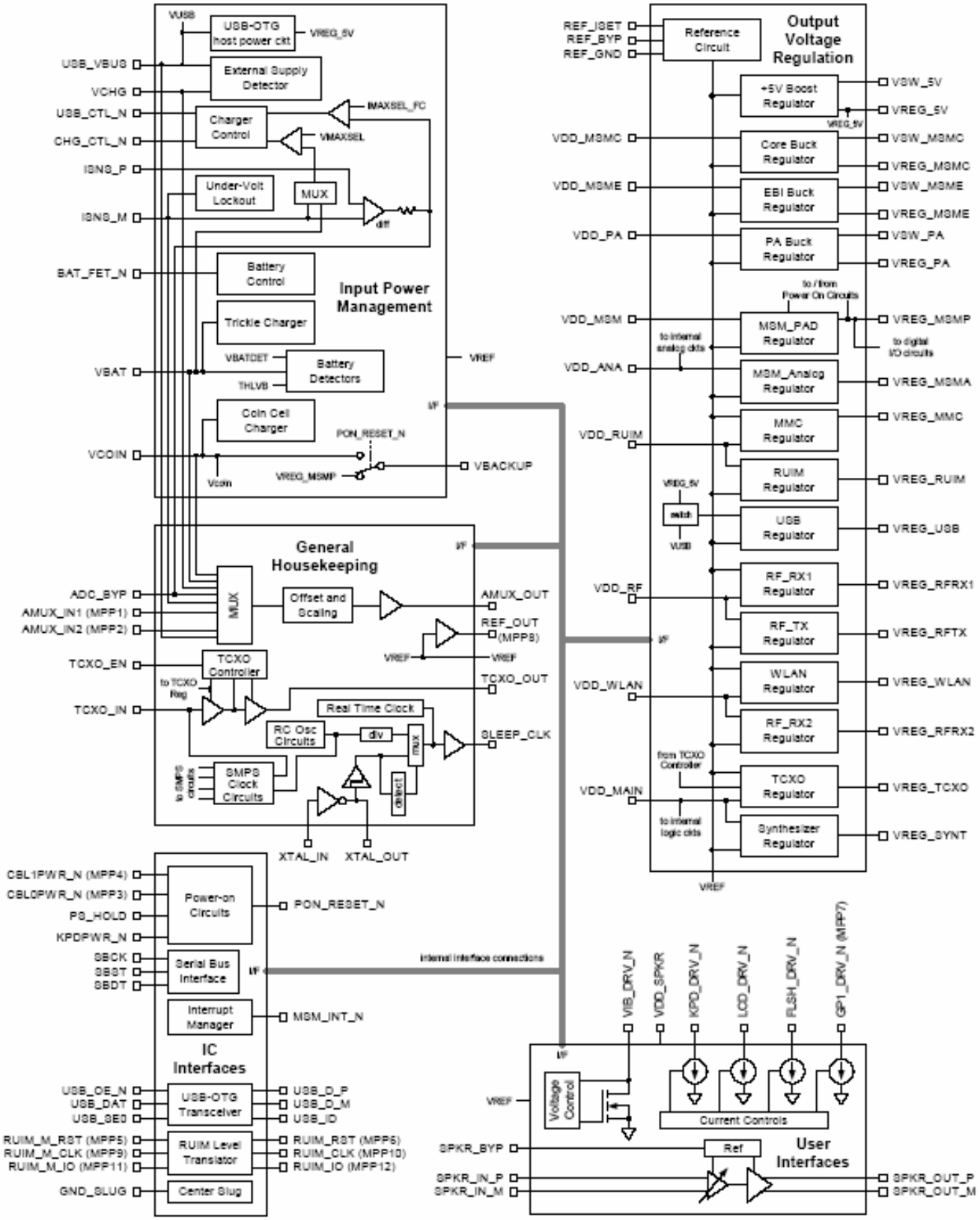


Figure 5-6: Power Management IC PM6650 - Functional Diagram

5.3.1 Overview of Supply Voltages

Voltage	Parameter	Minimum	Typical	Maximum	Testpoint
3.3V_IN	Supply voltage of Dustin, supplied by host (Laptop, PC)		3.3V		TP144, TP145
A3.3V	Analogue supply voltage for CardBus-to-USB bridge		3.3V		--
3.3V	Main supply voltage		3.3V		TP109
VREG_MSME	Switched-mode power supply for NAND-Flash and SD-RAM		1.8V		TP612
VREG_MSMP	Linear regulated supply voltage for MSM6275 peripheral functions, ETM debugging	2.7V (Transceiver)	2.85V	3.0V (Transceiver)	TP3, TP26, TP17
VREG_MSMA	Linear regulated supply voltage for MSM6275 analogue functions	tbd	tbd	tbd	TP110
VREG_MSMC	Switched-mode power supply for MSM6275's core voltage	tbd	1.3V	Tbd	TP114
VREG_UIM	Linear regulated supply voltage for USIM/SIM		1.8V/ 3.3V		
VREG_JTAG	Not built, yet	--	--	--	--
3.6V_OUT	Supply voltage for GSM/GPRS/EDGE PA	3.0V (PA)	3.6V	4.8V (PA)	TP150
VREG_SYNTH	Linear regulated supply voltage for frequency synthesizer circuits	2.7V (Transceiver)	2.85V	3.0V (Transceiver)	TP105, TP30
VREG_TCXO	Linear regulated supply voltage for TCXO	2.85V (TCXO)	3.0V	3.15V (TCXO)	TP31
VREG_RFTX	Linear regulated supply voltage for transmitter circuits	2.7V (Transceiver)	2.85V	3.0V (Transceiver)	TP106, TP29
VREG_RFRX_0	Linear regulated supply voltage for primary receiver circuits	2.7V (Receiver)	2.85V	3.0V (Receiver)	TP27
VREG_RFRX_1	Linear regulated supply voltage for diversity receiver circuits				TP28
V_CDMA_PA	Switched-mode power supply for WCDMA-PA	3.2V (PA)	3.4V	4.2V (PA)	TP25
GND	Ground		0V		TP146, TP147, TP148

Table 5-10: Values and tolerances of supply voltages for MSM6275 and RF part

5.3.2 RF Power Supply

Apart from the GSM PA Power supplies for the RF are provided by the Power management chip

PM6650 as per the Qualcomm Reference Schematic /1/.

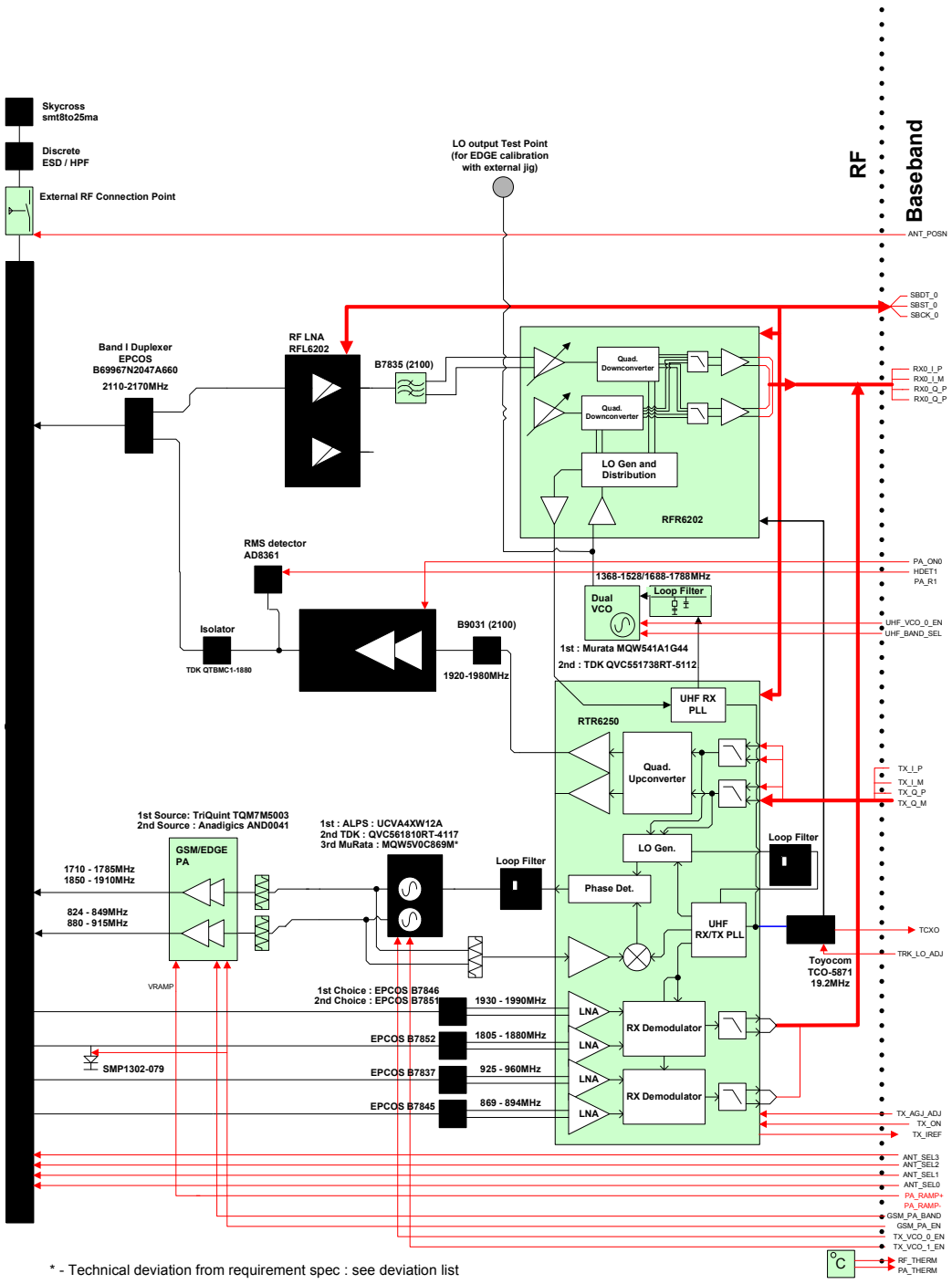
For the GSM PA's it is necessary to provide high peak currents during the transmit cycle due to the bursty nature of GSM. To achieve maximum power peak currents up to 2A may be required. The Cardbus standard allows only 1A peak. In order to meet this standard a Switched mode Power supply (SMPS) has been designed into the circuit which can provide the required currents at the GSM PA without exceeding the maximum peak current drawn from the 3.3V input. The Dustin datacard is GPRS class 10 – this means that it is capable on transmitting on 2 consecutive TX slots. Each slot has a duration of 577µS. The SMPS has 3 large capacity capacitors on the output to support the output voltage over the bursts. The capacitors have low ESR (to minimise voltage droop when the PA draws large current) and large capacity (1500uF each).

Currently the SMPS design is based on the MAX1687EUE device from Maxim. This device has been evaluated extensively and performs well – despite not being quite as efficient as some. However, unfortunately Maxim aren't an approved Siemens supplier therefore other devices are under consideration. For a detailed report on the SMPS please refer to the document /10/.

A power FET has been attached between the cardbus interface and the 3.3V supply so that it prevents a large inrush of current when the datacard is attached (capacitor charging). The FET is controlled by the NEC device using the POWERUP signal.

6 Radio Frequency (RF) Part

6.1 Block Diagram and Key Components



* - Technical deviation from requirement spec : see deviation list

Figure 6-1: Dustin RF Block Diagram

The RF-part of the Dustin shall be designed and verified in accordance to the 3GPP TS 51.010-1 /3/ and 3GPP TS.134.121 /4/.

According to the block diagram in Figure 6-1 the radio part consists of the following function blocks and key components:

- Transceiver Chip (Qualcomm RTR6250)
- WCDMA Receiver ICs (Qualcomm RFL6202/RFR6202)
- PA ‘s (RFMD and Anadigics)
- Receive SAWs (EPCOS)

In transmit mode the radio frequency part converts the I/Q base band signals supplied by the base band into a RF signal with characteristics as described by the GSM and WCDMA recommendation and which are then radiated by the antenna. In receive mode the radio part converts the RF signals supplied by the antenna into I/Q base band signals, which can then be further processed by the base band.

The radio part is designed for Quad-Band GSM operation and single-band WCDMA operation and can serve the GSM frequency bands GSM850, EGSM900, DCS1800 and PCS1900 a well as the WCDMA frequency band WCDMA2100.

The following definitions have been made:

- The radio part can never transmit in both bands simultaneously.
- The radio part can never receive in both bands simultaneously.
- The monitor time slot can be selected independently of the frequency band.
- The transmitter and receiver can never operate simultaneously.

6.2 RTR6250 - Transceiver IC

The Qualcomm RF transceiver IC RTR6250 is designed for operation in GSM 850 / GSM 900 / GSM 1800 / PCS 1900 cellular systems, and integrates most of the low power silicon functions of a transceiver. The RTR 6250 incorporates 3 RF LNAs (one LNA is shared for 850MHz / 900MHz), 2 direct conversion mixers which are I/Q demodulators, an auto offset calibrated programmable gain amplifier with baseband filter for both I/Q chains, RF synthesizer for the receiver, and an I/Q modulator, offset PLL and IF synthesizer for the transmitter.

A detailed description can be found in the RTR6250 data sheet.

6.3 RFL6202/RFR6202 - WCDMA Receiver

The receiver is using direct conversion technology, eliminating the need for a receive IF SAW filter. The incoming RF signal is passed through the appropriate duplex filter which removes unwanted out of band interference. The signal is then amplified by the LNA in the RFL6202. This LNA has adequate gain noise figure and input IP3 to meet the system requirements and has its gain selectable by software control via a 3 wire bus. The LNA requires external matching components to achieve the required 50ohms.

There is a WCDMA RX SAW that is placed between the LNA and mixer and in addition to providing extra isolation against out of band blocking is a unbalanced to balanced device. The balanced output is necessary as the RFR6202 mixer inputs are balanced.

The RFR6202 downconverts the RF signal to baseband in a direct conversion fashion and feeds out I and Q signals that attach to the MSM6275.

6.4 GSM TX VCO and Power Amplifier

The transmit path consists of a vector modulator within a translational loop. In this scheme, the analog

baseband I/Q signals are modulated with the mixing product of the transmitter output and the main oscillator signal. The unmodulated result is compared with a divided down LO at the phase frequency detector and the difference is used to control the TX VCO. The on-chip lowpass filter following the mixer attenuates the unwanted sidebands as well as harmonics.

A single TXVCO module is used. The VCO module has is dual outputs controlled by the signals TX_VCO_0_EN_N and TX_VCO_1_EN_N. One output is for high band and one for low band operation. The TXVCO has an output power of +6.5dBm and low enough phase noise such that the datacard meets the stringent transmitted noise in the GSM receive band requirements.

Table 6-1 : TXVCO Control Logic

Transmit Band	**TX_VCO_0_EN_N**	**TX_VCO_1_EN_N**
850/900	H	L
1800/1900	L	H
OFF	H	H

The GSM power amplifier is the TQM7M5003 from Triquint. It has integrated power control and has a package size of 7x7mm. Signals are provided from the MSM6275 processor to select the band of operation, setting the output power of the PA and enabling the PA. Anadigics are offering a near pin compatible part that has been qualified by Qualcomm and is an ideal second source to the Triquint part. The Dustin datacard has provision for both PAs in the form of select on build resistors.

6.5 WCDMA Power Amplifiers/ Isolators and Power Detector

The RFMD RF3164 is a GaAsHBT Linear amplifier module that is in a 16pin 3mm x 3mm package. The device can deliver up to +28dBm which is essential for meeting the +23dBm power output requirement at the antenna. The device is capable of operating over the UMTS2100 transmit band.

The VMODE pin allows the PA to be setup with a different internal bias. This is to improve efficiency at lower output levels.

For more information refer to the RF3164 evaluation report /5/.

The PA supply (VCDMA_PA) is a switched supply that connects the PA to either 3.3V directly (when operating at higher output power levels of approximately 10dBm and above). At lower output power VCDMA_PA is connected to a programmable SMPS where the output voltage is set lower to improve efficiency.

The isolators ensure that the PA devices are presented with a good 50ohm load. A tight spec on the input match (< 1.5:1 VSWR) is essential. PA devices tend to have a varying ACLR performance v output load of the PA. The isolation provided is approximately 15dB. Devices have been chosen from TDK as they offer the three transmit bands in a small 3.2x3.2mm package. At the time of writing this document TDK are sampling even smaller 2.5x3.2mm package isolators. Murata and Hitachi Metals offer devices with near identical electrical performance but different mechanical footprints.

The power detector is an Analog Devices part that provides a DC voltage that is proportional to the output power of the PA module. The baseband monitors the HDET1 signal and corrects accordingly the VGA in the RTR6250 to adjust the input power into the PA devices.

6.6 EDGE Transmit Description

The RTR6250 will phase modulate the TXVCO as before. However the Triquint PA has its ramp pin amplitude modulated by the baseband. The amplitude and phase component need to be accurately aligned such that the transmitted EVM is maintained. In order to perform the amplitude modulation the baseband will need to have a very good understanding of the characteristics of the PA. The critical parameters will be Vramp v gain and phase/group delay v Vramp. Qualcomm have been working very closely with Anadigics and Triquint to fully characterize their devices. Anadigics offer a near pin compatible part that can be used as a second source to the Triquint part.

6.7 Front End Switch and WCDMA Duplexers

The WCDMA duplexers ensure that the transmitted signal doesn't overload and block the receiver. It also provides transmit filtering that particularly help in meeting the transmitted harmonic specification and receive filtering to ensure that the receiver can operate when being subjected to external blocking signals.

A ceramic duplex filter has been chosen for UMTS2100.

The ceramic filter has low insertion loss but is bulky. The FBAR has excellent Q/rejection/rolloff and is used for the PCS band as the TX-RX band separation is only 1910-1930MHz. The SAW duplexer is the ideal choice at lower frequencies.

The datacard ideally requires a SP8T (single pole eight throw) device however this task can be achieved by using a SP7T and an SPDT device together. There are 4 control signal that enables the baseband to select the appropriate path.

Table 6-2 : Antenna Switch Control Logic

	ANT_SEL0	**ANT_SEL1**	**ANT_SEL2**	**ANT_SEL3**
GSM 850/900 TX	H	H	L	X
GSM1800/1900 TX	H	L	L	X
GSM1800 RX	L	L	H	X
GSM1900 RX	L	L	L	X
GSM900 RX	L	H	H	H
GSM850 RX	L	H	H	L
UMTS2100 TX/RX	H	L	H	X

6.8 VCTXCO

The 19.2 MHz reference signal is generated by an on-chip reference oscillator. Its frequency can be tuned using programmable capacitors (coarse tuning), as well as with an analog voltage, deduced from the AFC pulse number modulated baseband signal. The varactor diodes for analog tuning are on-chip.

For the base band the signal will be buffered and gained by a buffer integrated in the transceiver chip.

6.9 Antenna Interface

The Dustin Datacard will have an integrated internal antenna. This will be the Skycross part no 2-2390-B. In addition we will have 2 switchable external Antenna Connectors which are connected in series. Firstly Hirose MS 156-NB which will only be used for Production Test and Type Approval Tests. Secondly Hirose MS 151 which is available for the end user.

The antenna reference point (ARP) for type approval is the Hirose MS156-NB connector. The RF interface has a nominal impedance of 50Ω.

The Antenna is not soldered down to the PCB but has its connection made by physical contact onto two pads (signal and ground).

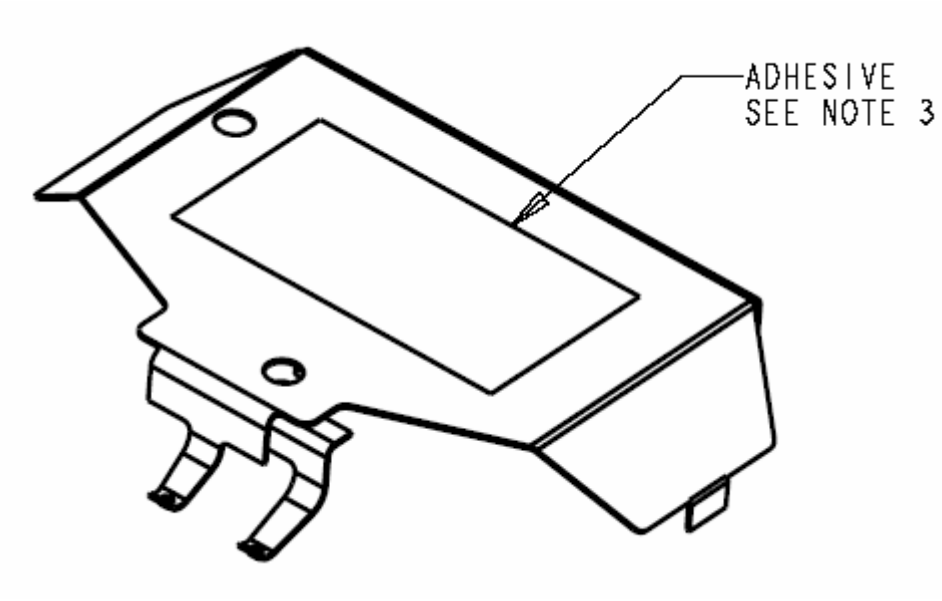


Figure 6-2 : Sycross Antenna for Dustin

7 Interfaces

7.1 RF to Baseband Interface

Details of most of the interface signal levels are Qualcomm proprietary information and as such are not published in detail in their datasheets.

Table 7-1: RF to Baseband description

Function	Signal Name	IO	Signal Level	Comment
Temperature Monitoring	RF_THERM	O	Dependant on temperature. ADC characteristics configurable.	Measurement of temperature in RF section.
	PA_THERM	O	Dependant on temperature. ADC characteristics configurable.	Measurement of temperature of PA modules. Placed near the CDMA PA. ADC characteristics configurable.
Isolation	CALPATH_CTLA	I		Switches in extra isolation from EDGE TX signal into the RTR6200 and UHF VCO.
RF connector physical detection	ANT_POSN	O	High until grounded via a 10K resistor in the presence of the external RF connector.	Provides detection if the external RF connector is used.
RTR6200 control	TX_ON_CAL	I		Switches ON/OFF RTR6200 IC.
RX Baseband Signals	RX0_I_M	O		Received baseband I and Q signals. Common for GSM RX and WCDMA RX
	RX0_I_P	O		
	RX0_Q_M	O		
	RX0_Q_P	O		
	RX1_I_M	O		Received Baseband IQ for the calibration of EDGE transmit
	RX1_I_P	O		
	RX1_Q_M	O		
	RX1_Q_P	O		
Serial BUS (IC control)	SBCK_0	IO?		Clock
	SBST_0	IO?		Strobe/Latch data
	SBDT_0	IO?		Data
GSM/EDGE PA output power control and AM modulation	PA_RAMP+	I	0-1.5V approximately (depending on PA output power setting)	PA ramp signals. May form differential voltage into an op amp configured with BW appropriate for EDGE.
	PA_RAMP-	I		

Antenna Switch Control	ANT_SEL0	I		See section 6.7 for truth table.
	ANT_SEL1	I		
	ANT_SEL2	I		
	ANT_SEL3	I		
PMIC programmable SMPS.	V_CDMA_PA	I	3.3V/Programmable	CDMA PA voltage source. This is either connected directly to the 3.3V supply (for higher output powers) or PMIC for lower output powers
	VREG_MSMP	I	TBD V	
	VREG_RFRX_0	I	TBD V	
	VREG_RFRX_1	I	TBD V	
	VREG_RFTX	I	TBD V	
	VREG_SYNTH	I	TBD V	
	VREG_TCXO	I	TBD V	
VCTCXO Control	TRK_LO_ADJ	I	PDM	VCTCXO frequency adjust voltage (PDM) from MSM6250. Has RC filter.
Power Detector	HDET1	O	ADC Input Range is GND to VREG_MSMA. Resolution 8-bits. DNL +/- 0.75 LSB. INL +/-1.5LSB. Input 5KOhms/ 12pF typ.	Voltage proportional to CDMA transmitted power.
Transmit baseband IQ signals	TX_I_M	O		Transmit I and Q baseband signals
	TX_I_P	O		
	TX_Q_M	O		
	TX_Q_P	O		
	TX_IREF	O		DC offset of transmit IQ baseband signal
	TX_ON	I		Turns on the RTR6250 transmitter
WCDMA PA control	PA_ON0	I	3.3V=ON, 0V=OFF	Turns on the UMTS2100/1900 PA module
	PA_ON1	I	3.3V=ON, 0V=OFF	Turns on the UMTS850 PA module
	PA_R0	I	High(?V) = High gain mode. Low (?V) = Low gain mode.	Switches PA module between 2 different bias states depending on output power setting.
	PA_R1	I	High(?V) = High gain mode. Low (?V) = Low gain mode.	Switches PA module between 2 different bias states depending on output power setting.

	TX_AGC_ADJ	I	PDM (requires RC filter)	Varies the gain of the ampifiers with the RTR6250 IC to change the output power of the device.
19.2MHz Clock	TCXO	O		19.2MHz reference signal from TCXO to baseband.
GSM/EDGE PA Control	GSM_PA_BAND	I	High = DCS/PCS band, Low = GSM850/900 band	
	GSM_PA_EN	I	H= Enable GSM/EDGE PA.	Turns on GSM/EDGE PA module. Also improves isolation of front end switch when activated.
TX VCO Control	TX_VCO_0_EN_N	I	H = GSM/EDGE Low band. L= GSM/EDGE high band.	GSM TX VCO Enable
	TX_VCO_1_EN_N	I	L = GSM/EDGE Low band. H= GSM/EDGE high band.	GSM TX VCO Enable
UHF VCO Control	UHF_VCO_0_EN	I	H= Enable UHF_VCO. L=Disable UHF VCO.	Turns on the UMTS RX VCO module.
	UHF_BAND_SEL	I	TBD	Switched the RX VCO module between the bands for UMTS RX downconversion and EDGE downconversion.

7.2 Electrical description of the Cardbus Interface

The CardBus PC Card interface requires a minimum of 46 signals for a target-only device and a minimum of 49 signals for a master to handle data and addressing, interface control, arbitration, and other functions.

All signals are organized in functional groups:

- System signals
- Address and Data signals
- Interface Control signals
- Arbitration signals
- Error Reporting signals
- Interrupt
- Additional signals
- Power and Ground

For a detailed description of the Electrical Specification of the PC CardBus interface refer to /11/.

Table 7-2: Electrical description of Cardbus Interface

Pin	Signal	I/O	Notes
1	GND	DC	Ground
2	CAD0	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PC Card supports both read and write bursts.
3	CAD1	I/O	
4	CAD3	I/O	
5	CAD5	I/O	
6	CAD7	I/O	
7	CCBE0#	I/O	CardBus PC Card Command and Byte Enables are multiplexed on the same CardBus PC Card pins.
8	CAD9	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PC Card supports both read and write bursts.
9	CAD11	I/O	
10	CAD12	I/O	
11	CAD14	I/O	
12	CCBE1#	I/O	CardBus PC Card Command and Byte Enables are multiplexed on the same CardBus PC Card pins.
13	CPAR	I/O	CardBus PC Card Parity is even2 parity across CAD[31::00] and CCBE[3::0]#.
14	CPERR#	I/O	CardBus PC Card Parity Error is only for the reporting of data parity errors during all CardBus PC Card transactions except a Special Cycle.
15	CGNT#	I	CardBus PC Card Grant indicates to the agent that access to the bus has been granted.
16	CINT#	O	Card Interrupt Request is an optional signal which is defined as level sensitive, and asserted low (negative

			true), using an open drain output driver.
17	Vcc	DC in	3.3V
18	Vpp/Vcore	DC in	No Connection
19	CCLK	I	CardBus PC Card Clock provides timing for all transactions on the CardBus PC Card interface and is an input to every CardBus PC Card device
20	CIRDY#	I/O	CardBus PC Card Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
21	CCBE2#	I/O	CardBus PC Card Command and Byte Enables are multiplexed on the same CardBus PC Card pins.
22	CAD18	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PCCard supports both read and write bursts.
23	CAD20	I/O	
24	CAD21	I/O	
25	CAD22	I/O	
26	CAD23	I/O	
27	CAD24	I/O	
28	CAD25	I/O	
29	CAD26	I/O	
30	CAD27	I/O	
31	CAD29	I/O	
32	RFU		Reserved for future use
33	CCLKRUN#	I/O	CardBus PC Card Clock Run is a required signal which is used by cards to request starting (or speeding up) the CardBus PC Card clock, **CCLK**.
34	GND	DC	Ground
35	GND	DC	Ground
36	CCD1#	O	Tells PC if CardBus or 16bit PC card
37	CAD2	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PC Card supports both read and write bursts.
38	CAD4	I/O	
39	CAD6	I/O	
40	RFU		Reserved for future use
41	CAD8	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PC Card supports both read and write bursts.
42	CAD10	I/O	
43	CVS1	I/O	Tells PC if CardBus or 16bit PC card
44	CAD13	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PC Card supports both read and write bursts.
45	CAD15	I/O	
46	CAD16	I/O	

47	RFU		Reserved for future use
48	CBLOCK#	I/O	CardBus PC Card Lock is an optional signal which indicates an atomic operation that may require multiple transactions to complete.
49	CSTOP#	I/O	CardBus PC Card Stop indicates the current target is requesting the master to stop the current transaction.
50	CDEVSEL#	I/O	CardBus PC Card Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access.
51	Vcc	DC in	3.3V
52	Vcc/Vcore	DC in	No Connection
53	CTRDY#	I/O	CardBus PC Card Target Ready indicates the agent's (selected target's) ability to complete the current data phase of the transaction.
54	CFRAME#	I/O	CardBus PC Card Cycle Frame is driven by the current master to indicate the beginning and duration of a transaction.
55	CAD17	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PCCard supports both read and write bursts.
56	CAD19	I/O	
57	CVS2	I/O	Tells PC if CardBus or 16bit PC card. Refer to
58	CRST#	I	CardBus PC Card Reset is used to bring CardBus PC Card specific registers, sequencers, and signals to a consistent state.
59	CSERR#	O	CardBus PC Card System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result could be catastrophic.
60	CREQ#	O	CardBus PC Card Request indicates to the arbiter that this agent desires use of the bus.
61	CCBE3#	I/O	CardBus PC Card Command and Byte Enables are multiplexed on the same CardBus PC Card pins.
62	CAUDIO	O	Card Audio is an optional digital audio output signal from a PC Card to the system's speaker. CardBus PC Card supports two types of audio signals: a single amplitude, binary waveform, and/or Pulse Width Modulation (PWM) encoded signal.
63	CSTSCHG	O	Card Status Changed is an optional signal used to alert the system to changes in the **READY,** **WP,** or **BVD[2::1]** conditions of the card.
64	CAD28	I/O	CardBus PC Card Address and Data are multiplexed on the same CardBus PC Card pins. A bus transaction consists of an address phase followed by one or more data phases. CardBus PC Card supports both read and write bursts.
65	CAD30	I/O	
66	CAD31	I/O	
67	CCD2#	O	Tells PC if CardBus or 16bit PC card
68	GND	DC	Ground

7.3 Pin Assignment (Cardbus connector – top view)

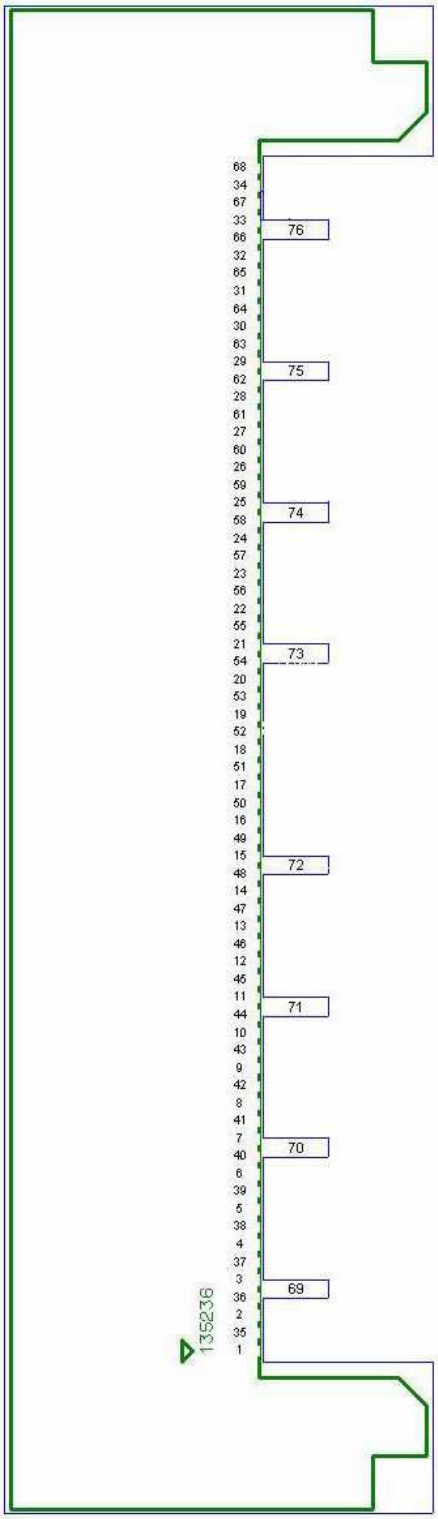


Figure 7-1:Pin assignment of application interface (68-way cardbus connector)

8 Technical data

8.1 Overview

Table 8-1: Technical Data for Dustin

Parameter	Conditions	Min.	Typical	Max.	Unit
Frequency range	GSM 850 Tx	824		849	MHz
	GSM 850 Rx	869		894	MHz
	EGSM 900 Tx	880		915	MHz
	EGSM 900 Rx	925		960	MHz
	DCS 1800 Tx	1710		1785	MHz
	DCS 1800 Rx	1805		1880	MHz
	PCS 1900 Tx	1850		1910	MHz
	PCS 1900 Rx	1930		1990	MHz
	WCDMA 2100 Tx	1920		1980	MHz
	WCDMA 2100 Rx	2110		2170	MHz
RF power @ARP at 50Ω Load Under normal conditions 3)	EGSM 900 / GSM 850 (Class 4)	31	33	35	dBm
	DCS 1800 / PCS 1900 (Class 1)	28	30	32	dBm
	EDGE 900/850 (Class E2)		27		dBm
	EDGE 1800/1900 (Class E2)		26		dBm
	UMTS : Class 3		24		dBm
Receiver input Sensitivity @ ARP **Under all propagation conditions according to GSM Spec.**	EGSM 900 / GSM 850	-102			dBm
	DCS 1800 / PCS 1900	-102			dBm
Receiver input Sensitivity @ ARP BER Class II <= 2.43% @ static input level (no fading)	EGSM 900 / GSM 850		-107		dBm
	DCS 1800 / PCS 1900		-106		dBm
Receiver input Sensitivity @ ARP **Under all propagation conditions according to UMTS Spec.**	UMTS	-106.7			dBm
GSM Class	Small MS				
FAX	Group 3, Class 1, Class 2				
Operating voltage	From Host (as defined by cardbus standard)		3.3		V
Voltage drop2)			TBD		mV

Parameter	Conditions	Min.	Typical	Max.	Unit
Voltage Ripple	Additional On 3.3V Supply-Lines in Tx Bursts Normal condition, power control level for $P_{out\ max}$ @ f<200kHz @ f>200kHz				 mV mV
Peak Current	Imax @antenna return loss = 6db			1	A
Power consumption I_Z[1)]	Idle mode			170	mA
Voltage drop[2)]	Power down			100	mA
Humidity range				80	% relative
Temperature range	Operation	0		+50	℃
Power consumption I_Z[1)]	Auto switch off	-25		+60	℃
GPRS/EDGE (EGPRS)	Multislot class10				
	Full PBCCH support				
GPRS User Data Rates (CS1-4)	Mobile station class B				
	DL			85.6	kbps
	UL			42.8	kbps
EDGE (EGPRS) User Data Rates MCS1-9	DL			237	kbps
	UL			118	kbps
UMTS FDD Mode	DL			384	kbps
	UL			384	kbps
UMTS HSDPA Mode (UE Cat 12, QPSK)	DL			1.8	Mbps
	UL			384	kbps
CSD	GSM			14.4	kbps
	UMTS			57.6	kbps
Physical Dimensions	Length		122		mm
	Width		54		mm
	Height (excluding 13mm high extension)		5		mm
Mass				60	g

[1] In addition, power consumption is extremely dependent on the relevant GSM/WCDMA network coverage.

[2] During transmit bursts, the voltage at the 3.6V_OUT test point may drop down to below TBDV. This is because (for GSM/EDGE operation) a SMPS boosts the 3.3V cardbus voltage to 3.6V. The output voltage is maintained by storage capacitors due to the limited 1A maximum draw on the cardbus interface. As the PA draw approximately 1.5A during the burst the ESR of the storage capacitors will drop the voltage then the voltage will fall linearly as the capacitors drain. The PA device needs to provide sufficient output power at the end of the transmitted slot.

[3] See following tables. This table shows the attenuation of RF power depending on voltage and temperature.

GSM		**LT**	**NT**	**HT**
PCL 5	**LV**	**31,5**	**31,5**	**31**
all values in dBm	**NV**	**32**	**31,75**	**31,5**
	HV	**32**	**32,5**	**31,5**

PCN		**LT**	**NT**	**HT**
PCL 0	**LV**	**29**	**28,75**	**28,25**
all values in dBm	**NV**	**29,25**	**29**	**28,5**
	HV	**29,25**	**29,5**	**28,5**

Table 8-2: RF-Power v operating voltage and temperature

NT: 50℃ norm temp	**55℃**	**HT: 60℃ high temp**
LT: 0℃ low temp	**5℃**	**NT: 10℃ norm temp**

Table 8-3: Definition of temperature thresholds for RF-power

8.2 Placement

The placement has been governed by numerous height restrictions on the Dustin datacard. Generally low components < 1mm have been fitted to the back, along with testpoints. Taller components have been fitted to the top side where a general maximum height of 2.35mm is available except under screening cans where the maximum height is 1.85mm. For a detailed PCB drawing please refer to Dustin PCB Drawing /7/.

On the PCB are several HW-Test points realized for Real Time Functional Test (RFT), calibration and measurement requirements. The RFT is a self-test to ensure the high quality standard of production in accordance to achieve the QS plan.

There are 3 different test points used on the Dustin datacard.

- 1.2mm Production Test Points

The production test points have been placed on a 2.54mm grid. They have routing keep out properties defined the inner 2 layers below the test point (this is so that the pin that probes the testpoint can puncture the outside copper and not short to any tracks below).

- 0.36mm Software Test points

Used for probing in design testing.

- 1.2mm SIM Card Test Points

Same physical size as the production testpoint, however routing keepout properties have been removed. This testpoint is for the design testing only and has been connected to the SIM terminals (A2 layout and later).

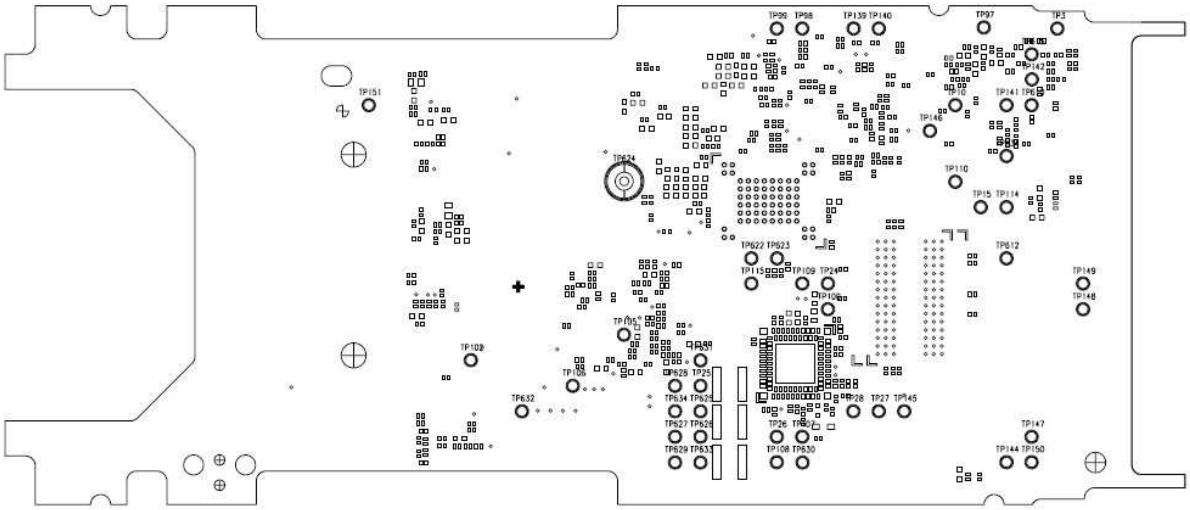


Figure 8-1 Dustin Bottom Side

9 EMC measures

9.1 Overvoltage Protection (including ESD)

Table 9-1 shows the of ESD protection for Dustin.

Refer to section 9.4 for detailed description of ESD protection of the SIM interface.

Table 9-1: ESD protection elements

Signal name	Serial resistor	ESD prot. diode	Spark gap & 27nH coil
SIM interface: CCVCC, CCIN, CCIO, CCCLK, CCRST	√	√	–
Antenna Interface	–	–	√

Table 9-2: Specification of contact and air discharge requirements

Specification / Requirements	Contact discharge	PRIO	Air discharge
CE ETS 300 342-1 (June 1997)			
ESD at SIM port	± 4kV	1	± 8kV
ESD at antenna port	± 4kV	1	± 8kV
ESD at 3.3V GND	± 4kV	1	± 8kV
Siemens			
ESD at SIM port	± 8kV	2	± 15kV
ESD at antenna port	± 8kV	2	± 15kV
ESD at 3.3V in , GND	± 8kV	2	± 15kV

These values are only valid for the reference configuration.

9.2 Ground Planes

Three ground planes (layers 3 (RF), 4 and 6) are implemented on Dustin. Special parts on layer 6 without soldering mask are intended to be used for heat convection. Other layers have been flooded where possible to improve grounding and heat dissipation. The exception to this is layer 2 where the RF section hasn't been grounded as the 50ohm tracks that run on the surface (layer 1) need to be referenced to layer 3 ground in order to maintain a sensible routing width.

9.3 Width of Copper Tracks

The default trace width on the Dustin card is 0.075mm (75um). PA supply tracks have thicker tracks (1mm for CDMA PA), 2mm for GSM/EDGE PA supply. Other supplies from the PMIC are routed in 0.3mm where possible.

9.4 Blocking against RF Interference

There are no blocking measures at the 68-way cardbus connector on Dustin to the external

application.

The SIM interface lines has extra protection to reduce EMI and ESD using a dedicated filter from ST Microelectronics (EMIF03-SIM01)

The EMIF03 Flip Chip packaging means the package size is equal to the die size. This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

- IEC61000-4-2 15kV (air discharge)
- 8 kV (contact discharge)
- MIL STD 883E - Method 3015-6 Class 3

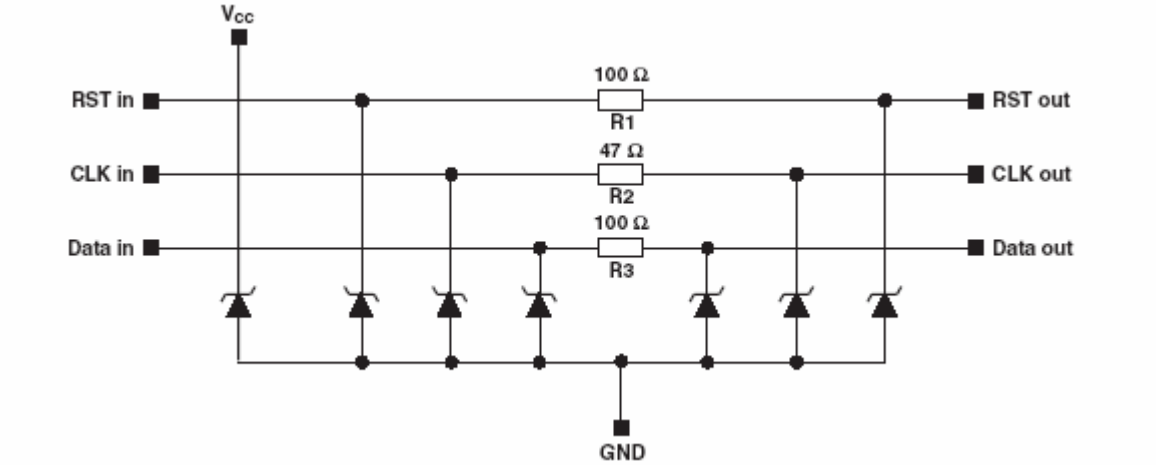


Figure 9-1 : ST Microelectronics EMI filter

9.5 Shielding Measures

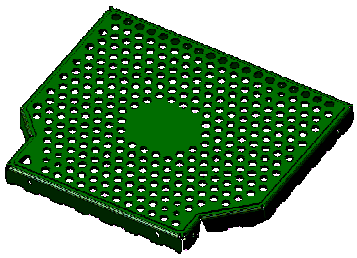
There are four screening cans (Fishcan) that cover the following sections:

- MSM6275 (Baseband IC)
- WCDMA TX
- WCDMA RX
- RTR6250 transceiver and GSM/EDGE section

The layout has been split such that the WCDMA RX section is electrically shielded from the transmitter therefore not compromising the required isolation between TX and RX.

Fishcan description

- Used on all new Siemen's 75 generation phones.
- Closed single-part shielding where the top surface can be opened to repair / replace components. To open the top surface it is pre-stamped in a certain area
- To open the shielding a tool has to be used.
- To close the shielding after repair, a repair cover has to be pressed on the shielding by hand.



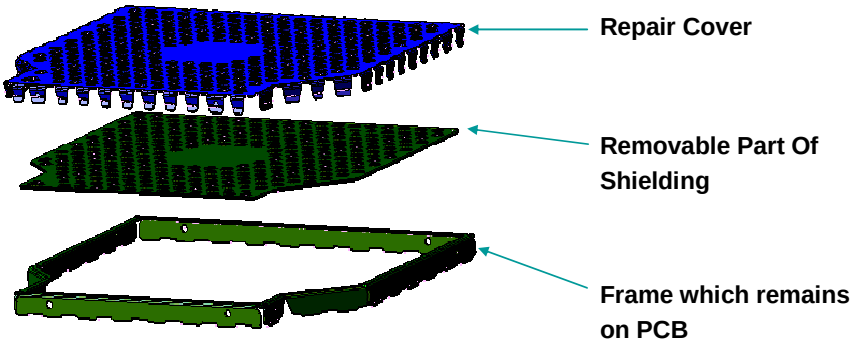


Figure 9-2 : Fishcan description

10 Safety Measures

10.1 Critical Components

There are no critical components in the design.

10.2 Protection against Incorrect Polarity of the Power Supply

There is no protection against incorrect polarity in the module as Dustin is a component.

10.3 Fuses

There are no fuses on Dustin.

10.4 Power Supply

The Dustin card uses the cardbus interface of a laptop as its power source. This can supply up to 1A. Although the Cardbus guidelines state a voltage range of 3.3V +/-10% - i.e. 3.0V to 3.6V, due to limitations of the QCT chipset, Dustin will be tested and qualified for a voltage range of 3.1V to 3.6V, nominally 3.3V. This is common for all Data Cards on the market based on QCT chipsets.

11 Mechanical Specification

11.1 Outlines of Dustin

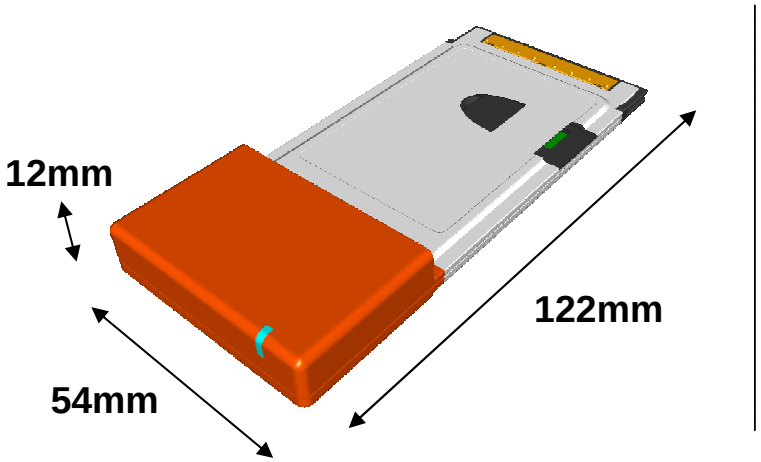


Figure 11-1: Mechanical dimensions of Dustin

The mechanical dimensions including height restrictions can be found in the drawing Dustin PCB Interface X72-LY-2246-006 /7/.

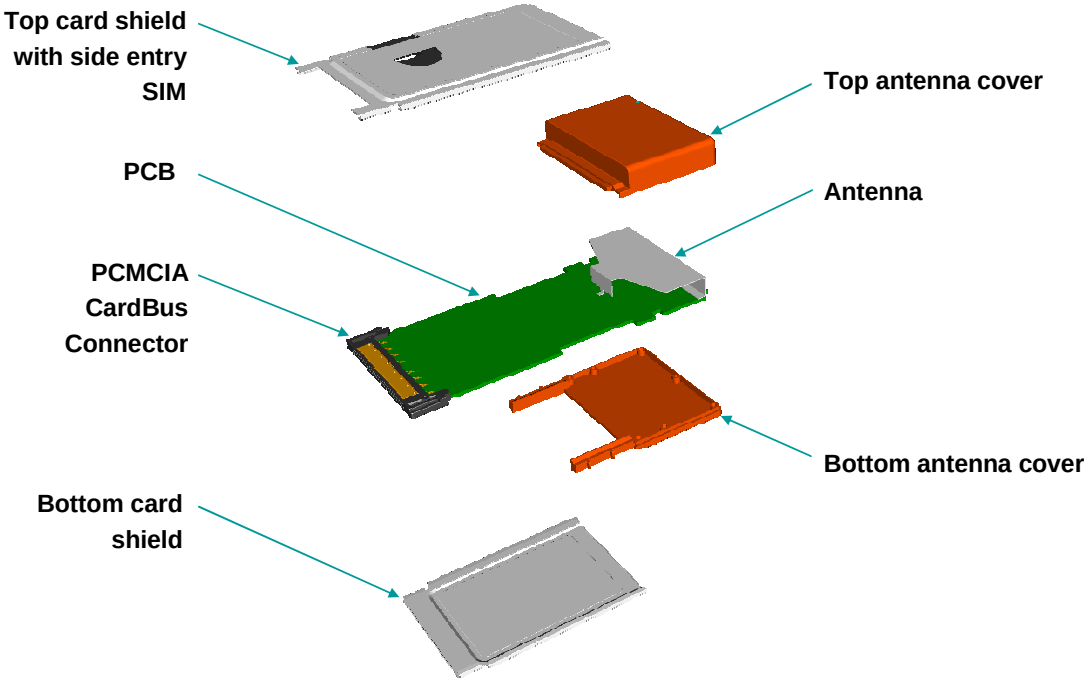
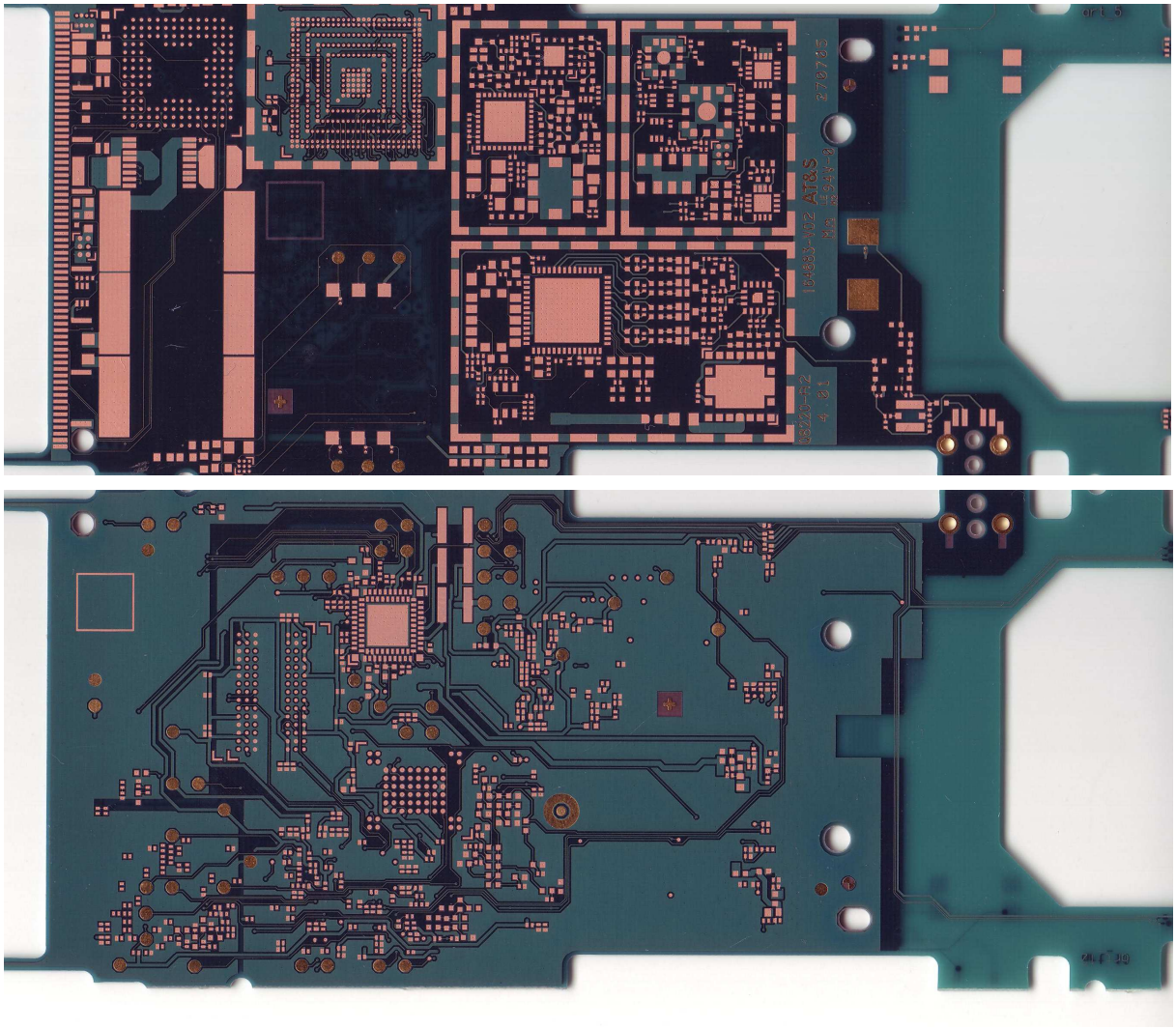


Figure 11-2 : Mechanical assembly of Dustin

Refer to document /8/ for a full mechanical description of Dustin.

12 PCB



The Dustin PCB construction is 8 layers where the outer 2 are ultra thin (80um) for the use of microvias. Microvias are essential to be able to break out the traces from the baseband IC the MSM6275. Microvias can be positioned in pads however they cannot be stacked on top of each other, although this may change in the future. The core vias span layers 3-6 and a physically much larger in comparison (0.3mm compared to 0.1mm holes).

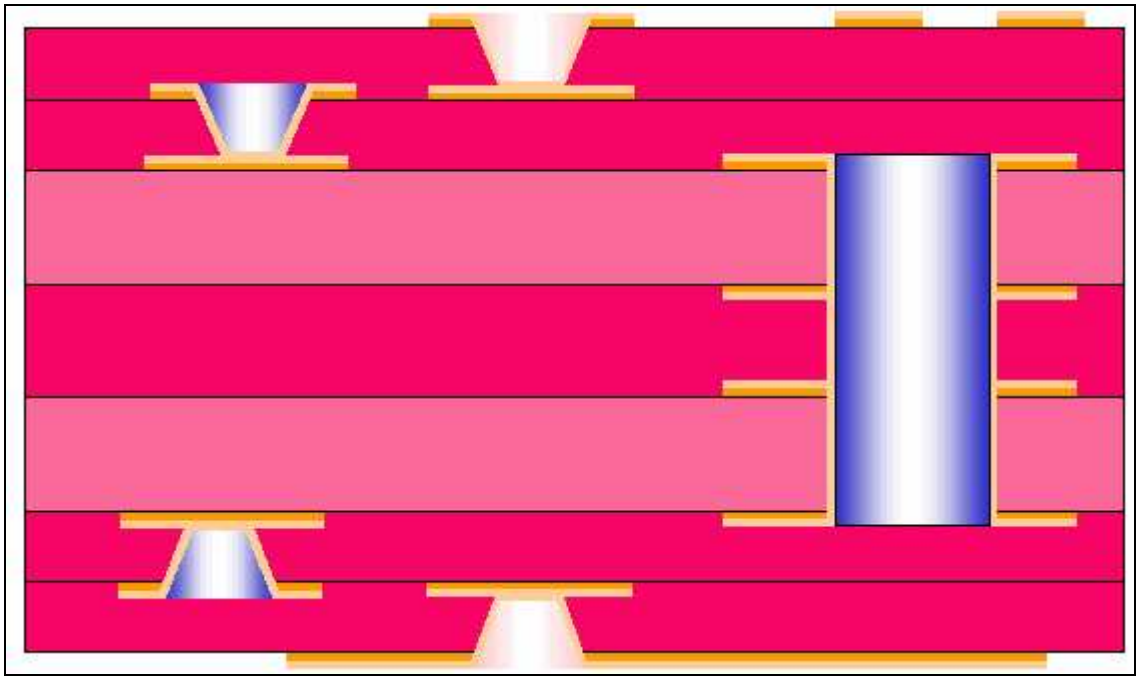


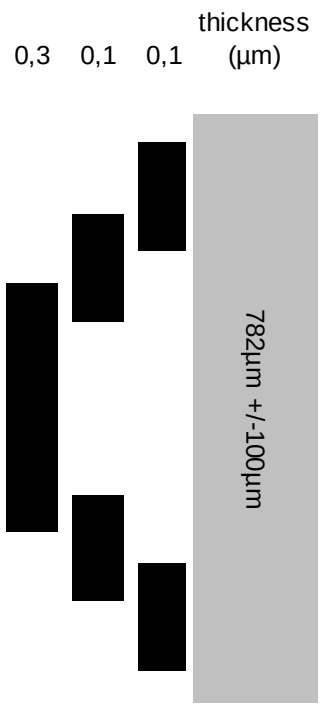
Figure 12-1 : Dustin PCB via structures

For Dustin the layer assignment is as follows:

1. RF components and 50ohms tracking
2. BB signalling
3. RF Ground/Power (3.3v)
4. Ground
5. Buried 50ohms traces. Buried non-50ohm signals
6. Ground
7. BB Signalling
8. RF decoupling/ Memory/ power tracks/general signalling.

Layer build up

layer name	layer type	finished (µm)	tolerance (µm)
mask top 1)	epoxy	20	+/-15
layer 1	copper (base + plating)	28	+/-12
	prepreg 106	45	+/-15
layer 2	copper (base + plating)	28	+/-12
	prepreg 106	40	+/-15
layer 3	copper (base + plating)	28	+/-12
	prepreg 1x2116	115	+/-38
layer 4	copper	17	+/-6
	core (1x1501)	150	+/-38
layer 5	copper	17	+/-6
	prepreg 1x2116	115	+/-38
layer 6	copper (base + plating)	28	+/-12
	prepreg 106	40	+/-15
layer 7	copper (base + plating)	28	+/-12
	prepreg 106	45	+/-15
layer 8	copper (base + plating)	28	+/-12
mask bot 1)	epoxy	20	+/-15



1) soldermask thickness according the specification is 25µm +/- 15µm, for the calculation 20µm will be used

Figure 12-2: Dustin Layer Build up

Raw material supplier: Matsushita halogenfree
Core: R-1566, Prepreg: R-1551

prepreg 106	Dielectric constant	1Ghz:	4,1
	Epsilon R:	2 Ghz:	4,08
resin content	Dissipation factor	1Ghz:	0,012
74%	Tangens delta	2 Ghz:	0,012
prepreg 2116	Dielectric constant	1Ghz:	4,4
	Epsilon R:	2 Ghz:	4,36
resin content	Dissipation factor	1Ghz:	0,011
55%	Tangens delta	2 Ghz:	0,012
core 150	Dielectric constant	1Ghz:	4,78
(1x1501)	Epsilon R:	2 Ghz:	4,75
resin content	Dissipation factor	1Ghz:	0,01
45%	Tangens delta	2 Ghz:	0,012

Figure 12-3 : Dustin PCB Dielectric constants

The smallest passives are 0201. The PCB in Micro Via technology (HDI) has 8 layers and is symmetrical in design. The minimum trace width is 75um technology.

13 Electrical and Mechanical Connections

13.1 68-way Cardbus Connector for Dustin

This chapter provides specifications and handling instructions for the 68-way cardbus connector used to connect Dustin to the host device (Laptop).

Table 13-1: Electrical and mechanical characteristics of the 68-way connector

Parameter	Specification (68-way connector)
Number of Contacts	68
Quantity delivered	2000 Connectors per Tape & Reel
Voltage	50V
Current Rating	0.4A max per contact
Resistance	0.05 Ohm per contact
Dielectric Withstanding Voltage	150V RMS AC for 1min
Operating Temperature	-40℃...+85℃
Contact Material	phosphor bronze finish: solder plating
Insulator Material	PPS, deep brown / Polyamide, beige
FFC/FPC Thickness	0.3mm ±0.05mm (0.012" ±0.002")
Maximum connection cycles	20 (@ 50mOhm max)
Cable	FFC (Flat Flexible Cable), max. length 200mm from SIM interface

13.2 Mechanical dimensions of the 68-way Cardbus connector

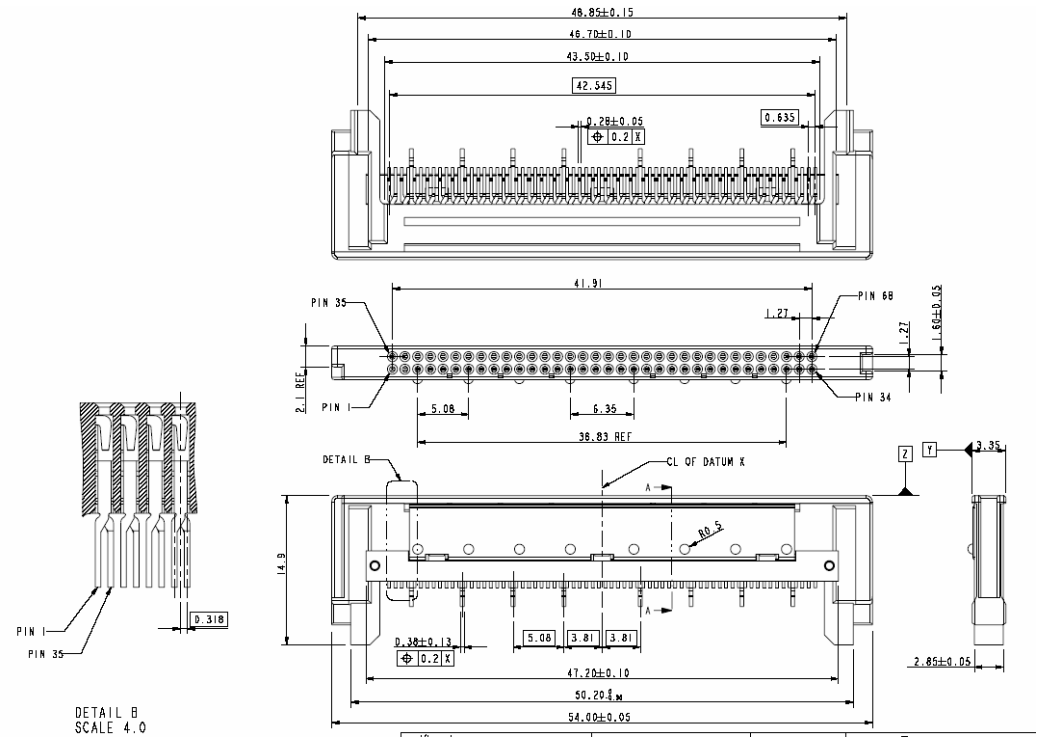


Figure 13-1:Mechanical dimensions of 68-way connector

The figure above was extracted from the datasheet.

13.3 External RF connector

2 Switchable External Antenna Connectors are provided to allow connection to a remote external Antenna. Firstly a Hirose MS-156NB is used as the Antenna Reference point and for Factory measurement and adjustment. Secondly a Hirose MS-151 is provided for the end user to connect an external Antenna to.

■Receptacle

●Without vacuum pick-up cap

Part Number	CL No.	Packaging
MS-156NB	358-0206-8	2,000 pieces/reel
MS-156NB(01)	358-0206-8-01	100 pieces/bag

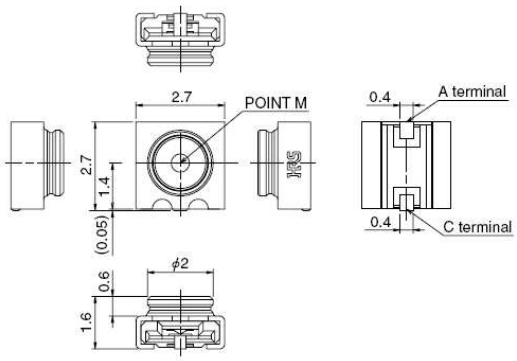


Figure 13-2 Hirose MS-156NB External Antenna Connector

The connector manufacturer and part no is Hirose MS151.

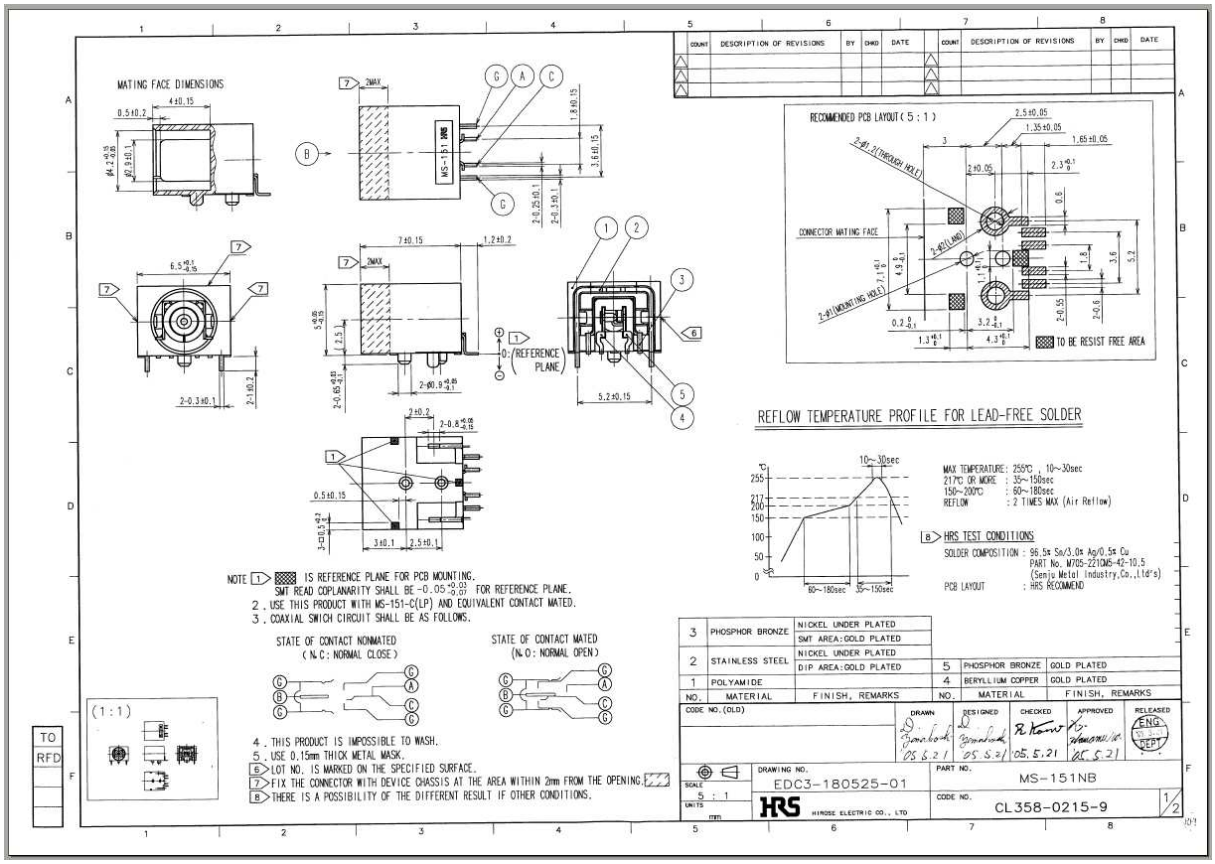


Figure 13-3 : Mechanical dimensions of external RF connector.

The figure above was extracted from the datasheet.