CIRCUIT DESCRIPTION

1、Frequency configuration

The receiver utilizes double conversion.The first IF is 38.85MHZ and the second IF is 450kHz. The first local oscillator signal is supplied from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies.Fig.1 shows the frequencies.

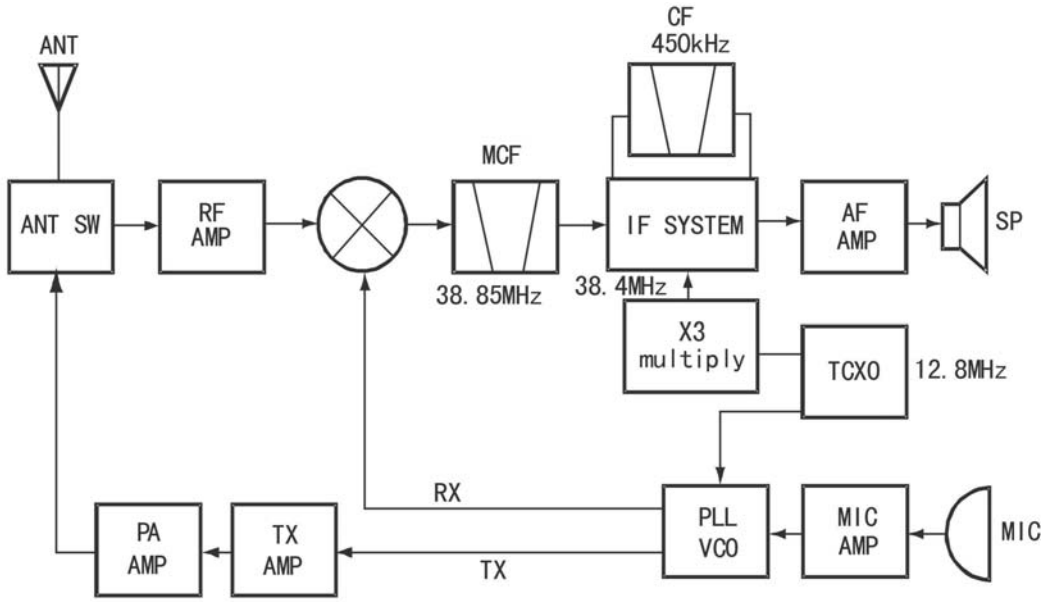

Fig.1 Frequency configuration

2、Receiver

The receiver is double conversion superheterodyne, designed to operate in the frequency range of 150 to 174MHz(M type),136 to 150MHz(M2 type).

The frequency configuration is shown in Fig.1

⑴Front-end RF amplifier

An incoming signal from the antenna is applied to an RF amplifier (Q203) after passing through a transmit/receive switch circuit (D102 and D103 are off)and a band pass filter L208,L209 and L210).After the signal is amplified (Q203), the signal is filtered through a band pass filter (L203 and L214)to eliminate unwanted signals before it is passed to the first mixer .Band pass filters (L208,L209,L210,L203 and L214)have varactor diodes (D203,D204,D206,D202 and D2010.

The voltage of these diodes are controlled by to track the MPU(IC403) center frequency of the band pass filter.(See.Fig2).

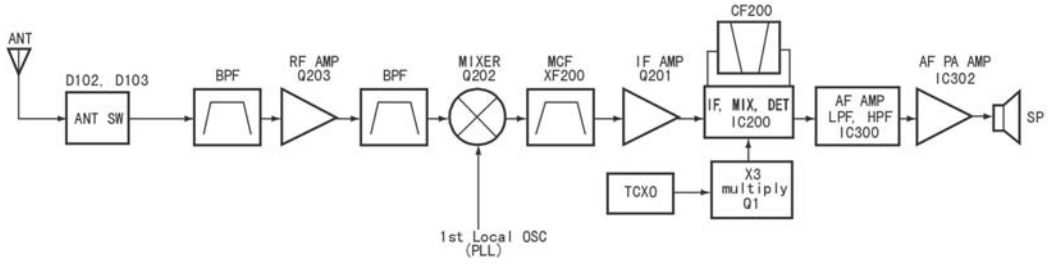

Fig.2 Receiver section configuration

⑵First Mixer

The signal from the RF amplifier is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (Q202)to create a 38.85MH first intermediate frequency (1st IF)signal.The first IF signal is then fed through two monolithic crystal filters(MCFs:XF200)to further remove spurious signals.

⑶IF amplifier

The first IF signal is amplified by Q201,and then enters IC200(FM processing IC).The signal is heterodyned again with a second local oscillator signal within IC200 to create a 450kHz second IF signal. The second IF signal is then fed through a 450kHz ceramic filter (CF200) to further eliminate unwanted signals before it is amplified and FM detected in IC200.

XF200:

Item	Rating
Nominal center frequency	38.850MHz
Pass band width	+/-5.0 kHz or more at 3dB
40dB stop band width	+/-20.0kHz or less
Ripple	1.0dB or less
Insertion loss	4.0dB or less
Guaranteed attenuation	80dB or more at 10-910kHz
Terminal impedance	610 ohm/3PF

CF200:

Item	Rating
Nominal center frequency	450MHz
6dB band width	+/-6.0 kHz or more
50dB band width	+/-12.5kHz or less
Ripple	2.0dB or less at 10+/-4kHz
Insertion loss	6.0dB or less
Guaranteed attenuation	35.0dB or more at 10+/-100kHz
Terminal impedance	2.0 ohm

⑷AF amplifier

The recovered AF signal obtained from IC200 is amplified by IC300(1/4), filtered by the IC300 low-pass filter (2/4)and IC300 high-pass filter (3/4)and (4/4),and de-emphasized by R303 and C306. The AF signal is then passed through a WIDE/NARROW switch (Q303),The processed AF signal passes through an AF volume control and is amplified to a sufficient level to drive a loud speaker by an AF power amplifier(IC302).

⑸Squelch

Part of the AF signal from the IC enters the FM IC again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level.

The DC signal from the FM IC goes to the analog port of the microprocessor (IC403),IC403 determines whether to output sounds from the speaker by checking whether the input boltage is higher or lower than the preset value.

To output sounds from the speaker,IC403 sends a high signal to the MUTE and AFCO lines and turn IC302 on through Q304,Q305,Q306andQ307.(See Fig.3)

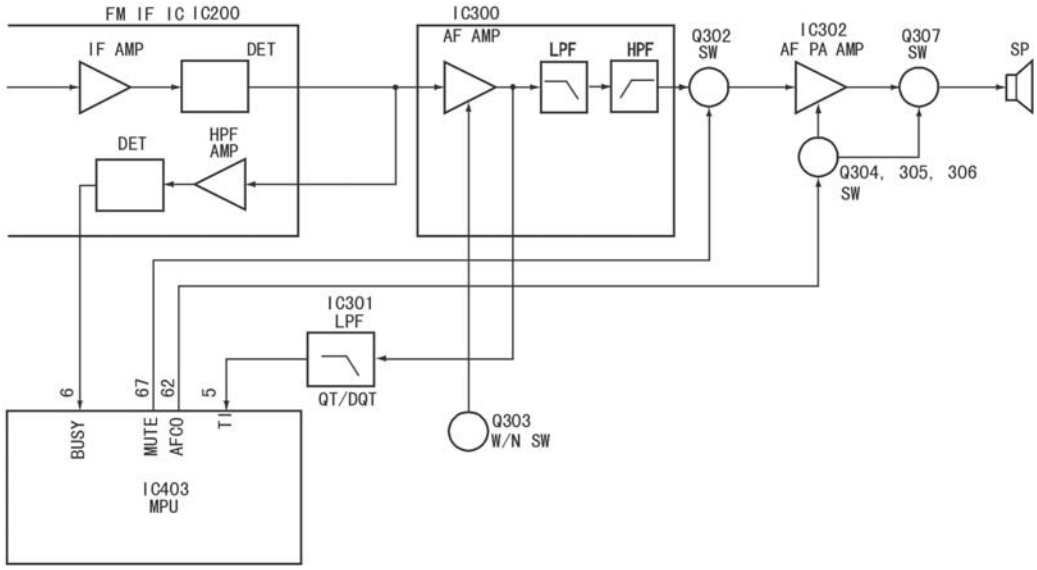

Fig.3 AF Amplifier and squelch

⑹Receive signaling

QT/DQT

300 Hz and higher audio frequencies of the output signal from IF IC are cut by a low-pass filter (IC301),The resulting signal enters the microprocessor(IC403).IC403 determines whether the QT or DQT matches the preset value, and controls the MUTE and AFCO and the speaker output sounds according to the squelch results.

3、PLL frequency synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

⑴PLL

The frequency step of the PLL circuit is 5 or 6.25kHz.A 12.8MHz reference oscillator signal is divided at IC1 by a fixed counter to produce the 5 or 6.25kHz reference frequency, The voltage controlled oscillator(VCO)output signal is buffer amplified by Q6,then divided in IC1 by a dual-module programmable counter ,The divided signal is compared is phase with the 5 or 6.25kHz reference signal in the phase comparator in IC1. The output signal from the phase comparator is filtered through a low-pass filter and passed to the VCO to control the oscillator frequency.(See Fig.4)

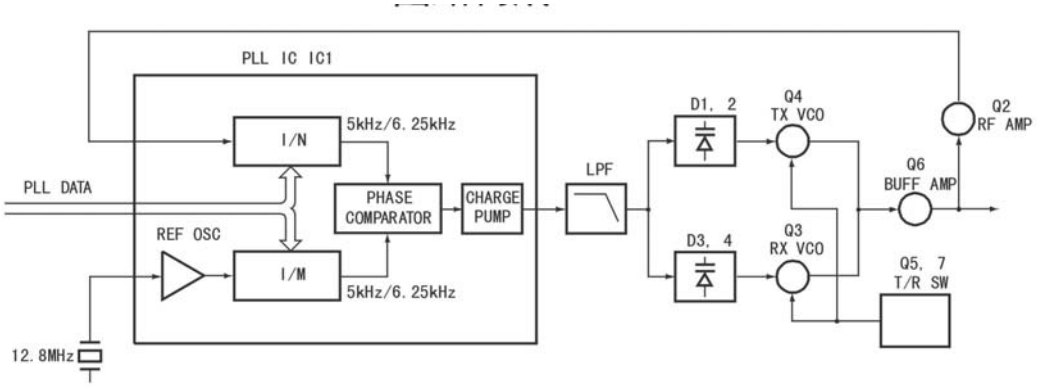

Fig.4 PLL circuit

⑵VCO

The operating frequency is generated by Q4 in transmit mode and Q3 in receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D2 and D4 in transmit mode and D1 and D3 in receive mode). The T/R pin is set high in receive mode causing Q5 and Q7 to turn Q4 off, and turn Q3 on .The T/R pin is set low in transmit mode .The outputs from Q3 and Q4 are amplified by Q6 and sent to the buffer amplifiers.

⑶UNLOCK DETECTOR

If a pulse signal appears at the LD pin of Lc1, an unlock condition occurs, and C1 causes the voltage applied to the UL pin of the microprocessor to go low. When the microprocessor detects this condition, the transmitter is disabled, ignoring the push-to-talk switch input signal. (See Fig.5)

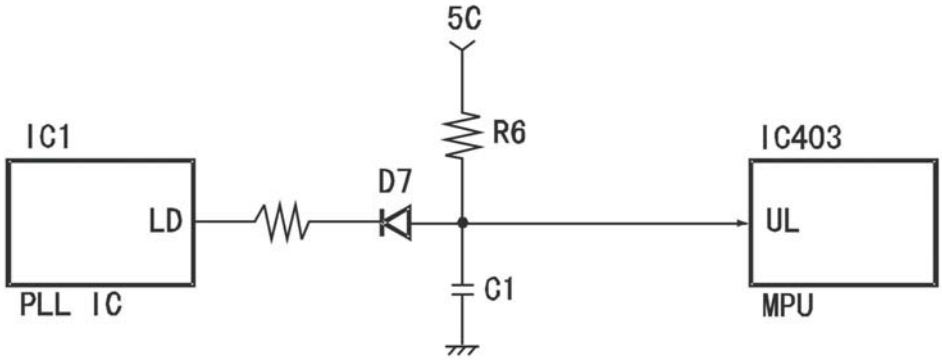

Fig.5 Unlock detector circuit

4、Transmitter

⑴Transmit audio

The modulation signal from the microphone is amplified by IC500(1/2), passes through a preemphasis circuit , and amplified by the other IC500(1/2)to perform IDC operation. The signal then passes through a low-pass filter (splatter filter)(Q501 and Q502)and cuts 3kHz and higher frequencies. The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation.(See Fig.6)

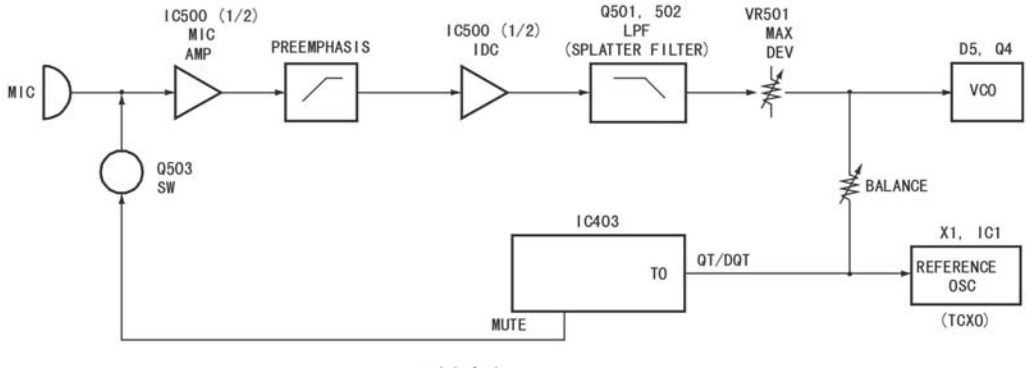

Fig.6 Transmit audio QT/DQT

⑵QT/DQT encoder

A necessary signal for QT/DQT encoding is generated by IC403 and FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher ,modulation is performed at the VCO side by adjusting the balance.(See Fig,6)

⑶VCO and RF amplifier

The transmit signal obtained from the VCO buffer amplifier Q100,is amplified by Q101.The amplified signal is passed to the power amplifier, Q102 and Q105, which consists of a 2-stage FET amplifier and is capable of producing up to 5W of power.(See Fig.7)

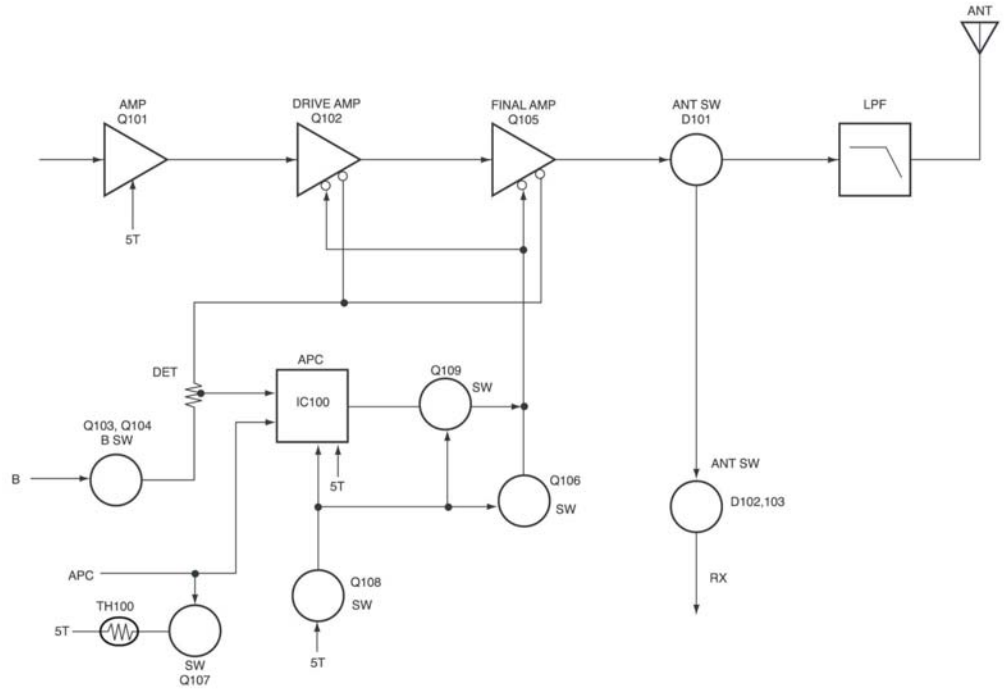

Fig. 7 APC system

⑷ANT switch and LPF

The RF amplifier output signal is passed through a low- pass filter network and a transmit/receive switching circuit before it is passed to the antenna terminal. The transmit/receive

switching circuit is comprised of D101,D102 and D103.D102and D103 tuned on(conductive)in transmit mode and off(isolated) in receive mode.

⑸APC

The automatic power control (APC) circuit stabilizes the transmitter output power at a predetermined level by sensing the drain current of the final amplifier Field Effect Transistor (FET).The voltage comparator, IC100(2/2),compares the voltage obtained from the above drain current with a reference voltage which is set using the microprocessor. An APC voltage proportional to the difference between the sensed voltage and the reference voltage appears at the output of IC100(1/2).This output voltage controls the gate of the FET power amplifier, which keeps the transmitter output power constant. The transmitter output power can be varied by the microprocessor which in turn changes the reference voltage and hence the output power.

⑹Terminal protection circuit

When the thermistor (TH100) reaches about 80℃, the protection circuit turns on Q107 to protect transmitting final amplifier(Q105)from the over heating.

5、Power supply

A 5v reference power supply [5M] for the control circuit is derived from an internal battery. This reference is used to provide a 5V supply in transmit mode [5T], a 5V supply in receive mode [5V] based on the control signal sent from the microprocessor.

6、Control system

The IC403 CPU operates at 7.37MHz. This oscillator has a circuit that shifts the frequency according to the EEPROM data.