

MS Series Encoder Data Structure

The MS Series encoder is designed to securely register button presses or switch closures over a wireless link for remote control applications. It will turn eight parallel input lines into a secure, encoded serial bit stream output. It will turn eight parallel input lines into a secure, encoded serial bit stream output.

The MS Series algorithm is designed to create a data stream with a 50% duty cycle by using the same number of high bits and low bits. Two wait times reduce this duty cycle to just below 50%.

Logic State Description:

1 = HIGH
0 = LOW

Total bits, including start and stop bits = 80

Total 1's = 40

Total 0's = 40

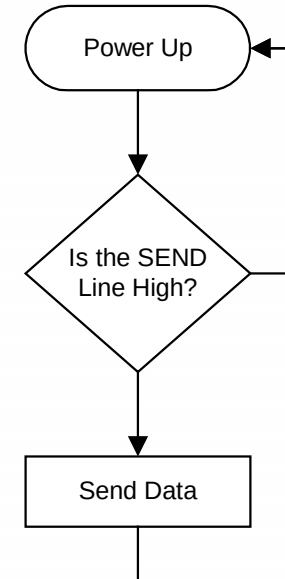
Value for each bit per baud rate:

2400bps = 417uS or 1.18% of duty cycle

9600bps = 104uS or 1.01% of duty cycle

19200bps = 52uS or 0.85% of duty cycle

28800bps = 35uS or 0.74% of duty cycle



Wait Time	Processing Time		Wait Time	Wake	Noise Filter	Error Check	ADDR-H	ADDR-M	ADDR-L	Data Byte	Error Check
680uS	11111111	00000000	465uS	1010	800uS	0 01101000 1	0 10101010 1	0 01010101 1	0 00000000 1	0 11111111 1	0 11101010 1

$$\begin{aligned}
 \text{Duty Cycle} &= \frac{\text{Time High}}{\text{Total Time}} \longrightarrow \frac{40 \text{ bits} + 800\text{uS}}{80 \text{ bits} + 680\text{uS} + 465\text{uS} + 800\text{uS}} \longrightarrow \frac{(40 \times 417\text{uS}) + 800\text{uS}}{(80 \times 417\text{uS}) + 1,945\text{uS}} = \frac{17,480\text{uS}}{35,305\text{uS}} = 49.51\%
 \end{aligned}$$

MS Series Encoder Data Structure

The MS Series encoder is designed to securely register button presses or switch closures over a wireless link for remote control applications. It will turn eight parallel input lines into a secure, encoded serial bit stream output.

The MS Series algorithm is designed to create a data stream with a 50% duty cycle by using the same number of high bits and low bits. Two wait times reduce this duty cycle to just below 50%.

Logic State Description:

1 = HIGH
0 = LOW

Total bits, including start and stop bits = 80

Total 1's = 40

Total 0's = 40

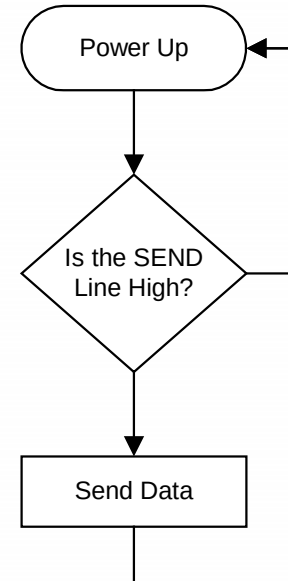
Value for each bit per baud rate:

2400bps = 417uS or 1.18% of duty cycle

9600bps = 104uS or 1.01% of duty cycle

19200bps = 52uS or 0.85% of duty cycle

28800bps = 35uS or 0.74% of duty cycle



Wait Time	Processing Time		Wait Time	Wake	Noise Filter	Error Check	ADDR-H	ADDR-M	ADDR-L	Data Byte	Error Check
680uS	11111111	00000000	465uS	1010	800uS	0 01101000 1	0 10101010 1	0 01010101 1	0 00000000 1	0 10001000 1	0 11101010 1

$$\text{Duty Cycle} = \frac{\text{Time High}}{\text{Total Time}} \longrightarrow \frac{40 \text{ bits} + 800\text{uS}}{80 \text{ bits} + 680\text{uS} + 465\text{uS} + 800\text{uS}} \longrightarrow \frac{(34 \times 417\text{uS}) + 800\text{uS}}{(80 \times 417\text{uS}) + 1,945\text{uS}} = \frac{14,978\text{uS}}{35,305\text{uS}} = 42.42\%$$