

Table of Contents	
DDR SDRAM	Sheet 2
Serial Communications	Sheet 3
Power Supply	Sheet 4
Reset Configuration	Sheet 5
10/100 Ethernet	Sheet 6
BDM Connector	Sheet 7
I/O Header	Sheet 8
Flash & SRAM	Sheet 9
ZigBee Transciever	Sheet 10
Reset & IRQ	Sheet 11
MCU Power Rails	Sheet 12
Clock	Sheet 13

Revision History

Rev.	Date	Designer	Comments
A	18 Apr. 05	G Rouse	Initial release.
B	30 Aug. 05	G Rouse	Changed U3 to ST LD29080. Changed U9-VIN to 3V3. Removed unnecessary jumpers. Renamed jumpers. Added 10K pullup to *ATTN. Rationalized resistors into resistor packs. Renamed MCF5208 signal names for consistency with MCF5208RM.pdf.

M5208EVB Evaluation Board

TITLE: M5208EVB_Rev_B

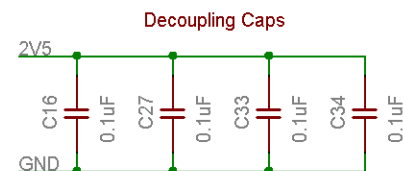
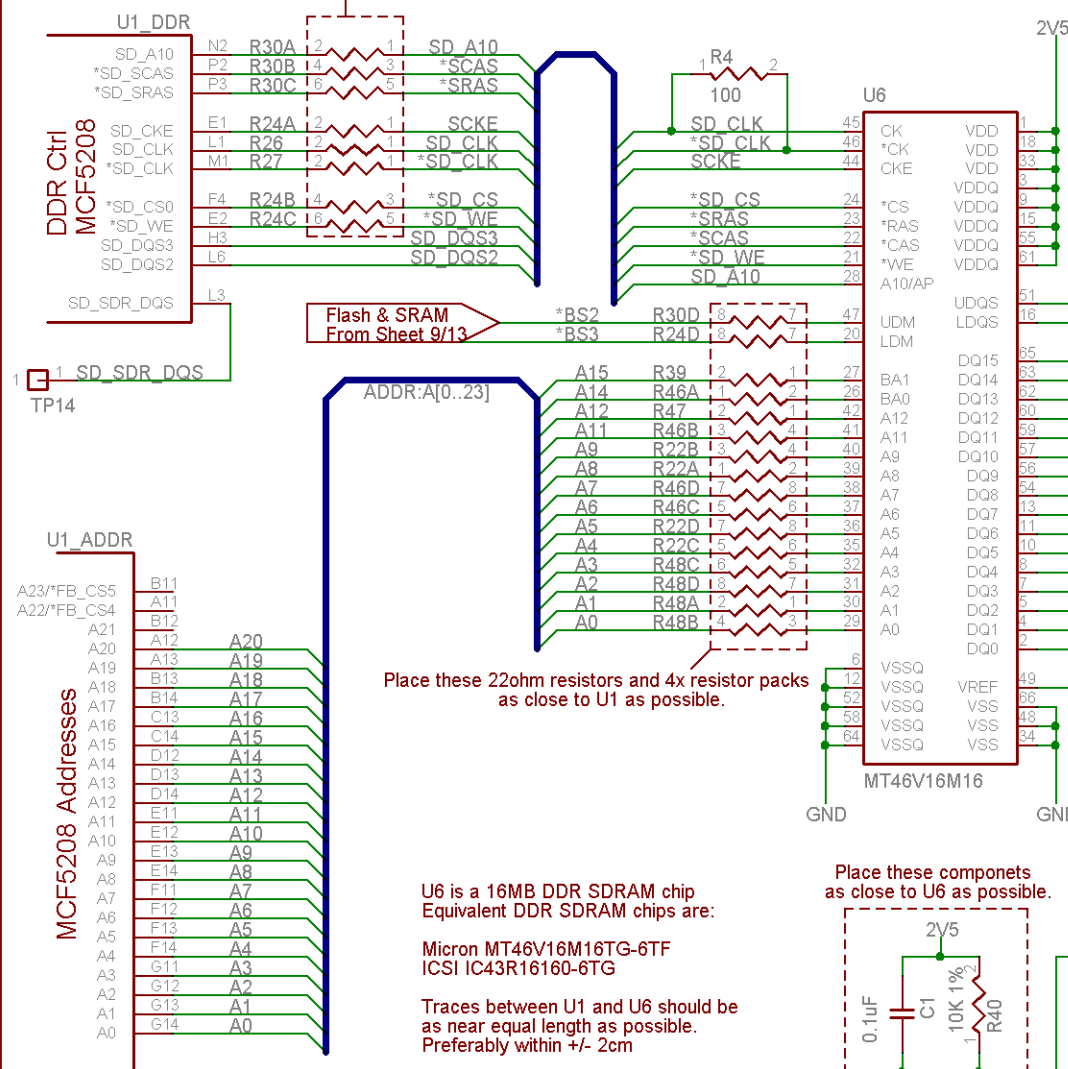
Document Number:

REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 1/13

Place these 22ohm resistors and 4x resistor packs as close to U1 as possible.



High and low data bytes are swapped to minimize routing.
 Bits within high and low data byte are shuffled to minimize routing.

Place these 4x22ohm resistor packs centrally between U1 and U6.

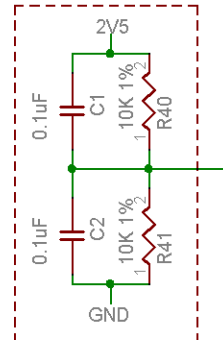
Place these 22ohm resistors and 4x resistor packs as close to U1 as possible.

Place these components as close to U6 as possible.

U6 is a 16MB DDR SDRAM chip
 Equivalent DDR SDRAM chips are:

Micron MT46V16M16TG-6TF
 ICSI IC43R16160-6TG

Traces between U1 and U6 should be as near equal length as possible.
 Preferably within +/- 2cm



DDR SDRAM

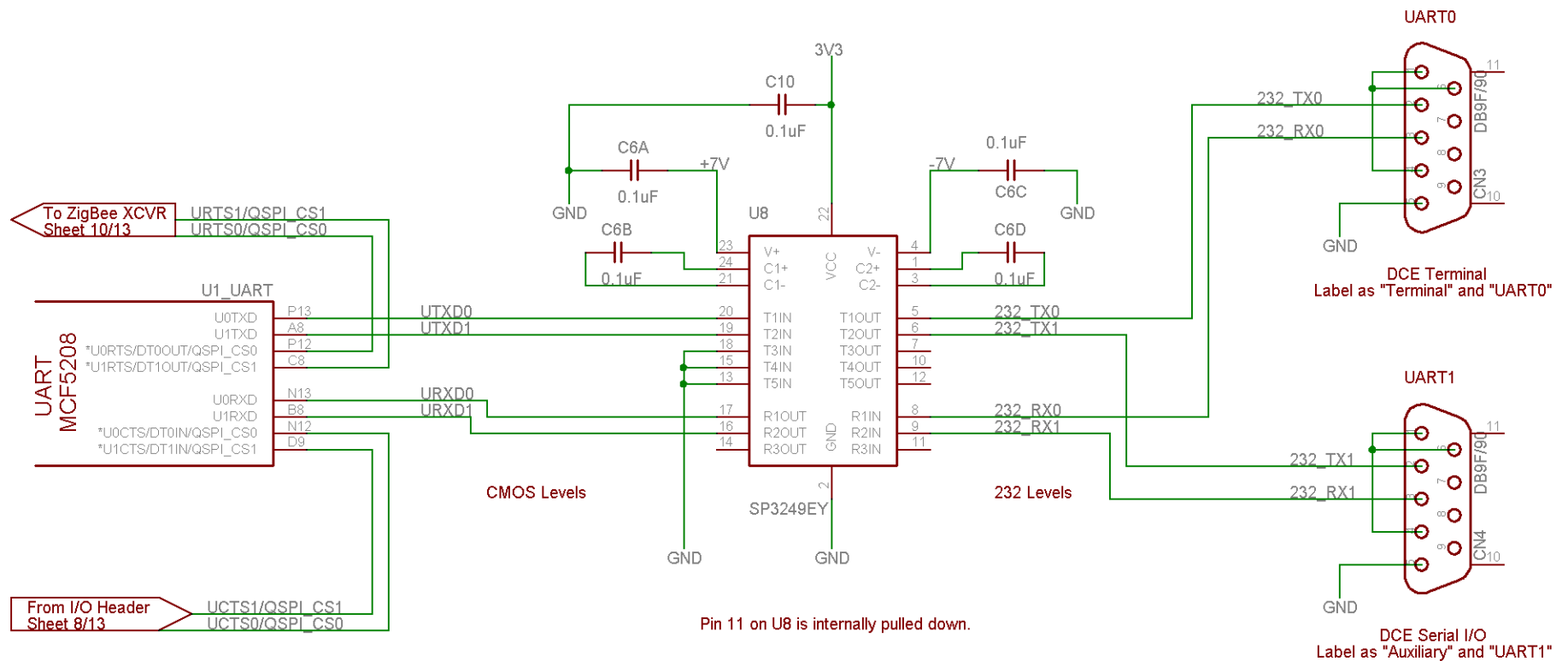
TITLE: M5208EVB_Rev_B

Document Number:

REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 2/13



Add pulldowns resistors to U0TXD and U1TXD to prevent these lines from floating during reset.

Serial Communications

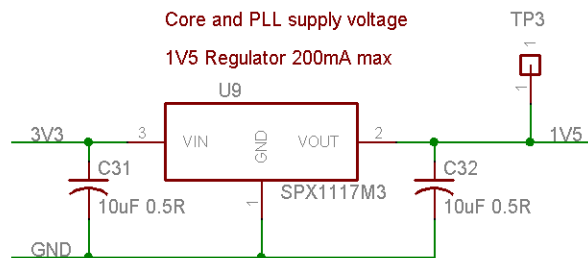
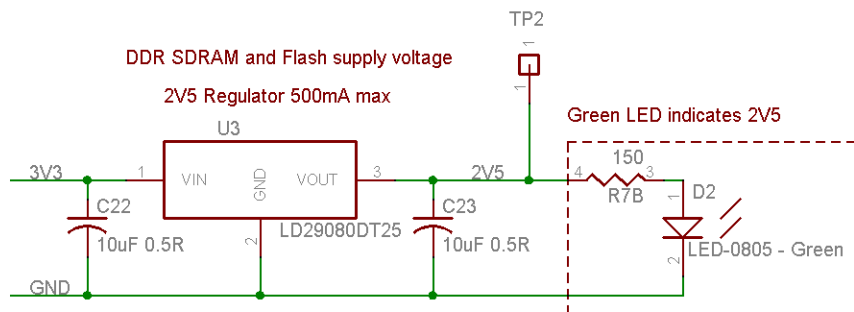
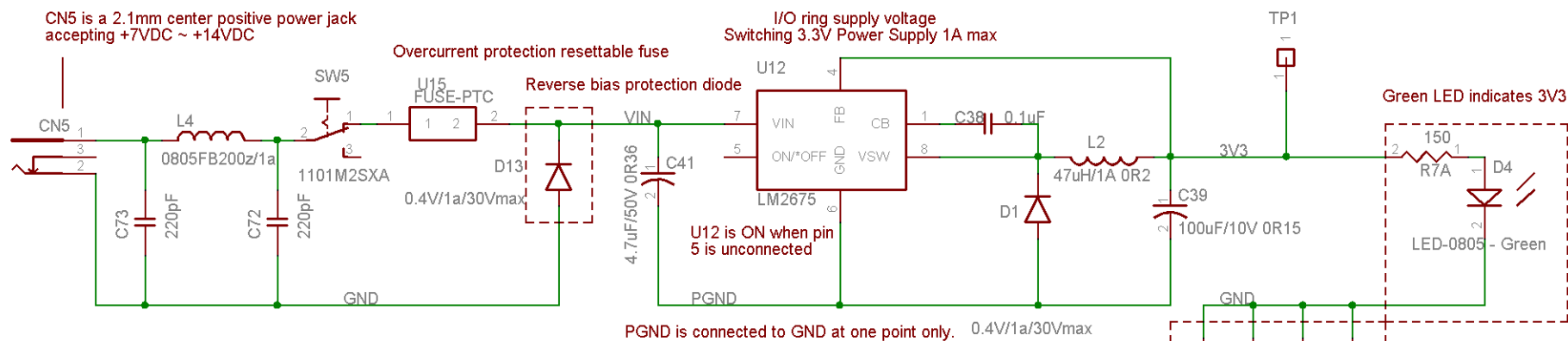
TITLE: M5208EVB_Rev_B

Document Number:

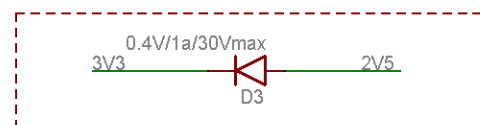
REV:
B

Date: 8/30/2005 12:20:51p

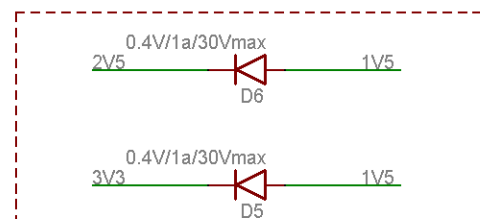
Sheet: 3/13



Shottky diode feedback to prevent 2V5 from exceeding 3V3 during shutdown



Shottky diodes feedback to prevent 1V5 from exceeding 3V3 or 2V5 during shutdown



Power Supply

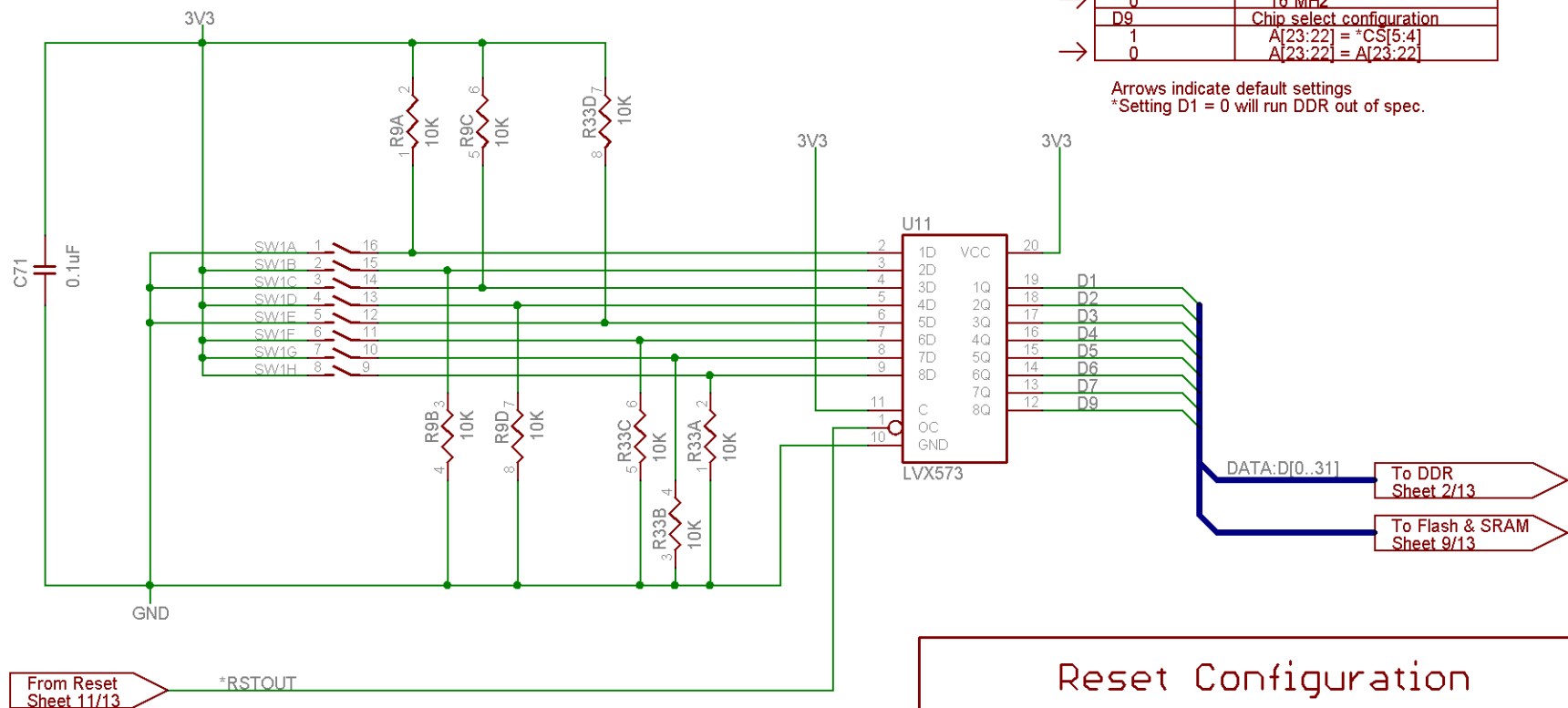
TITLE: M5208EVB_Rev_B

Document Number:

REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 4/13



Reset Configuration

→	D1	PLL Mode
	1	166.67/83.33 MHz operation
	0	88/44 MHz operation *
→	D2	Oscillator Mode
	1	Oscillator bypass mode
	0	Crystal oscillator mode
→	D[4:3]	Boot port size
	00, 11	32-bit port
	01	16-bit port
	10	8-bit port
→	D5	Output pad drive strength
	1	High drive strength
	0	Low drive strength
→	D6	Limp mode
	1	Limp mode
	0	Normal PLL mode
→	D7	Clock Frequency Input
	1	16.67 MHz
	0	16 MHz
→	D9	Chip select configuration
	1	A[23:22] = *CS[5:4]
	0	A[23:22] = A[23:22]

Arrows indicate default settings
 *Setting D1 = 0 will run DDR out of spec.

Reset Configuration

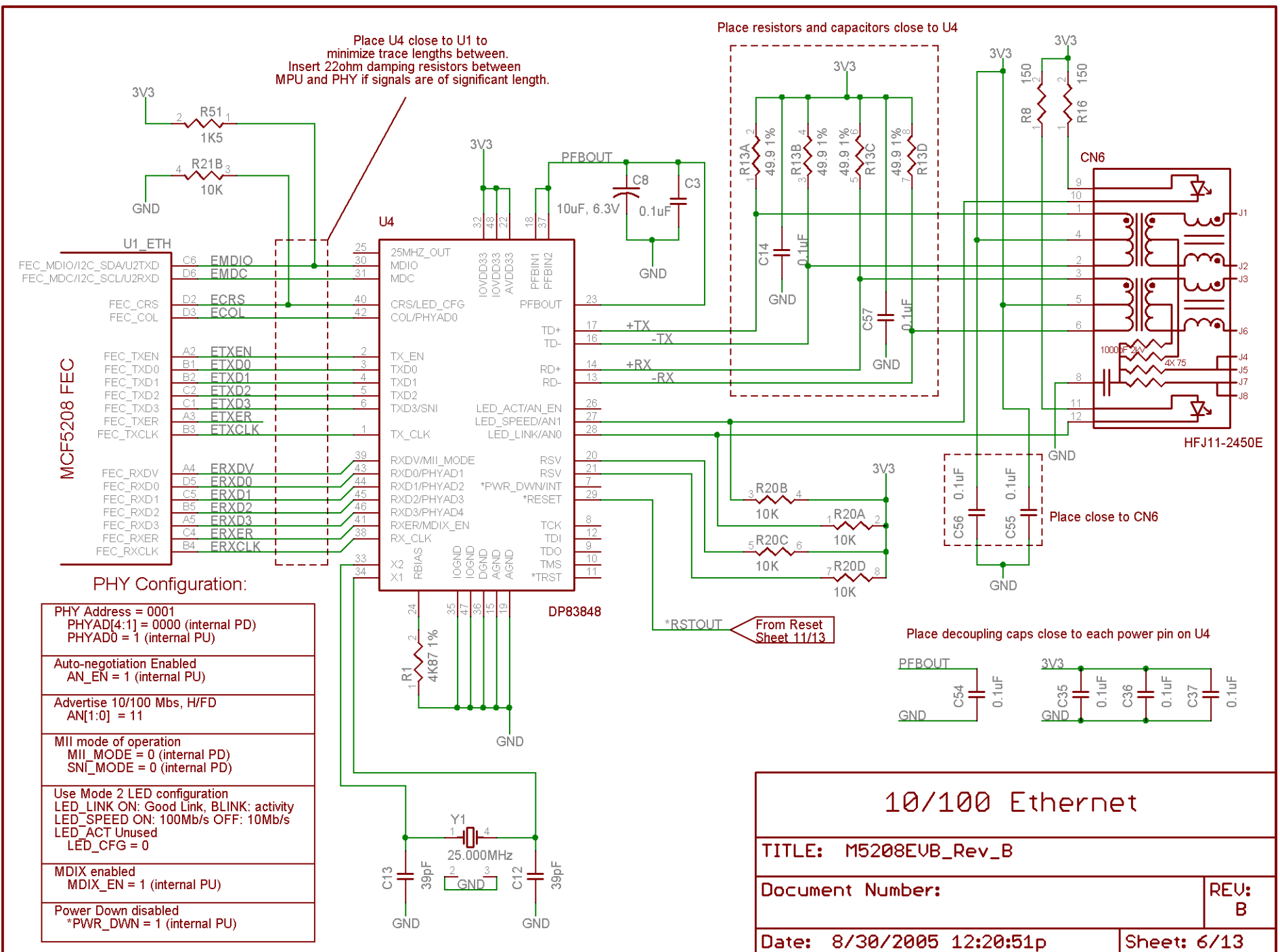
TITLE: M5208EVB_Rev_B

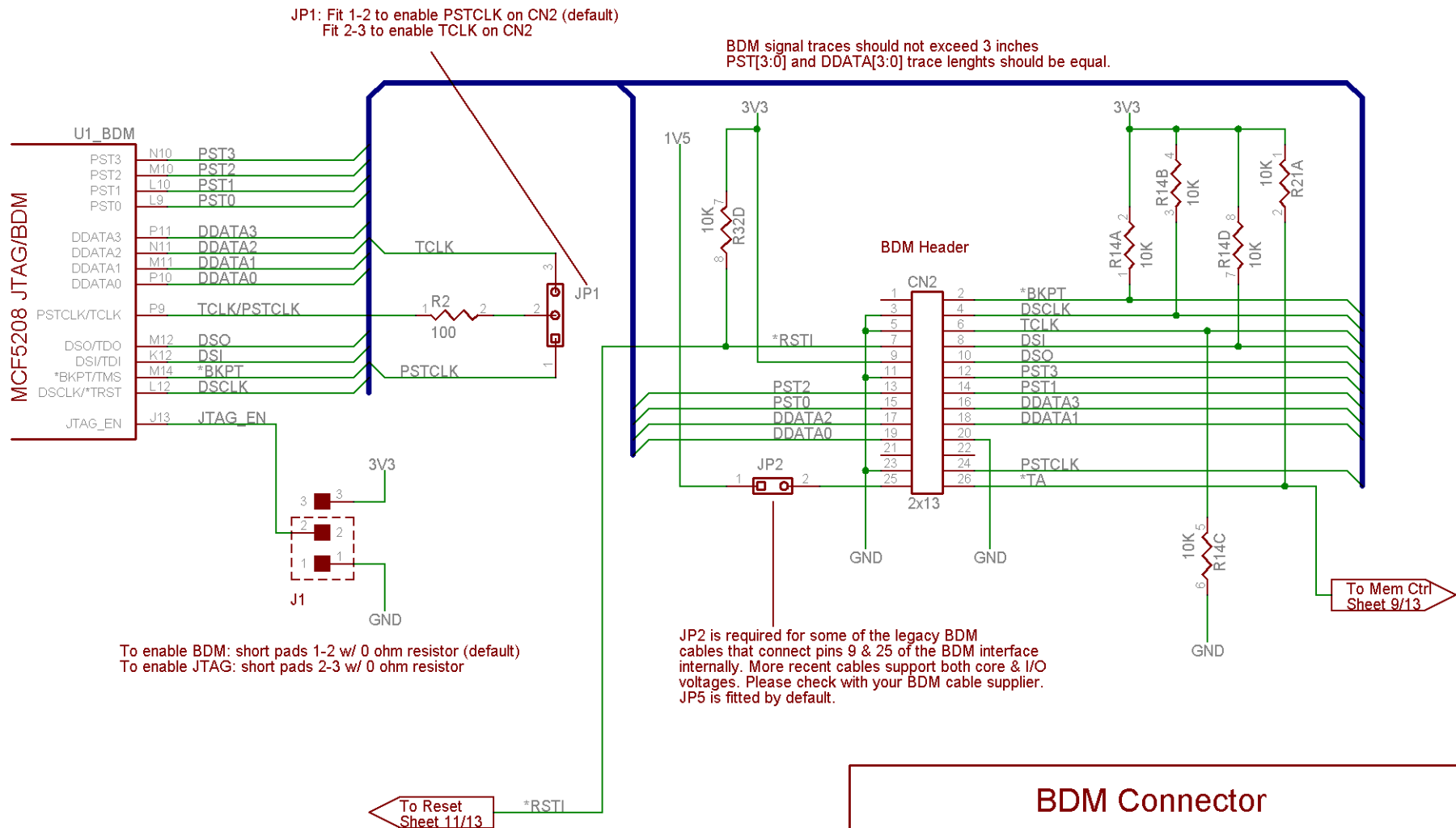
Document Number:

REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 5/13





BDM Connector

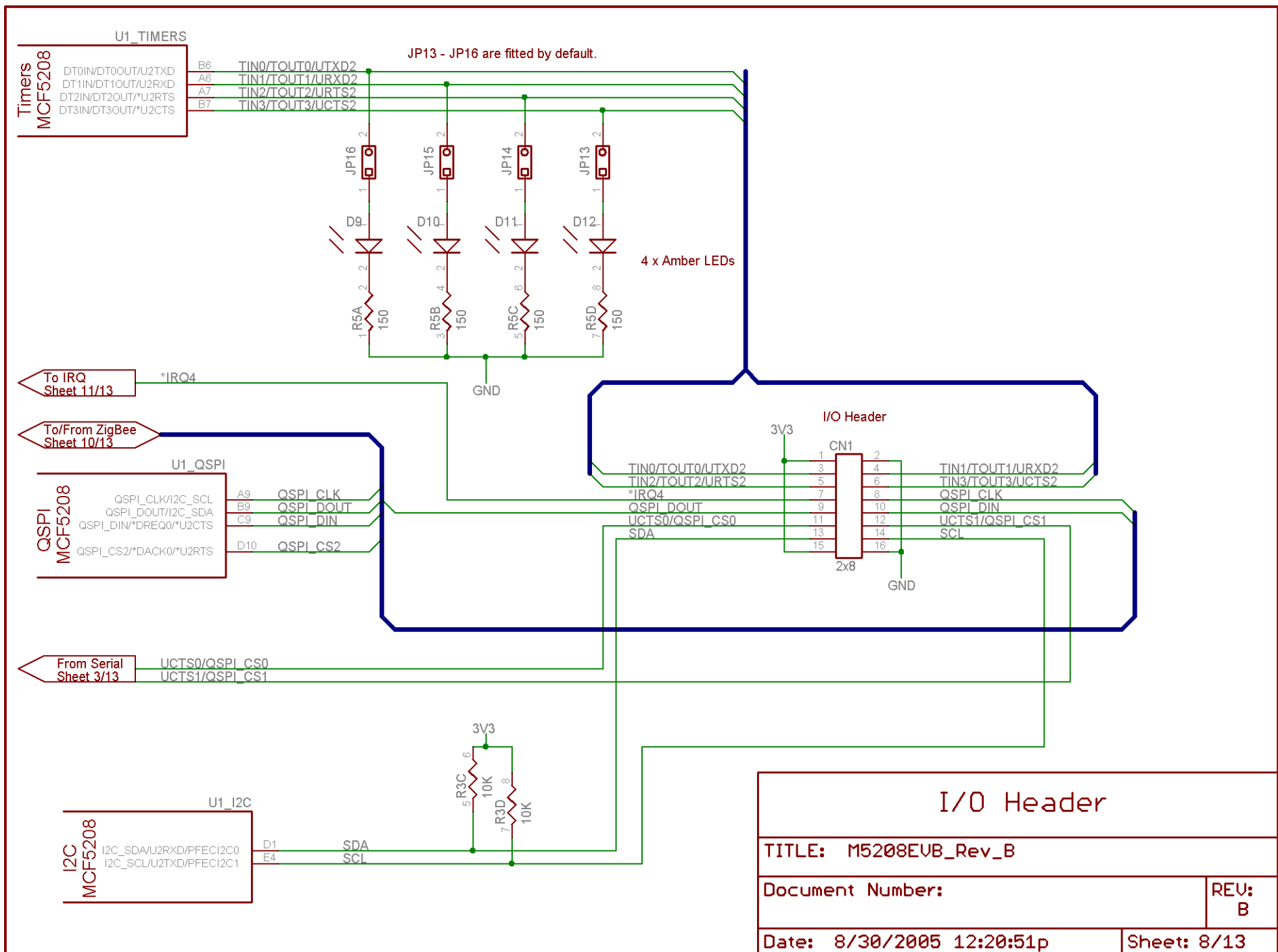
TITLE: M5208EVB_Rev_B

Document Number:

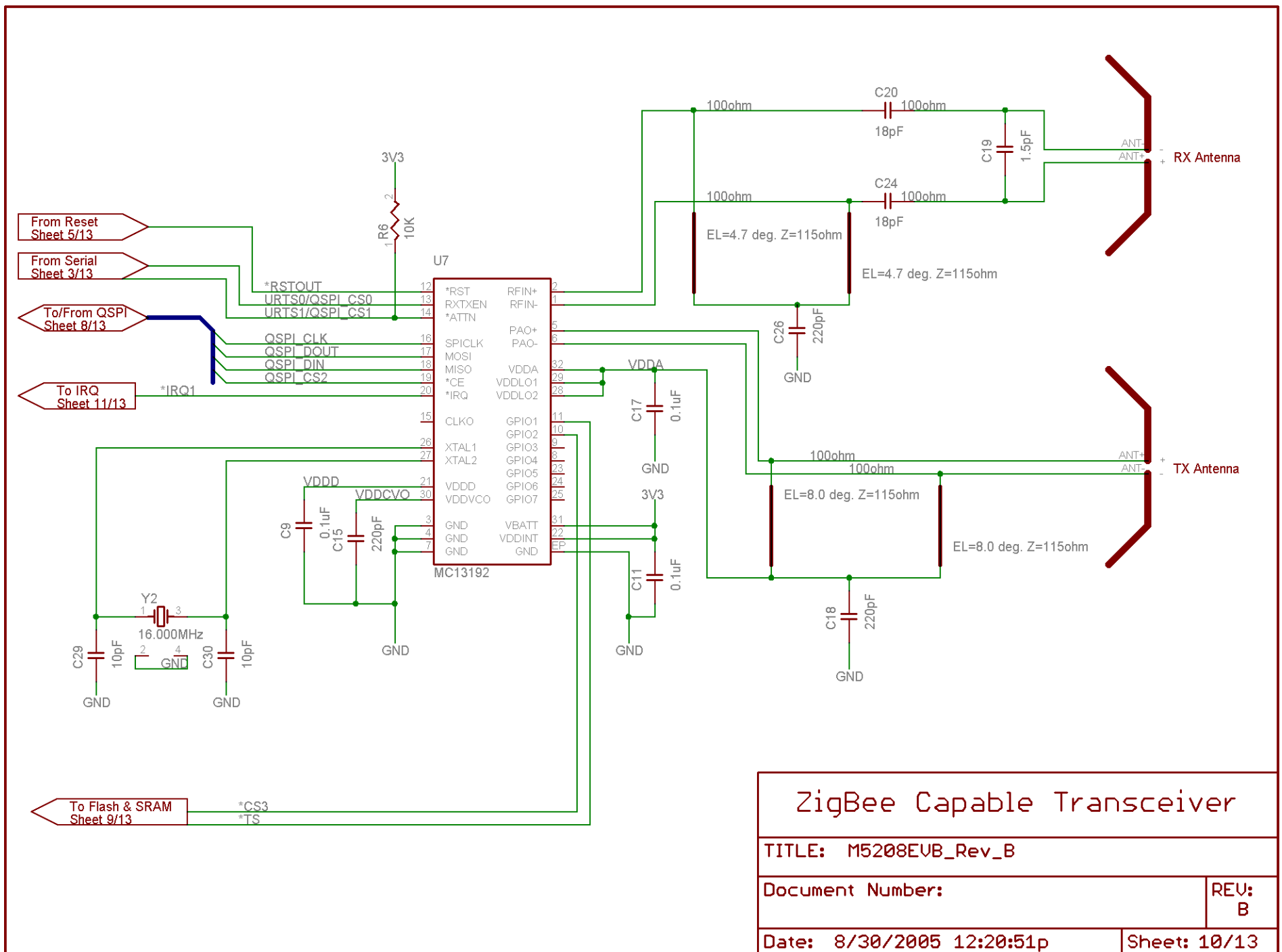
REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 7/13



I/O Header	
TITLE: M5208EVB_Rev_B	
Document Number:	REV: B
Date: 8/30/2005 12:20:51p	Sheet: 8/13



ZigBee Capable Transceiver

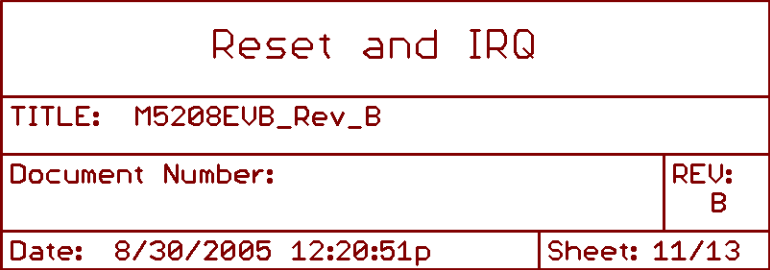
TITLE: M5208EVB_Rev_B

Document Number:

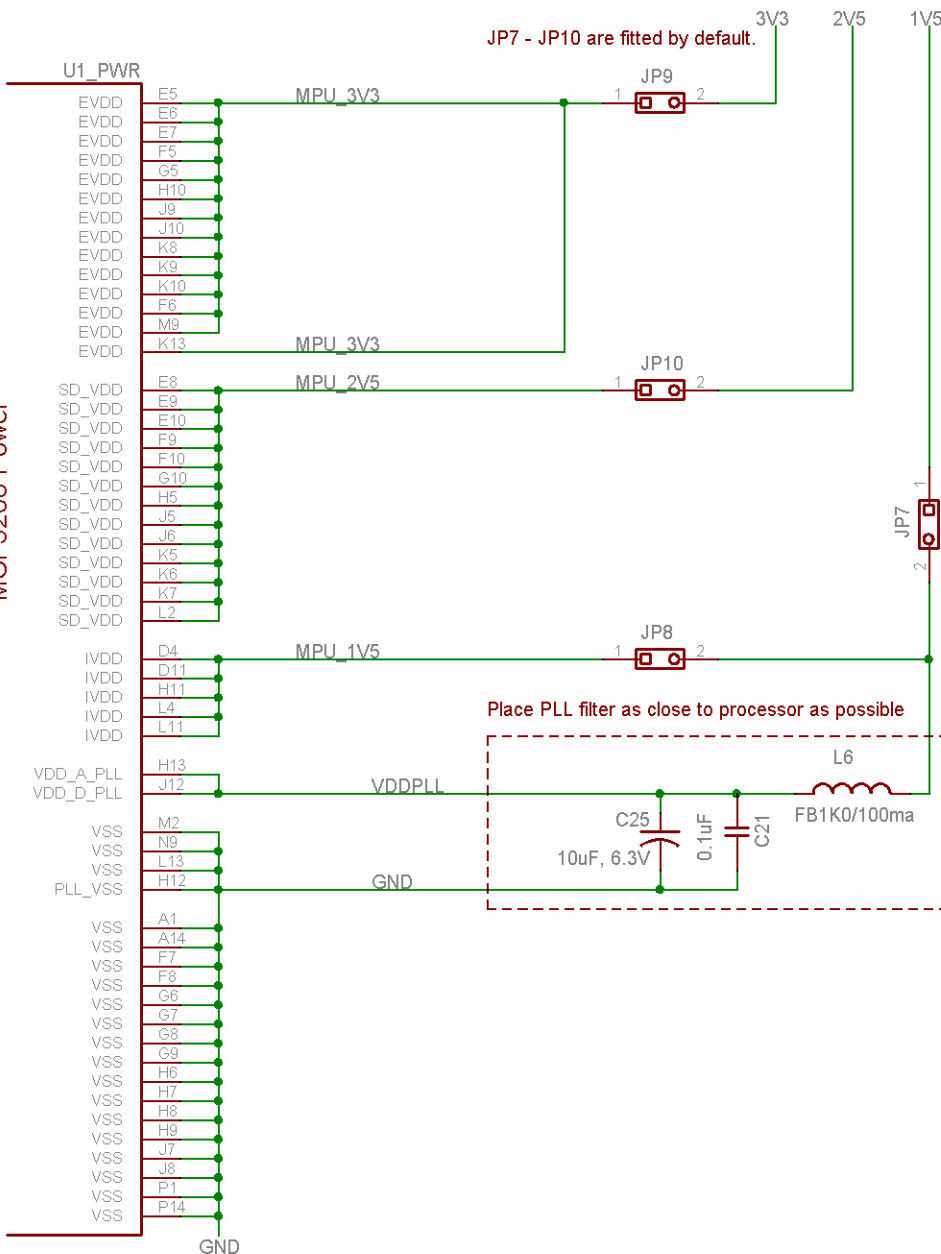
REV:
B

Date: 8/30/2005 12:20:51p

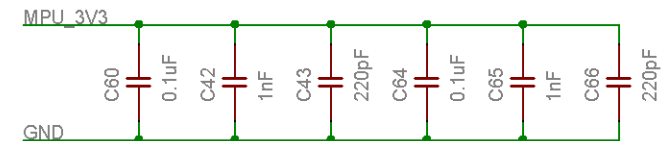
Sheet: 10/13



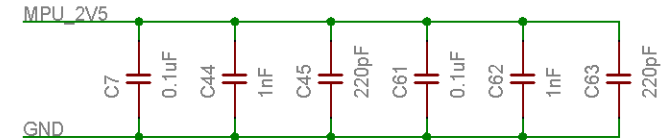
MCF5208 Power



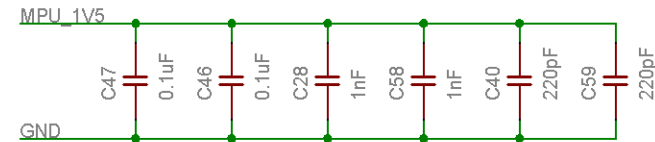
3.3V Decoupling



2.5V Decoupling



1.5V Decoupling



MCU Power Rails

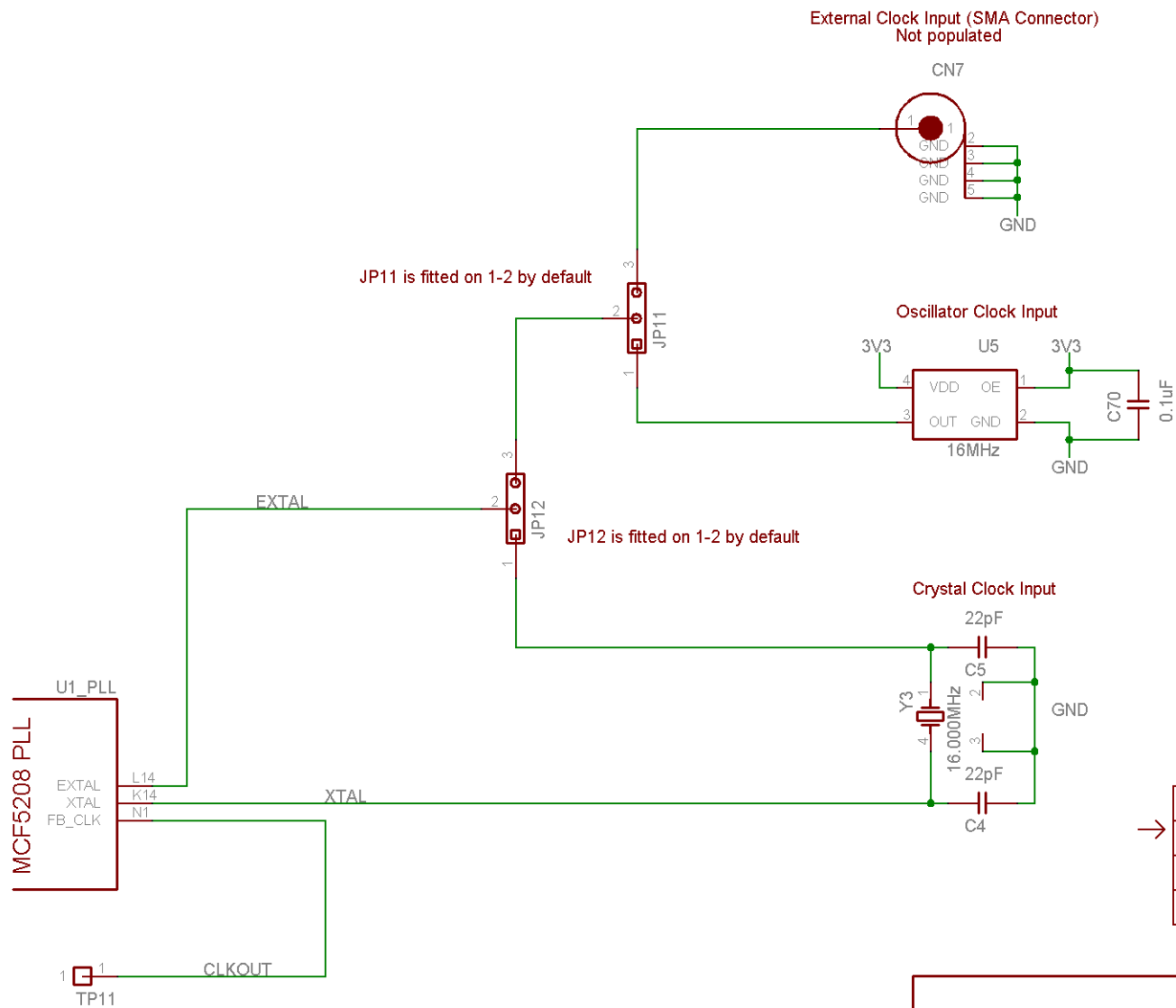
TITLE: M5208EVB_Rev_B

Document Number:

REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 12/13



Clock Input Selection

→

Clock Source	JP11	JP12
16MHz Crystal	1-2	---
16MHz Oscillator	2-3	1-2
External Clock	2-3	2-3

Clock

TITLE: M5208EVB_Rev_B

Document Number:

REV:
B

Date: 8/30/2005 12:20:51p

Sheet: 13/13