BlueCore™3-Multimedia

Single Chip Bluetooth® v1.2 System

Production Information Data Sheet For

BC358239A

December 2005

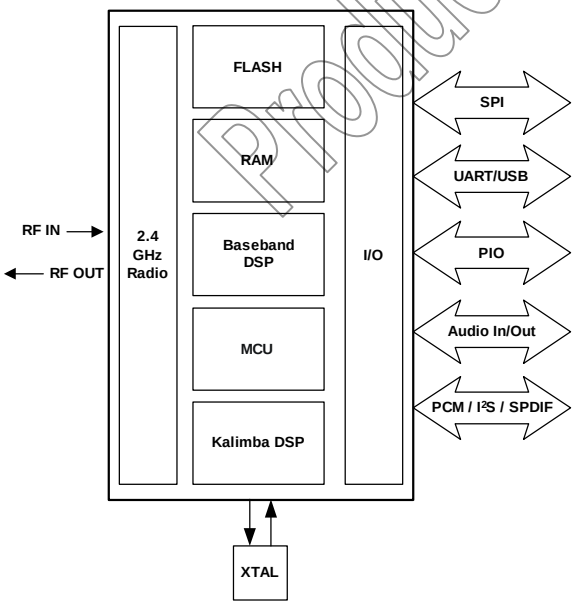
Device Features

- Fully Qualified Bluetooth system
- Bluetooth v1.2 Specification Compliant
- Kalimba DSP Open Platform Co-Processor
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Low Power 1.8V Operation
- 10 x 10mm 96-ball LFBGA Package
- Minimum External Components
- Integrated 1.8V regulator
- Dual UART Ports
- 16-bit Stereo Audio CODEC
- I^2S and SPDIF Interfaces
- RF 'Plug 'n' Go' package
- RoHS Compliant

General Description

BlueCore3-Multimedia is a single chip radio and baseband IC for Bluetooth 2.4GHz systems.

BC358239A contains 8Mbit of internal Flash memory. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v1.2 of the specification for data and voice communications.



BlueCore3-Multimedia System Architecture

Applications

- Stereo Headphones
- Automotive Hands-Free Kits
- Echo Cancellation
- High Performance Telephony Headsets
- Enhanced Audio Applications
- A/V Profile Support

BlueCore3-Multimedia contains the Kalimba DSP which is an open platform digital signal processor (DSP) co-processor allowing for support of enhanced audio applications.

BlueCore3-Multimedia has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v1.2 Specification.

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1 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs available
- Bluetooth v1.2 Specification compliant
- Antenna matching and filtering within the IC

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down, and wake up commands with an integrated low power oscillator for ultra-low power Park/Sniff/Hold mode
- 'Clock request' output to control an external clock
- On-chip linear regulator; 1.8V output from a 2.2-4.2V input
- Power-on-reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications

Kalimba DSP

- DSP co-processor, 32MIPs, 24-bit fixed point core
- Single cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 4Kword program memory, 2 x 8Kword data memory
- Flexible interfaces to BlueCore3 subsystem

Baseband and Software

- Internal 8Mbit Flash for complete system solution
- Internal 32Kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 1.5Mbaud with an optional bypass mode
- Full speed USB v1.1 interface supports OHCI and UHCI host interfaces
- Bi-directional serial programmable audio interface supporting PCM, I^2S and SPDIF formats
- Optional I^2C™ compatible interface

Stereo Audio CODEC

- 16-bit resolution, standard sample rates of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz and 48kHz (DAC only)
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving microphone and speakers with minimum external components

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded RFCOMM
- Customised builds with embedded application code

Package Options

- 96-ball LFBGA, 10 x 10 x 1.4mm, 0.8mm pitch

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2 10 x 10mm LFBGA Package Information

2.1 BC358239A-INN-E4 Pinout Diagram

Orientation from top of device

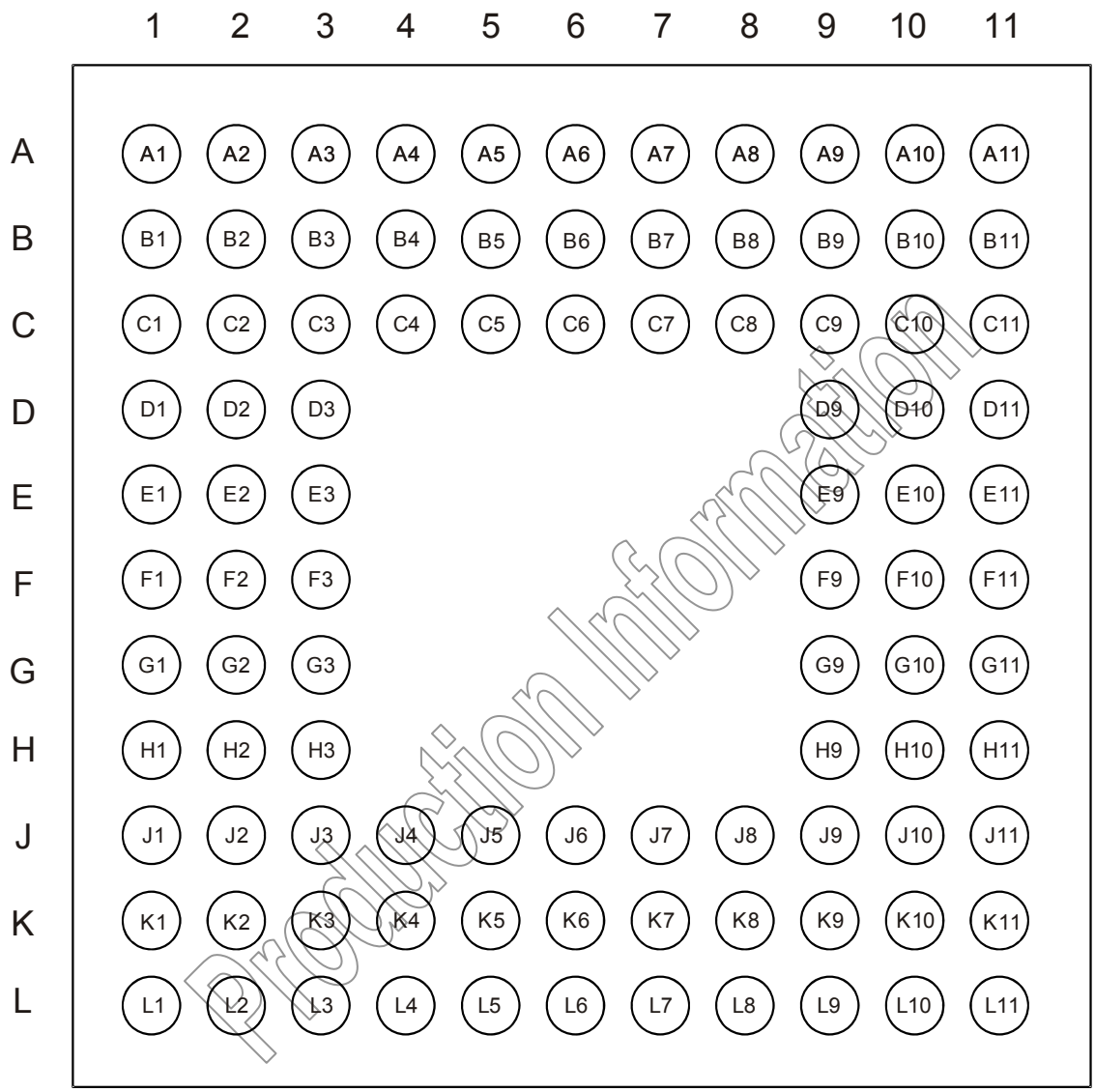

Figure 2.1: BC358239A BlueCore3-Multimedia Device Pinout

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2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D2	Analogue	Single ended receiver input
PIO[0]/RXEN	D3	Bi-directional with programmable strength internal pull-up/down	Control output for external TX/RX (if fitted)
PIO[1]/TXEN	C4	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted)
BAL_MATCH	A1	Analogue	Tie to VSS_RADIO
RF_CONNECT	B1	Analogue	50Ω RF matched I/O
AUX_DAC	C2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L3	Analogue	For crystal or external clock input
XTAL_OUT	L4	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tri-state, with weak internal pull-up	UART data output
UART_RX	J11	CMOS input with weak internal pull-down	UART data input
UART_RTS	L11	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	L9	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L8	Bi-directional	USB data minus

PCM Interface[1]	Ball	Pad Type	Description
PCM_OUT	G10	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

Notes:

(1) Pin names may be redefined dependent on chosen interface, see Table 6.1

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PIO Port	Ball	Pad Type	Description
PIO[11]	A5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	A4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]/UART_RX(1)	K9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]/CLK_REQ/ UART_CTS(1)	K8	Bi-directional with programmable strength internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[5]/USB_DETACH/ UART_RTS(1)	J9	Bi-directional with programmable strength internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[4]/USB_ON/ UART_TX(1)	H9	Bi-directional with programmable strength internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore3-Multimedia)
PIO[3]/USB_WAKE_UP/ HOST_CLK_REQ	B2	Bi-directional with programmable strength internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or clock request input from host controller
PIO[2]/CLK_REQ	C3	Bi-directional with programmable strength internal pull-up/down	PIO or external clock request
AIO[0]	K5	Bi-directional	Programmable input/output line
AIO[1]	J7	Bi-directional	Programmable input/output line
AIO[2]	K7	Bi-directional	Programmable input/output line
AIO[3]	J8	Bi-directional	Programmable input/output line

Test and Debug	Ball	Pad Type	Description
RESET	F9	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	G9	CMOS input, with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C10	CMOS input with weak internal pull-	Chip select for Synchronous Serial Interface active low
SPI_CLK	D10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	D11	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C11	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	E9	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

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CODEC	Ball	Pad Type	Description
AUDIO_IN_P_LEFT	K2	Analogue	Microphone input positive (left side)
AUDIO_IN_N_LEFT	K3	Analogue	Microphone input negative (left side)
AUDIO_IN_P_RIGHT	L1	Analogue	Microphone input positive (right side)
AUDIO_IN_N_RIGHT	L2	Analogue	Microphone input negative (right side)
AUDIO_OUT_P_LEFT	J4	Analogue	Speaker output positive (left side)
AUDIO_OUT_N_LEFT	J3	Analogue	Speaker output negative (left side)
AUDIO_OUT_P_RIGHT	J6	Analogue	Speaker output positive (right side)
AUDIO_OUT_N_RIGHT	J5	Analogue	Speaker output negative (right side)

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Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L7	VDD/Regulator input	Linear regulator input
VDD_USB	L10	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC(2)
VDD_PADS	E11	VDD	Positive supply for all other digital Input/Output ports (3)
VDD_CORE	F11, C7, L6	VDD	Positive supply for internal digital circuitry and 1.8V regulated output for digital circuitry, see further information in Section 8.14.1
VDD_RADIO	E3	VDD/Regulator sense	Positive supply for RF circuitry
VDD_LO	J2	VDD	Positive supply for local oscillator circuitry
VDD_ANA	L5	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VDD_BAL	F1	VDD	Positive supply for balun
VDD_MEM	C8, B11, K6	VDD	Positive supply for internal memory and AIO ports
VSS_PADS	D9, E10, K10	VSS	Ground connections for input/output
VSS_CORE	F10, C6	VSS	Ground connection for internal digital circuitry
VSS_RADIO	E2, F3, G2	VSS	Ground connections for RF circuitry
VSS_LO	G3, H3	VSS	Ground connections for local oscillator
VSS_ANA	K4	VSS	Ground connections for analogue circuitry
VSS	C9	VSS	Ground connection for internal package shield
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_BAL	G1	VSS	Ground connection for balun
VSS_MEM	C5	VSS	Ground connection for internal memory, AIO and extended PIO ports
VSS_RF	J1, K1	VSS	Ground connection for RF circuitry

Notes:

(1) Transparent UART port maps directly to main UART port

(2) Positive supply for PIO[3:0] and PIO[11:8]

(3) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
	A6, A7, A8, A9, A10, A11, B5, B6, B7, B8, B9, B10, C1, D1, E1, F2, H1, H2	Leave unconnected

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3 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA, VDD_BAL and VDD_CORE	-0.4V	2.2V
Supply Voltage: VDD_MEM, VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range	-40°C	+105°C
Guaranteed RF performance range (1)	-25°C	+85°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply Voltage: VDD_MEM, VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V(2)

Note:

(1) Typical figures are given for RF performance between -40°C and +105°C

(2) The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.2V

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Input/Output Terminal Characteristics				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage (Iload = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[(1)(2)]	-	-	1	mV rms
Load Regulation (Iload < 100 mA)	-	-	50	mV/A
Settling Time[(1)(3)]	-	-	50	µs
Maximum Output Current	140	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2[(6)]	V
Dropout Voltage (Iload = 70 mA)	-	-	350	mV
Quiescent Current (excluding load, Iload < 1mA)	25	35	50	µA
Low Power Mode[(4)]				
Quiescent Current (excluding load, Iload < 100µA)	4	7	10	µA
Disabled Mode[(5)]				
Quiescent Current	1.5	2.5	3.5	µA

Notes:

For optimum performance the VDD_ANA ball adjacent to VREG_IN should be used for regulator ouput

(1) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(2) Frequency range 100Hz to 100kHz.

(3) 1mA to 70mA pulsed load.

(4) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(5) Regulator is disabled when VREG_EN is pulled low. It can also be disabled by VREG_IN when it is either open circuit or driven to the same voltage as VDD_ANA

(6) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore3, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

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Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		+0.2	+1.0	+5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input leakage current				
VSS_PADS < V_{IN} < VDD_USB[(1)]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage levels to correctly terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

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Input/Output Terminal Characteristics (Continued)				
Power-on reset	**Min**	**Typ**	**Max**	**Unit**
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Input/Output Terminal Characteristics (Continued)					
Auxiliary ADC		**Min**	**Typ**	**Max**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[2]		-	-	700	Samples/s

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size[3]	12.5	14.5	17.0	mV
Output Voltage		monotonic[2]		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity[3]	-2	-	+2	LSB
Settling time (50pF load)	-	-	10	µs

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Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency(4)	8.0	-	32.0	MHz
Digital trim range(5)	5.0	6.2	8.0	pF
Trim step size(5)	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(6)	870	1500	2400	Ω
External Clock				
Input frequency(7)	7.5	-	40.0	MHz
Clock input level(8)	0.2	-	VDD_ANA	V pk-pk
Allowable Jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

Stereo Audio CODEC Characteristics							
Analogue to Digital Converter							
Parameter	**Symbol**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	NOB			-	-	16	Bits
Input Sample Rate	F_{sample}			8	-	44.1	kHz
Signal to Noise Ratio + Distortion	SINAD	0→½F_{sample}, f_{in} = 1kHz	F_{sample} = 8kHz	-	84	-	dB
			F_{sample} = 11.025kHz	-	83	-	dB
			F_{sample} = 16kHz	-	84	-	dB
			F_{sample} = 22.050kHz	-	83	-	dB
			F_{sample} = 32kHz	-	80	-	dB
			F_{sample} = 44.1kHz	-	74	-	dB
Digital Gain				-24		21.5	dB

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Digital to Analogue Converter							
Parameter	**Symbol**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	NOB			-	-	16	Bits
Output Sample Rate	F_{sample}			8	-	48	kHz
Gain Resolution				-	3	-	dB
Signal to Noise Ratio + Distortion	SINAD	0→20kHz, f_{in} = 1kHz	F_{sample} = 8kHz	-	79	-	dB
			F_{sample} = 11.025kHz	-	78	-	dB
			F_{sample} = 16kHz	-	79	-	dB
			F_{sample} = 22.050kHz	-	88	-	dB
			F_{sample} = 32kHz	-	90	-	dB
			F_{sample} = 44.1kHz	-	90	-	dB
			F_{sample} = 48kHz	-	89	-	dB
Digital Gain				-24	-	21.5	dB

Audio Input, Microphone Amplifier	Min	Typ	Max	Unit
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gain	-	400	-	mV rms
Gain resolution	-	3	-	dB
Distortion at 1kHz	-		-74	dB
Input referenced rms noise	-	8	-	µV rms
3dB Bandwidth	-	17	-	kHz
Input impedance	-	20	-	kΩ
THD+N (microphone input) @ 30mV rms input	-	-66	-	dB
THD+N (line input) @ 300mV Ω input[9]	-	-74	-	dB

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Audio Output, Speaker Output						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Allowed Load		Resistive	16	-	O.C.	Ω
		Capacitive	-	-	500	pF
Max output voltage		R_L=600Ω	-	2.0	-	V pk-pk
Max output current		R_L=22Ω	-	75	-	mA
Total Harmonic Distortion plus Noise	THD+N	f_{IN}=1kHz, BW=22Hz to 22kHz R_L=600Ω	-	0.015	-	%
Output noise relative to full scale	SNR	A Weighted, Po=digital silence, R_L=600Ω, BW=22Hz to 22kHz	-	-91	-	dB
Channel Separation (Crosstalk)	CS	f_{IN}=10kHz, analogue output set to maximum gain	-	-	-60	dB
Power Supply Rejection Ratio	PSRR	V_{ripple}=200mV_{pk-pk} sinewave, 10kHz at VREG_IN. 2.3V ≤ VREG_IN ≤ 4.1V, analogue output set to maximum gain	-	TBD	-	dB
Second Harmonic Level		1kHz sinewave, 1dB below full scale 600Ω	-	<-95	-	dB
Third Harmonic Level		1kHz sinewave, 1dB below full scale 600Ω	-	-95	-	dB

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Audio Output, Speaker Output (Continued)				
Typical THD+N Relative to Full Scale				
Full Scale Output, mV rms	**600Ω**		**22Ω**	
	%	**dB**	**%**	**dB**
10	0.180	-54.7	0.180	-54.7
14	0.120	-58.2	0.120	-58.2
20	0.090	-60.7	0.090	-60.7
28	0.060	-64.2	0.062	-63.9
40	0.046	-66.5	0.048	-66.1
57	0.032	-69.7	0.036	-68.6
80	0.025	-71.8	0.030	-70.2
113	0.018	-74.6	0.024	-72.1
160	0.015	-76.2	0.022	-72.9
226	0.015	-76.2	0.020	-73.7
320	0.015	-76.2	0.019	-74.2
453	0.015	-76.2	0.019	-74.2
640	0.014	-76.8	0.019	-74.2
905	0.014	-76.8	0.019	-74.2
1280	0.014	-76.8	0.022	-72.9
1810	0.014	-76.8		

Notes:

VDD_CORE, VDD_RADIO, VDD_LO, VDD_BAL and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled

(2) Access of ADC is through VM function and therefore sample rate given is achieved as part of this function

(3) Specified for an output voltage between 0.2V and VDD_PIO -0.2V. Output is high impedance when chip is in Deep Sleep mode

(4) Integer multiple of 250kHz

(5) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(6) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(7) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(8) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

(9) Input signal amplitudes are expressed as the differential voltages between the MIC_P and MIC_N terminals

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3.1 Power Consumption

Typical Average Current Consumption		
VDD=1.8V Temperature = +20°C Output Power = +4dBm		
Mode	**Average**	**Unit**
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	21	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	21	mA
SCO connection HV3 (No Sniff Mode) (Slave)	28	mA
SCO connection HV1 (Slave)	42	mA
SCO connection HV1 (Master)	42	mA
ACL data transfer 115.2kbps UART no traffic (Master)	5	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	22	mA
ACL data transfer 720kbps UART (Master or Slave)	45	mA
ACL data transfer 720kbps USB (Master or Slave)	45	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	3.2	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.45	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.55	mA
Standby Mode (Connected to host, no RF activity)	47.0	µA
Reset (RESET high or RESETB low)	15.0	µA
DSP		
DSP core (including PM memory access)		
Minimum (NOP)	0.25	mA/MIPS
Maximum (MAC)	0.65	mA/MIPS
DSP memory access (DM1 or DM2)	0.15	mA/MIPS
CODEC		
Microphone inputs and ADC / channel	0.85	mA
DAC and loudspeaker driver, no signal / channel	1.4	mA
Digital audio processing subsystem	8	mA

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4 Radio Characteristics

4.1 Temperature +20°C

4.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)(2)(3)	-	6.5	-	-6 to +4(4)	dBm
Variation in RF power over temperature range with compensation enabled (±)(4)	-	0.5	-	-	dB
Variation in RF power over temperature range with compensation disabled (±)(4)	-	2.5	-	-	dB
RF power control range(1)(2)	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power F=F0 ± 2MHz(5)	-	-35	-	≤-20	dBm
Adjacent channel transmit power F=F0 ± 3MHz(5)	-	-45	-	≤-40	dBm
Adjacent channel transmit power F=F0 >± 3MHz(5)	-	-55	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	165	-	140<f1avg<175	kHz
Δf2max "Minimum Modulation"	-	150	-	115	kHz
Δf1avg/Δf2avg	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/ 50µs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	8	-	≤40	kHz
2nd Harmonic Content	-	-55	-	≤-30	dBm
3rd Harmonic Content	-	-50	-	≤-30	dBm

Notes:

(1) Power at the chip pads

(2) Measured according to the Bluetooth specification v1.2

(3) The firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(4) Class 2 RF transmit power range, Bluetooth specification v1.2

(5) Measured at F_0 = 2441MHz

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4.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-85	-	≤-70	dBm
	2.441	-	-86	-		dBm
	2.480	-	-85	-		dBm
Maximum received signal at 0.1% BER		-	3	-	≥-20	dBm
C/I co-channel		-	6	-	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1)(2)		-	-5	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1)(2)		-	-2	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1)(2)		-	-35	-	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1)(2)		-	-22	-	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1)(2)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1)(2)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I F=FImage (1)(2)		-	-20	-	≤-9	dB
Maximum level of intermodulation interferers (3)		-	-30	-	≥-39	dBm
Spurious output level (4)		-	-140	-	-	dBm/Hz

Notes:

(1) Up to five exceptions are allowed in v1.2 of the Bluetooth specification. BlueCore3-Multimedia is guaranteed to meet the C/I performance as specified by the Bluetooth specification v1.2.

(2) Measured at F_0= 2441MHz

(3) Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c. i.e. wanted signal at -64dBm

(4) Integrated in 100kHz bandwidth. Actual figure is typically below -140dBm/Hz except for multiples of 800MHz. Spurious typically -70dBm in the Bluetooth band

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4.2 Temperature -40°C

4.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	8	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3)(4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3)(4)	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F=F_0 >\pm 3MHz$(3)(4)		-55	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max "Minimum Modulation"	-	145	-	115	kHz
Δf2avg / Δf1avg	-	0.95	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

Notes:

(1) BlueCore3-Multimedia firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to five exceptions are allowed in v1.2 of the Bluetooth specification

4.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-87.0	-	≤-70	dBm
	2.441	-	-88.0	-		
	2.480	-	-87.0	-		
Maximum received signal at 0.1% BER		-	1	-	≥-20	dBm

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4.3 Temperature -25°C

4.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(1)	-	7.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3)(4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3)(4)	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F=F_0 >\pm 3MHz$(3)(4)		-55	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	165	-	$140 \le \Delta f1_{avg} \le 175$	kHz
Δf2max "Minimum Modulation"	-	145	-	115	kHz
Δf2avg / Δf1avg	-	0.95	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	8	-	≤40	kHz

Notes:

(1) BlueCore3-Multimedia firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to five exceptions are allowed in v1.2 of the Bluetooth specification

4.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-87	-	≤-70	dBm
	2.441	-	-88	-		
	2.480	-	-87	-		
Maximum received signal at 0.1% BER		-	1	-	≥-20	dBm

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4.4 Temperature +85°C

4.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(1)	-	3.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3)(4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3)(4)	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F=F_0 >\pm 3MHz$(3)(4)		-55	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	165	-	$140 \le \Delta f1_{avg} \le 175$	kHz
Δf2max "Minimum Modulation"	-	145	-	115	kHz
Δf2avg / Δf1avg	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	9	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore3-Multimedia firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to five exceptions are allowed in v1.2 of the Bluetooth specification

4.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-81.5	-	≤-70	dBm
	2.441	-	-82.5	-		
	2.480	-	-81.5	-		
Maximum received signal at 0.1% BER		-	5	-	≥-20	dBm

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4.5 Temperature +105°C

4.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C					
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(1)	-	2	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3)(4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3)(4)	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F=F_0 >\pm 3MHz$(3)(4)		-55	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	165	-	$140 \le \Delta f1_{avg} \le 175$	kHz
Δf2max "Minimum Modulation"	-	130	-	115	kHz
Δf2avg / Δf1avg	-	0.9	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	9	-	≤20	kHz/50µs
Drift (single slot packet)	-	9	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore3-Multimedia firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to five exceptions are allowed in v1.2 of the Bluetooth specification

4.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-81	-	≤-70	dBm
	2.441	-	-81.5	-		
	2.480	-	-81	-		
Maximum received signal at 0.1% BER		-	5	-	≥-20	dBm

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5 Device Diagram

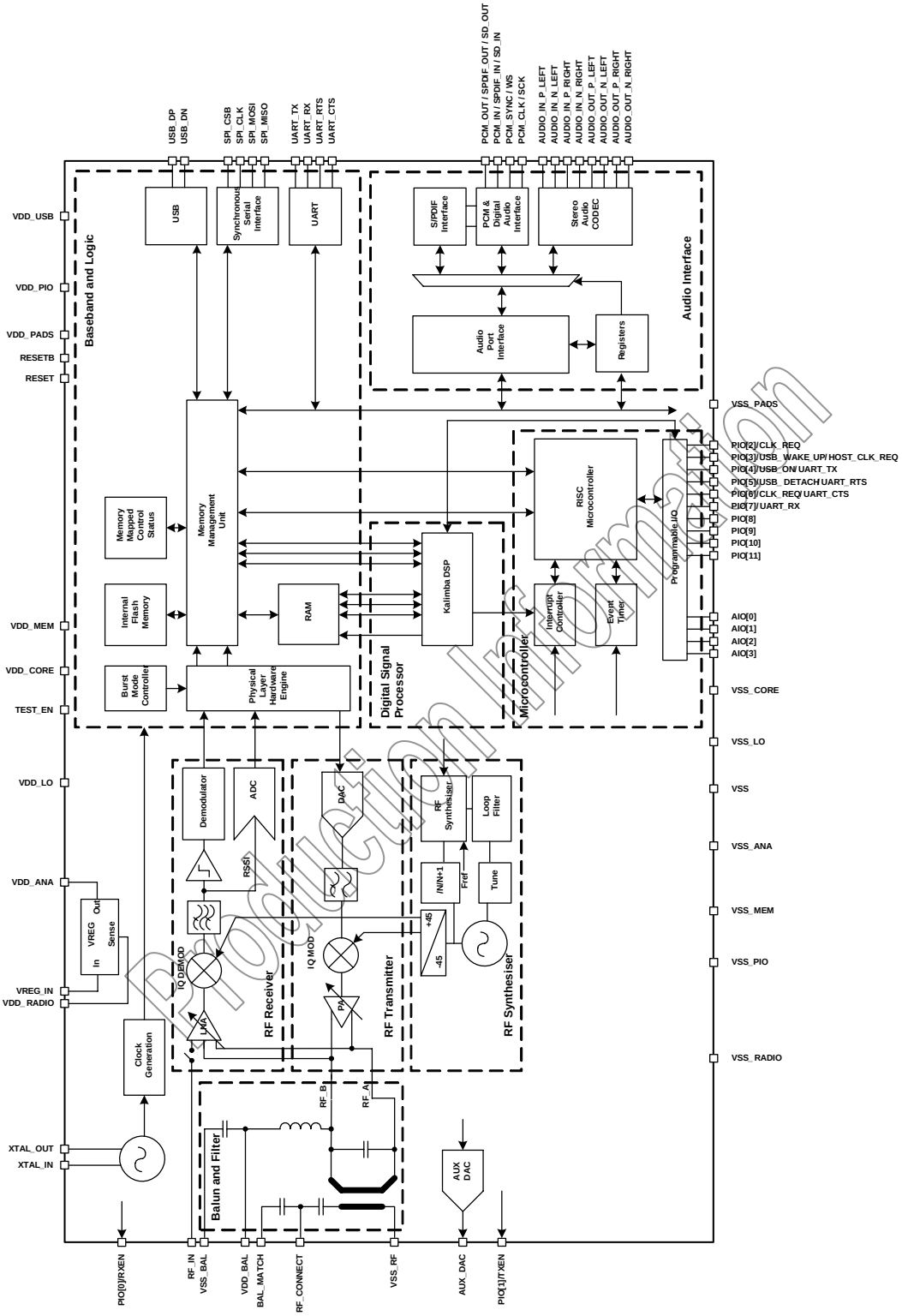

Figure 5.1: BlueCore3-Multimedia Device Diagram

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6 Description of Functional Blocks

6.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore3-Multimedia to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

6.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Differential mode is used for Class 2 operation.

6.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

6.2 RF Transmitter

6.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

6.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-Multimedia to be used in Class 2 and Class 3 radios without an external RF PA.

6.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA or any other customer specific application.

6.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth specification v1.2.

6.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

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6.5 Baseband and Logic

6.5.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

6.5.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

6.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware suports all optional and mandatory features of Bluetest v1.2 including AFH and eSCO

6.5.4 RAM

32Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

6.5.5 Kalimba DSP RAM

Further on-chip RAM is provided to support the Kalimba DSP as follows:

- 8K x 24-bit for data memory 1 (DM1)
- 8K x 24-bit for data memory 2 (DM2)
- 4K x 32-bit for program memory (PM)

6.5.6 FLASH Memory

8Mbits of internal Flash is available on the BC358239A. The Flash memory is provided for system firmware and the DSP co-processor code implementation.

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6.5.7 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore3-Multimedia acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

6.5.8 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

6.5.9 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

6.6 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

6.6.1 Programmable I/O

BlueCore3-Multimedia has a total of 16 (12 digital and 4 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

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6.7 Kalimba DSP

The Kalimba DSP is an open platform Kalimba DSP allowing signal processing functions to be performed on over air data or CODEC data in order to enhance audio applications. Figure 6.1 shows how the Kalimba DSP interfaces to other functional blocks within BlueCore3-Multimedia.

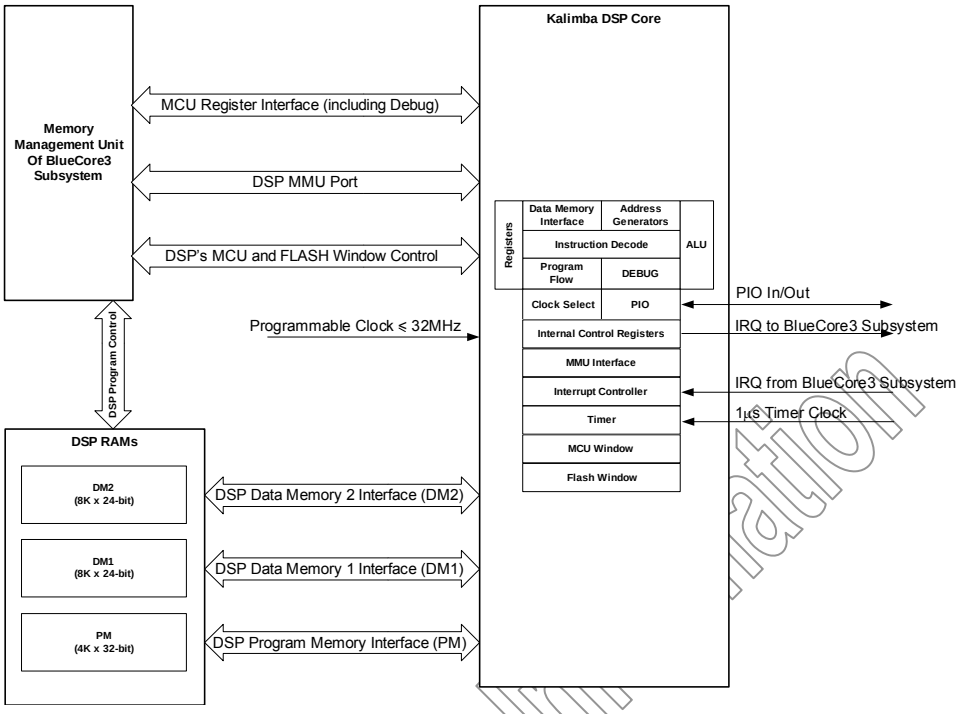

Figure 6.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 32MIPS performance, 24-bit fixed point DSP Core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping and branching
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

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6.8 Audio Interface

The audio interface circuit consists of a stereo audio CODEC, dual audio inputs and outputs, and a PCM, I^2S or SPDIF configurable interface. Figure 6.2 outlines the functional blocks of the interface. The CODEC supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the CODEC each contain two independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

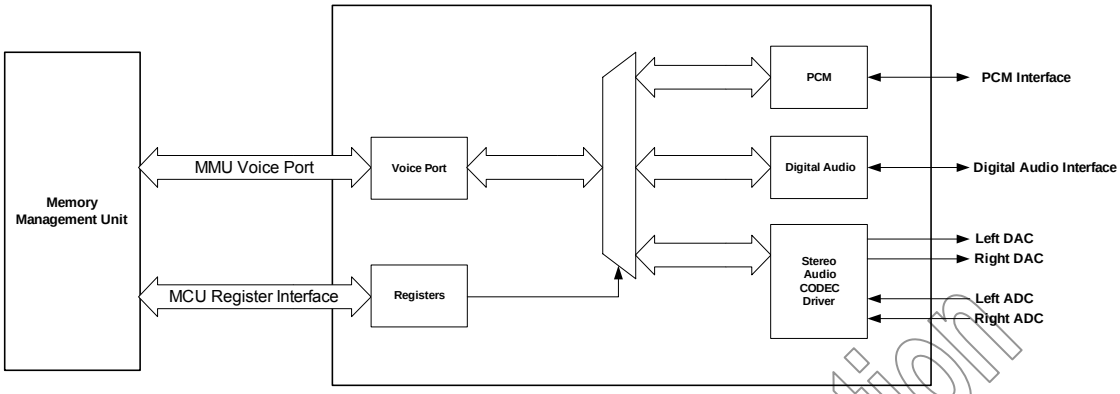

Figure 6.2: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM CODEC Interface described in Section 8.9.9 which means each of the audio busses are mutually exclusive in their usage. The pin out

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for the PCM interface with alternative pin descriptions can be seen in the device diagram shown in

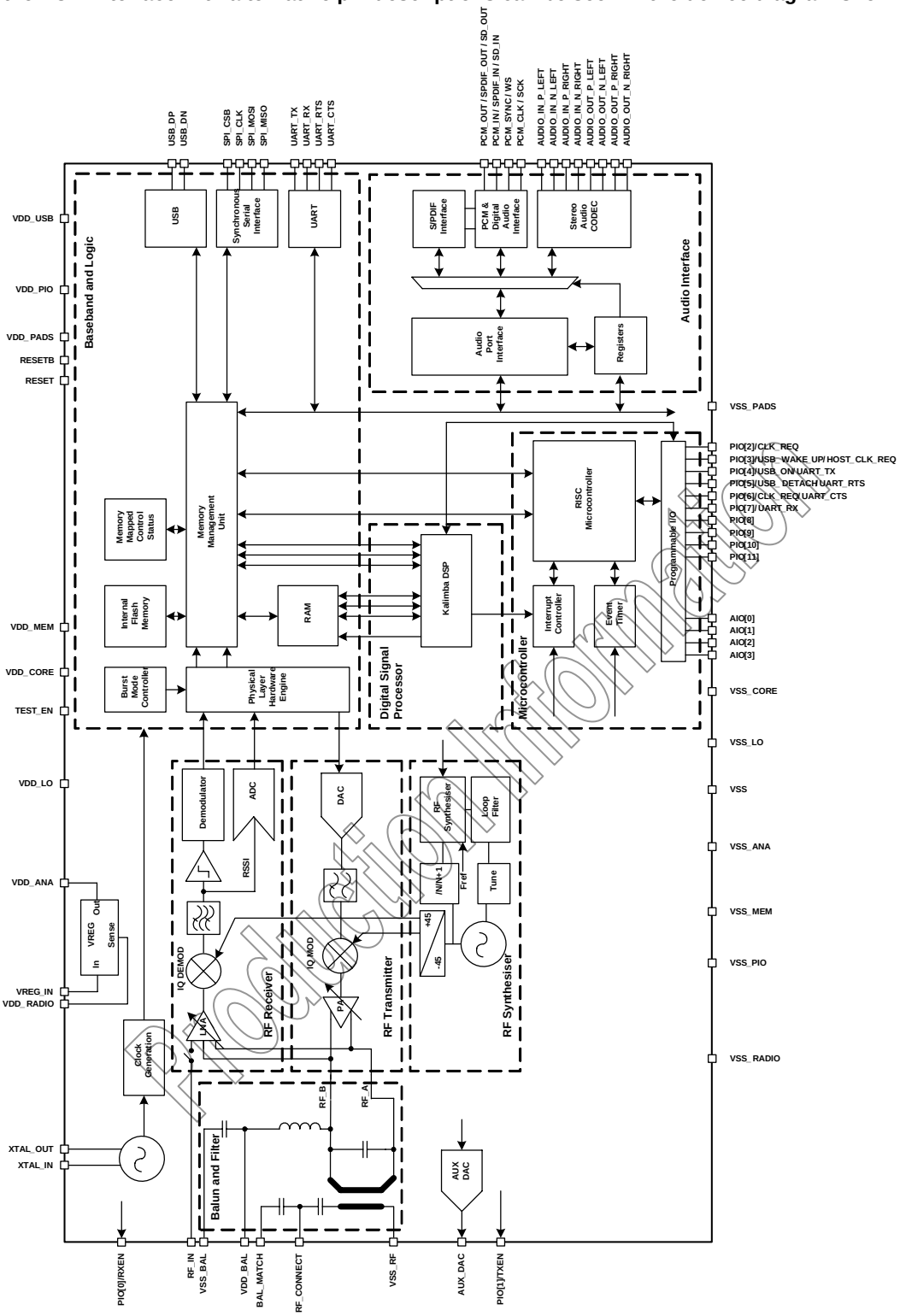

Figure 5.1 and Table 6.1 lists these alternative functions.

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PCM Interface	SPDIF Interface	I^2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

Table 6.1: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

6.8.1 Audio Input and Output

The audio input circuitry consists of a dual audio input that can be configured to be either single ended or fully differential and programmed for either microphone or line input. It has a programmable gain stage for optimisation of different microphones.

The audio output circuitry consists of a dual differential class A-B output stage.

6.8.2 Digital Audio Interface

The digital audio bus supports various digital audio bus standard, which include I^2S, and the interfaces contained within the IEC 60958 specification such as SPDIF and AES3. [(1)].

Notes:

[(1)] Subject to firmware support. Contact CSR for current status

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7 CSR Bluetooth Software Stacks

BlueCore3-Multimedia is supplied with Bluetooth v1.2 compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore3-Multimedia software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

7.1 BlueCore HCI Stack

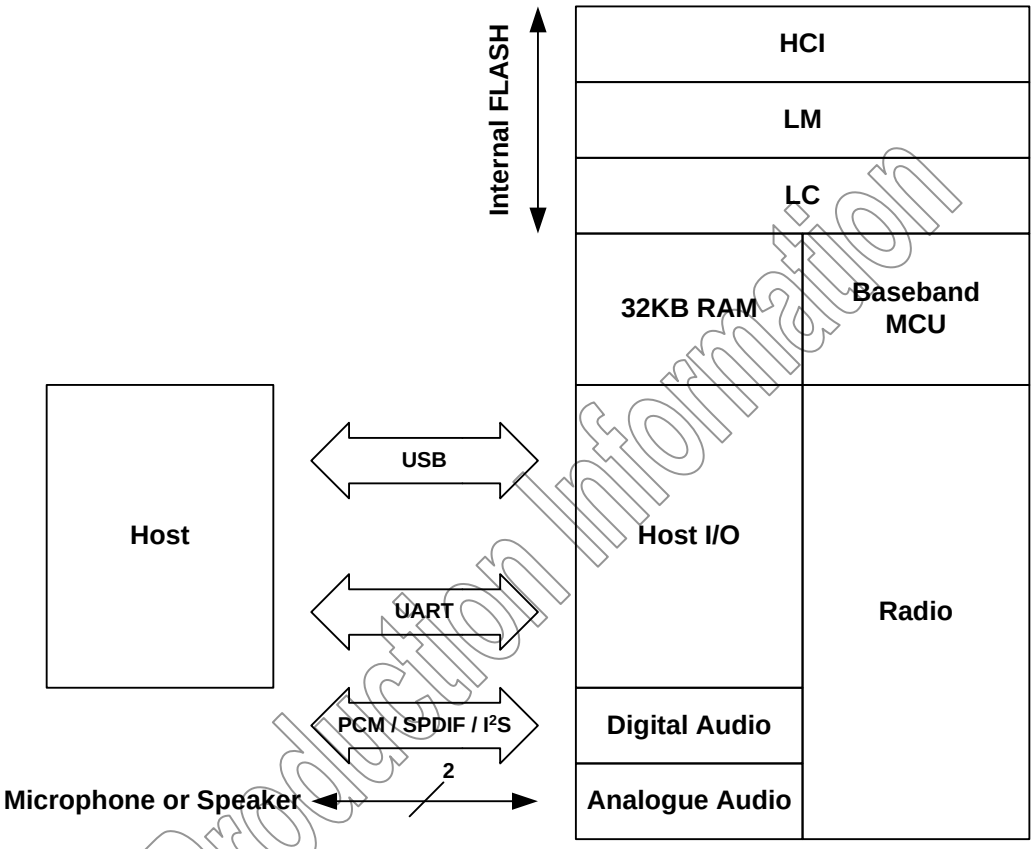

Figure 7.1: BlueCore HCI Stack

In the implementation shown in Figure 7.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

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7.1.1 Key Features of the HCI Stack - Standard Bluetooth Functionality

New Bluetooth v1.2 Mandatory Functionality:

- Adaptive frequency hopping (AFH), including classifier
- Faster connection
- LMP improvements
- Parameter ranges

Optional v1.2 functionality supported:

- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware has been written against the Bluetooth Core Specification v1.2.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kbps asymmetric(1)
- Operation with up to 7 active slaves(1)
- Operation as slave to one master while master of several slaves (Scatternet “2.0”)
- Page and Inquiry scanning while slave and master (Scatternet “2.5”)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding, plus “transparent SCO”
- Standard operating modes; page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

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The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from http://www.csr.com.

Note:

(1) Maximum allowed by Bluetooth specification v1.2

(2) BlueCore3-Multimedia supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.2

7.1.2 Key Features of the HCI Stack - Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command"), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's "persistent store" configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:
  1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  3. With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a deep sleep state
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LED's via the chip's PIO port.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

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7.2 Stand-Alone BlueCore3-Multimedia and Kalimba DSP Applications

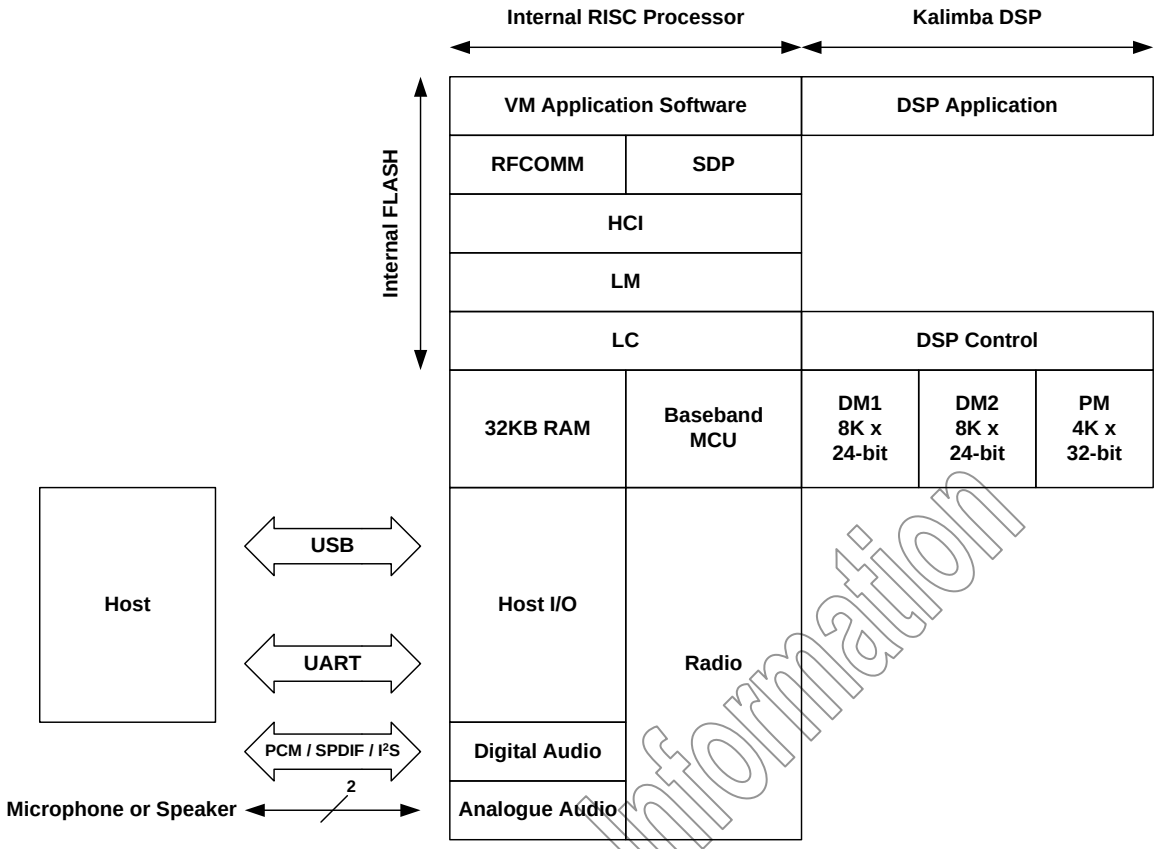

Figure 7.2: Kalimba DSP Stack

In Figure 7.2, this version of the stack firmware shown requires no host processor (but can use a host processor for debugging etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

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7.3 Host-Side Software

BlueCore3-Multimedia can be ordered with companion host-side software:

- BlueCore3-PC includes software for a full Windows®98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.
- BlueCore3-Mobile includes software for a full host-side stack designed for modern ARM based mobile handsets together with IC hardware described in this document.

7.4 Device Firmware Upgrade

BlueCore3-Multimedia is supplied with boot loader software, which implements a Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the Flash memory through BlueCore3--Multimedia UART or USB ports.

7.5 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore IC's. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application e.g. a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains 3 elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). With BCHS also come example applications in ANSI C, which makes the process of writing the application easier.

7.6 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore3-Multimedia, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as ‘C’ source or object code.

7.7 CSR Development Systems

CSR’s BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore3-Multimedia hardware and software, and as toolkits for developing on-chip and host software.

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8 Device Terminal Descriptions

8.1 RF Ports

The BlueCore3-Multimedia RF_IN terminal can be configured as either a single ended or differential input. The operational mode is determined by the setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x20).

8.1.1 Single-Ended Input (RF_IN)

This is the single ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

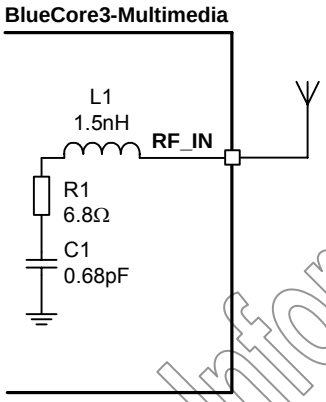

Figure 8.1: Circuit RF_IN

Note:

Both terminals must be externally DC biased to VDD_RADIO.

8.1.2 RF Plug 'n' Go

The 10 x 10mm 96-ball LFBGA package used on the BlueCore3-Multimedia device is a RF Plug 'n' Go package where the terminal RF_CONNECT forms an unbalanced ouput with a nominal 50Ω impedance. This terminal can be directly connected to an antenna requiring no impedance matching network as shown in Figure 8.2.

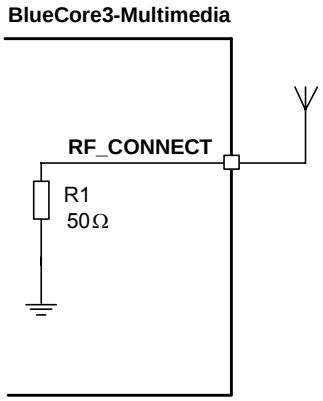

Figure 8.2: Circuit for RF_CONNECT

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8.2 Transmit Port Impedances for Plug-n-Go Package

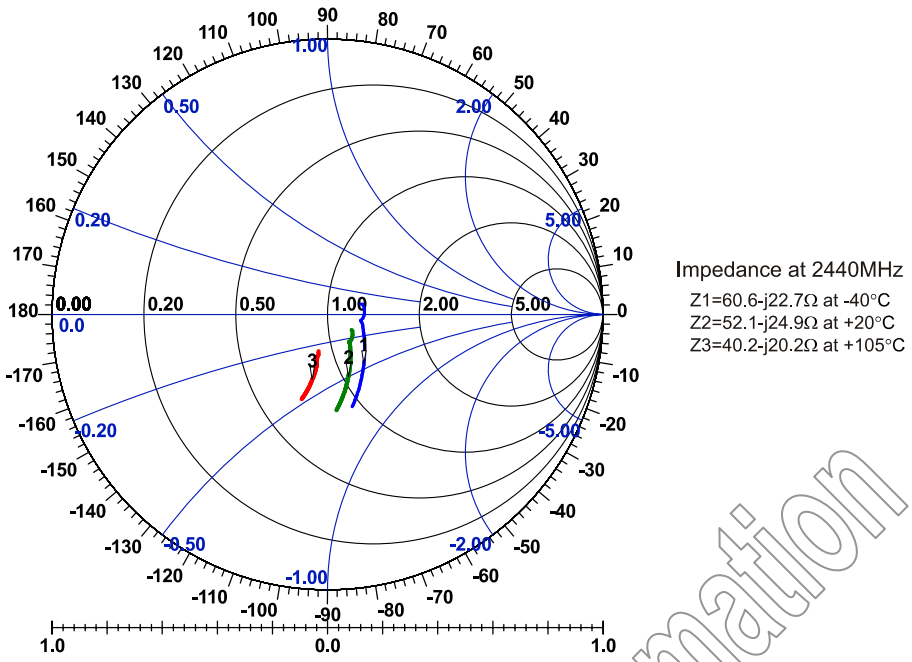

Figure 8.3: RF_CONNECT Output at Power Setting 35

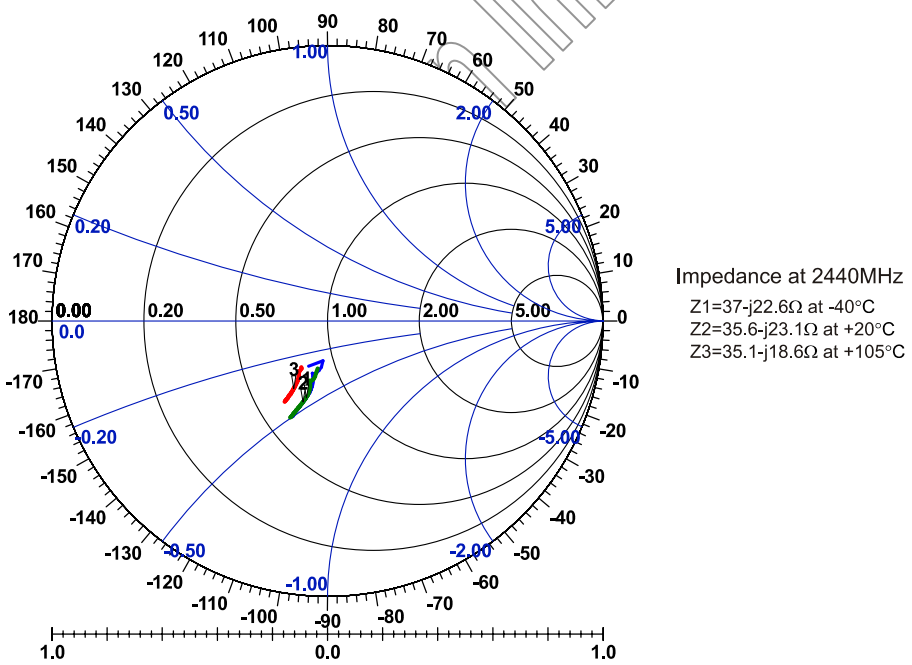

Figure 8.4: RF_CONNECT Output at Power Setting 50

Note:

Power setting 50 corresponds to about 3dBm.

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8.3 Receive Port Impedances for Plug-n-Go Package

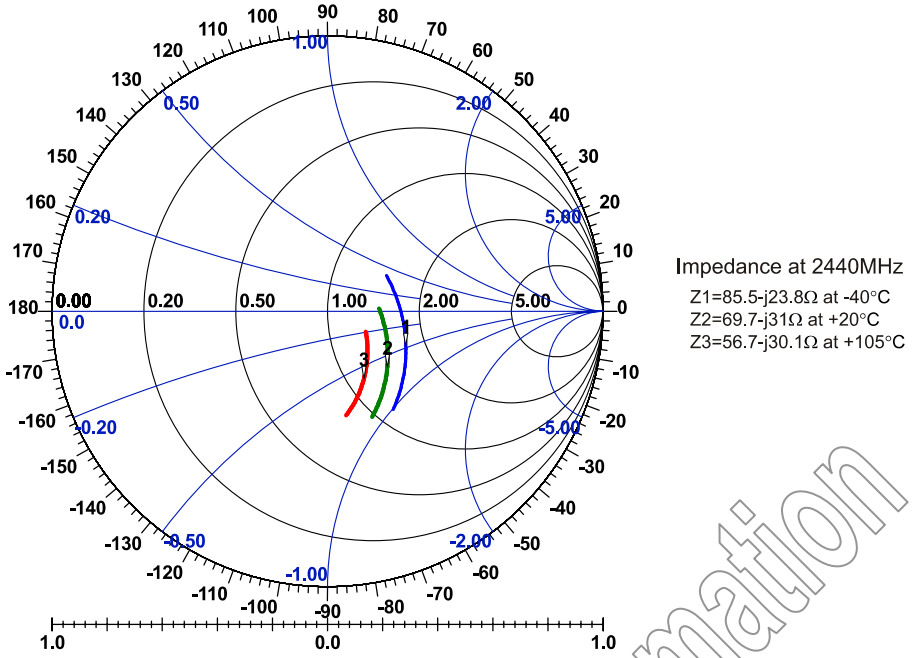

Figure 8.5: RF_CONNECT Matched in Receive Mode

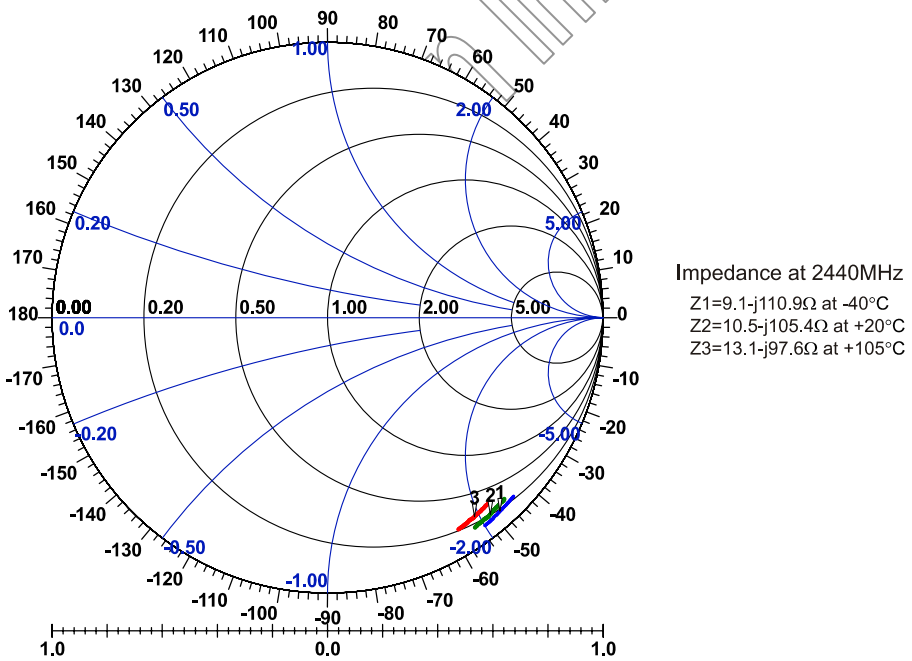

Figure 8.6: RF_IN Unmatched in Receive Mode

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8.4 External Reference Clock Input (XTAL_IN)

The BlueCore3-Multimedia RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore3-Multimedia XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in Section 8.5.

8.4.1 External Mode

BlueCore3-Multimedia can be configured to accept an external reference clock (from another device, such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 8.1:

	Min	Typ	Max
Frequency(1)	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA(2)(3)

Table 8.1: External Clock Specifications

Notes:

(1) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(2) VDD_ANA is 1.8V nominal

(3) If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk

8.4.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

8.4.3 Clock Timing Accuracy

As Figure 8.7 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v1.2 specification. Radio activity may occur after 11ms, therefore at this point, the timing accuracy of the external clock source must be within 20ppm.

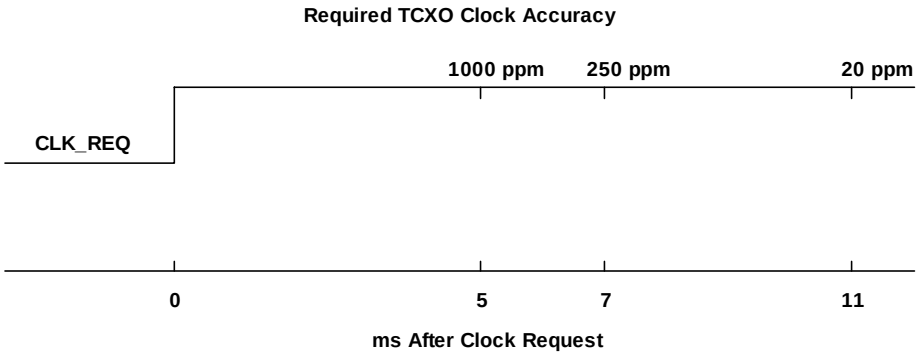

Figure 8.7: TCXO Clock Accuracy

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8.4.4 Clock Start-Up Delay

BlueCore3-Multimedia hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore3-Multimedia firmware provides a software function which will extend the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore3-Multimedia as low as possible. BlueCore3-Multimedia will consume about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

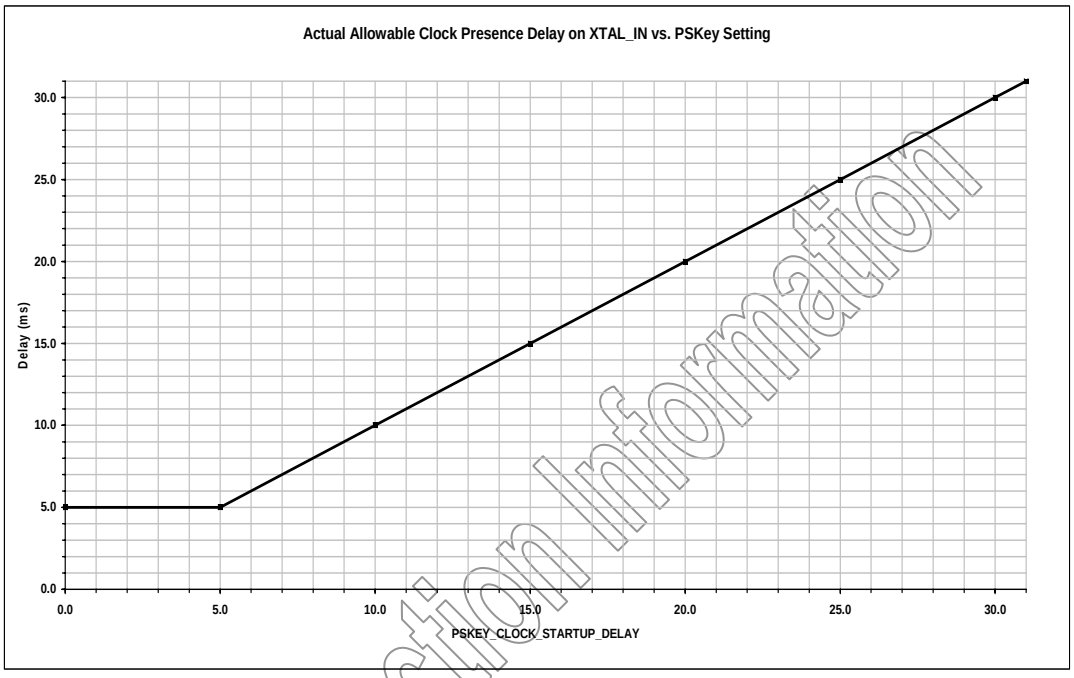

Figure 8.8: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key Setting

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8.4.5 Input Frequencies and PS Key Settings

BlueCore3-Multimedia should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250KHz. The input frequency default setting in BlueCore3-Multimedia is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. This is accomplished by also changing PSKEY PLLX_FREQ_REF (0xabc).

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 8.2: PS Key Values for CDMA/3G Phone TCXO Frequencies

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8.5 Crystal Oscillator (XTAL_IN, XTAL_OUT)

The BlueCore3-Multimedia RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore3-Multimedia XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external reference clock mode is described in Section 8.2.

8.5.1 XTAL Mode

BlueCore3-Multimedia contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

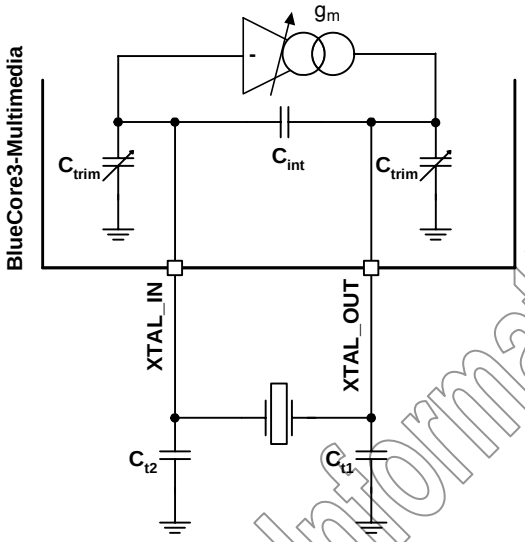

Figure 8.9: Crystal Driver Circuit

Figure 8.10 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

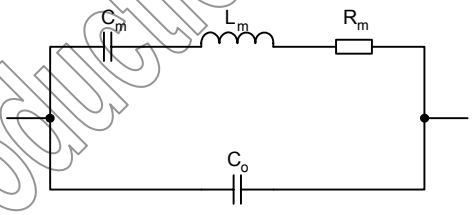

Figure 8.10: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore3-Multimedia contains variable internal capacitors to provide a fine trim.

The BlueCore3-Multimedia driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

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8.5.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore3-Multimedia provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on chip clocks are referred. Crystal load capacitance, C_l is calculated with the following equation:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Equation 8.1: Load Capacitance

Where:

Ctrim = 3.4pF nominal (Mid range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance, it is the driver self capacitance

8.5.3 Frequency Trim

BlueCore3-Multimedia enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the Persistent Store Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110\ \text{fF} \times \text{PSKEY_ANA_FTRIM}$$

Equation 8.2: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 8.3:

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 55 \times 10^{-3} (\text{ppm/LSB})$$

Equation 8.3: Frequency Trim

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 8.4:

$$\frac{\partial(F_x)}{\partial(C)} = F_x \cdot \frac{C_m}{4(C_l + C_0)^2}$$

Equation 8.4: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 8.10.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

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8.5.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore3-Multimedia uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$g_m > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{(2\pi F_x)^2 R_m((C_0+C_{int})(C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 8.5: Transconductance Required for Oscillation

BlueCore3-Multimedia guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk–pk. The drive level is determined by the crystal driver transconductance, by setting the Persistent Store KEY_XTAL_LVL (0x241).

8.5.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore3-Multimedia crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 8.6:

$$R_{neg} > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{g_m(2\pi F_x)^2(C_0+C_{int})((C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 8.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore3-Multimedia driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 8.3: Crystal Oscillator Specification

8.5.6 Crystal PS Key Settings

See tables in Section 8.4.5.

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8.5.7 Crystal Oscillator Characteristics

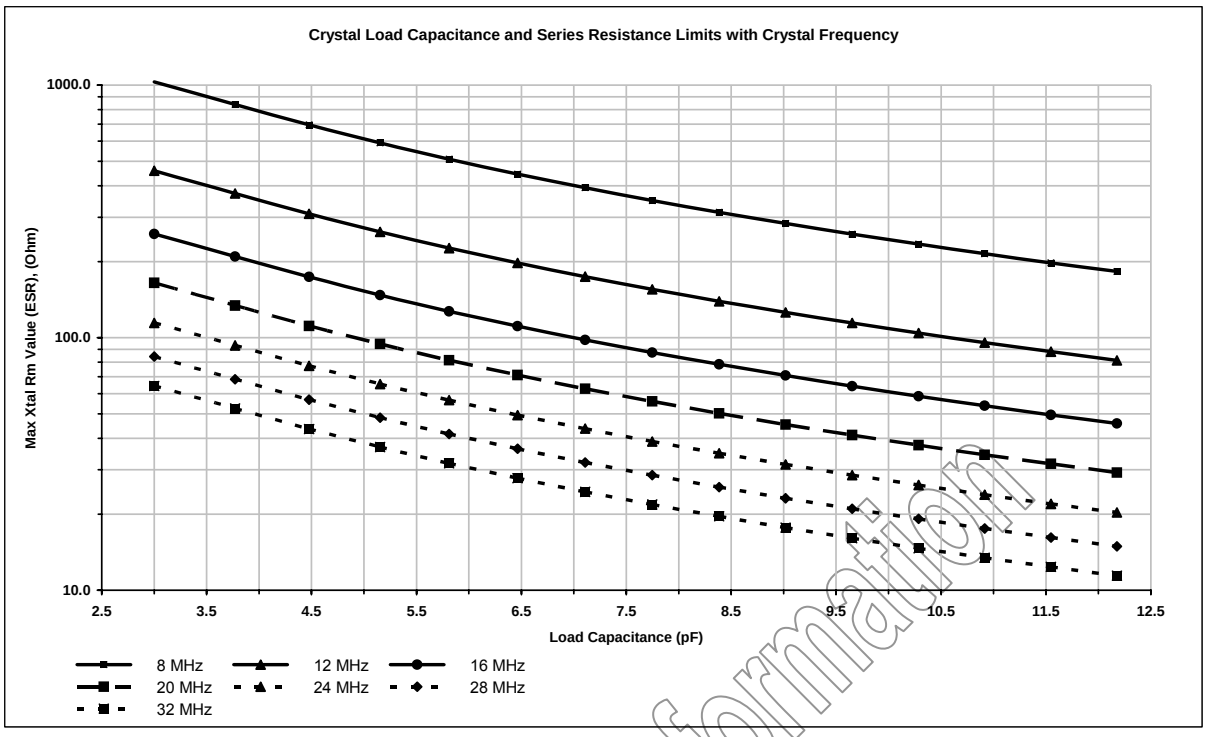

Figure 8.11: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore3-Multimedia crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

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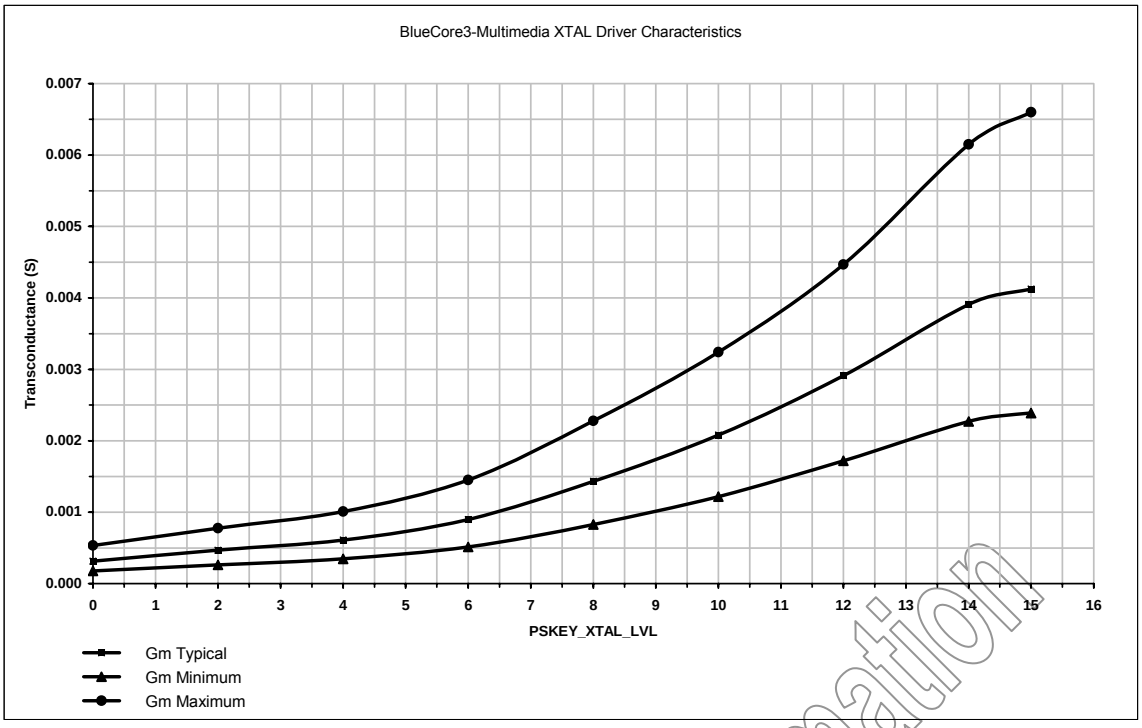

Figure 8.12: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by Persistent Store Key PSKEY_XTAL_LVL (0x241).

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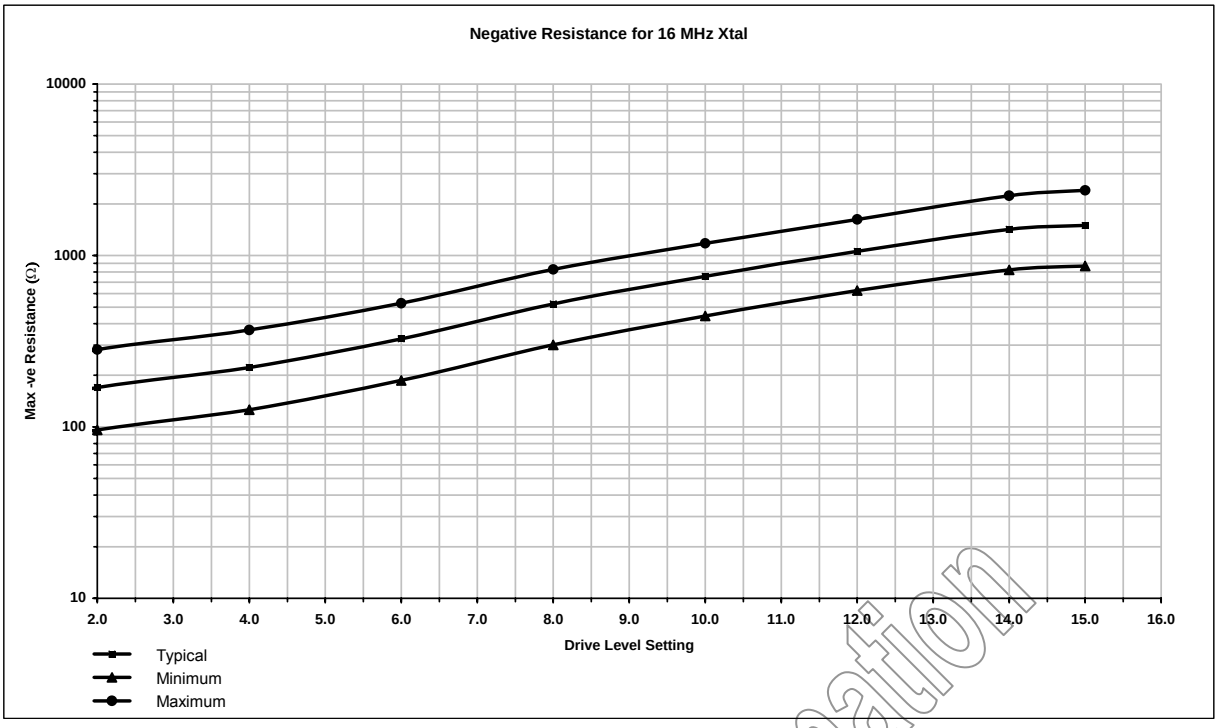

Figure 8.13: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (Please refer to your software build release note for frequencies supported);

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

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8.6 UART Interface

BlueCore3-Multimedia Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol[(1)].

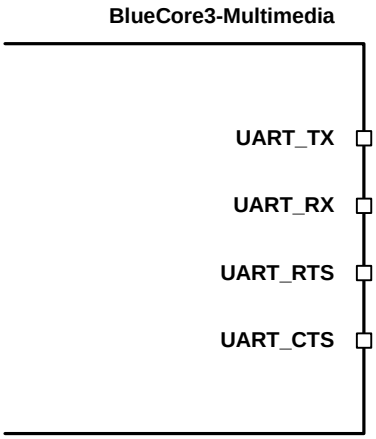

Figure 8.14: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 8.14. When BlueCore3-Multimedia is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as Baud rate and packet format, are set using BlueCore3-Multimedia software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud (≤2%Error)
		9600 Baud (≤1%Error)
	Maximum	1.5MBaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 8.4: Possible UART Settings

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The UART interface is capable of resetting BlueCore3-Multimedia upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 8.15. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore3-Multimedia can emit a Break character that may be used to wake the Host.

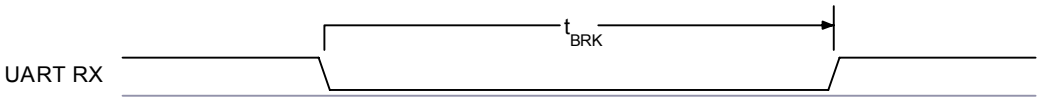

Figure 8.15: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 8.5 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation 8.7.

$$\text{Baud Rate} = \frac{\text{PSKEY_UART_BAUD_RATE}}{0.004096}$$

Equation 8.7: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%

Table 8.5: Standard Baud Rates

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8.6.1 UART Bypass

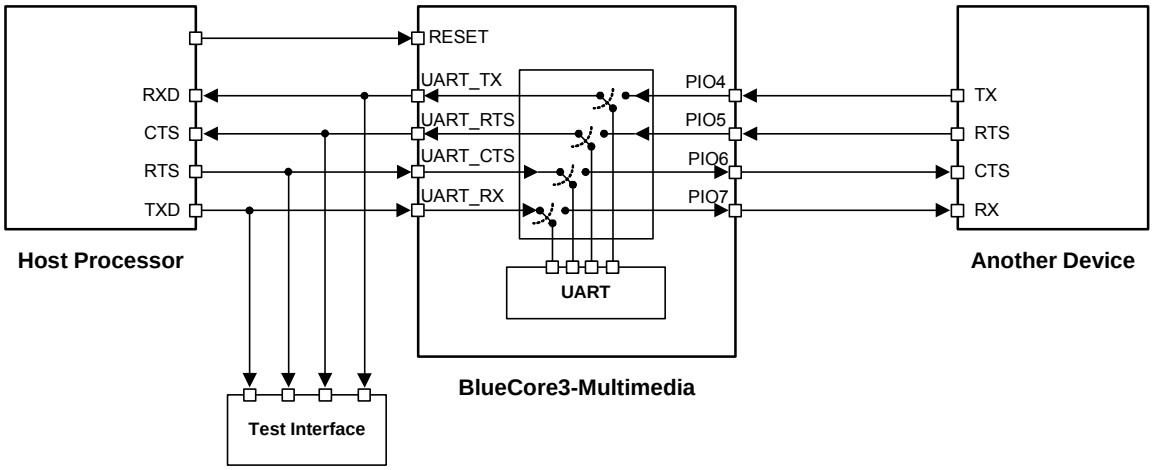

Figure 8.16: UART Bypass Architecture

8.6.2 UART Configuration While RESET is Active

The UART interface for BlueCore3-Multimedia while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore3-Multimedia reset is de-asserted and the firmware begins to run.

8.6.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore3-Multimedia can be used. The default state of BlueCore3-Multimedia after reset is de-asserted, this is for the host UART bus to be connected to the BlueCore3-Multimedia UART, thereby allowing communication to BlueCore3-Multimedia via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS[(1)].

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore3-Multimedia upon this, it will switch the bypass to PIO[7:4] as shown in Figure 8.16. Once the bypass mode has been invoked, BlueCore3-Multimedia will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore3-Multimedia, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

8.6.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

Note:

(1) The range of the signalling level for the standard UART described in Section 8.6 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent. For BlueCore3-Multimedia the standard UART is supplied by VDD_USB so has signalling levels of 0V and VDD_USB. Whereas in the UART bypass mode the signals appear on the PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

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8.7 USB Interface

BlueCore3-Multimedia devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v1.2 or alternatively can appear as a set of endpointd appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), BlueCore3-Multimedia only supports USB Slave operation.

8.7.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore3-Multimedia and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP / USB_DN and the cable.

8.7.2 USB Pull-Up Resistor

BlueCore3-Multimedia features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore3-Multimedia is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

8.7.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

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8.7.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore3-Multimedia via a resistor network (R_{vb1} and R_{vb2}), so BlueCore3-Multimedia can detect when VBUS is powered up. BlueCore3-Multimedia will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in BlueCore is only suitable for bus powered USB devices i.e. dongles.

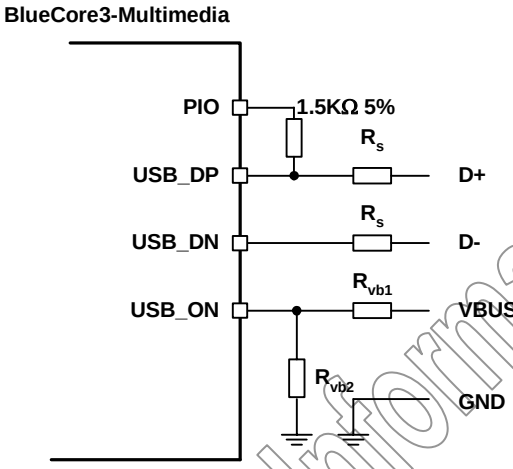

Figure 8.17: USB Connections for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

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8.7.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore3-Multimedia negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus powered mode, BlueCore3-Multimedia requests 100mA during enumeration.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore3-Multimedia will result in reduced receive sensitivity and a distorted RF transmit signal.

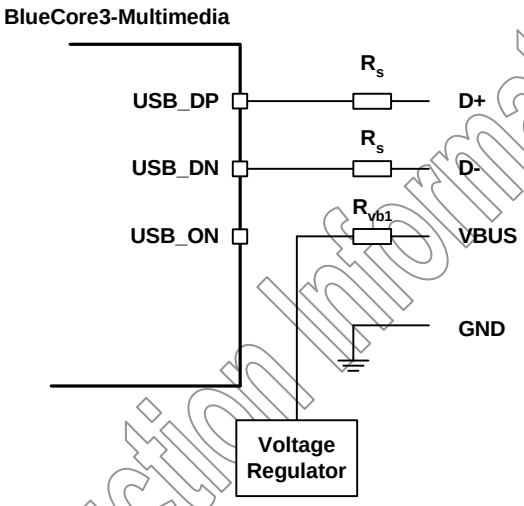

Figure 8.18: USB Connections for Bus Powered Mode

Note:

USB_ON is shared with BlueCore3-Multimedia PIO terminals

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 8.6: USB Interface Component Values

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8.7.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend, bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore3-Multimedia. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

8.7.7 Detach and Wake_Up Signalling

BlueCore3-Multimedia can provide out-of-band signalling to a host controller by using the control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore3-Multimedia into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore3-Multimedia to put USB_DN and USB_DP in a high impedance state and turned off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore3-Multimedia will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while BlueCore3-Multimedia is effectively disconnected from the bus.

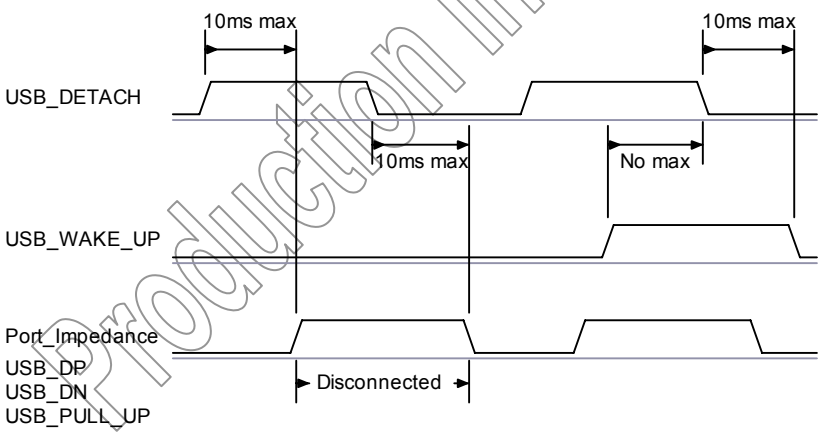

Figure 8.19: USB_DETACH and USB_WAKE_UP Signal

8.7.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore3-Multimedia and Bluetooth software running on the host computer. Suitable drivers are available from www.csrsupport.com.

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8.7.9 USB 1.1 Compliance

BlueCore3-Multimedia is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore3-Multimedia meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

8.7.10 USB 2.0 Compatibility

BlueCore3-Multimedia is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

8.8 Serial Peripheral Interface

BlueCore3-Multimedia uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore3-Multimedia via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

8.8.1 Instruction Cycle

The BlueCore3-Multimedia is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The instruction cycle for a SPI transaction is shown in Table 8.7.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 8.7: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore3-Multimedia on the rising edge of the clock line SPI_CLK. When reading, BlueCore3-Multimedia will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is teminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore3-Multimedia offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

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8.8.2 Writing to BlueCore3-Multimedia

To write to BlueCore3-Multimedia, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

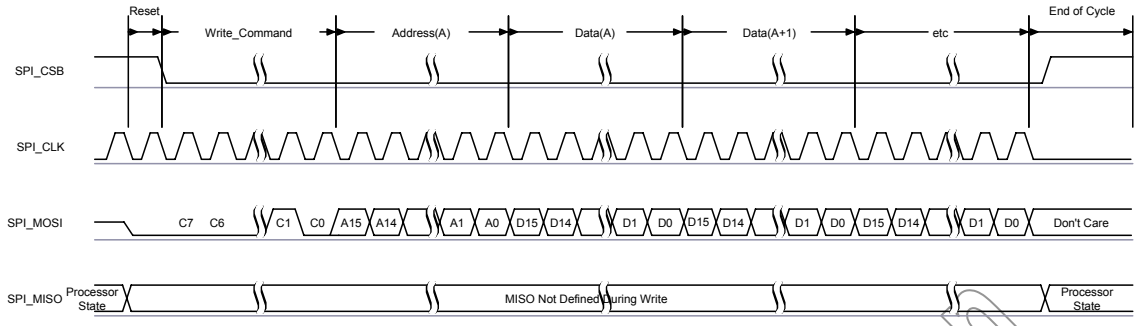

Figure 8.20: Write Operation

8.8.3 Reading from BlueCore3-Multimedia

Reading from BlueCore3-Multimedia is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore3-Multimedia then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

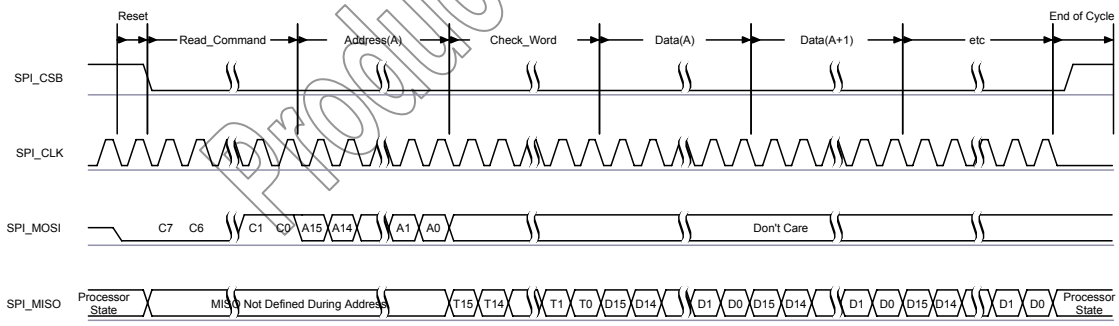

Figure 8.21: Read Operation

8.8.4 Multi Slave Operation

BlueCore3-Multimedia should not be connected in a multi slave arrangement by simple parallel connection of slave MISO lines. When BlueCore3-Multimedia is deselected (SPI_CSB = 1), the SPI_MISO line does not float, instead, BlueCore3-Multimedia outputs 0 if the processor is running or 1 if it is stopped.

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8.9 Stereo Audio Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I^2S
- Support for IEC-60958 standard stereo digital audio bus standards i.e. S/PDIF and AES3/EBU
- Support for PCM interfaces including PCM master CODECs that require an external system clock

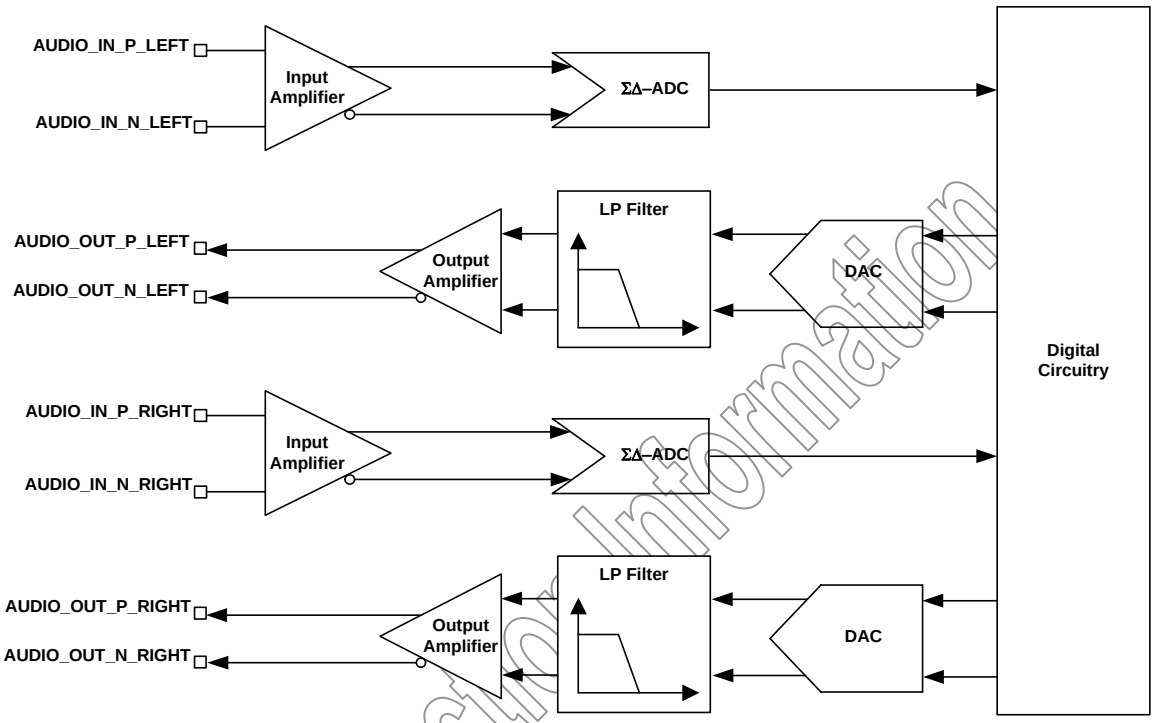

Figure 8.22: Stereo CODEC Audio Input and Output Stages

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.8V and uses a minimum of external components.

Important Note:

To avoid any confusion with respect to stereo operation this data book with respect to hardware explicitly states which is the left and right channel for audio input and output. With respect to software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel for both input and output.

For mono operation this data book uses the left channel for standard mono operation for audio input and output and with respect to software and any registers, channel 0 or channel A represents the standard mono channel for audio input and output. In mono operation the second channel which is the right channel, channel 1 or channel B could be used as a second mono channel if required and this channel will be known as the auxilliary mono channel for audio input and output.

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8.9.1 Stereo CODEC Set-Up

The configuration and control of the ADC is through VM functions which are described in appropriate BlueLab Multimedia documentation. This section covers an overview of the parameters that can be set-up using the VM functions.

The Kalimba DSP can communicate its requirements of the CODEC to the MCU and hence the VM by exchange of messages. The messages used between the Kalimba DSP and the embedded MCU are based on interrupts: one interrupt between the MCU and Kalimba DSP and one interrupt between the Kalimba DSP and the MCU. Message content is transmitted using shared memory. There are VM and DSP library functions to send and receive messages; for further details refer to BlueLab Multimedia documentation.

8.9.2 ADC

The ADC consists of two second order Sigma Delta converters allowing two separate channels that are identical in functionality, as shown in Figure 8.22.

8.9.3 ADC Sample Rate Selection and Warping

Each ADC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.05kHz
- 24kHz
- 32kHz
- 44.1kHz

One of the main concerns for stereo wireless music applications is, the ability to keep sample rates for the CODECs at both ends of the wireless link in synchronisation. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by ±3%, in steps of $1/2^{17}$, or 7.6 ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

8.9.4 ADC Gain

The ADC contains two gain stages for each channel, an analogue and a digital gain stage.

The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarised in Table 8.8.

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Gain Selection Value	ADC Digital Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 8.8: ADC Digital Gain Rate Selection

The ADC analogue amplifier is a two stage amplifier. The first stage of the analogue amplifier is responsible for selecting the correct gain for either microphone input or line input and therefore has two gain settings, one for the microphone and one for the line input, see Section 8.9.24 and Section 8.9.25 for details on the microphone and line inputs respectively. In simple terms the first stage amplifier has a selectable 20dB gain stage for the microphone and this creates the dual programmable gain required for the microphone or the line input. The equivalent block diagram for the two stage is shown in Figure 8.23.

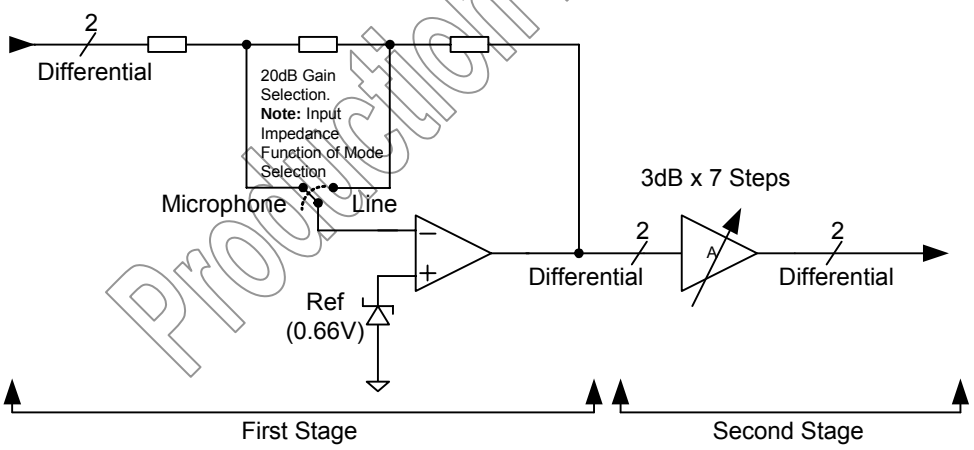

Figure 8.23: First Stage of ADC Analogue Amplifier Block Diagram

The second stage of the analogue amplifier shown in Figure 8.23 has a programmable gain with seven individual 3dB steps. In simple terms, by combining the 20dB gain selection of the microphone input with the seven individual 3dB gain steps, the overall range of the analogue amplifier is approximately -4dB to 40dB. The overall gain control of the ADC is controlled by the a VM function and this setting is a combined function of the digital and analogue amplifier settings, so that the fullscale range of the input to the ADC is kept to approximately 400mV rms

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8.9.5 DAC

The DAC consists of two second order Sigma Delta converters allowing two separate channels that are identical in functionality as shown in Figure 8.22.

8.9.6 DAC Sample Rate Selection and Warping

Each DAC supports the following samples rates:

- 48kHz
- 44.1kHz
- 32kHz
- 24kHz
- 22.050kHz
- 16kHz
- 11.025kHz
- 8kHz

Like the ADC, one of the main concerns for the DAC used in stereo wireless music applications is, the ability to keep sample rates for the CODECs at both ends of the wireless link in synchronisation. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The DAC warp function allows the sample rate to be changed by ±3%, in steps of $1/2^{17}$, or 7.6 ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

8.9.7 DAC Gain

The DAC contains two gain stages for each channel, a digital and an analogue gain stage.

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings summarised by Table 8.9.

Gain Selection Value	DAC Digital Gain Setting (dB)
0	0
1	3.5
2	6
3	9.5
4	12
5	15.5
6	18
7	21.5
8	-24
9	-20.5
10	-18
11	-14.5
12	-12
13	-8.5
14	-6
15	-2.5

Table 8.9: DAC Digital Gain Rate Selection

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The DAC analogue amplifier unlike the ADC is a single stage amplifier with the same structure as the second stage of the ADC analogue amplifier as shown in Figure 8.23. The structure of the DAC analogue amplifier is similar to the second stage of the ADC analogue amplifier, consisting of programmable gain with seven individual 3dB steps.

The overall gain control of the DAC is controlled by the a VM function and this setting is a combined function of the digital and analogue amplifier settings, therefore for a 1V rms nominal digital output signal from the digital gain stage of the DAC, the following approximate output values of the analogue amplifier of the DAC can be expected:

Analogue Gain Index	Analogue Gain (dB)
7	0
6	-3
5	-6
4	-9
3	-12
2	-15
1	-18
0	-21

Table 8.10: DAC Analogue Gain Settings

8.9.8 Mono Operation

Mono operation is single channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is auxilliary mono channel that may be used in dual mono channel operation. See Section 8.9 for an important note on stereo and mono definitions.

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8.9.9 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore3-Multimedia has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore3-Multimedia offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore3-Multimedia allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore3-Multimedia can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore3-Multimedia is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

BlueCore3-Multimedia interfaces directly to PCM audio devices including the following:

- WM8731 Audio CODEC from Wolfson Micro
- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore3-Multimedia is also compatible with the Motorola SSI™ interface

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8.9.10 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore3-Multimedia generates PCM_CLK and PCM_SYNC.

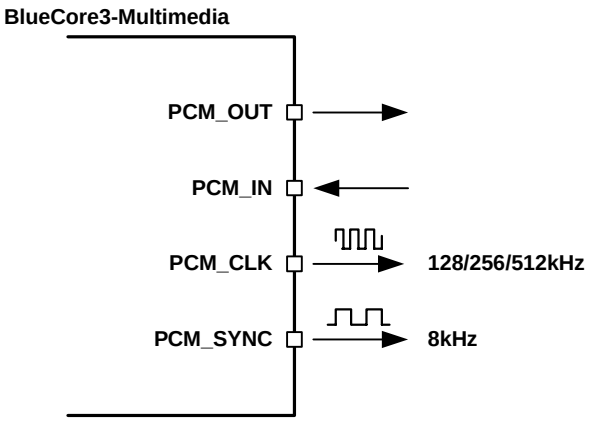

Figure 8.24: BlueCore3-Multimedia as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore3-Multimedia accepts PCM_CLK rates up to 2048kHz.

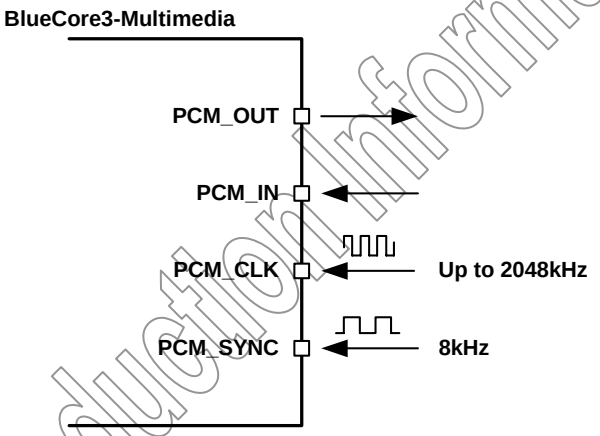

Figure 8.25: BlueCore3-Multimedia as PCM Interface Slave

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8.9.11 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore3-Multimedia is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore3-Multimedia is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

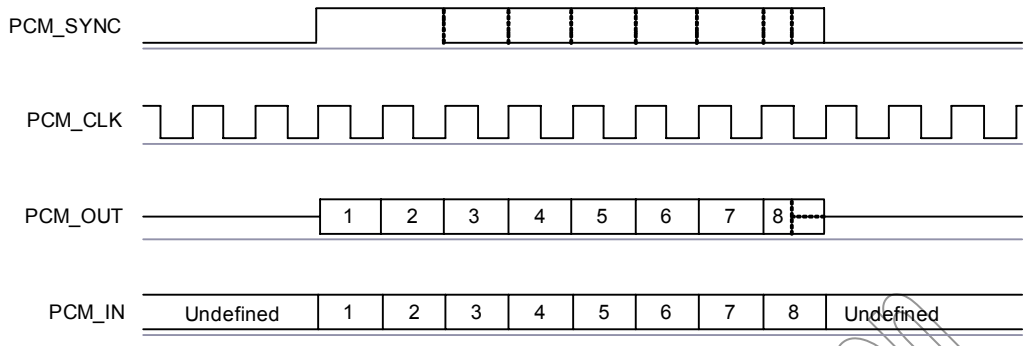

Figure 8.26: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore3-Multimedia samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.9.12 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

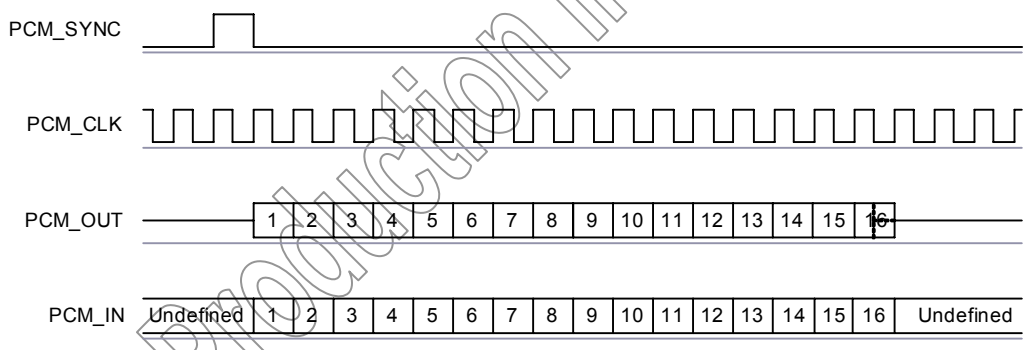

Figure 8.27: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore3-Multimedia samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

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8.9.13 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

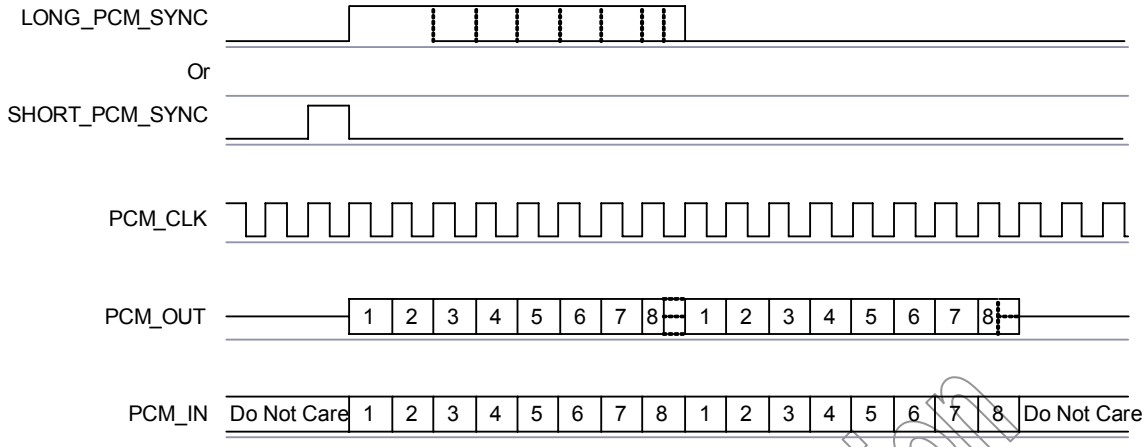

Figure 8.28: Multi Slot Operation with Two Slots and 8-bit Companded Samples

8.9.14 GCI Interface

BlueCore3-Multimedia is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

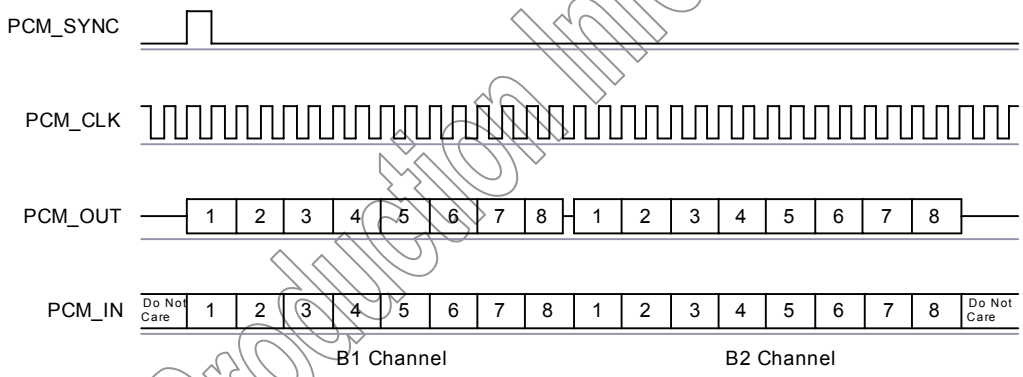

Figure 8.29: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore3-Multimedia in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

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8.9.15 Slots and Sample Formats

BlueCore3-Multimedia can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Duration's of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

BlueCore3-Multimedia supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

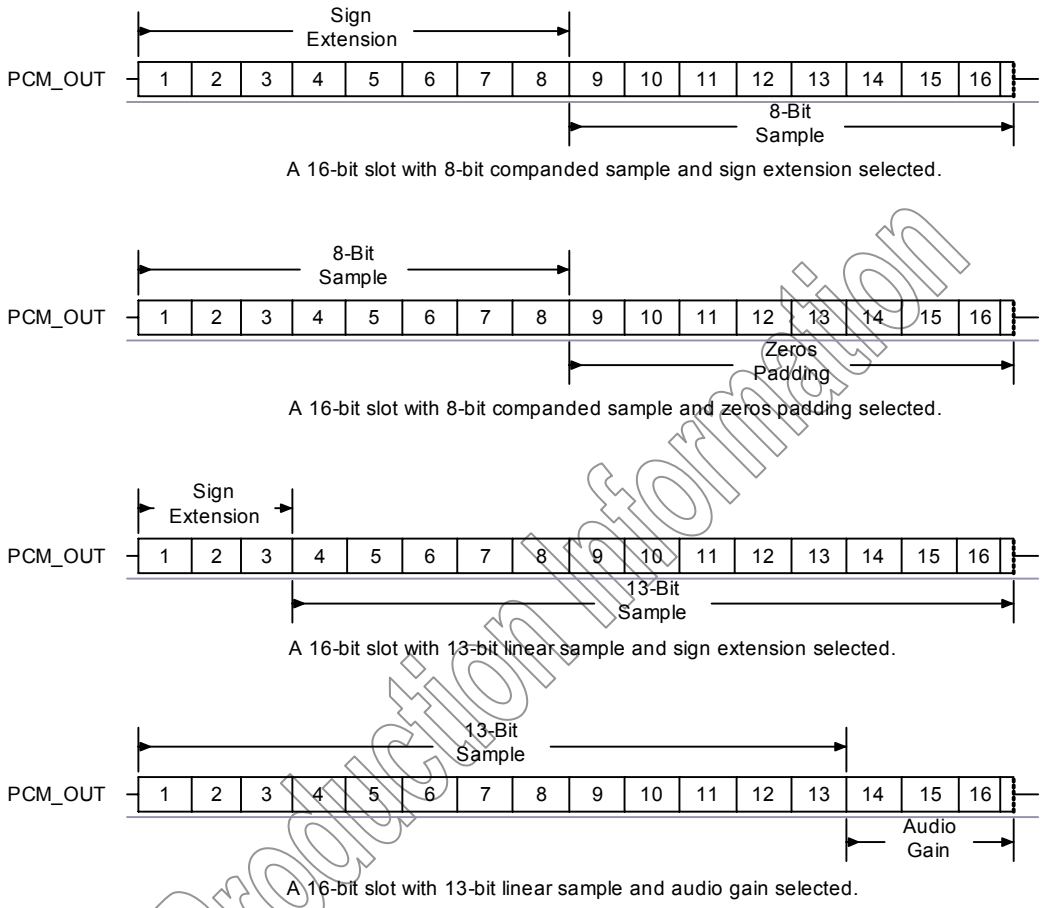

Figure 8.30: 16-Bit Slot Length and Sample Formats

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8.9.16 Additional Features

BlueCore3-Multimedia has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

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8.9.17 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable, see Table 8.13	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable, see Table 8.14 and Section 8.9.19	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh} (1)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (1)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 8.11: PCM Master Timing

Note:

(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

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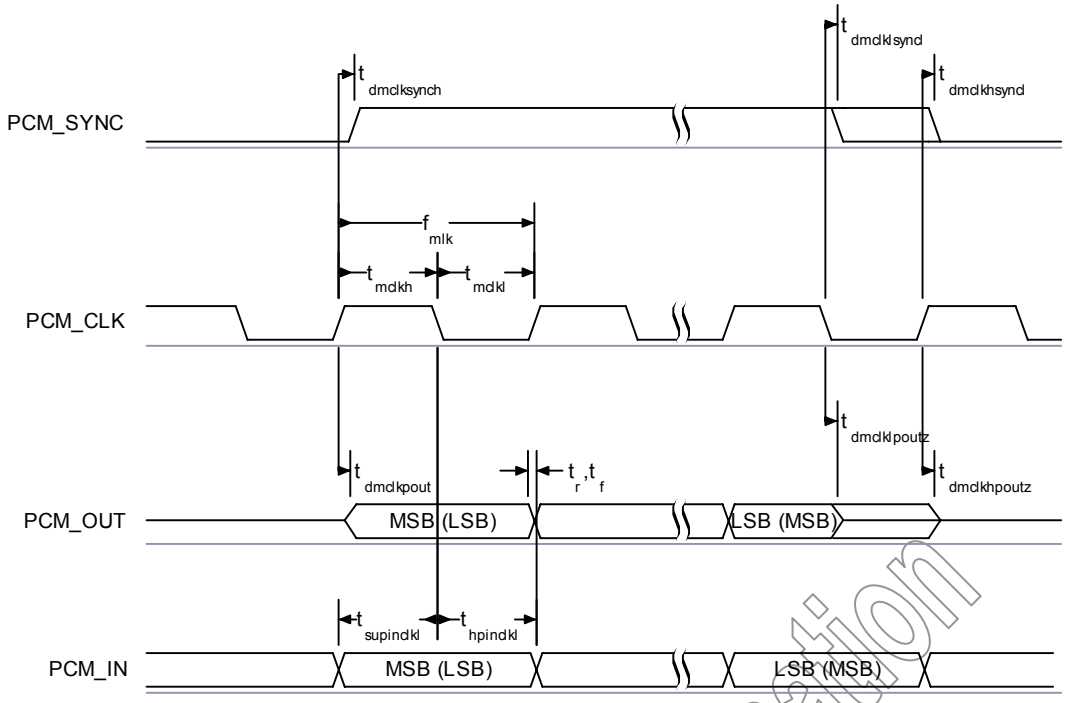

Figure 8.31: PCM Master Timing Long Frame Sync

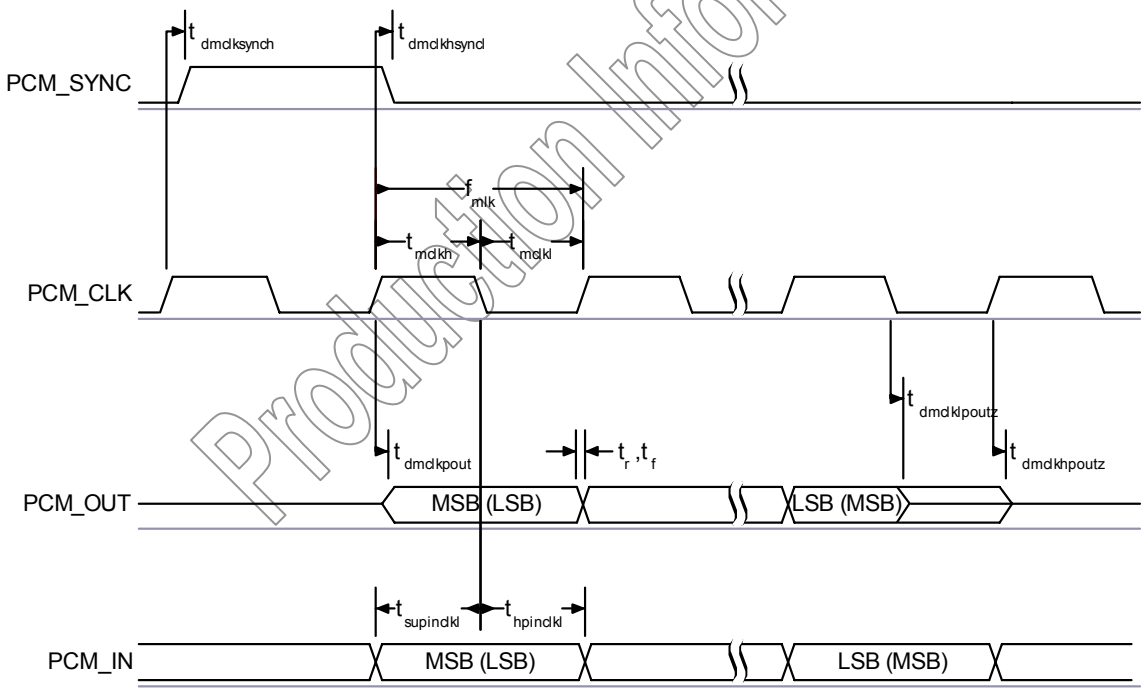

Figure 8.32: PCM Master Timing Short Frame Sync

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8.9.18 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns

Table 8.12: PCM Slave Timing

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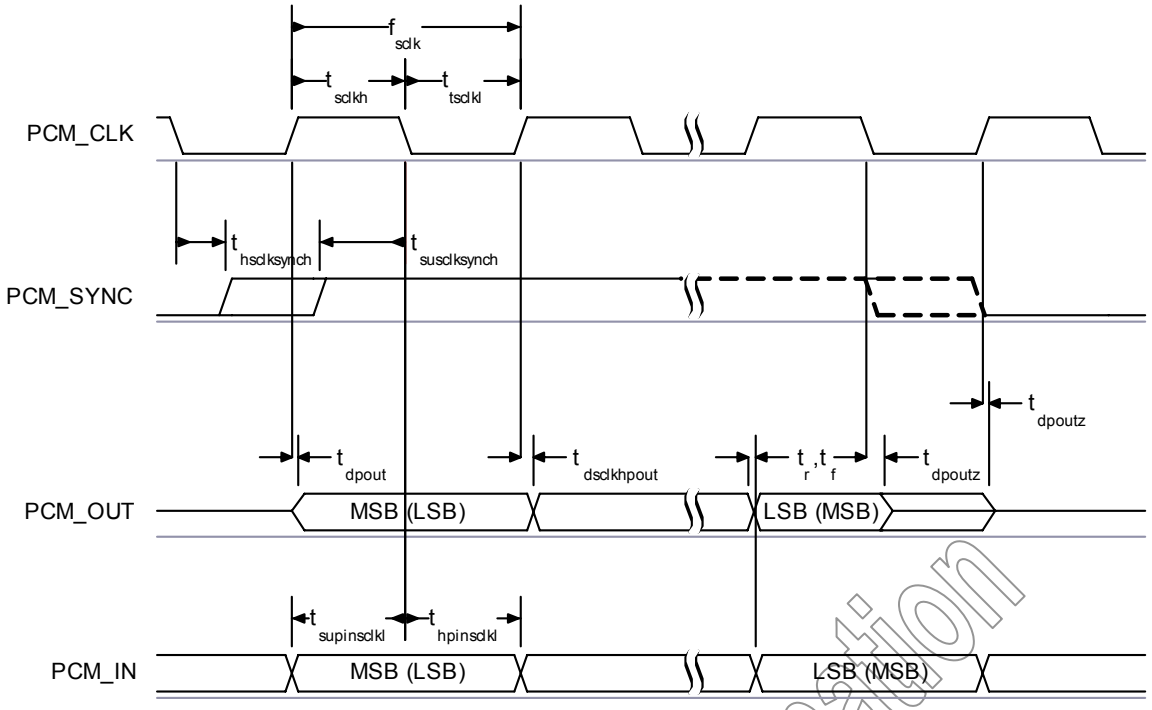

Figure 8.33: PCM Slave Timing Long Frame Sync

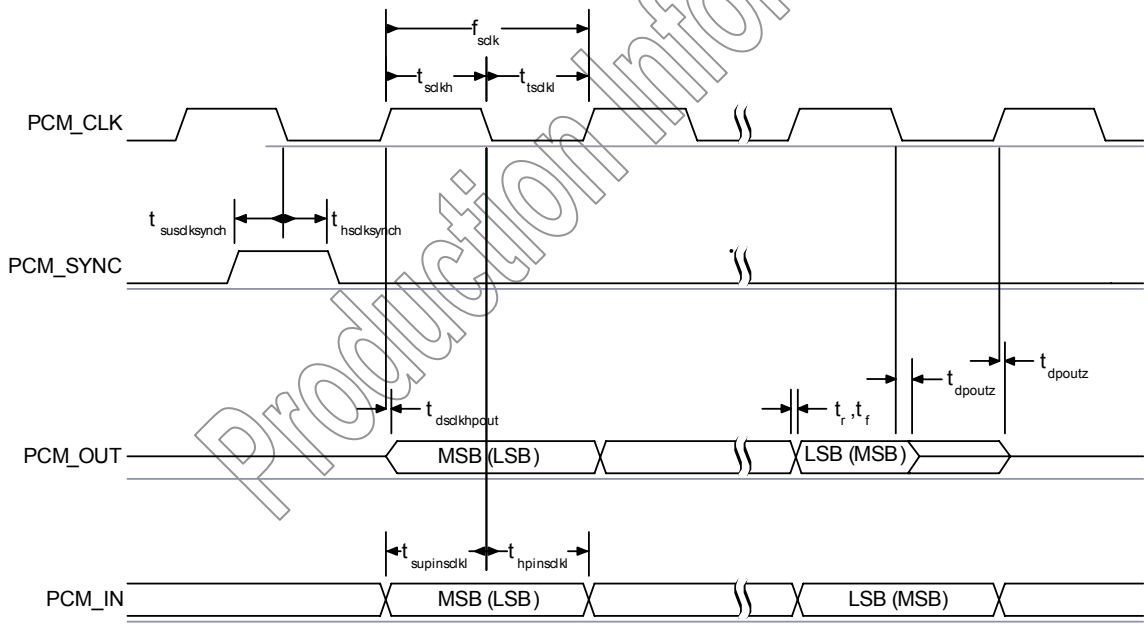

Figure 8.34: PCM Slave Timing Short Frame Sync

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8.9.19 PCM_CLK and PCM_SYNC Generation

BlueCore3-Multimedia has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore3-Multimedia internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit '48M_PCM_CLK_GEN_EN' in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by 'LONG_LENGTH_SYNC_EN' in PSKEY_PCM_CONFIG32.

The Equation 8.8 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT_RATE}{CNT_LIMIT} \times 24MHz$$

Equation 8.8: PCM_CLK Frequency When Being Generated Using the Internal 48MHz clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$f = \frac{PCM_CLK}{SYNC_LIMIT \times 8}$$

Equation 8.9: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

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8.9.20 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristating of PCM_OUT. PSKEY_PCM_LOW_JITTER_CONFIG is described in Table 8.14.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore2-External. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is '0001'. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 8.13: PSKEY_PCM_CONFIG32 Description

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Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 8.14: PSKEY_PCM_LOW_JITTER_CONFIG Description

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8.9.21 Digital Audio Bus

The digital audio interface supports the industry standard formats for I^{2}S, left-justified (LJ) or right-justified(RJ)[(1)]. The interface shares the same pins as the PCM interface as shown in Table 6.1 and the timing diagram is shown in Figure 8.35.

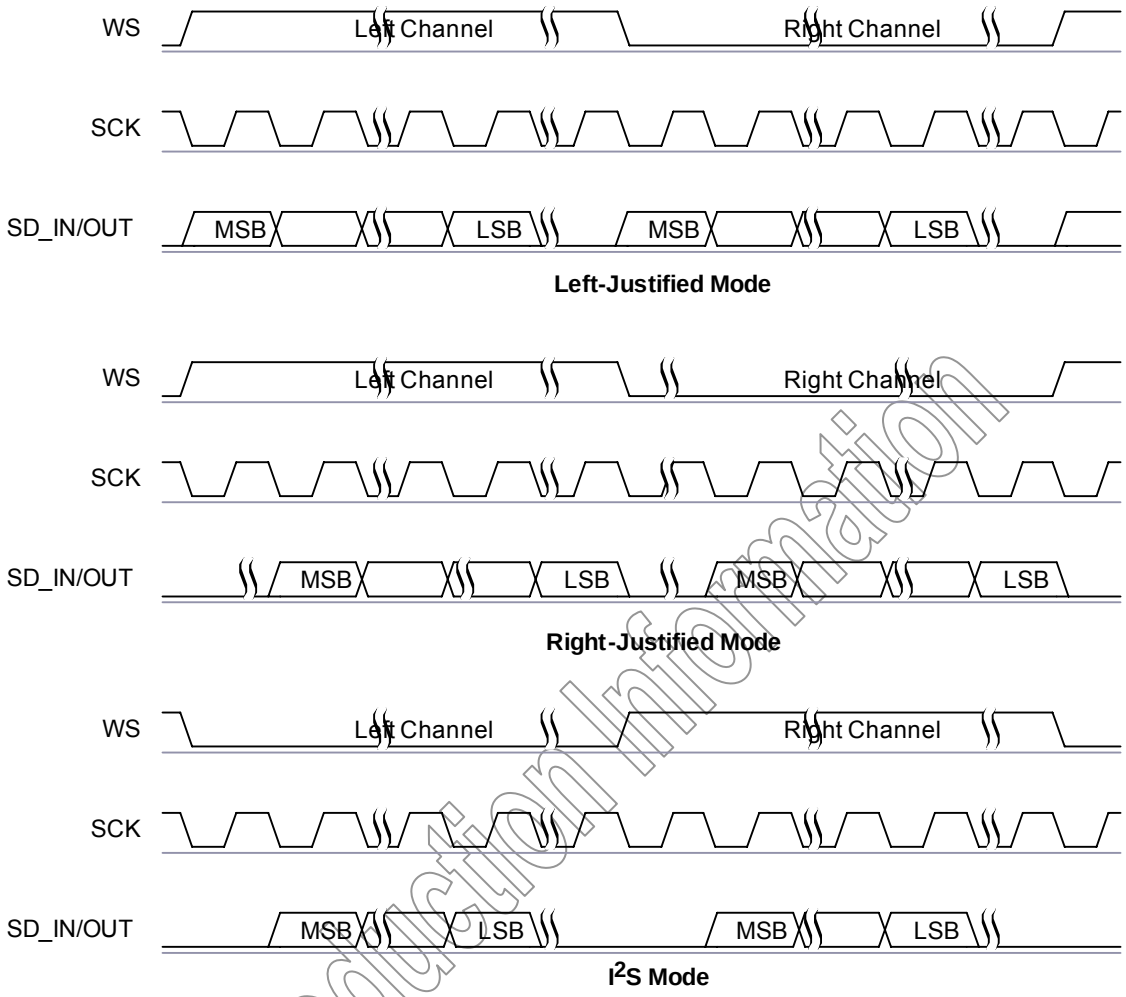

Figure 8.35: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore3-Multimedia is 16-bit and data on SD_OUT is limited to 16-bit per channel. On SD_IN, if more than 16-bit per channel is present will round considering the 17th bit.

SCK typically operates 64 x WS frequency and cannot be less than 36 x WS.

Note:

(1) Subject to firmware support, contact CSR for current status

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Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency			6.2	MHz
-	WS Frequency			96	kHz
t_{ch}	SCK high time				ns
t_{cl}	SCK low time				ns
t_{opd}	SCK to SD_OUT delay				ns
t_{ssu}	WS to SCK high set-up time				ns
t_{sh}	WS to SCK high hold time				ns
t_{isu}	SD_IN to SCK high set-up time				ns
t_{ih}	SD_IN to SCK high hold time				ns

Table 8.15: Digital Audio Interface Slave Timing

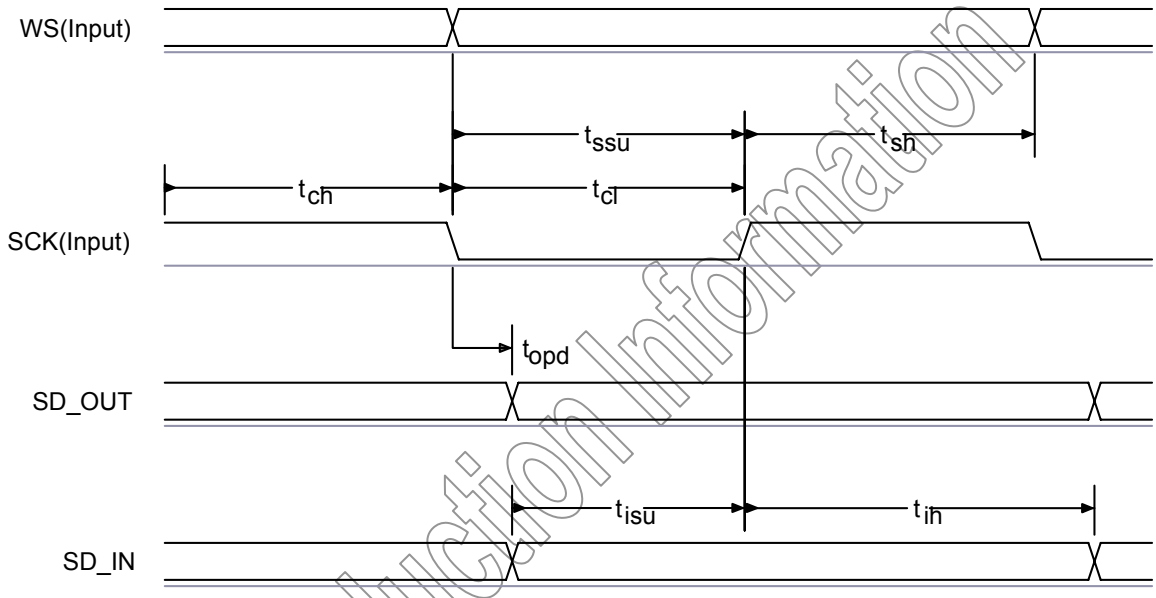

Figure 8.36: Digital Audio Interface Slave Timing

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Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency			6.2	MHz
-	WS Frequency			96	kHz
t_{opd}	SCK to SD_OUT delay				ns
t_{spd}	SCK to WS delay				ns
t_{isu}	SD_IN to SCK high set-up time				ns
t_{ih}	SD_IN to SCK high hold time				ns

Table 8.16: Digital Audio Interface Master Timing

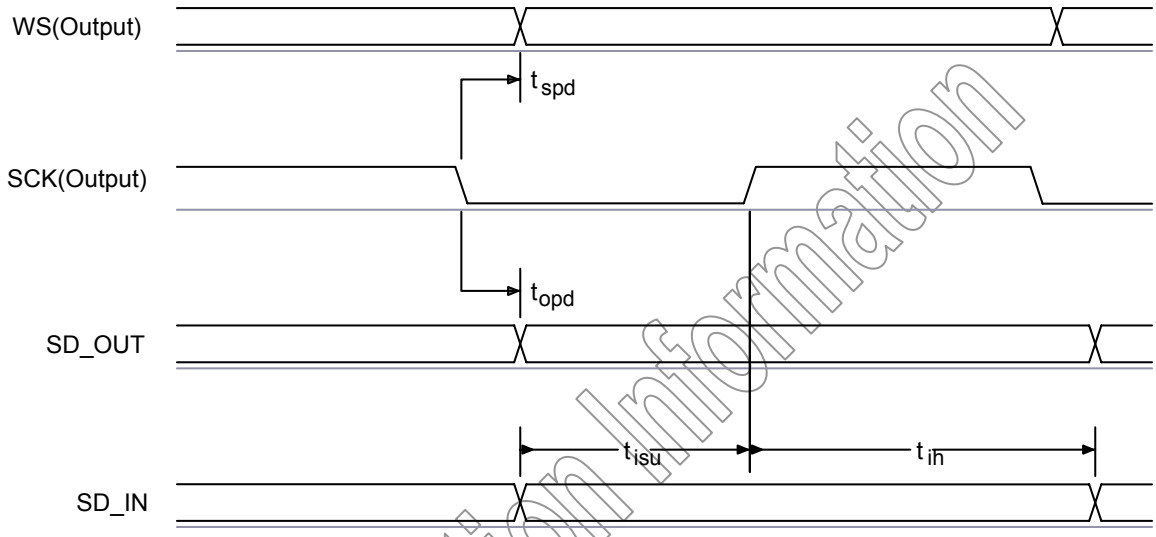

Figure 8.37: Digital Audio Interface Master Timing

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8.9.22 IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and allows the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the two industry standards AES/EBU and the Sony and Philips interface specification SPDIF. The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4. [(1)].

Note:

[(1)] Subject to firmware support, contact CSR for current status

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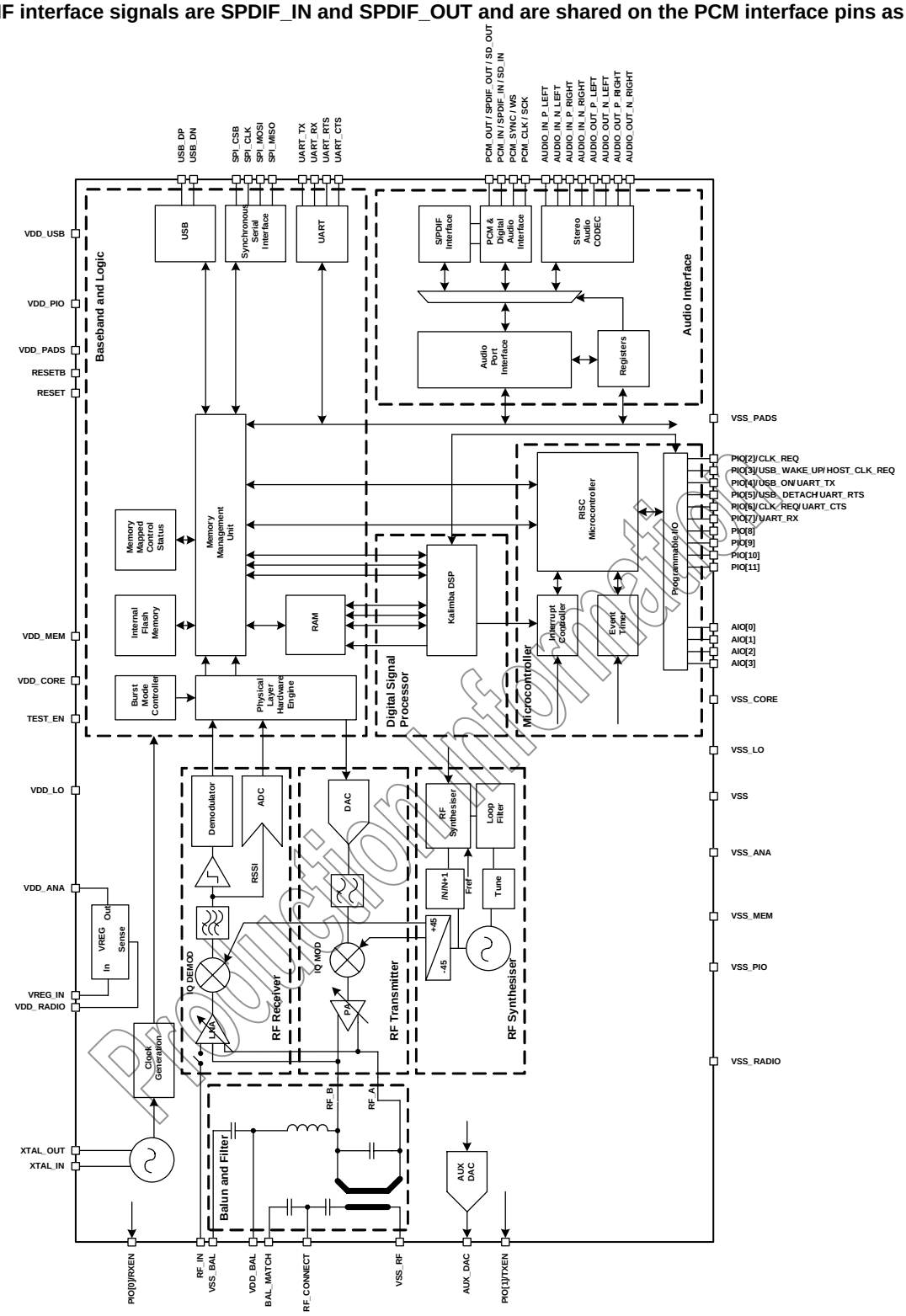
The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins as



shown in

Figure 5.1. The input and output stages of the SPDIF pins can interface either 75Ω coaxial cable with an RCA connector or there is an option to use an optical link that uses Toslink optical components. Typical output and input stage interfaces for the coaxial solution interface is shown in Figure 8.38 and Figure 8.39 and the equivalent optical solution is shown in Figure 8.40 and Figure 8.41.

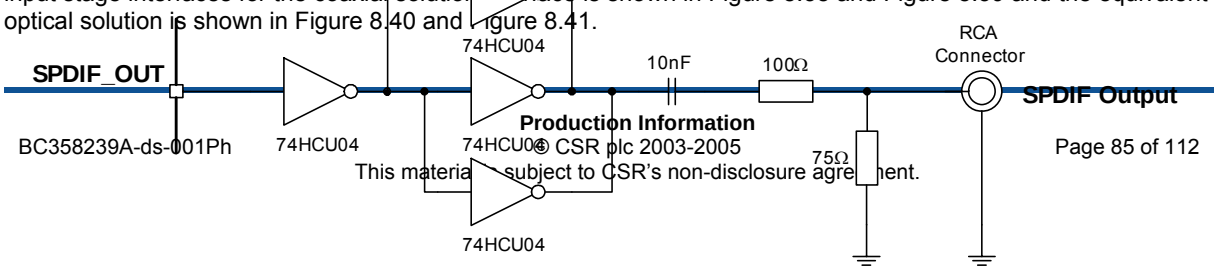


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Figure 8.38: Example Circuit for SPDIF Interface with Coaxial Output

Note:

The 100Ω and 75Ω resistors are dependent on the supply voltage and therefore subject to change

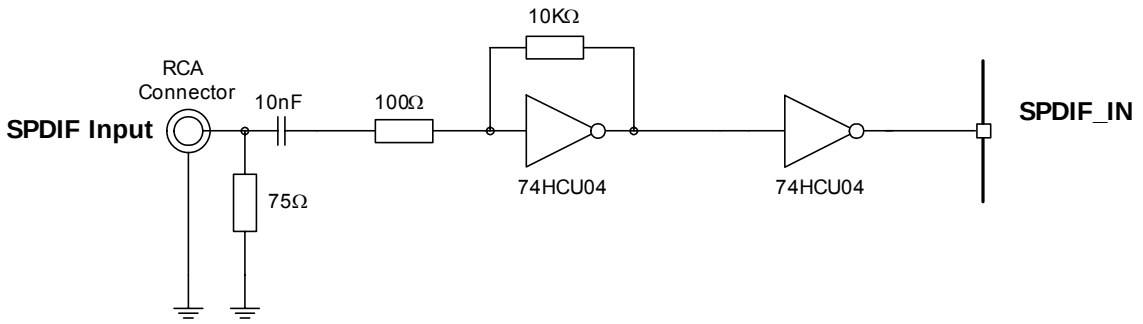

Figure 8.39: Example Circuit for SPDIF Interface with Coaxial Input

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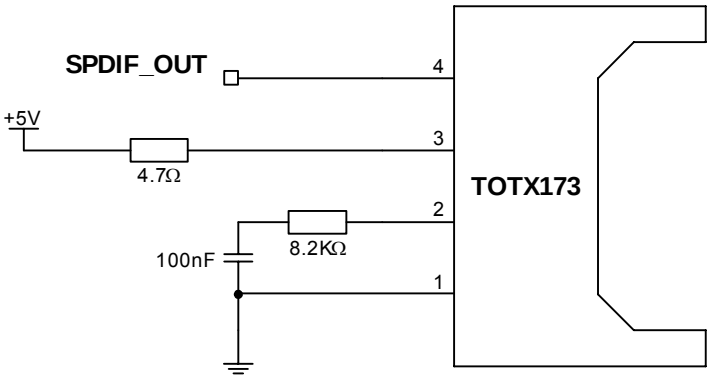

Figure 8.40: Example Circuit for SPDIF Interface with Optical Output

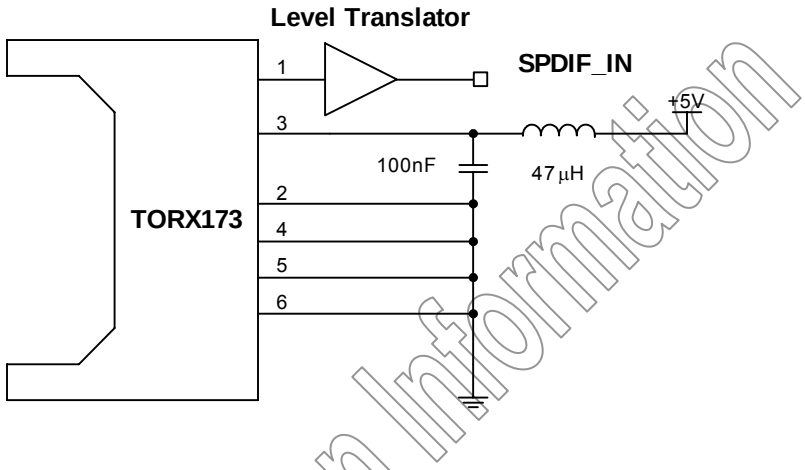

Figure 8.41: Example Circuit for SPDIF Interface with Optical Input

8.9.23 Audio Input Stage

The input stage of BlueCore3-Multimedia consists of a low noise input amplifier, which receives its analogue input signal from pins AUDIO_IN_P_LEFT and AUDIO_IN_N_LEFT to a second-order Σ-Δ ADC that outputs a 4MBit/sec single-bit stream into the digital circuitry. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

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8.9.24 Microphone Input

The audio-input is intended for use from 1μV@94dB SPL to about 10μV@94dB SPL. With biasing-resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40Dbv/Pa and –60dBV/Pa. The microphone for each channel should be biased as shown in Figure 8.42.

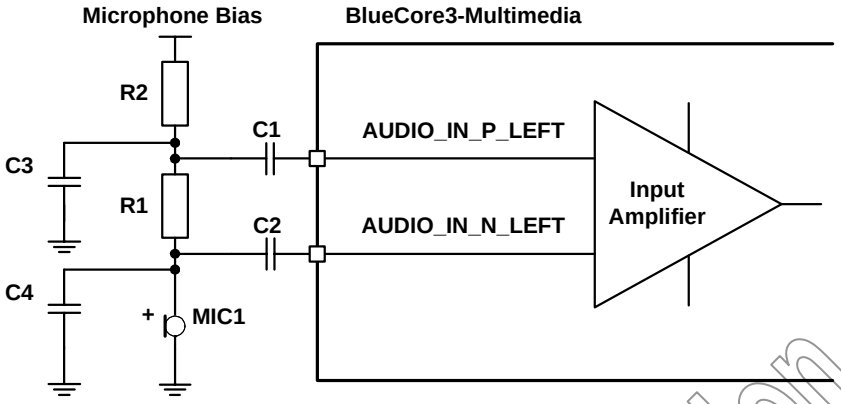

Figure 8.42: Microphone Biasing (Left Channel Shown)

The input impedance at AUDIO_IN_N_LEFT, AUDIO_IN_P_LEFT, AUDIO_IN_N_RIGHT and AUDIO_IN_P_RIGHT is typically 20kΩ. C1 and C2 should be 47nF. R1 sets the microphone load impedance and is normally in a range of 1 to 2 kΩ. R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required in the specification. R2 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the AUX_DAC output (which is ground referenced and so provides good rejection of the supply), which maybe configured to provide bias only when the microphone is required.

8.9.25 Line Input

If the input gain is set to less than 21dB BlueCore3-Multimedia automatically selects line input mode. In this mode the input impedance at AUDIO_IN_N_LEFT, AUDIO_IN_P_LEFT, AUDIO_IN_N_RIGHT and AUDIO_IN_P_RIGHT are increased to 130kΩ typically. In line-input mode, the full-scale input signal is about 400mV rms. Figure 8.43 and Figure 8.44 show two circuits for line input operation and show connections for either differential or single ended inputs.

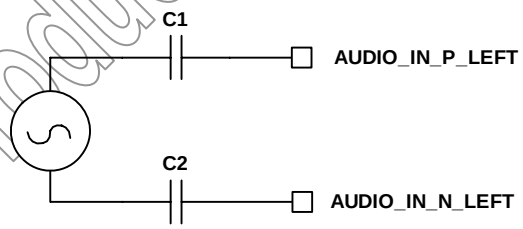

Figure 8.43: Differential Input (Left Channel Shown)

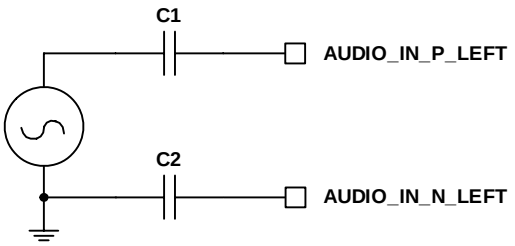

Figure 8.44: Single Ended Input (Left Channel Shown)

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8.9.26 Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to an 8 MBits/sec bit stream, which is fed into the analogue output circuitry.

The output circuit comprises a digital to analogue converter with gain setting and output amplifier. Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk- differential into a load of 32Ω and 500pF with a typical THD+N of -74dBc. The output is available as a differential signal between AUDIO_OUT_N_LEFT and AUDIO_OUT_P_LEFT for the left channel as shown in Figure 8.45; and between AUDIO_OUT_N_RIGHT and AUDIO_OUT_P_RIGHT for the right channel. The output is capable of driving a speaker directly if its impedance is at least 16Ω if only one channel is connected or an external regulator is used.

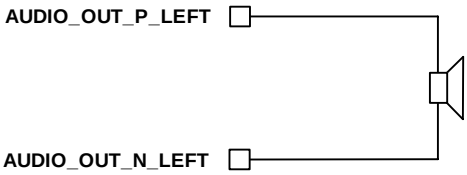

Figure 8.45: Speaker Output (Left Channel Shown)

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The single bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz. It uses its high open loop gain in the closed loop application circuit to achieve low distortion while operating with low standing current.

8.10 I/O Parallel Ports

Sixteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [3:0] are powered from VDD_MEM.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore3-Multimedia is provided from a system application specific integrated circuit (ASIC). Using PSKEY_CLOCK_REQUEST_ENABLE, (0x246) this terminal can be configured to be low when BlueCore3-Multimedia is in deep sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] or PIO[2] to avoid losing timing accuracy in certain Bluetooth operating modes.

BlueCore3-Multimedia has four general purpose analogue interface pins, AIO[0], AIO[1], AIO[2] and AIO[3], also known as the extended PIO lines. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other three may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_MEM (1.8V).

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8.10.1 PIO Defaults for BlueCore3-Multimedia

CSR cannot guarantee that these terminal functions remain the same. Please refer to the software release note for the implementation of these PIO lines, as they are firmware build specific.

8.11 I²C Interface

PIO[8:6] can be used to form a Master I²C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Note:

PIO lines need to be pulled-up through 2.2kΩ resistors.

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMS for use with BlueCore. This provides information on the type of devices which are currently supported.

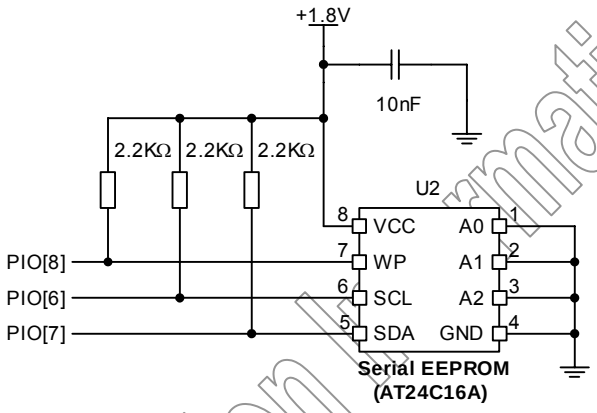

Figure 8.46: Example EEPROM Connection

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8.12 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore3-Multimedia where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore3-Multimedia.

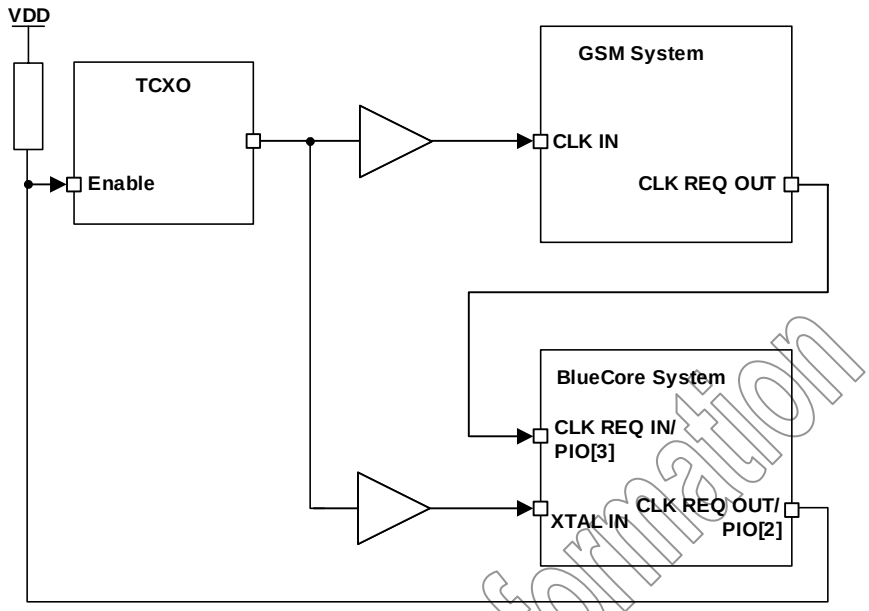

Figure 8.47: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

8.13 RESET and RESETB

BlueCore3-Multimedia may be reset from several sources: RESET or RESETB pins, power on reset, a UART break character or via a software configured watchdog timer.

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is 'ORed' on chip with the active high RESET with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tristated. The PIOs have weak pull-downs.

Following a reset, BlueCore3-Multimedia assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore-Multimedia is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore3-Multimedia free runs, again at a safe frequency.

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8.13.1 Pin States on Reset

Table 8.17 shows the pin states of BlueCore3-Multimedia on reset.

Pin name	State: BlueCore3-Multimedia
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[3:0]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
AUX_DAC	High impedance
RX_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 8.17: Pin States of BlueCore3-Multimedia on Reset

8.13.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset[(1)]: Baud rate and RAM data not available

Note:

(1) Cold Reset consititutes one of the following:

- Power cycle
- System reset (firmware fault code)
- Reset signal, see Section 8.13

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8.14 Power Supply

8.14.1 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a 2.2µF low ESR capacitor and 2.2Ω resistor[(1)] be placed on the output VDD_ANA adjacent to VREG_IN.

The regulator is switched into a low power mode when the device is sent into deep sleep mode. When the on chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

8.14.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA be powered at the same time. The order of powering supplies for VDD_CORE, VDD_PIO, VDD_PADS and VDD_USB is not important. However if VDD_CORE is not present, all inputs have a weak pull-down irrespective of the reset state.

8.14.3 Sensitivity to Disturbances

It is recommended that if you are supplying BlueCore3-Multimedia from an external voltage source that VDD_LO, VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided. A simple RC filter is recommended for VDD_CORE as this reduces transients put back onto the power supply rails.

The remaining supplies VDD_MEM, VDD_PIO, VDD_PADS and VDD_USB can be connected together with the VREG_IN to the 3.3V supply and simply decoupled as shown in Figure 10.1.

The transient response of the regulator is also important. At the start of a packet, power consumption will jump to high levels, see average current consumption section. The regulator should have a response time of 20µs or less, it is essential that the power rail recovers quickly.

Note:

(1) One of the VDD_CORE pins, L6 is internally connected by a 2.2Ω resistor to the output of the internal regulator, therefore the external 2.2Ω resistor may be removed. All VDD_CORE pins should be connected together externally but may not need to be connected to an external 1.8V supply. However, it may be the case that if the Kalimba DSP is very active and consuming significant power then the internally connected 2.2Ω resistor may cause a problem, in which case VDD_CORE should be connected to a 1.8V supply externally via an inductor to choke the noise and bypass the internal resistor connection by fitting this external 2.2Ω resistor in parallel with the inductor.

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9 Typical Audio CODEC Performance

9.1 Output

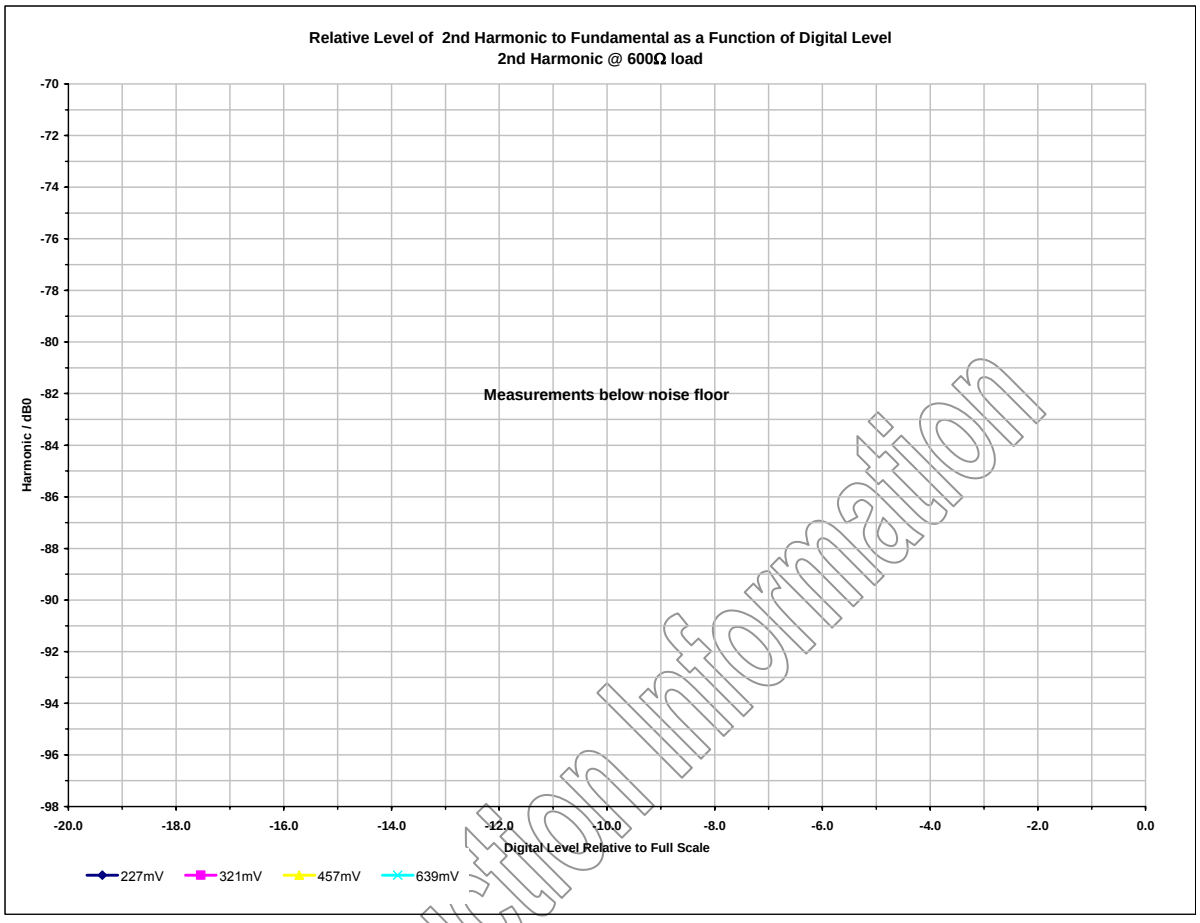

Figure 9.1: Relative Level of 2nd Harmonic to Fundamental, P_L = 600Ω

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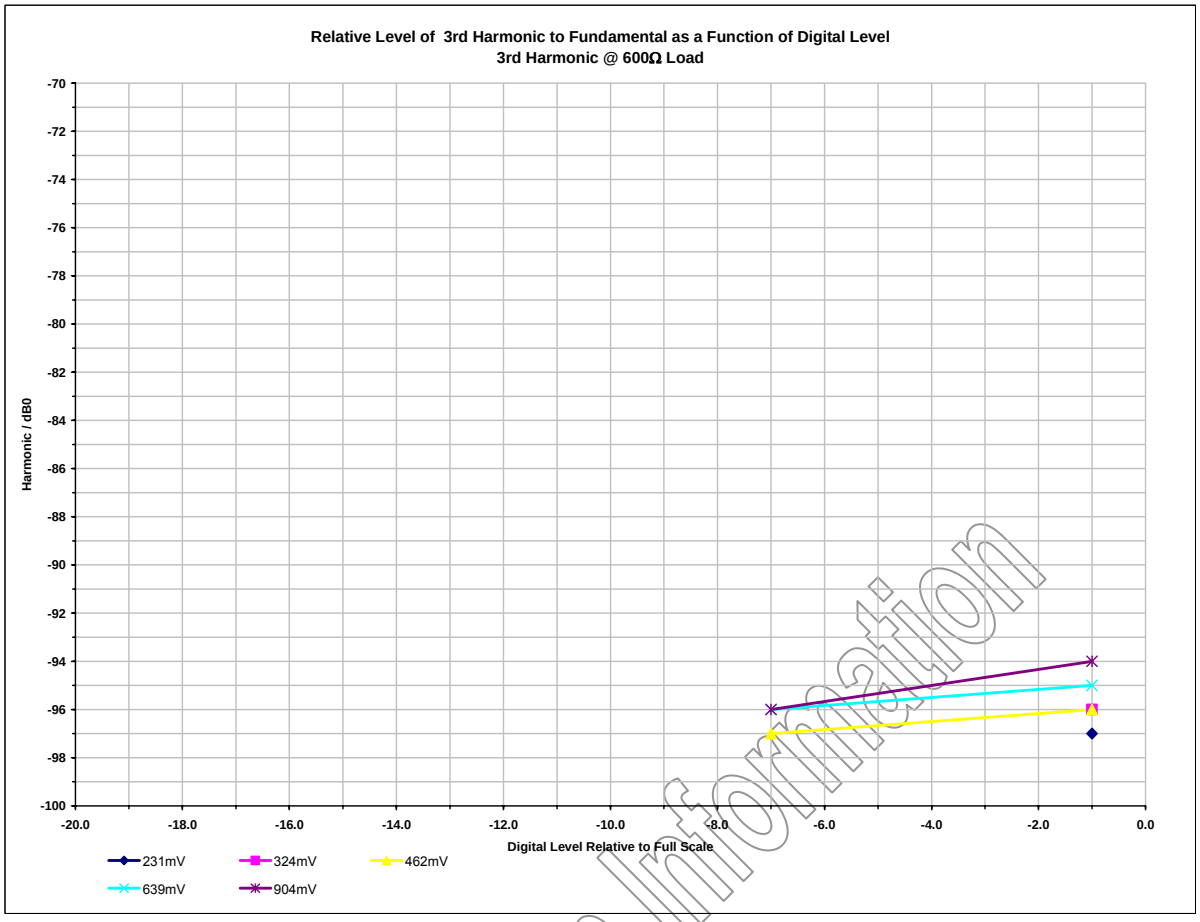

Figure 9.2: Relative Level of 3rd Harmonic to Fundamental, P_L = 600Ω

Note:

Signal below full scale – 7dB are below measurement system's noise floor

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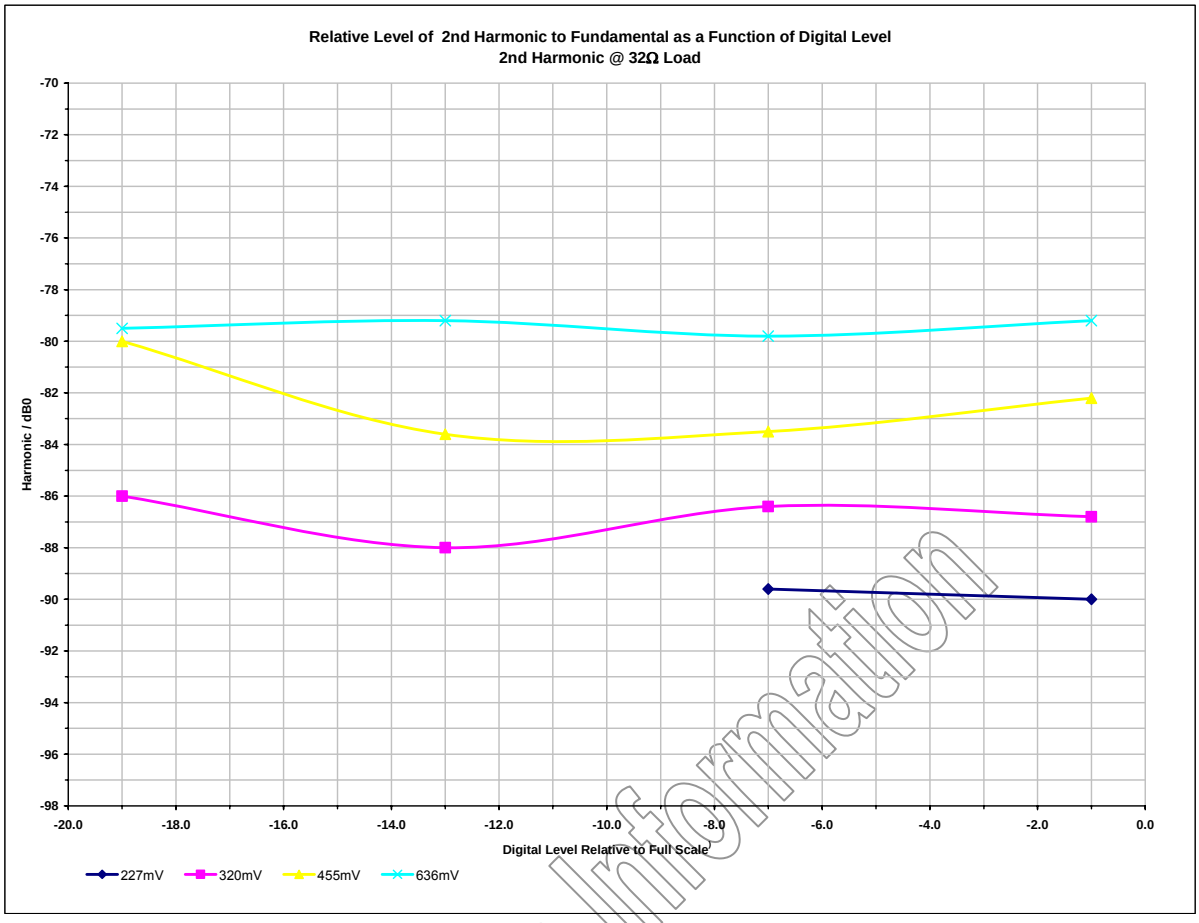

Figure 9.3: Relative Level of 2nd Harmonic to Fundamental, P_L = 32Ω

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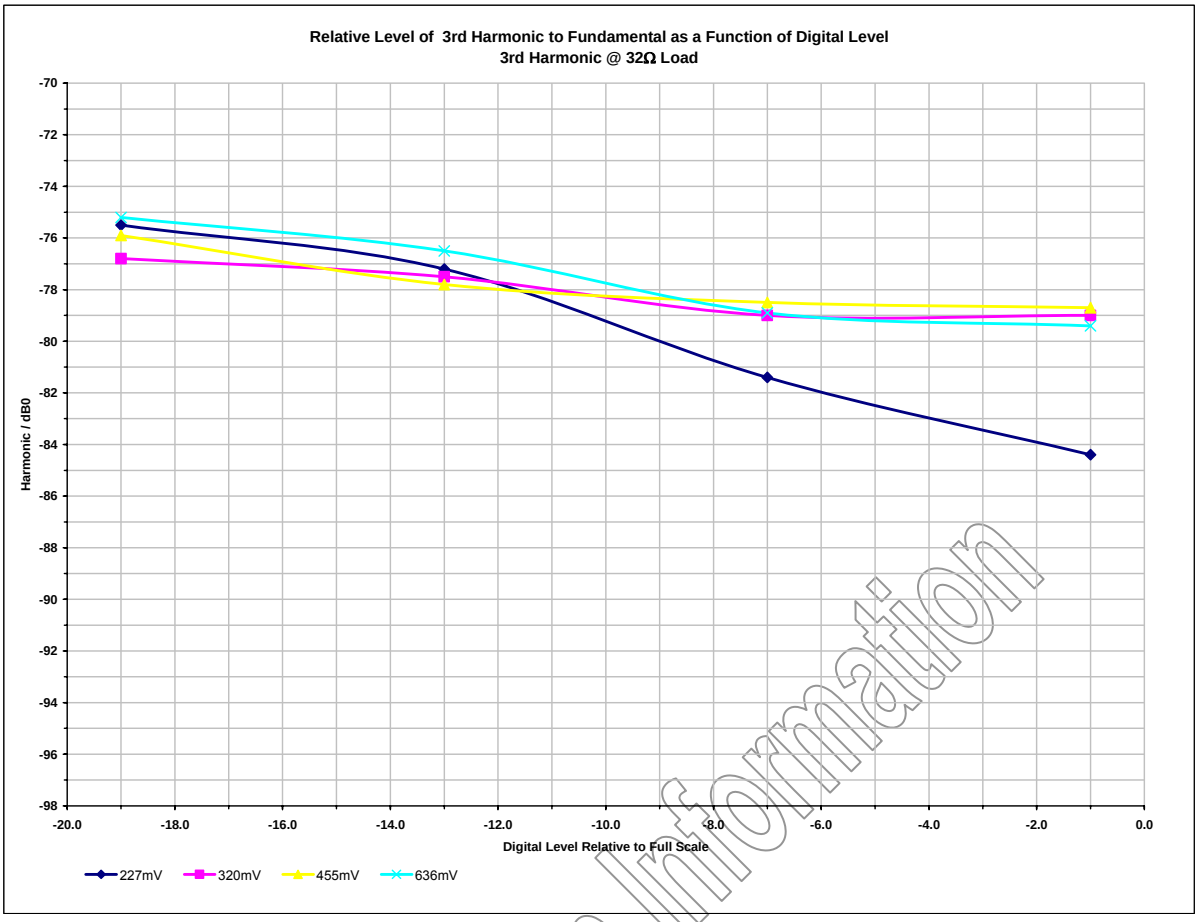

Figure 9.4: Relative Level of 3rd Harmonic to Fundamental, P_L = 32Ω

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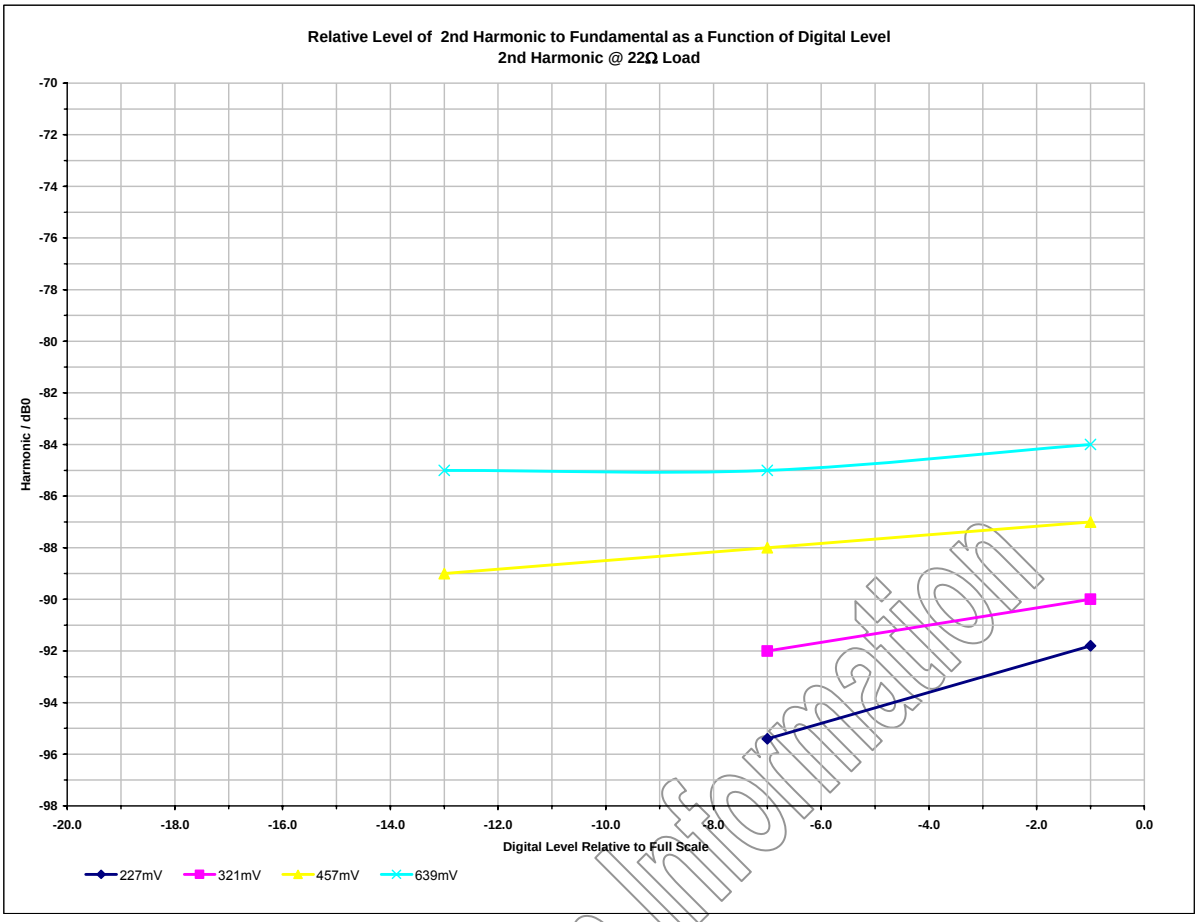

Figure 9.5: Relative Level of 2nd Harmonic to Fundamental, P_L = 22Ω

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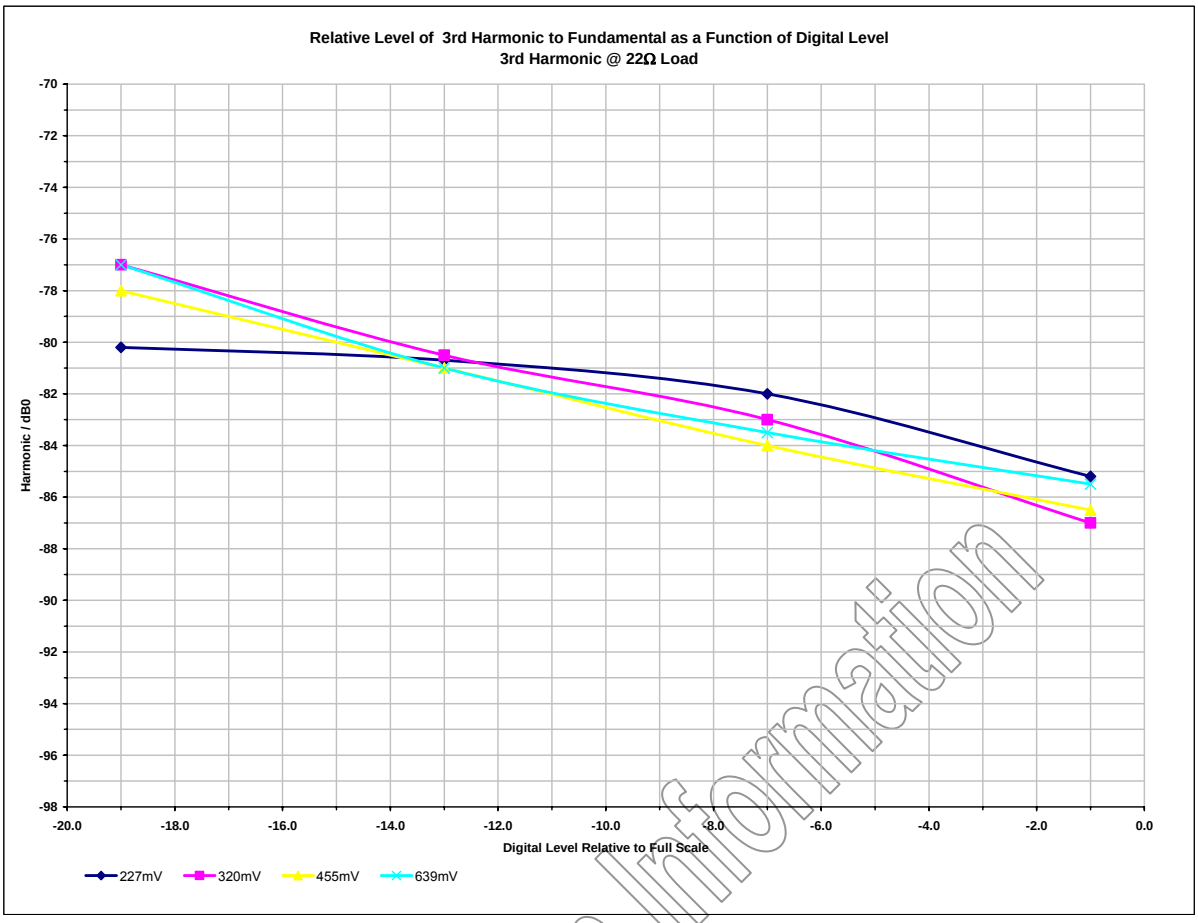

Figure 9.6: Relative Level of 3rd Harmonic to Fundamental, P_L = 22Ω

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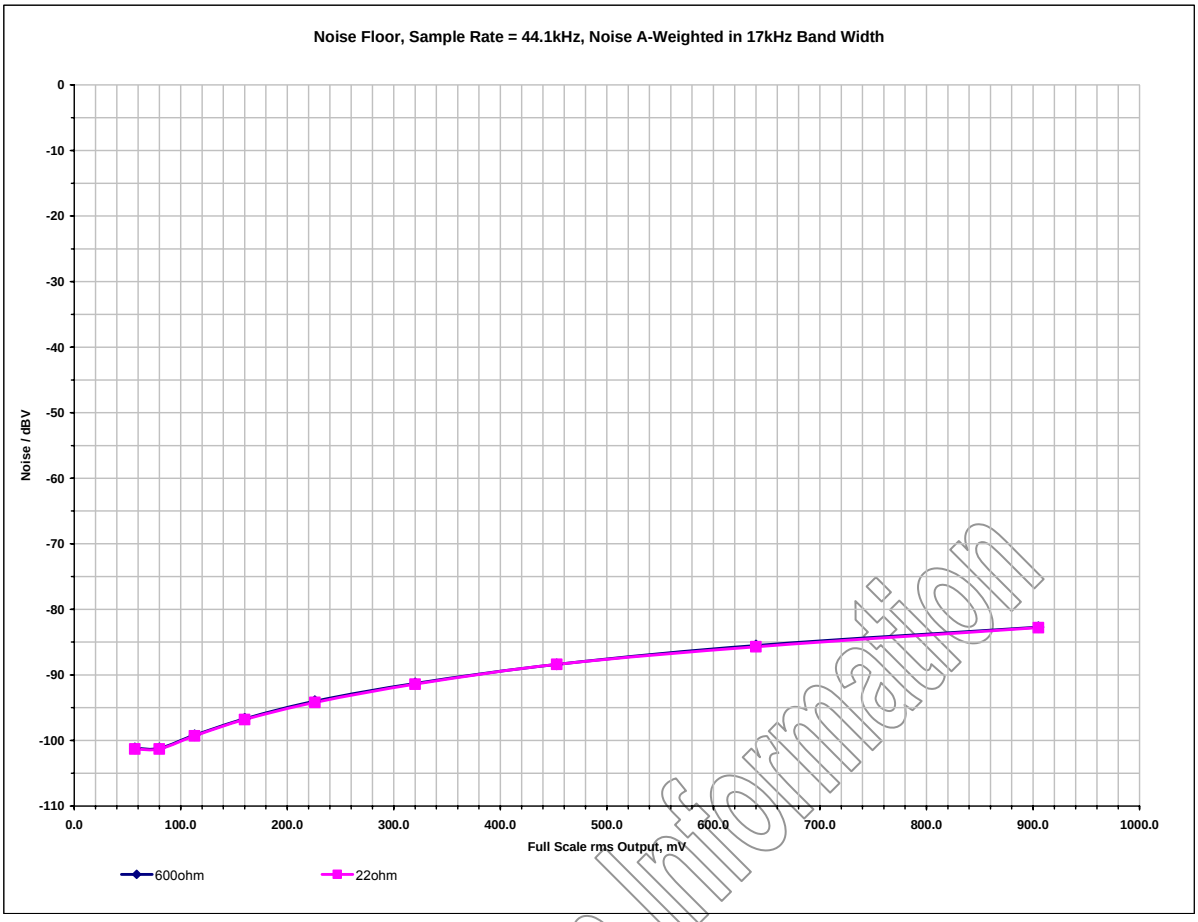

Figure 9.7: Noise Floor

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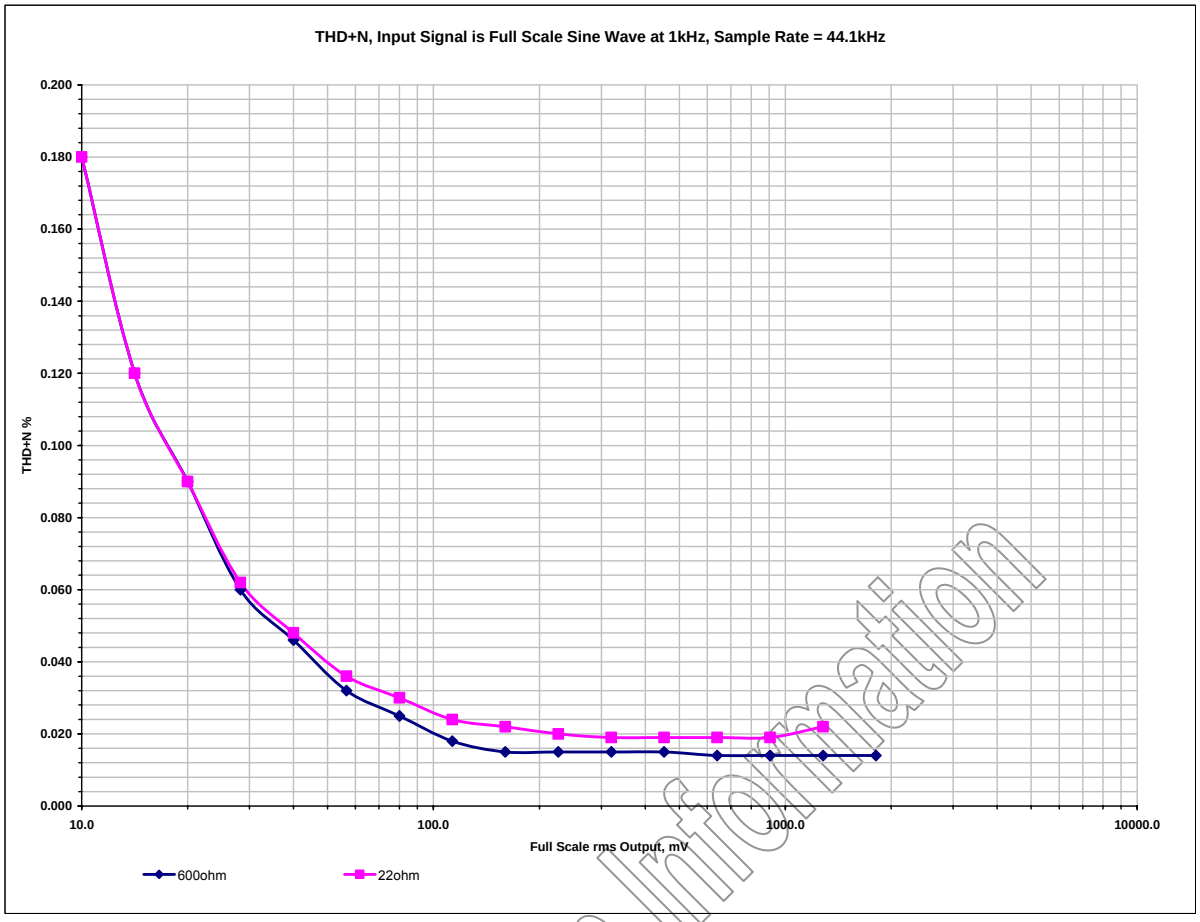

Figure 9.8: THD+N

Production Information

10 Application Schematic

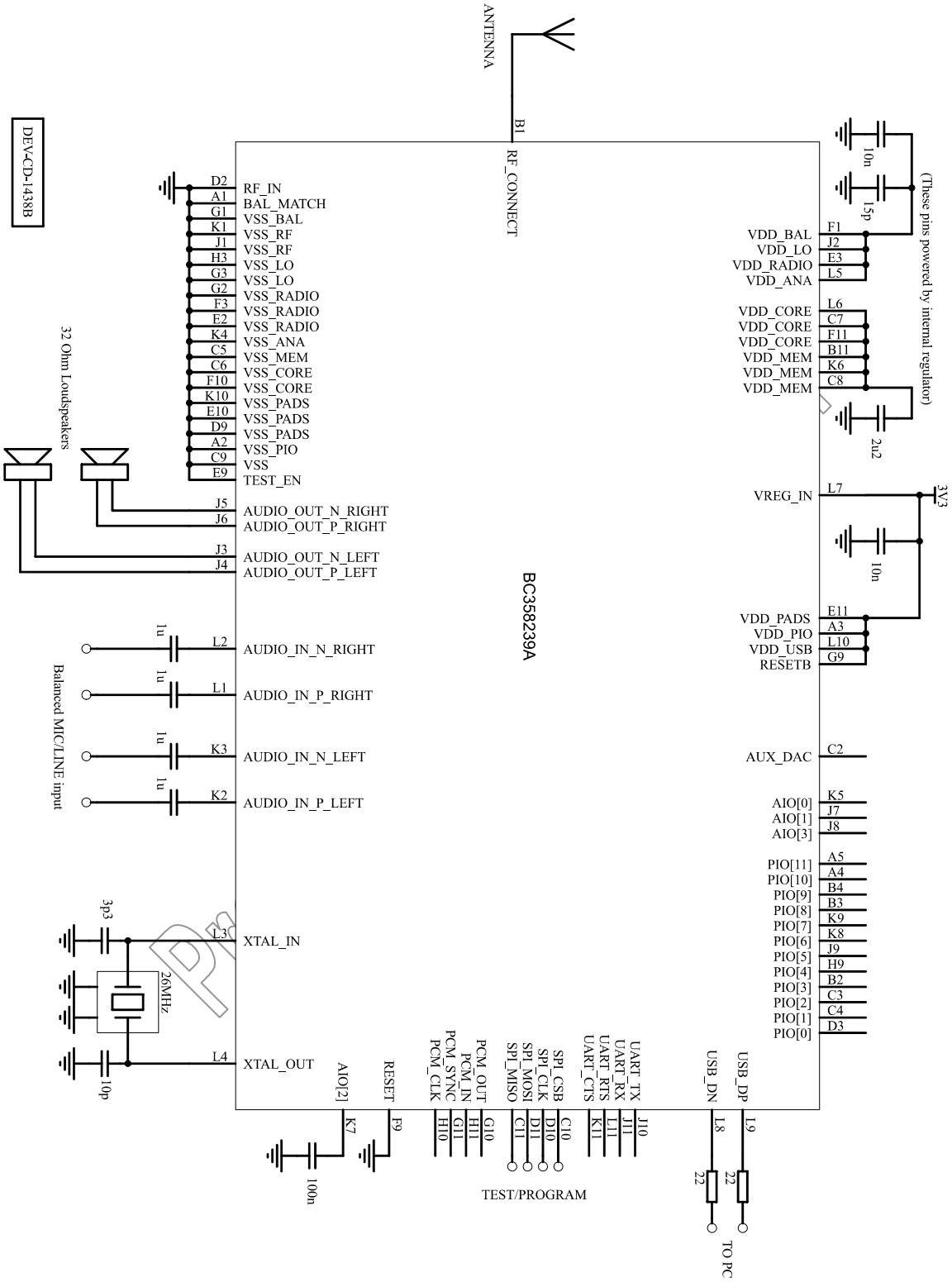

Figure 10.1: Application Circuit for Radio Characteristics Specification for 10 x 10 LFBGA Package

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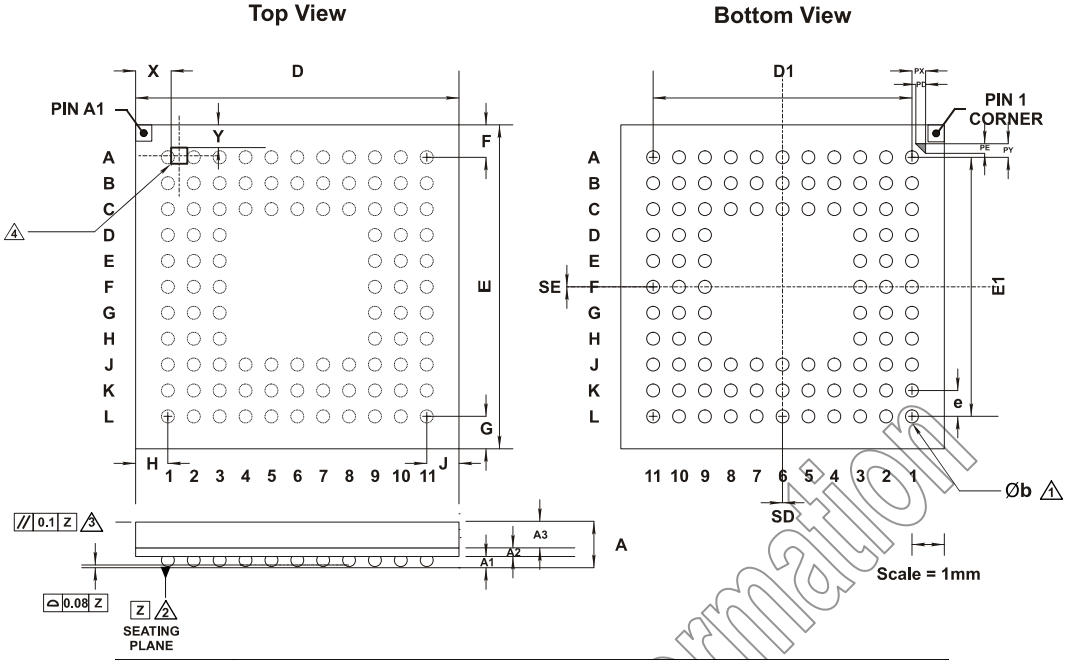
11 Package Dimensions

11.1 10 x 10mm LFBGA 96-Ball Package



Description	96-Ball Low-Profile Fine-Pitch Ball Grid Array (LFBGA)			
Size	10 x 10 x 1.4mm			
Pitch	0.8mm			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			1.4	1 Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.27	0.32	0.37	
A2		0.26		
A3		0.80		
B	0.35	0.40	0.45	2 Datum Z is defined by the spherical crowns of the solder balls
D	9.90	10.00	10.10	
E	9.90	10.00	10.10	
e		0.80		3 Parallelism measurement shall exclude any effect of mark on top surface of package
D1		8.00		
E1		8.00		
F	0.950	1.000	1.050	
G	0.950	1.000	1.050	4 Polarity Mark. The dimensions of the polarity mark are 0.5 x 0.5mm.
H	0.950	1.000	1.050	
J	0.950	1.000	1.050	
PD		-		
PX		-		
PE		-		
PY		-		
SD		0		
SE		0		
X		-		
Y		-		
JEDEC	MO-210			
Unit	mm			

Figure 11.1: BlueCore3-Multimedia 96-Ball LFBGA Package Dimensions

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12 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. See Table 12.1 for a description of the four zones.

Zone	Description
Preheat Zone	This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
Equilibrium Zone	This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
Reflow Zone	The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
Cooling Zone	The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

Table 12.1: Solder Profile Zones

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12.1 Solder Re-flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

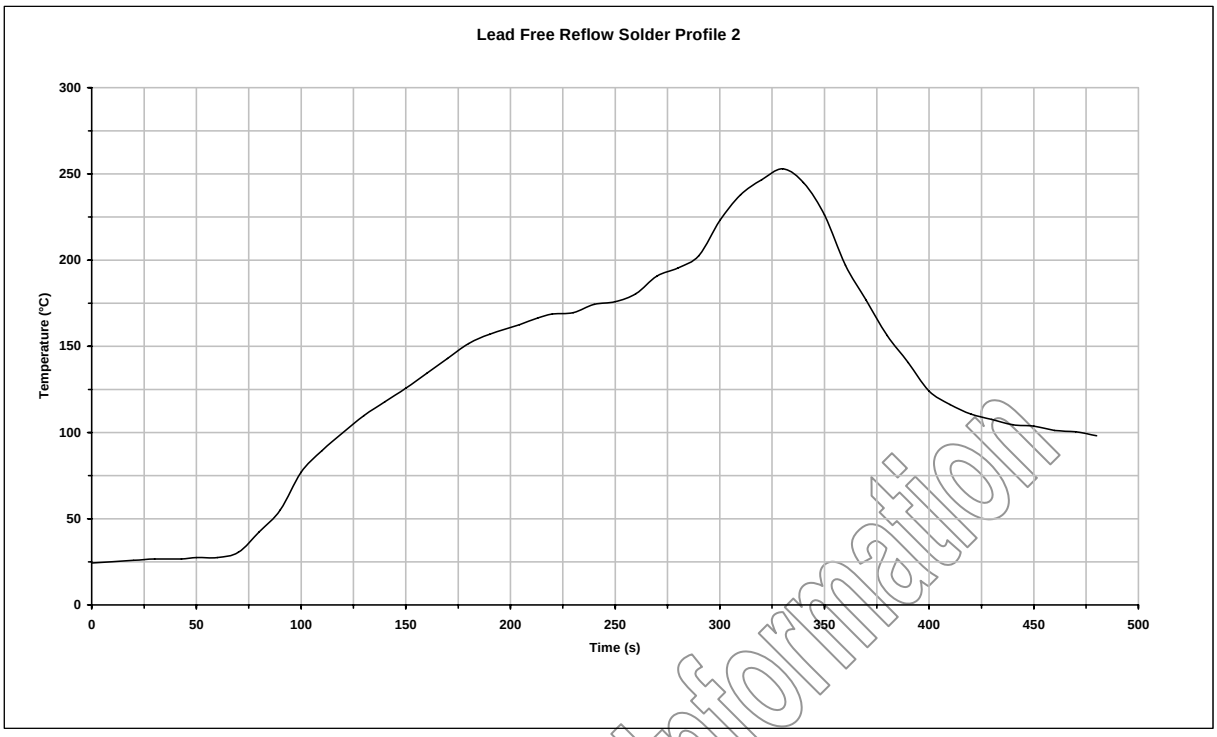

Figure 12.1: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to 3 reflows to a maximum temperature of 260°C.

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13 Ordering Information

13.1 BlueCore3-Multimedia

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	96-Ball LFBGA (Pb free)	10 x 10 x 1.4mm	Tape and reel	BC358239A-INN-E4

Minimum Order Quantity

2kpcs Taped and Reeled

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14 Contact Information

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15 Document References

Document:	Reference, Date:
Specification of the Bluetooth System	v1.2, 05 November 2003
Universal Serial Bus Specification	v2.0, 27 April 2000
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008Pb, 30 September 2003

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Terms and Definitions

BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BMC	Burst Mode Controller
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
DNL	Differential Linearity Error
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
FIR	Finite Impulse Response
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
IIR	Infinite Impulse Response
INL	Integral Linearity Error
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
Kalimba	DSP core for CSR's range of chips
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LFBGA	Low profile Fine Ball Grid Array
LNA	Low Noise Amplifier

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LPF	Low Pass Filter
LSB	Least-Significant Bit
MCU	MicroController Unit
μ-law	Audio Encoding Standard
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
MISO	Master In Serial Out
NOB	Number Of Bits
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SINAD	SIgnal to Noise ratio And Distortion
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)
www	world wide web

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Document History

Date:	Revision	Reason for Change:
FEB 03	a	Original publication of this document. (CSR reference: BC358239A-db-001Pa)
JUN 03	b	Pinout added and associated changes. Plus updates with respect to performance data of initial devices
FEB 04	c	Moved to Pre-Production Status Additional information to Device Terminal Description Section, Software Stacks, Solder Profile and Crystal Characteristics. Lead free only device. **Important Notice:** Major additions to CODEC including modifications to pinout
AUG 04	d	Update to power consumption table, to include 'Digital audio processing subsystem' figure. Datasheet still at Pre-Production status.
SEP 04	e	Moved to Production status and corresponding Databook published (CSR reference: BC358239A-db-001Pa) Package dimension drawing updated to new style Application Schematic added Stereo CODEC audio parameters added and appearance of tables modified
JUN 05	f	Tape and reel information added
AUG 05	g	Amendment to PIO[7], Device Terminal Functions, 10x10mm LFBGA Package Information; amendment to PIO[7], Device Diagram Updated bulleted list concerning supported and device-compatible CODECs, PCM CODEC Interface, Device Terminal Descriptions Updated note (5) concerning VREG_EN and VREG_IN, Linear Regulator table, Electrical Characteristics Updated note (3) concerning specified output voltage in the Auxilliary DAC table (Input/Output Terminal Characteristics), Electrical Characteristics Moved Power Consumption subsection from Radio Characteristics to Electrical Characteristics Changed title of Record of Changes to Document History; changed title of Acronyms and Abbreviations to Terms and Definitions Changed copyright information on Status Information page Updated Contact Information
DEC 05	h	Updated Table 8.10:DAC Analogue Gain Settings in Device Terminal Descriptions, Stereo Audio Interface; Corrected Microphone Input in Device Terminal Descriptions, Stereo Audio Interface; Updated copyright information

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BlueCore™3-Multimedia

Product Data Sheet

BC358239A-ds-001Ph

December 2005

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