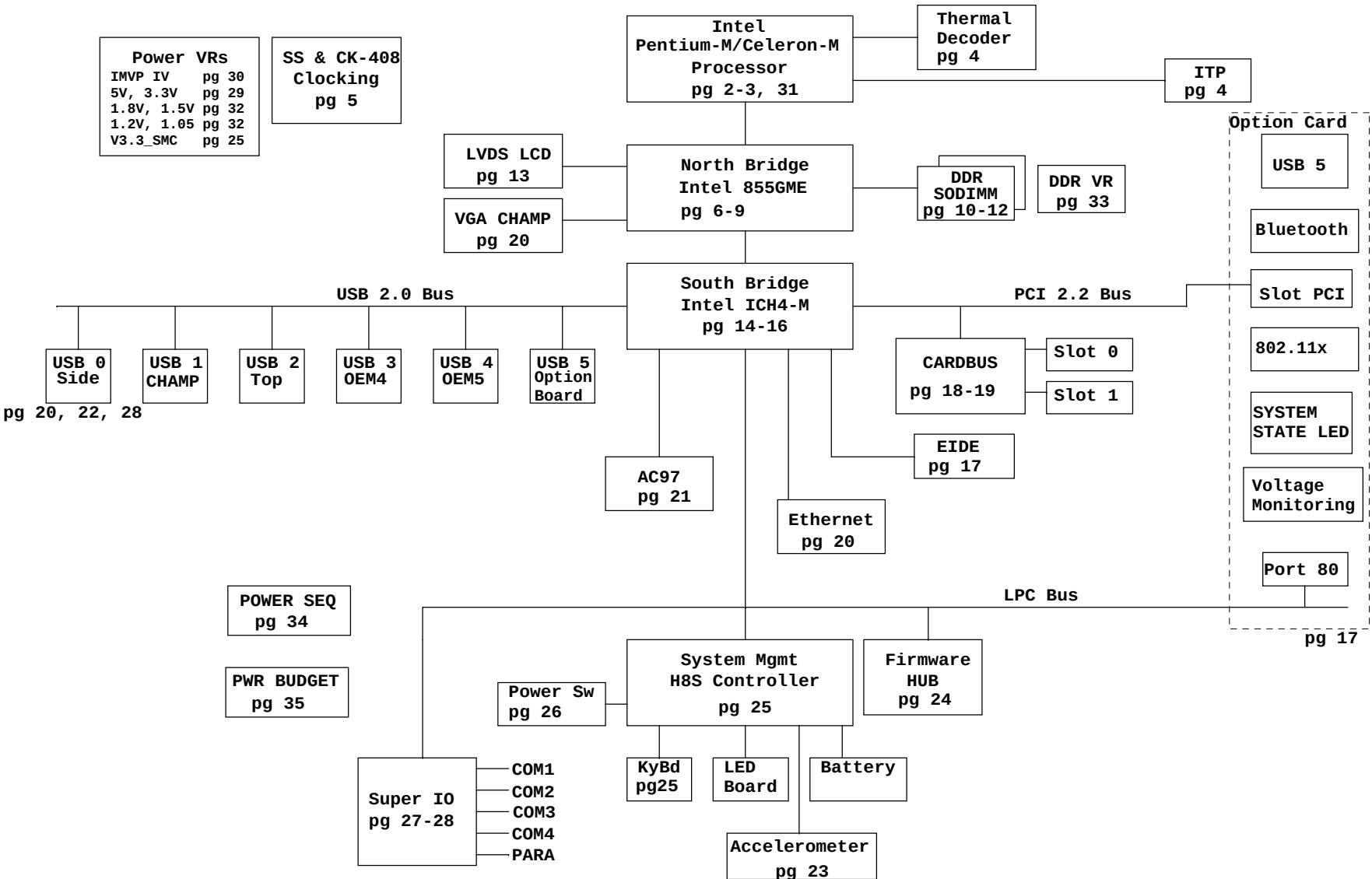


REVISIONS				BY
ECO#	REV	DESCRIPTION OF CHANGE		
18687	G	G1. SHEET 13 - CHANGED J5 FROM 3 PIN CONNECTOR TO 4 PIN		TET

Hammerhead XRT-Centrino Tablet



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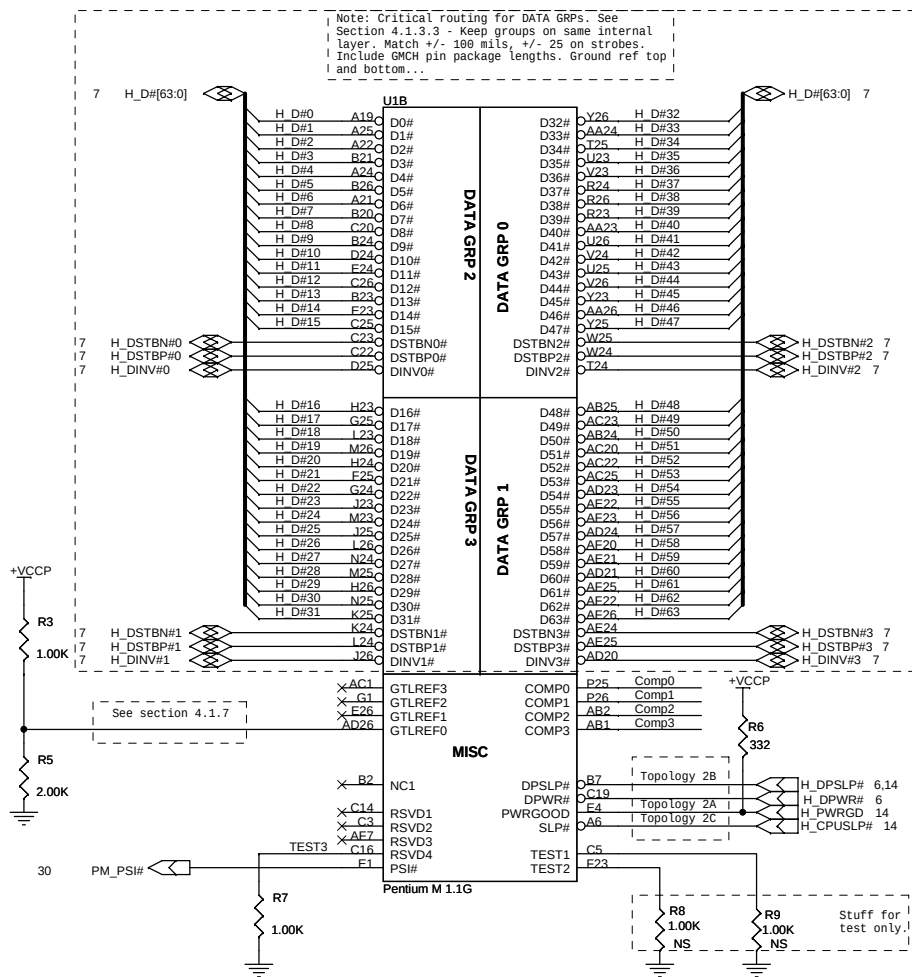
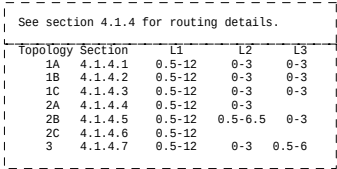
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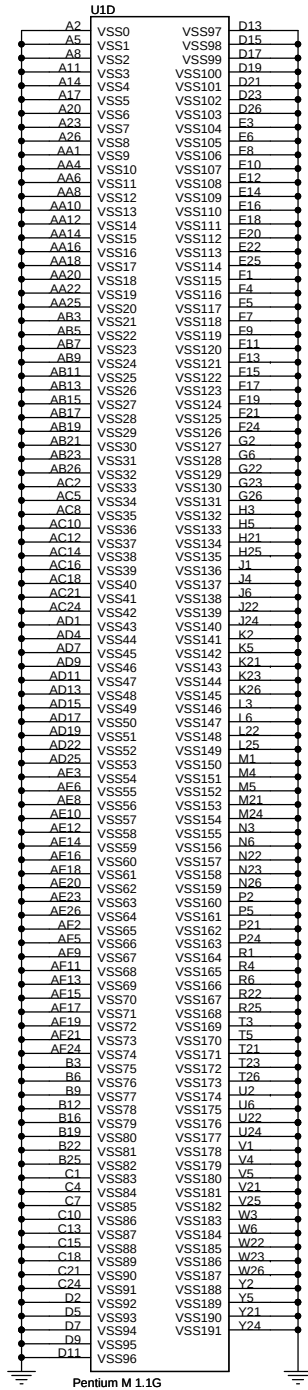
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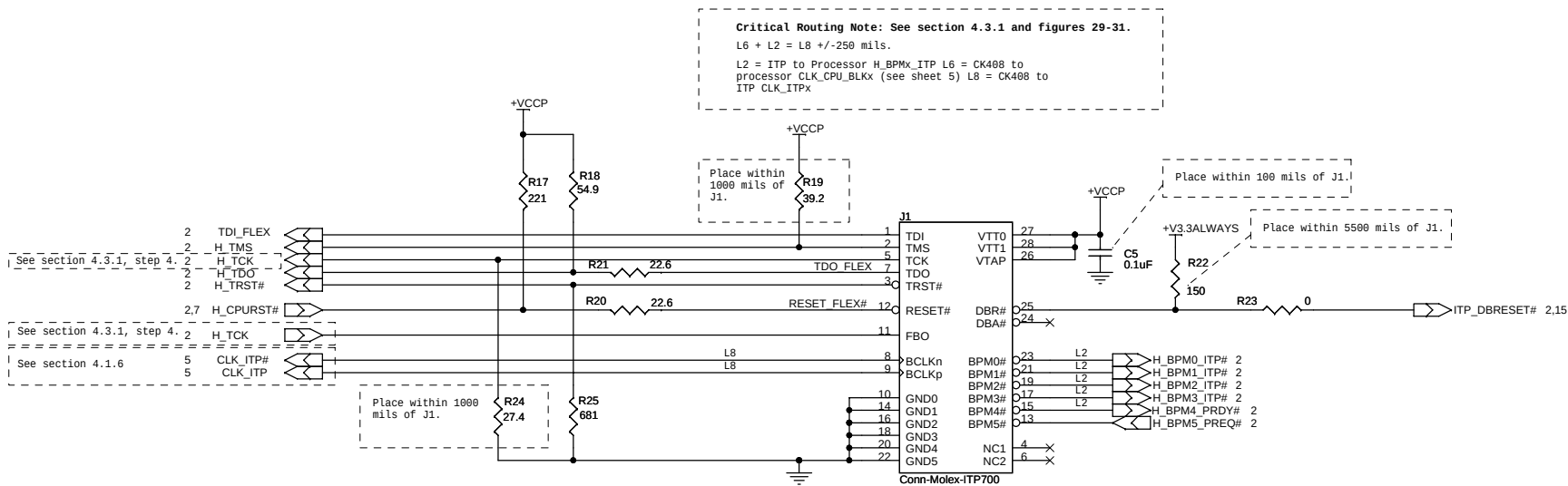
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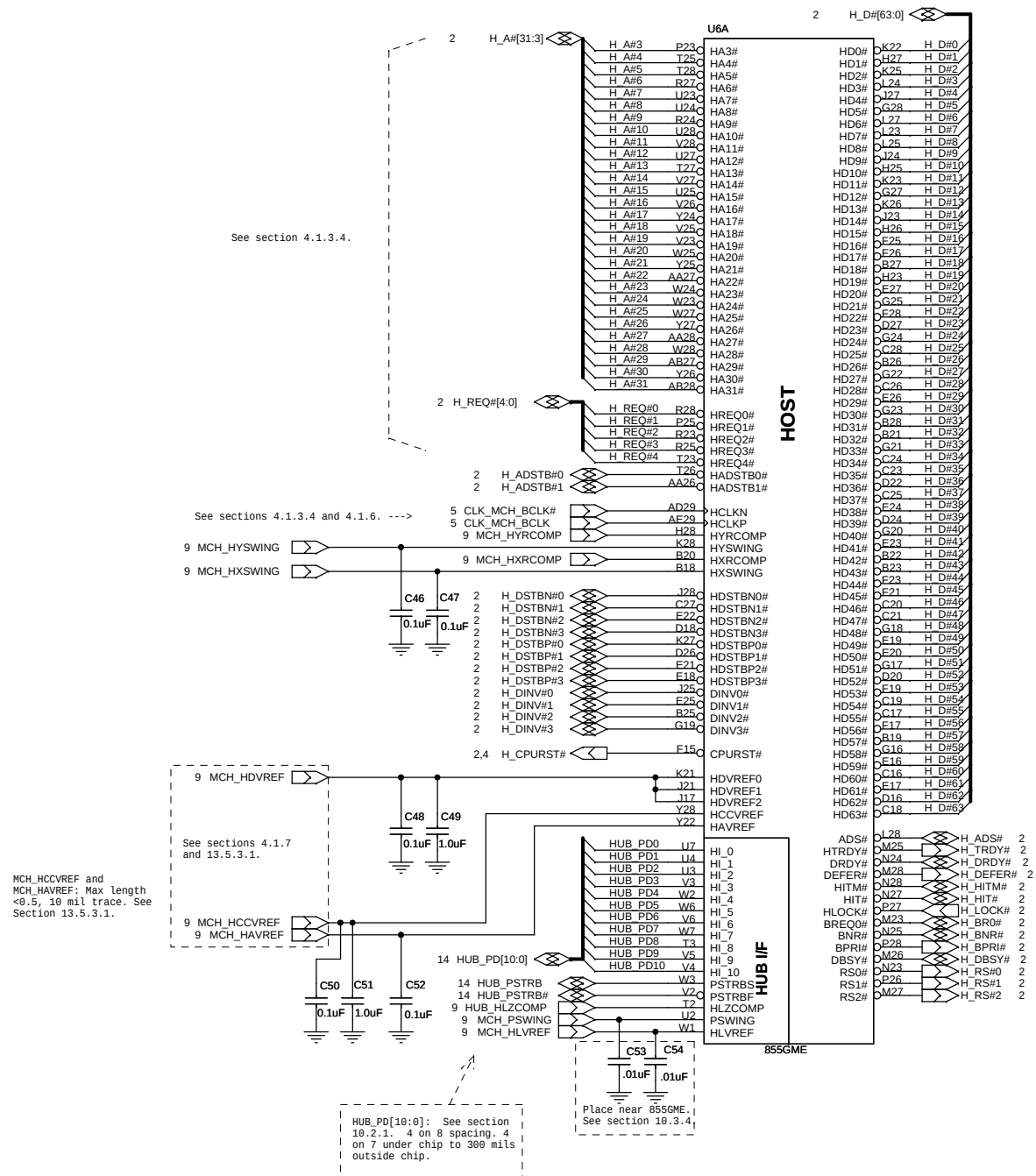
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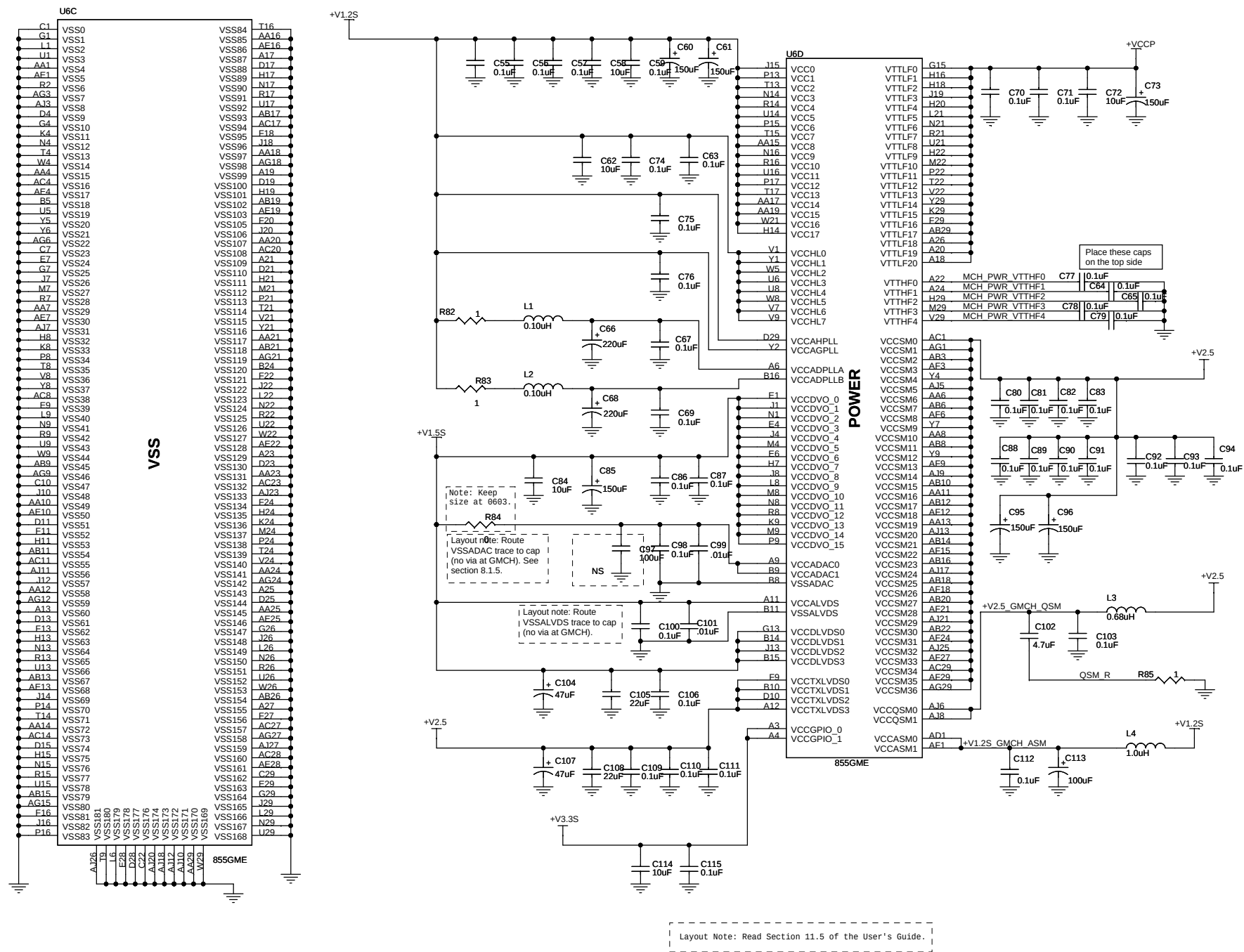


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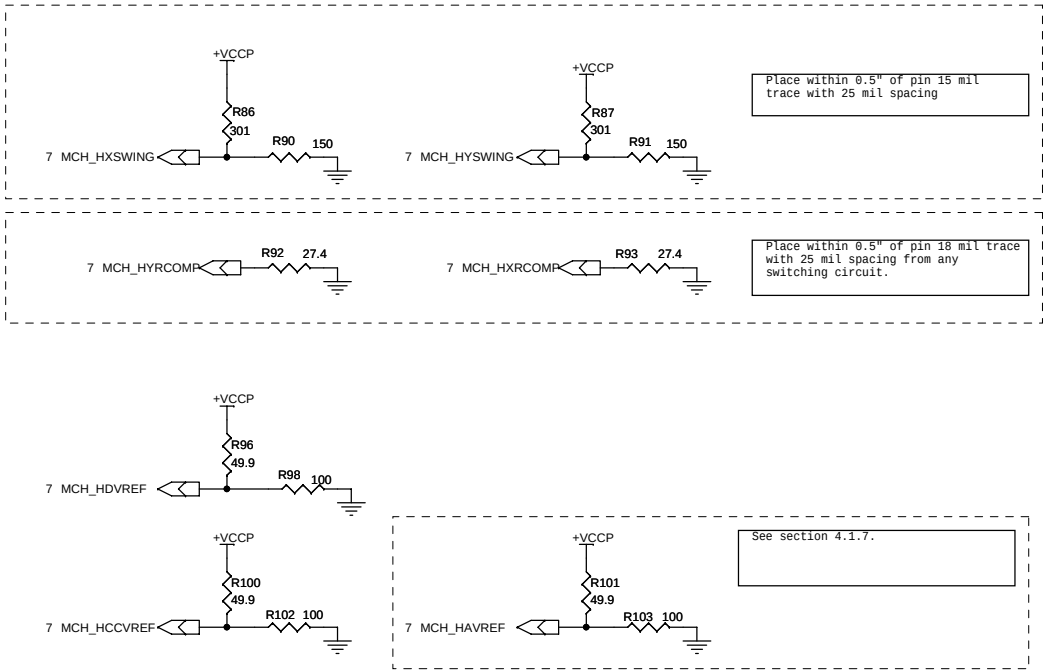




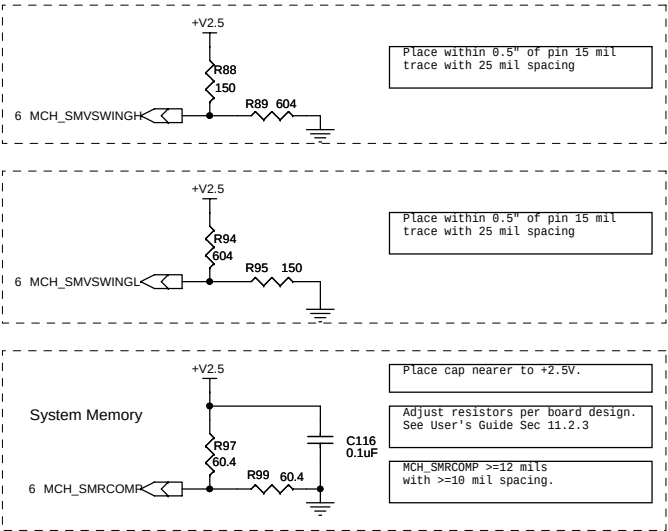
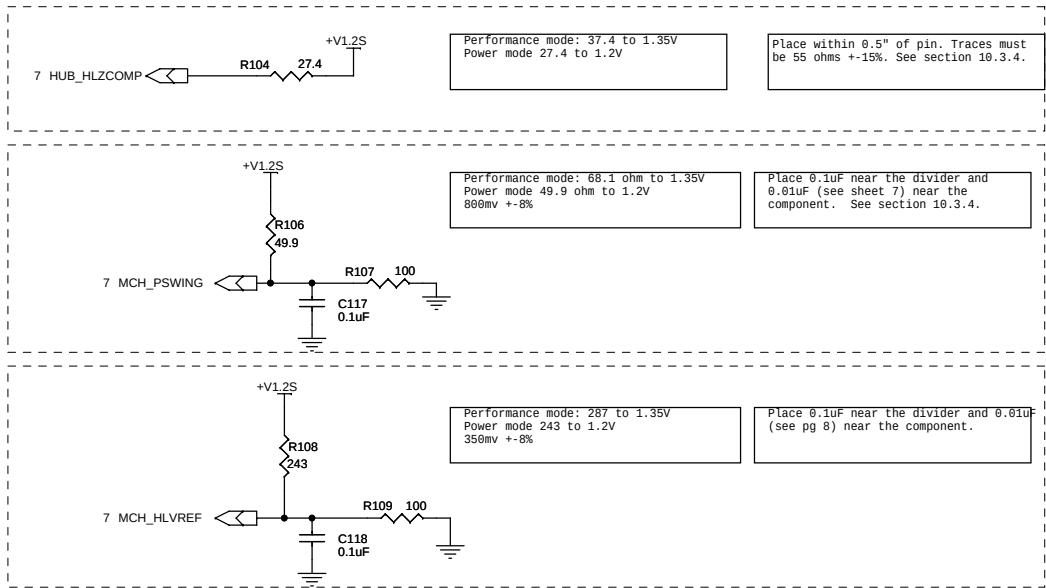


GMCH Compensation & Reference Voltages

Host



Hub Interface



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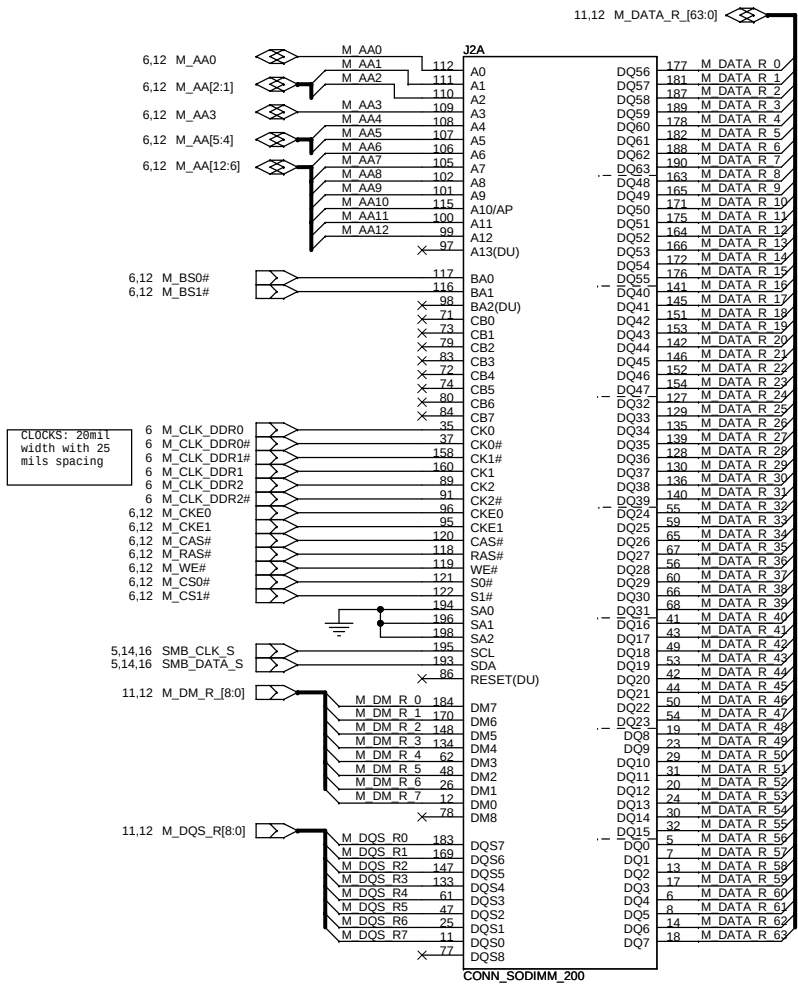
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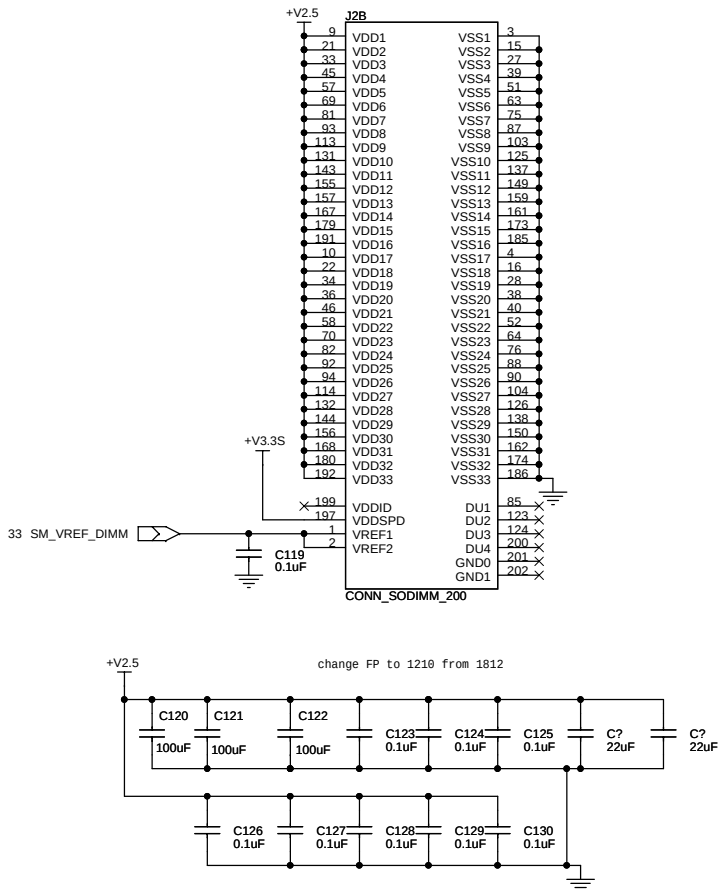
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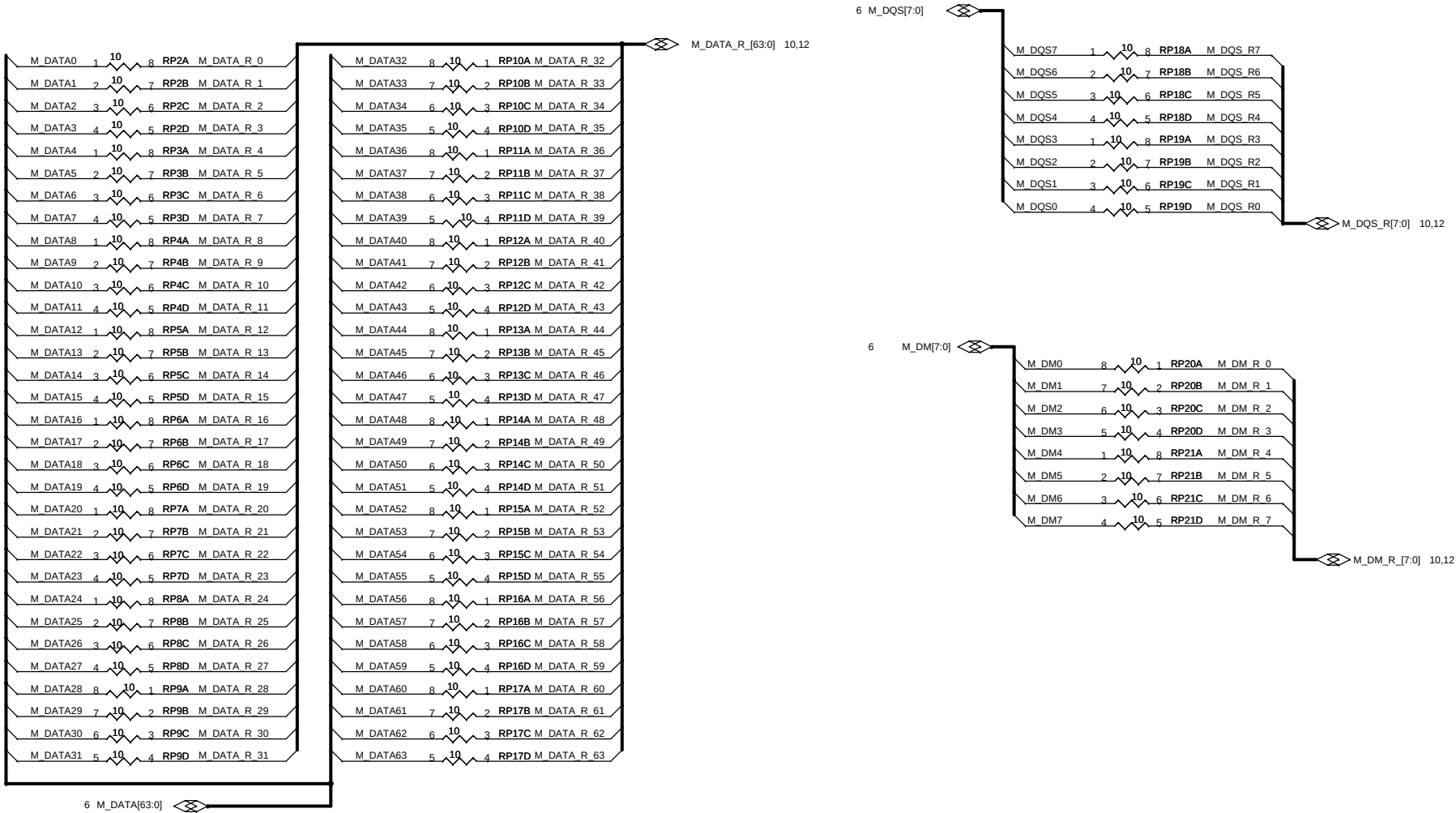
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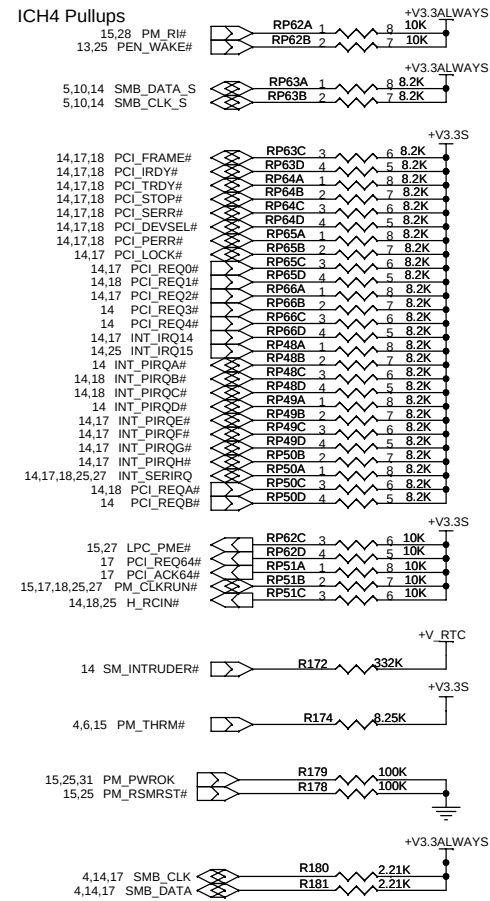
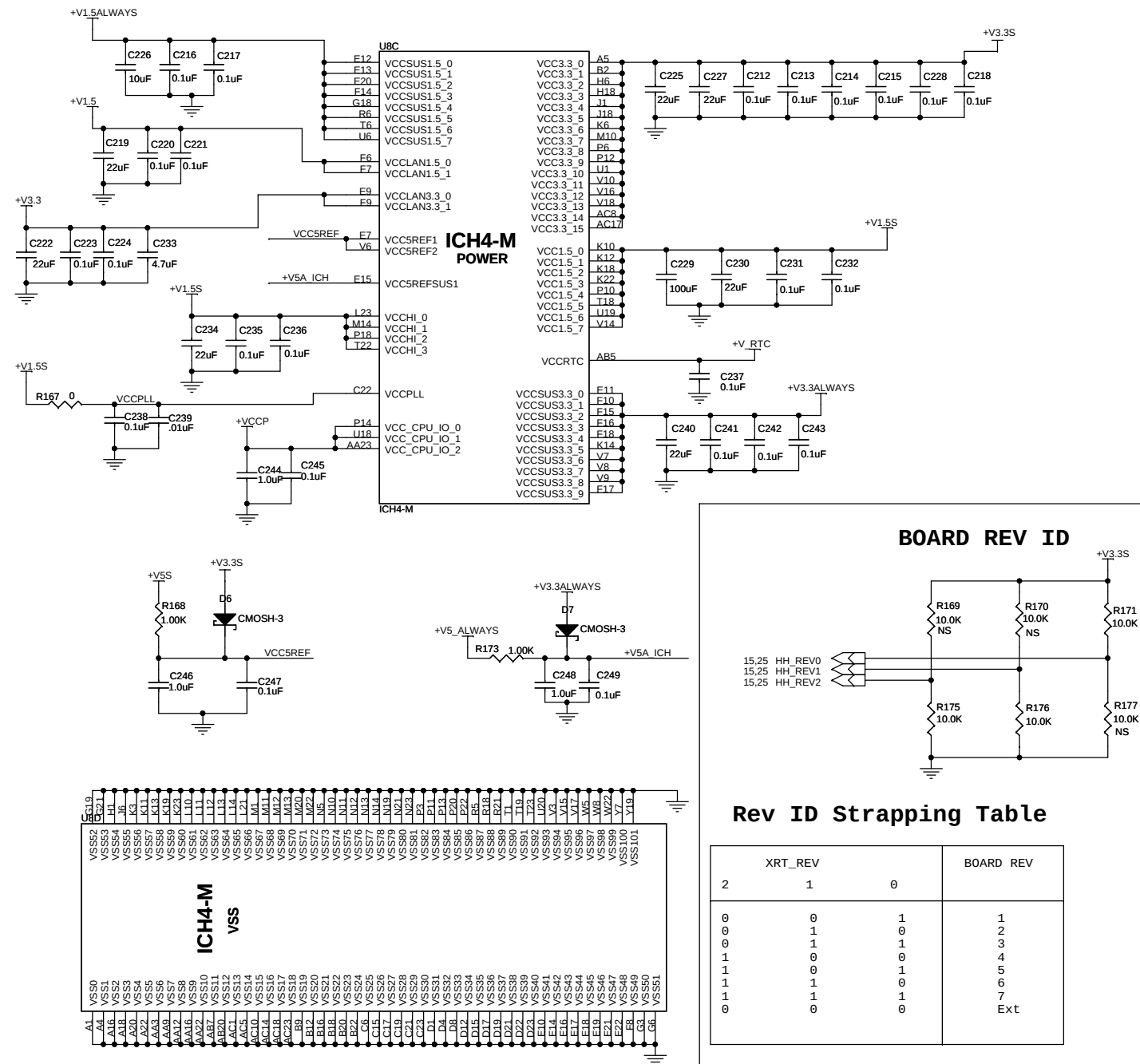
Layout note: Complex layout instructions are available in section 6 of the User's Guide.



Layout note: Place capacitors as near to the DDR connector as possible.

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BOARD REV ID

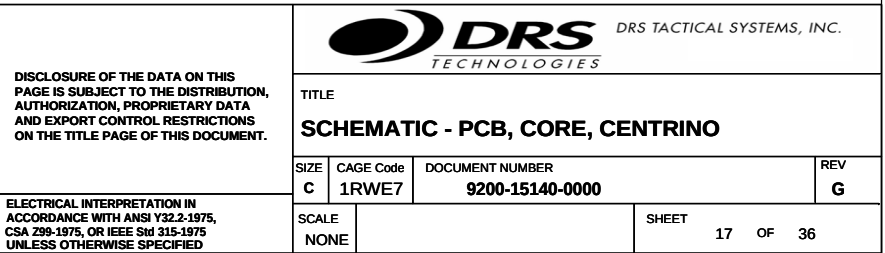
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15.25 HH_REV1
15.25 HH_REV2

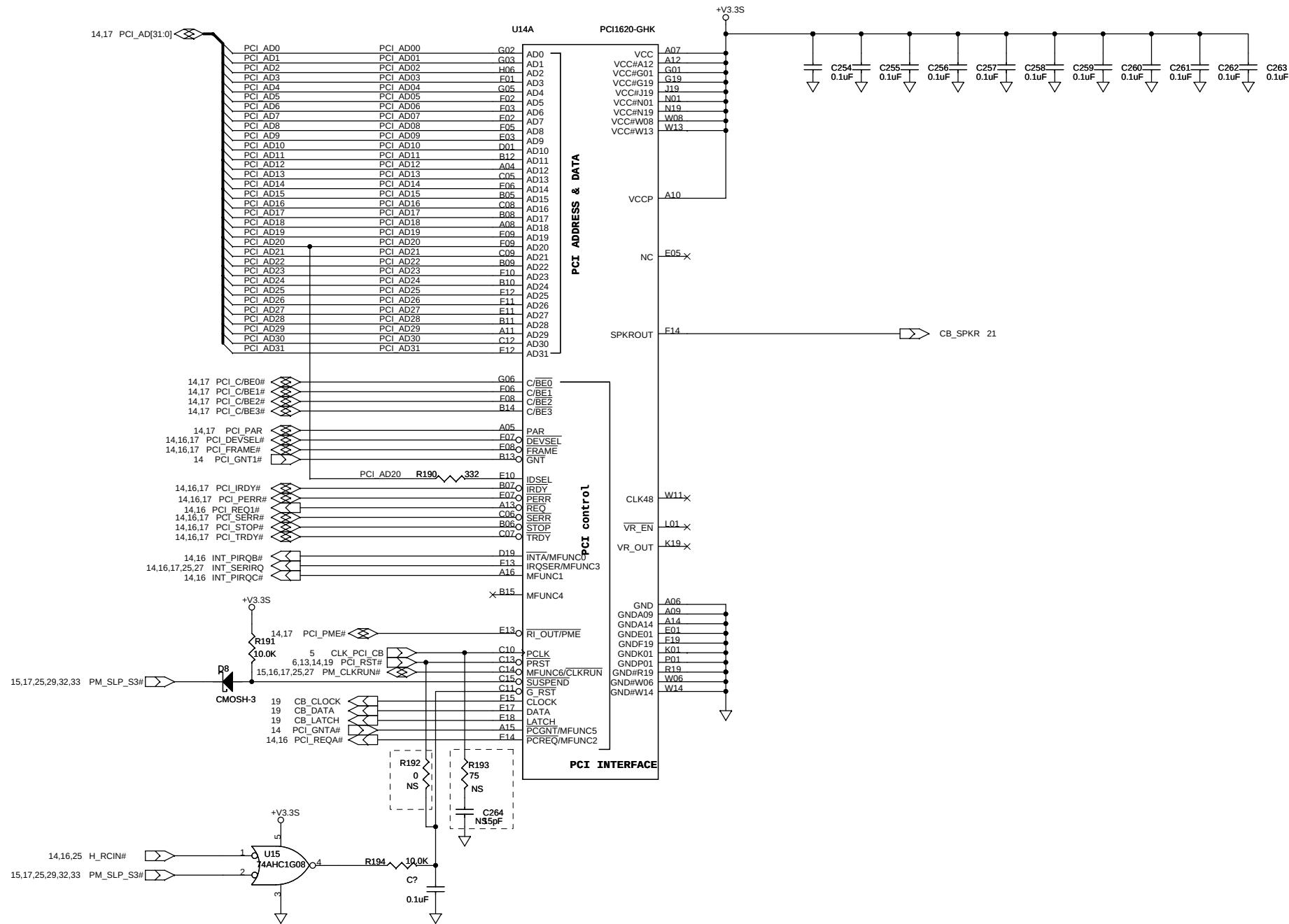
R169 10.0K NS
R170 10.0K NS
R171 10.0K NS
R175 10.0K NS
R176 10.0K NS
R177 10.0K NS

+V3.3S

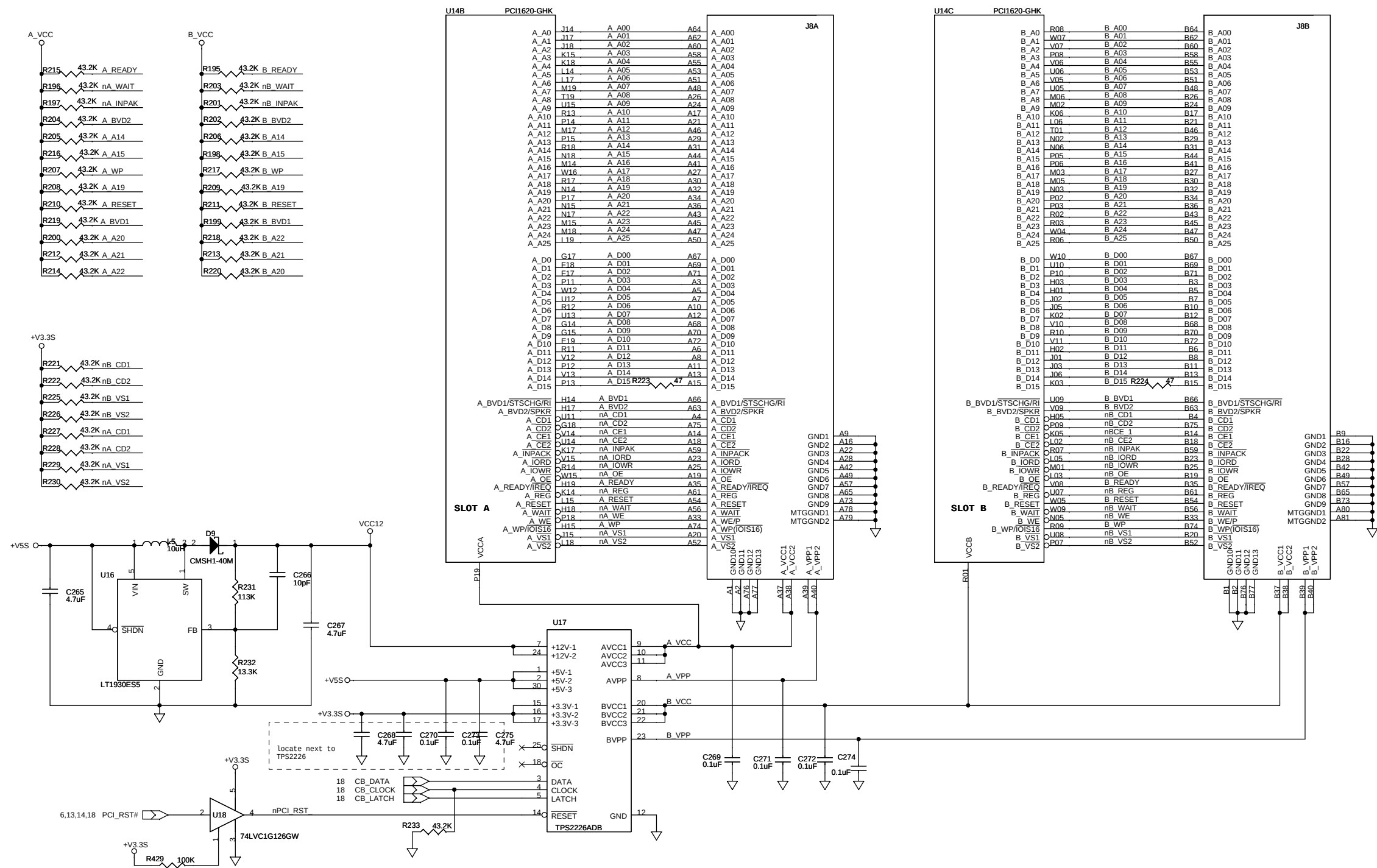
Rev ID Strapping Table

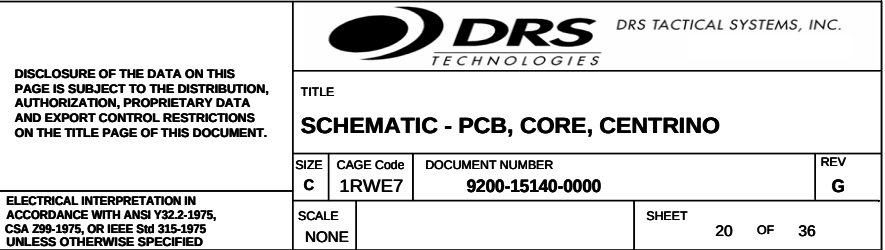
XRT_REV			BOARD_REV
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0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	Ext

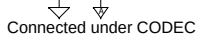


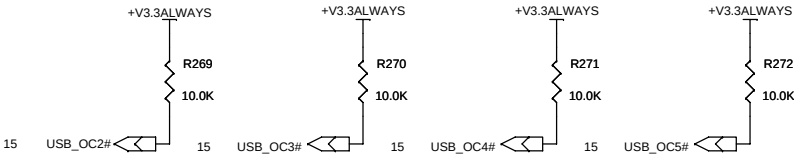


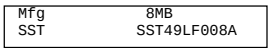
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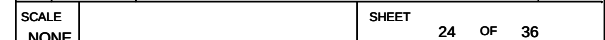


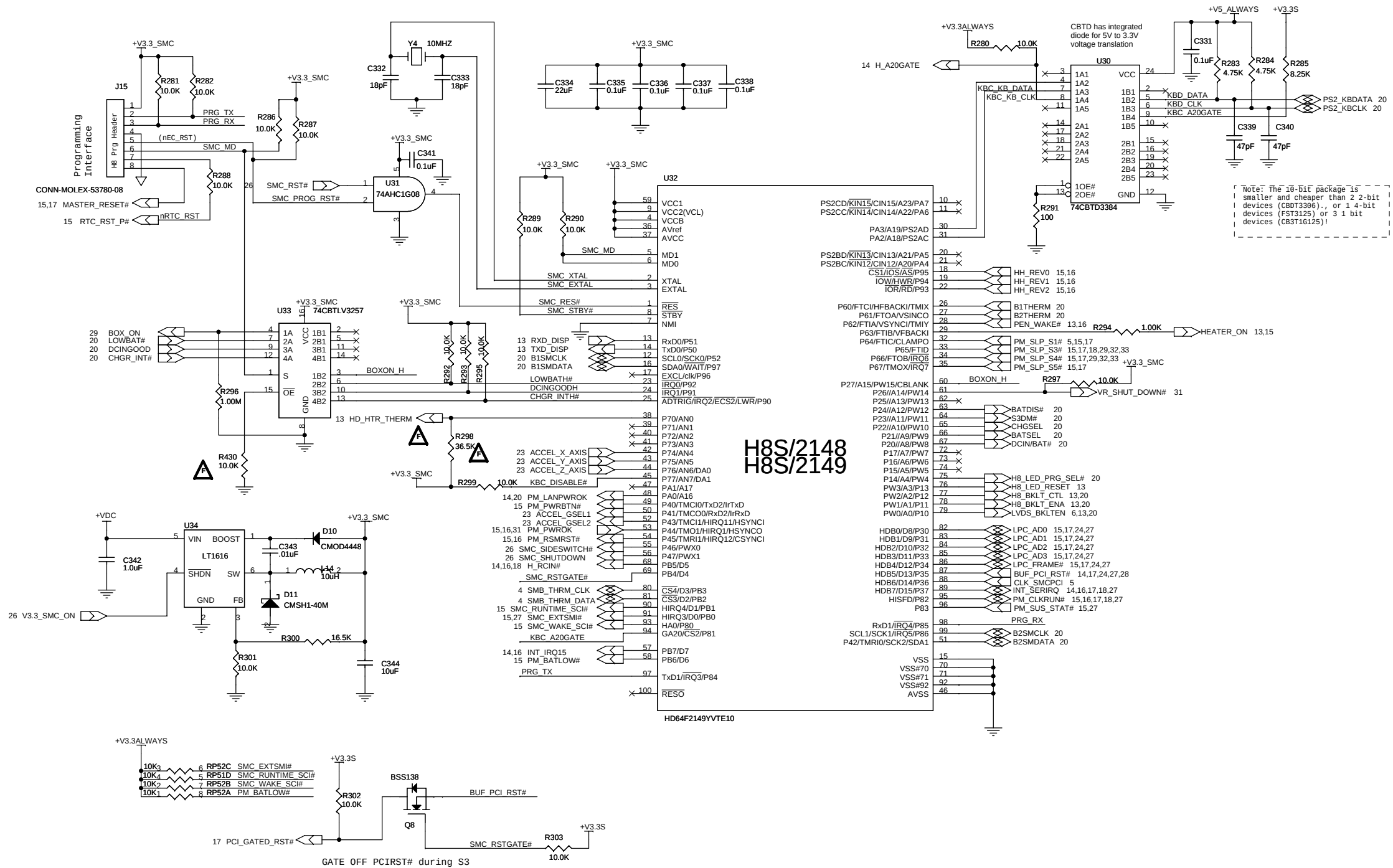




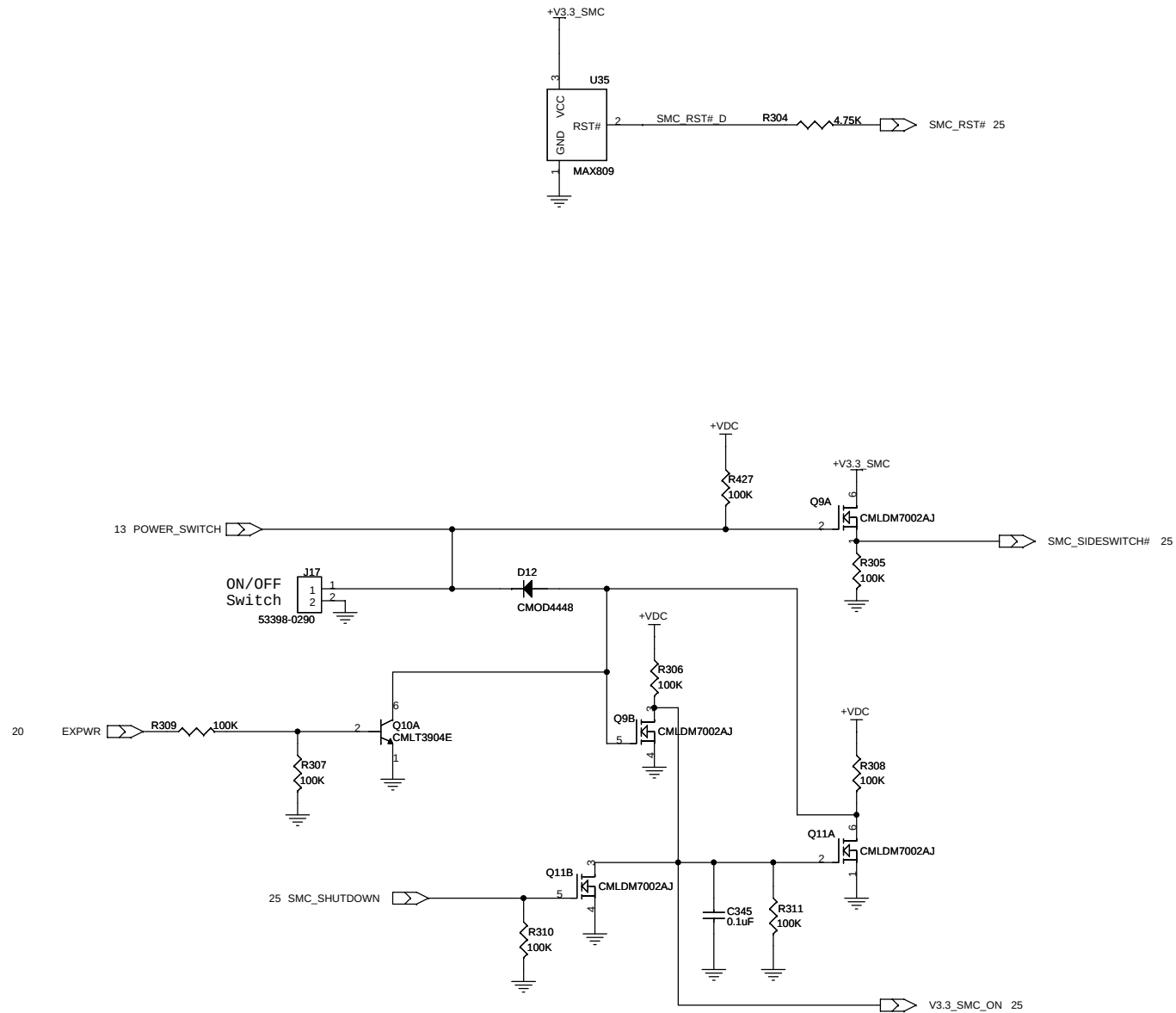


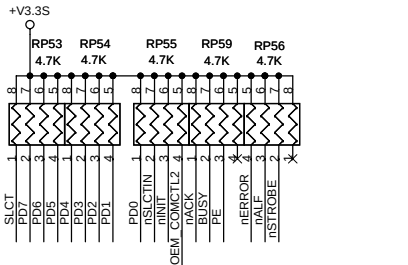
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CSA Z99-1975, OR IEEE Std 315-1975
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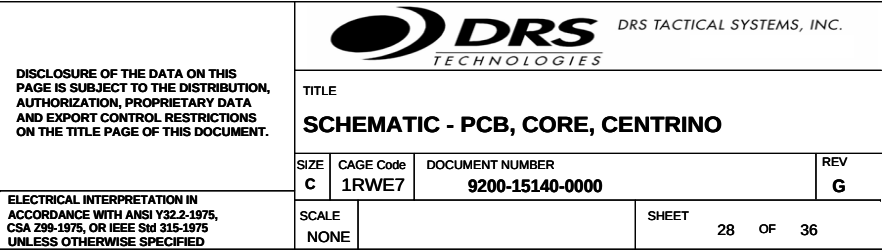




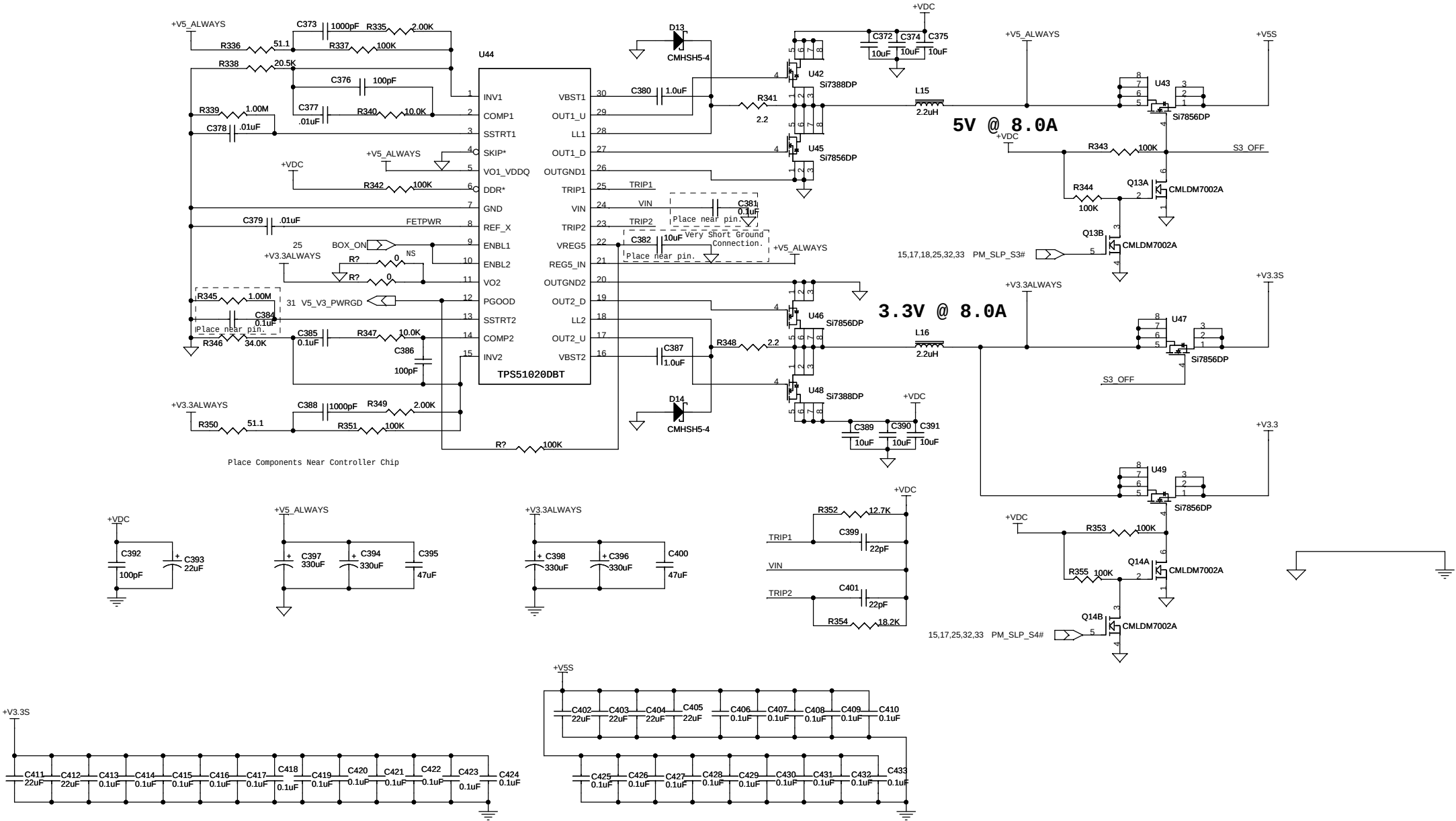
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SCHEMATIC - PCB, CORE, CENTRINO

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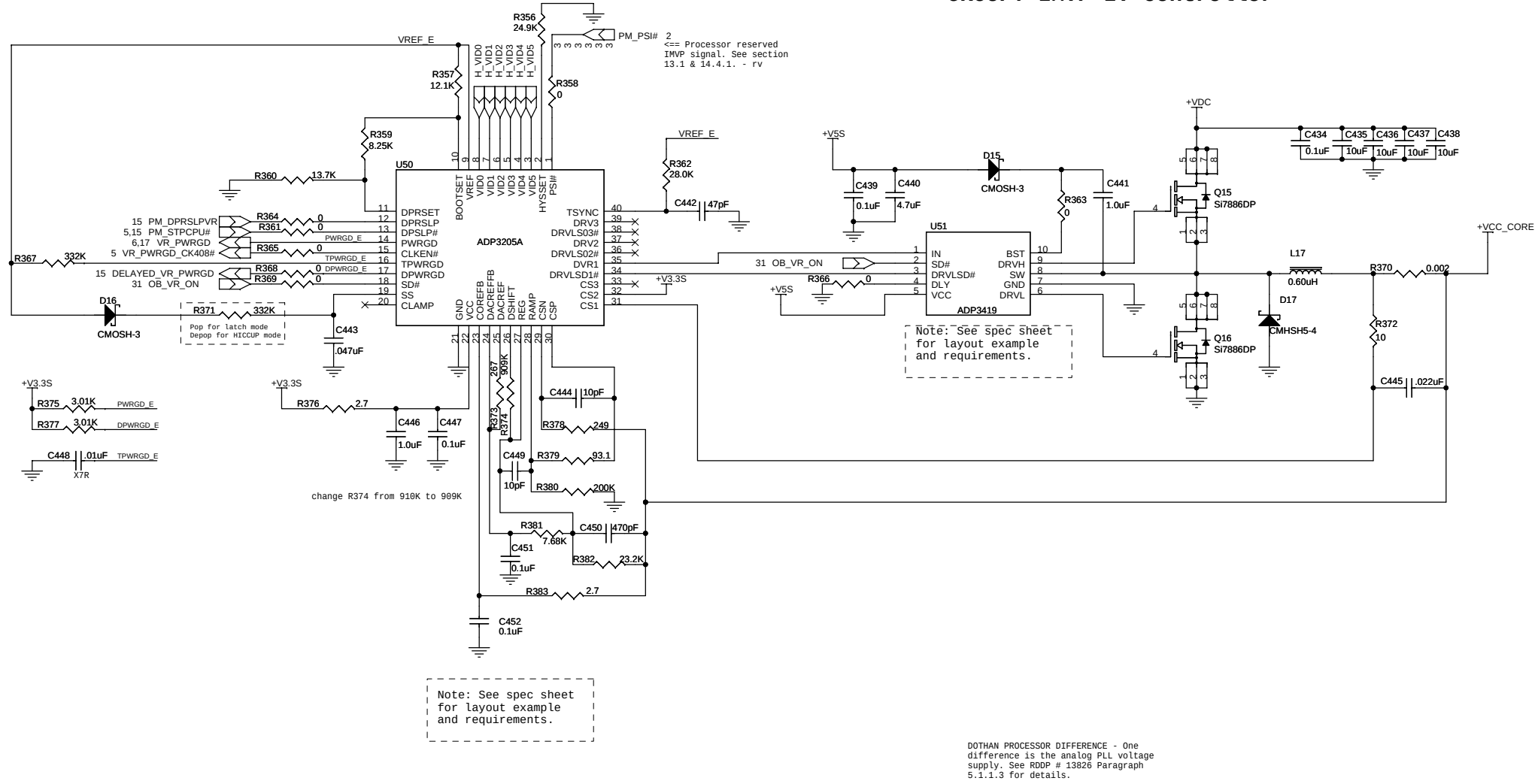


GROUP: V3 V5 Supply



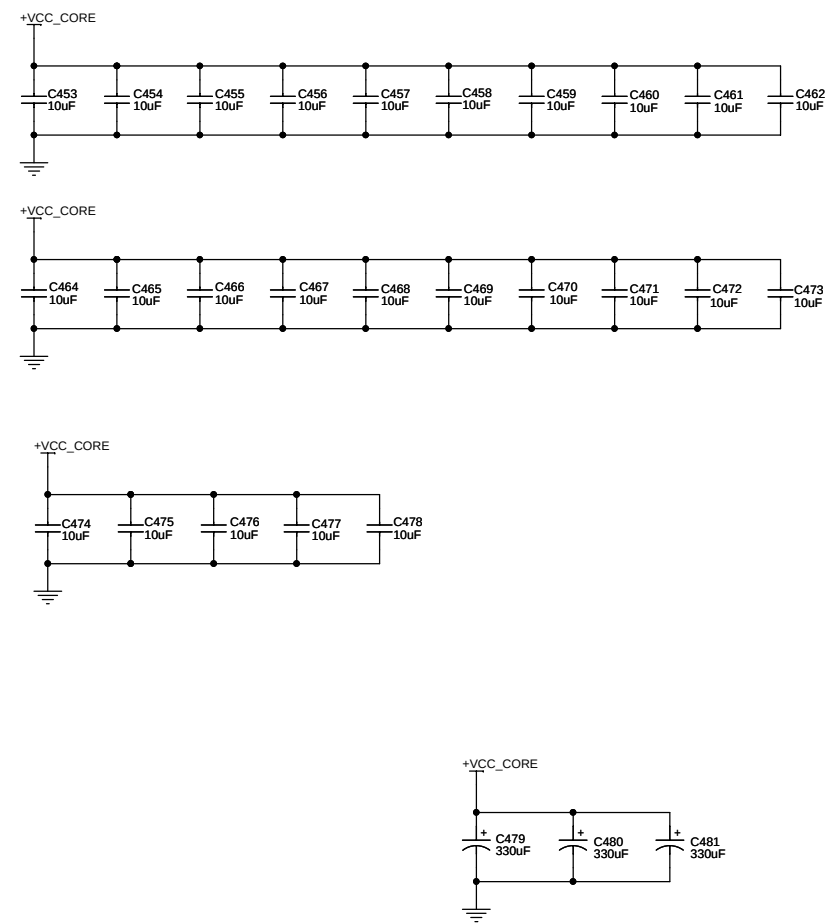
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GROUP: IMVP IV Controller

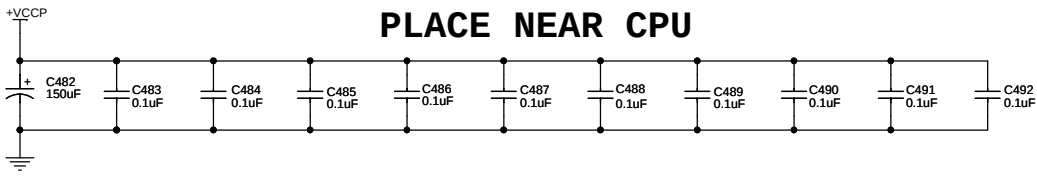


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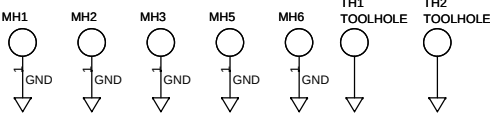
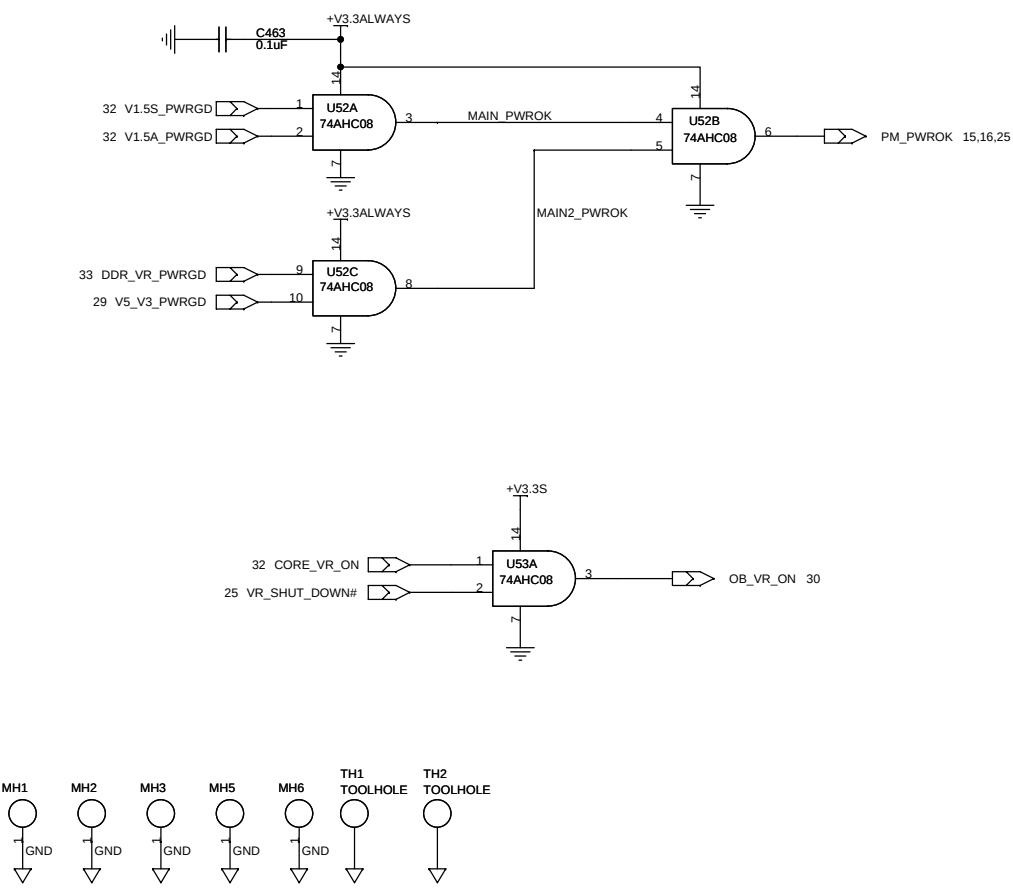
VCore HF and Bulk Decoupling

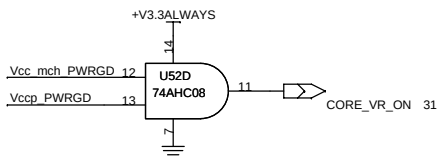
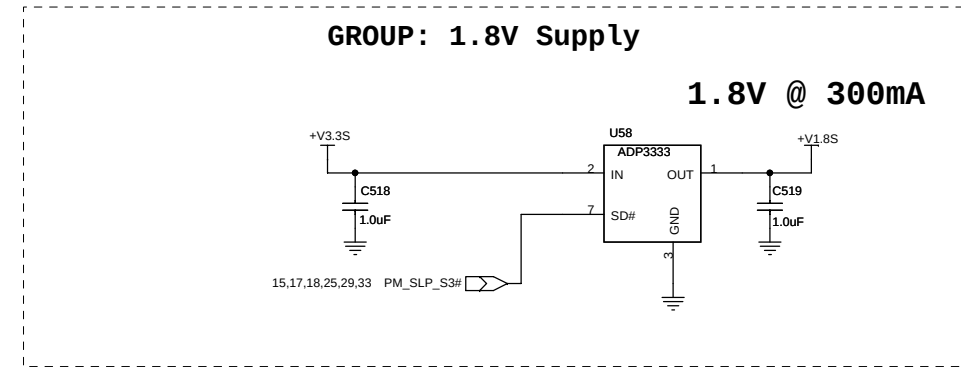
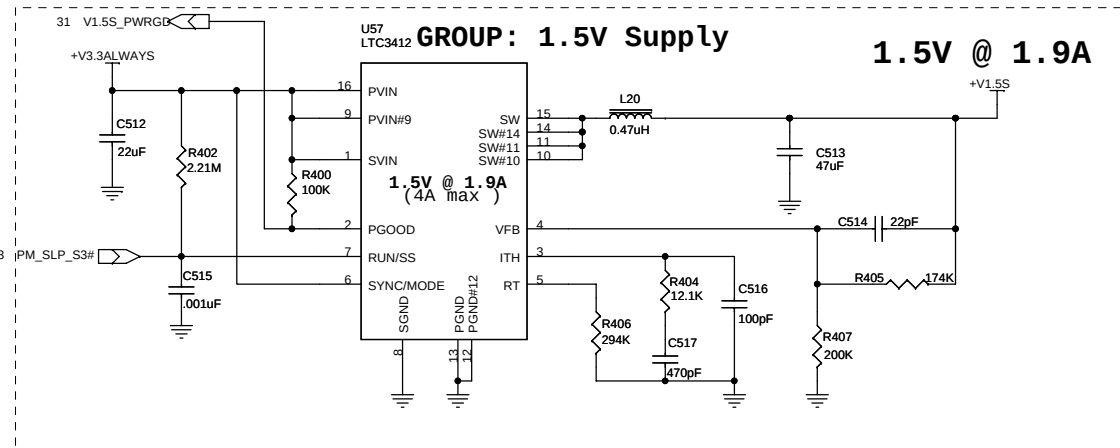
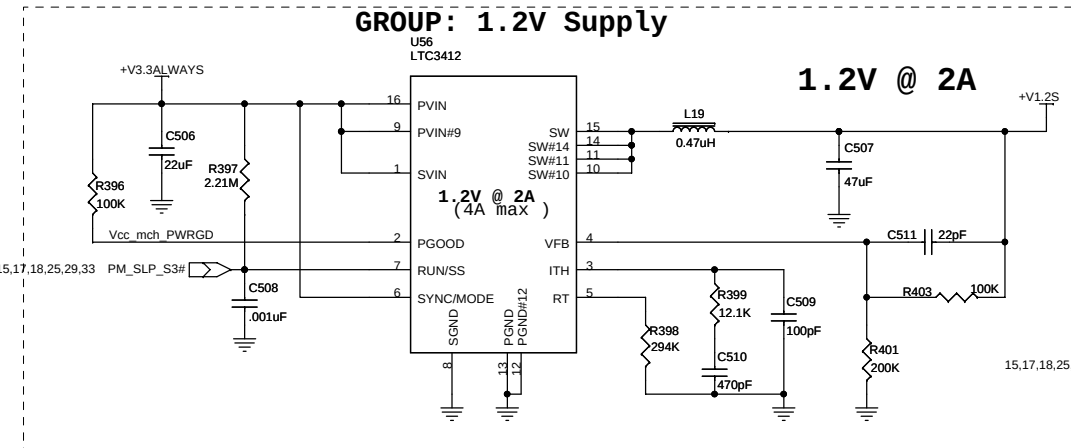
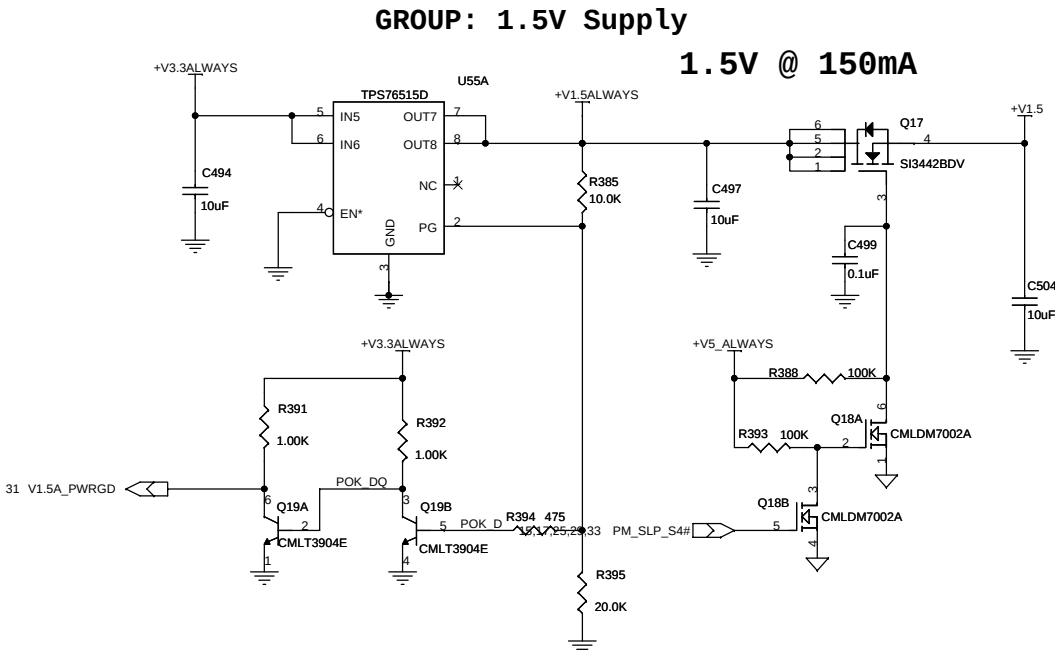
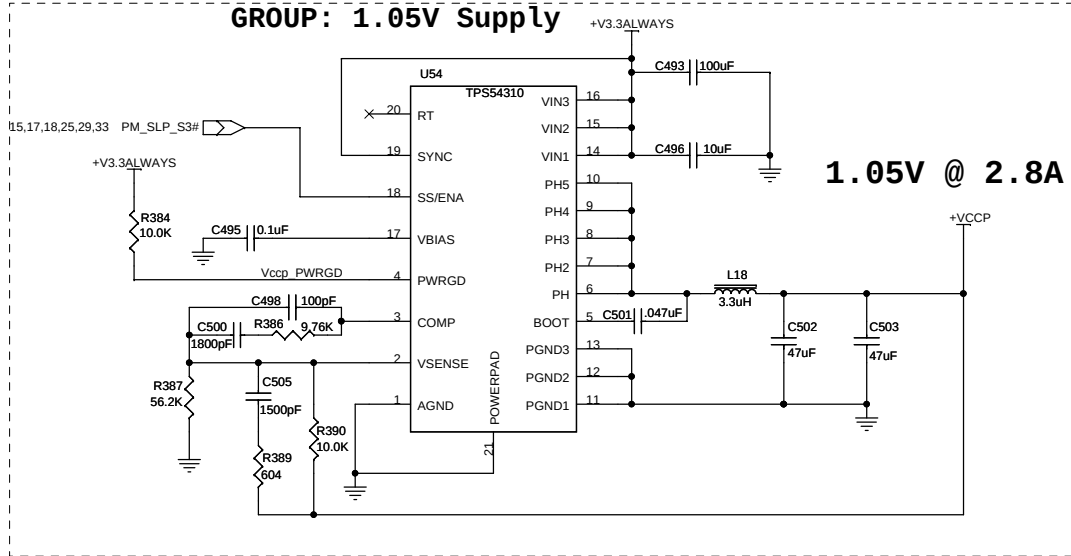


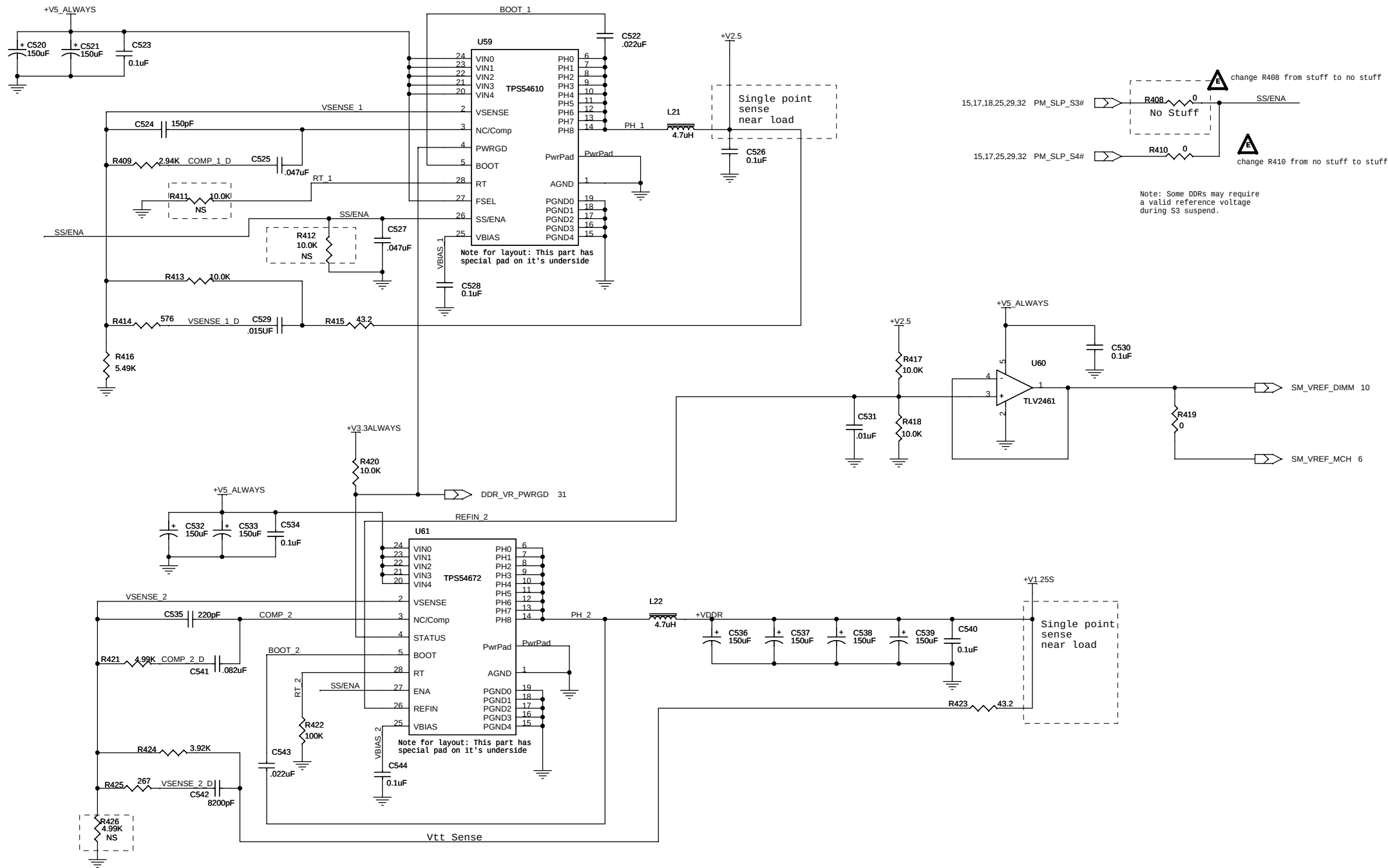
VCCP Decoupling



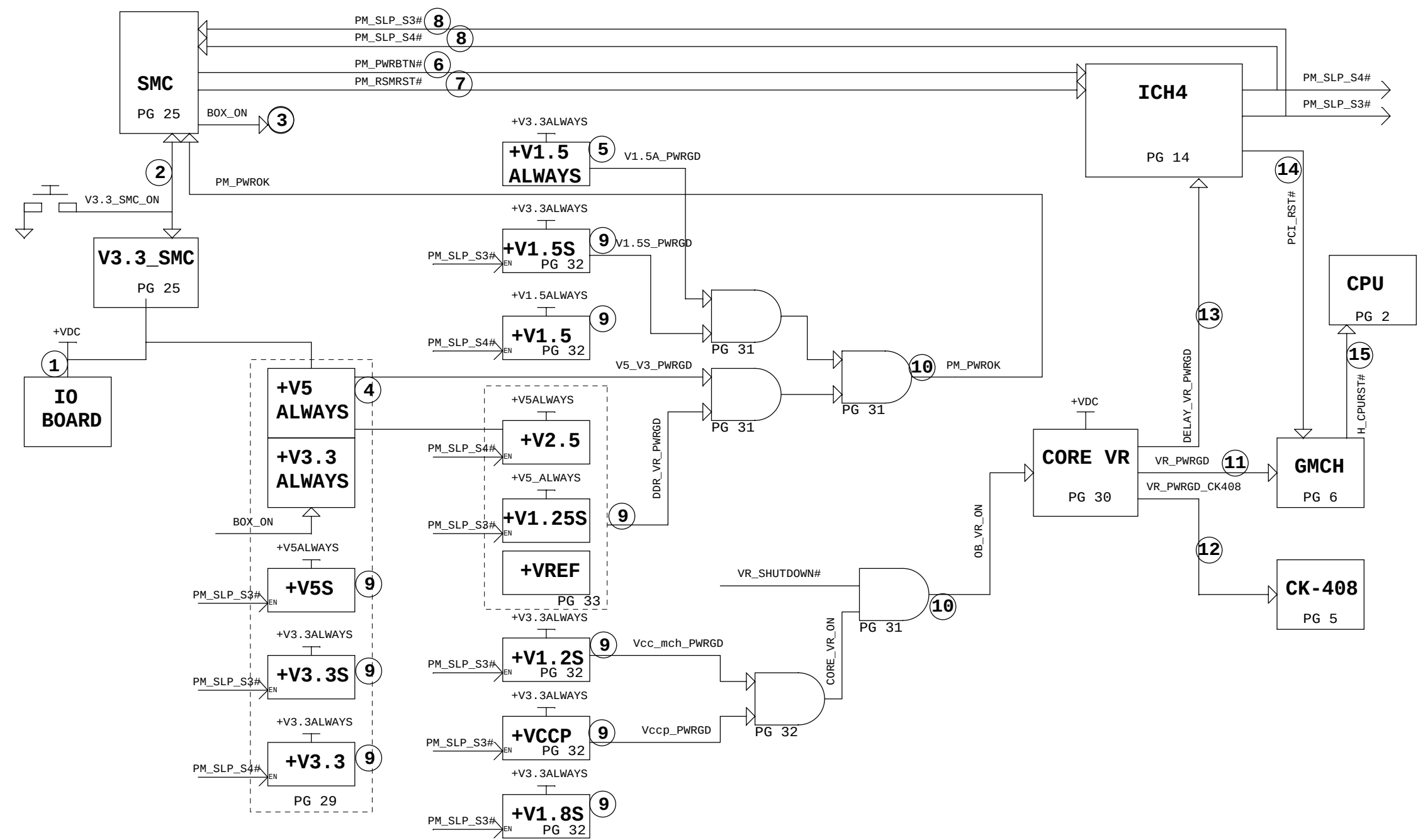
Power Good Circuitry

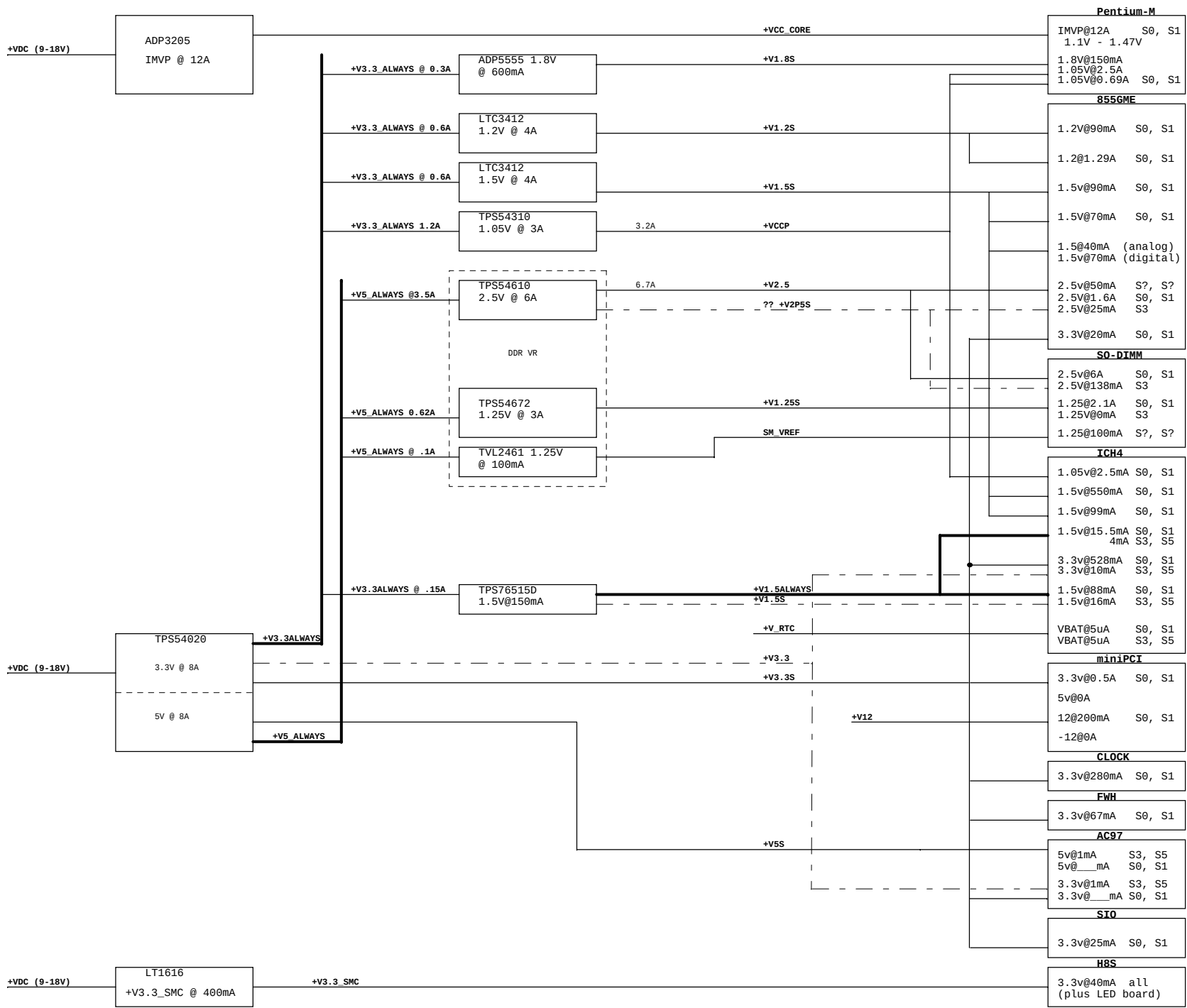




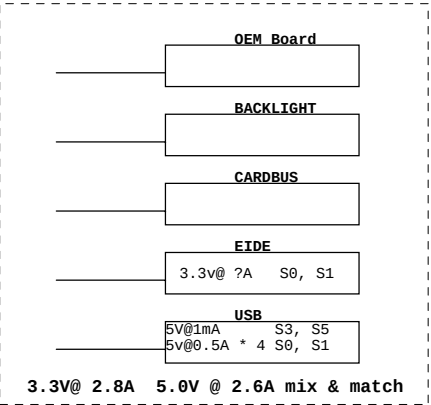


Power On Sequence





Voltage	S0,S1	S3,S5
1.05v	3.19A	0A
1.2v	1.38A	0A
1.25v	2.2A	0A
VREF	100mA	0A
1.5v	1.007A	16mA
2.5v	6.65A	163mA
3.3v	1.42A	1mA
5.0v	2A	5mA
12v	200mA	0A
-12v	0A	0A 0A
1.8V	300mA	
IMVP	9A	



HAMMERHEAD XRT-CENTRINO

Voltage Wells

+VDC	Primary DC system power supply (10 to 21V)
+VCC_CORE	Core voltage for processor
+VCCP	1.05V rail for processor PSB, 855-GME PSB
+V1.8S	1.8V for processor PLL and VID circuitry
+V1.2S	1.2V for 855-GME core
+V1.25S	1.25V DDR Termination voltage
+V1.5S	1.5V switched power rail (off in S3-S5)
+V1.5ALWAYS	1.5V always on power rail
+V1.5	1.5V power rail (off in S4-S5)
+V2.5	2.5V power rail for DDR
+V3.3ALWAYS	3.3V always on power rail
+V3.3	3.3V power rail (off in S4-S5)
+V3.3S	3.3V switched power rail (off in S3-S5)
+V5ALWAYS	5.0V for ICH4 VCC5REFSUS
+V5	5.0V power rail (off in S4-S5)
+V5S	5.0V switched power rail (off in S3-S5)

I2C / SMB Addresses

Device	Address	Hex	Bus

S0-DIMM0	1010 000x	A0	SMB_ICH_S
CLOCK CHIP	1101 001x	D2	SMB_ICH_S
SPREAD CLK	1101 010x	D4	SMB_ICH_S
THERMAL CHP	1001 100x	98	SMB_ICH

EMI Information

Freq	Name	CK-408	Sinks

100 MHz	HOST_CLK	CPU	CPU GMCH DebugPort
66 MHz	CLK66	3v66	GMCH ICH4
33 MHz	CLK33	PCI_F	ICH4 SIO FWH
33 MHz	PCICLK	PCI	Option Connector
14.1MHz	CLK14	REF0	ICH4 SIO
48 MHz	DOTCLK	48MHz	GMCH
48/66	SSCCLK	VCH	GMCH (spreadSpc)
48 MHz	USBCLK	48MHz	ICH4
33 MHz	ACPICLK	INT_	ICH4
5-50MHz	LAN_CLK	LAN_JCKL	ICH4