2SC4226

NPN Silicon RF Transistor

NPN Epitaxial Silicon RF Transistor for High-Frequency Low-Noise Amplification 3-pin super Minimold

R09DS0022EJ0200
Rev.2.00
Jun 29, 2011

DESCRIPTION

The 2SC4226 is a low supply voltage transistor designed for VHF, UHF low noise amplifier.

It is suitable for a high density surface mount assembly since the transistor has been applied 3-pin super minimold package.

FEATURES

- Low noise : NF = 1.2 dB TYP. @ V_{CE} = 3 V, I_C = 7 mA, f = 1 GHz
- High gain : $|S_{21e}|^2$ = 9 dB TYP. @ V_{CE} = 3 V, I_C = 7 mA, f = 1 GHz
- 3-pin super minimold package

<R> ORDERING INFORMATION

Part Number	Order Number	Package	Quantity	Supplying Form
2SC4226	2SC4226-A	3-pin super Minimold (Pb-Free)	50 pcs (Non reel)	• 8 mm wide embossed taping
2SC4226-T1	2SC4226-T1-A		3 kpcs/reel	• Pin 3 (Collector) face the perforation side of the tape

Remark To order evaluation samples, please contact your nearby sales office.
The unit sample quantity is 50 pcs.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Collector to Base Voltage	V_{CBO}	20	V
Collector to Emitter Voltage	V_{CEO}	12	V
Emitter to Base Voltage	V_{EBO}	3	V
Collector Current	I_C	100	mA
Total Power Dissipation	P_{tot} Note	150	mW
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	–65 to +150	°C

Note Free air

CAUTION

Observe precautions when handling because these devices are sensitive to electrostatic discharge.

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
DC Characteristics						
Collector Cut-off Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	1.0	μA
Emitter Cut-off Current	I_{EBO}	V_{EB} = 1 V, I_C = 0	–	–	1.0	μA
DC Current Gain	h_{FE} Note 1	V_{CE} = 3 V, I_C = 7 mA	40	110	250	–
RF Characteristics						
Gain Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 7 mA	3.0	4.5	–	GHz
Insertion Power Gain	$\lvert S_{21e} \rvert^2$	V_{CE} = 3 V, I_C = 7 mA, f = 1 GHz	7	9	–	dB
Noise Figure	NF	V_{CE} = 3 V, I_C = 7 mA, f = 1 GHz	–	1.2	2.5	dB
Reverse Transfer Capacitance	C_{re} Note 2	V_{CB} = 3 V, I_E = 0, f = 1 MHz	–	0.7	1.5	pF

Notes 1. Pulse measurement: PW ≤ 350 μs, Duty Cycle ≤ 2%

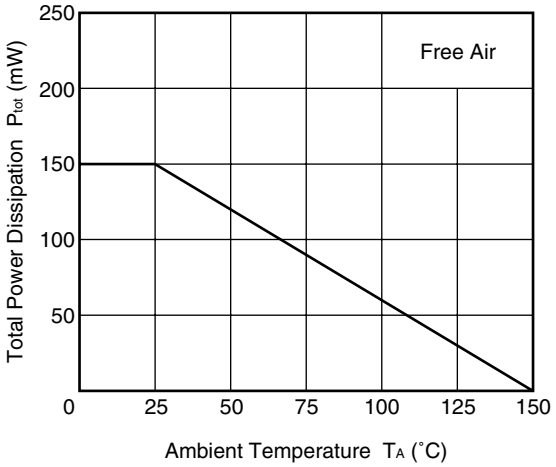
2. Collector to base capacitance when the emitter grounded

<R> h_{FE} CLASSIFICATION

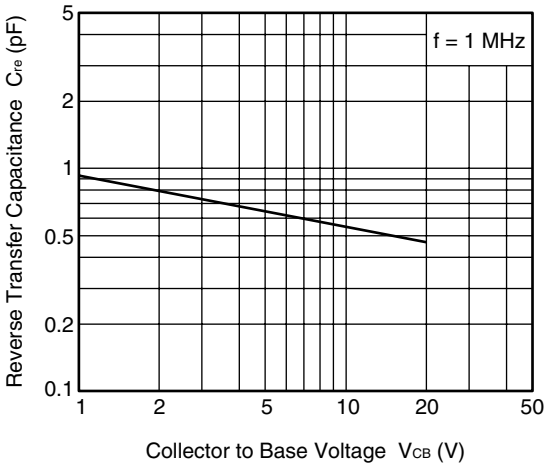
Rank	R23/Y23	R24/Y24	R25/Y25
Marking	R23	R24	R25
h_{FE} Value	40 to 80	70 to 140	125 to 250

TYPICAL CHARACTERISTICS (T_A = +25°C, unless otherwise specified)

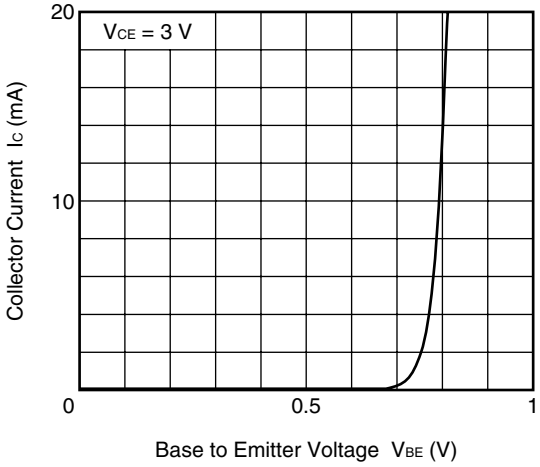
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



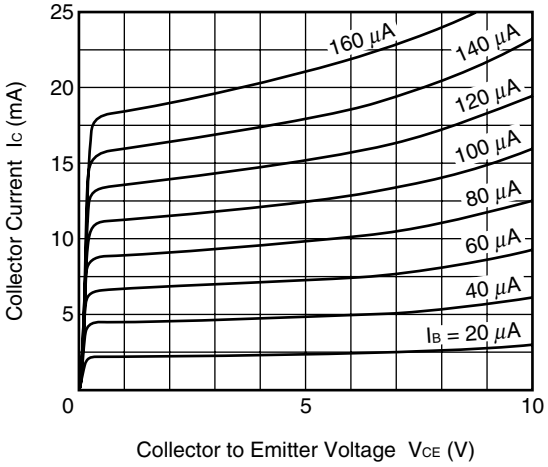
REVERSE TRANSFER CAPACITANCE vs. COLLECTOR TO BASE VOLTAGE



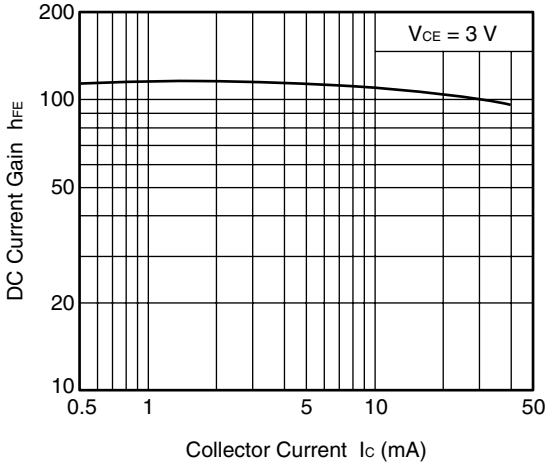
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



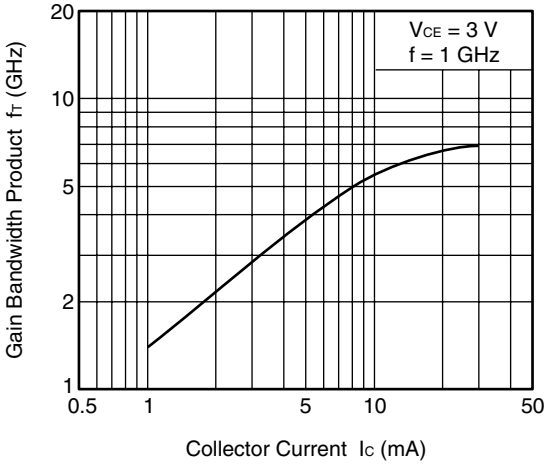
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN vs. COLLECTOR CURRENT

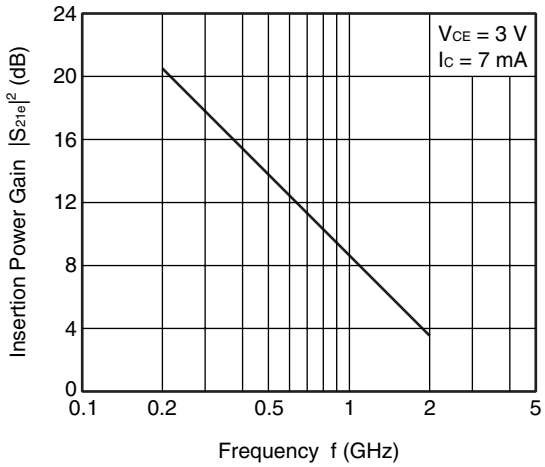


GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT

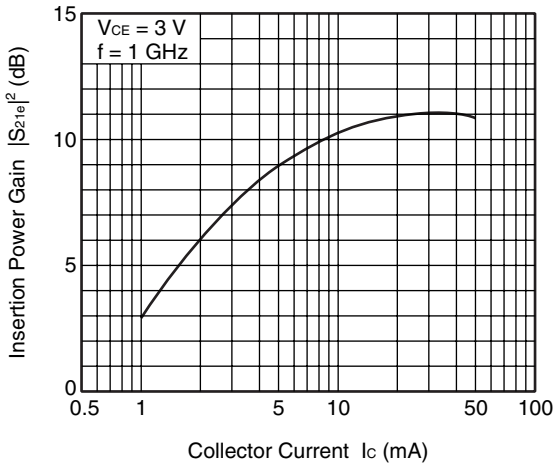


Remark The graphs indicate nominal characteristics.

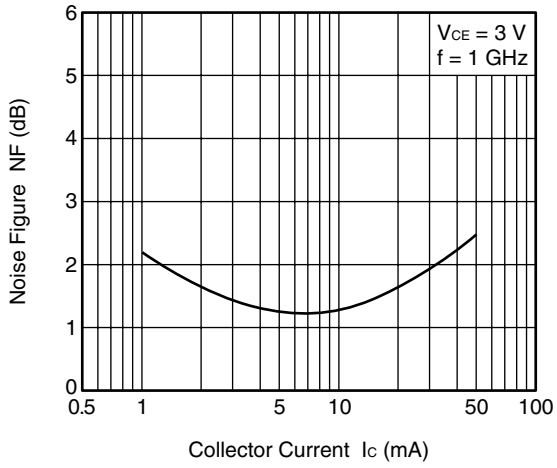
INSERTION POWER GAIN
vs. FREQUENCY



INSERTION POWER GAIN
vs. COLLECTOR CURRENT



NOISE FIGURE vs.
COLLECTOR CURRENT



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

S-parameters and noise parameters are provided on our Web site in a format (S2P) that enables the direct import of the parameters to microwave circuit simulators without the need for keyboard inputs.

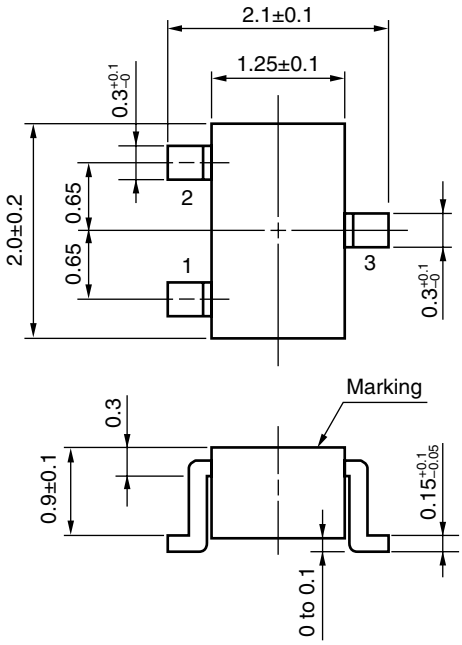
Click here to download S-parameters.

[RF and Microwave] → [Device Parameters]

URL http://www2.renesas.com/microwave/en/download.html

PACKAGE DIMENSIONS

3-PIN SUPER MINIMOLD (UNIT: mm)



PIN CONNECTIONS

1. Emitter
2. Base
3. Collector

(EIAJ : SC-70)

Revision History	2SC4226 Data Sheet

Rev.	Date	Description	
		Page	Summary
–	Dec 2003	–	Previous No. :PU10450EJ01V0DS
2.00	Jun 29, 2011	p.1	Modification of **ORDERING INFORMATION**
		p.2	Modification of **h_{FE} CLASSIFICATION**

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Colophon 1.1

ATF-501P8

High Linearity Enhancement Mode[1] Pseudomorphic HEMT in 2x2 mm² LPCC[3] Package

Data Sheet

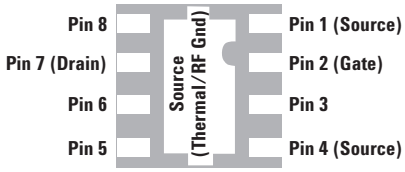
Description

Avago Technologies's ATF-501P8 is a single-voltage high linearity, low noise E-pHEMT housed in an 8-lead JEDEC-standard leadless plastic chip carrier (LPCC[3]) package. The device is ideal as a medium-power amplifier. Its operating frequency range is from 400 MHz to 3.9 GHz.

The thermally efficient package measures only 2mm x 2mm x 0.75mm. Its backside metalization provides excellent thermal dissipation as well as visual evidence of solder reflow. The device has a Point MTTF of over 300 years at a mounting temperature of +85°C. All devices are 100% RF & DC tested.

Notes:
1. Enhancement mode technology employs a single positive V_{gs}, eliminating the need of negative gate voltage associated with conventional depletion mode devices.
2. Refer to reliability datasheet for detailed MTTF data.
3. Conforms to JEDEC reference outline MO229 for DRP-N.
4. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

Pin Connections and Package Marking



Bottom View

Top View

Note:
Package marking provides orientation and identification:
"0P" = Device Code
"x" = Date code indicates the month of manufacture.

Features

- Single voltage operation
- High Linearity and P1dB
- Low Noise Figure
- Excellent uniformity in product specifications
- Small package size: 2.0 x 2.0 x 0.75 mm³
- Point MTTF > 300 years[2]
- MSL-1 and lead-free
- Tape-and-Reel packaging option available

Specifications

- 2 GHz; 4.5V, 280 mA (Typ.)
- 45.5 dBm Output IP3
- 29 dBm Output Power at 1dB gain compression
- 1 dB Noise Figure
- 15 dB Gain
- 14.5 dB LFOM[4]
- 65% PAE
- 23°C/W thermal resistance

Applications

- Front-end LNA Q2 and Q3, Driver or Pre-driver Amplifier for Cellular/PCS and WCDMA wireless infrastructure
- Driver Amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-pHEMT for other high linearity applications

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1C)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

ATF-501P8 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain–Source Voltage[2]	V	7
V_{GS}	Gate–Source Voltage[2]	V	-5 to 0.8
V_{GD}	Gate Drain Voltage[2]	V	-5 to 1
I_{DS}	Drain Current[2]	A	1
I_{GS}	Gate Current	mA	12
P_{diss}	Total Power Dissipation[3]	W	3.5
$P_{in\ max.}$	RF Input Power	dBm	30
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{ch_b}	Thermal Resistance[4]	°C/W	23

Notes:
1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Board (package belly) temperatureT_B is 25°C. Derate 43.5 mW/°C for T_B > 69.5°C.
4. Channel-to-board thermal resistance measured using 150°C Liquid Crystal Measurement method.

Product Consistency Distribution Charts at 2 GHz, 4.5V, 200 mA [5,6]

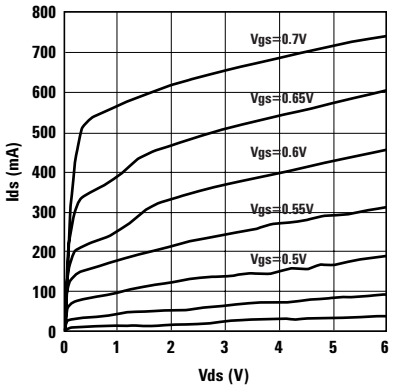


Figure 1. Typical IV curve (Vgs = 0.01V) per step.

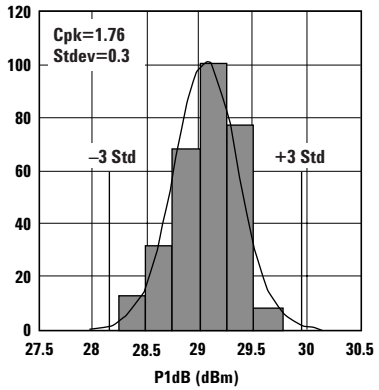


Figure 2. P1dB.

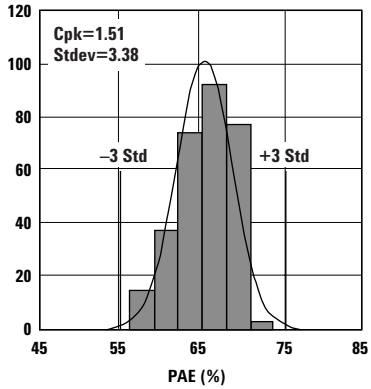


Figure 3. PAE.

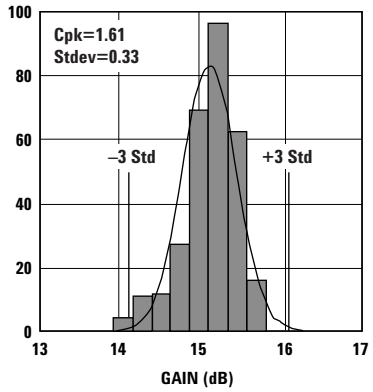


Figure 4. Gain.

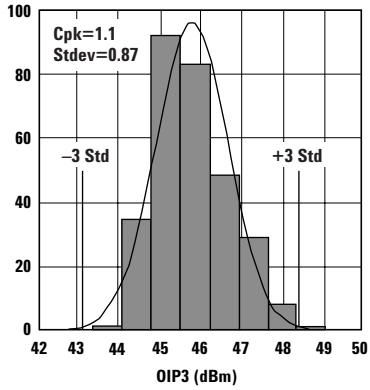


Figure 5. OIP3.

Notes:
5. Distribution data sample size is 300 samples taken from 3 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements are made on production test board, which represents a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

ATF-501P8 Electrical Specifications

T_A = 25°C, DC bias for RF parameters is Vds = 4.5V and Ids = 280 mA unless otherwise specified.

Symbol	Parameter and Test Condition		Units	Min.	Typ.	Max.
Vgs	Operational Gate Voltage	Vds = 4.5V, Ids = 280 mA	V	0.42	0.55	0.67
Vth	Threshold Voltage	Vds = 4.5V, Ids = 32 mA	V	—	0.33	—
Idss	Saturated Drain Current	Vds = 4.5V, Vgs = 0V	µA	—	5	—
Gm	Transconductance	Vds = 4.5V, Gm = ΔIds/ΔVgs; ΔVgs = Vgs1 – Vgs2 Vgs1 = 0.55V, Vgs2 = 0.5V	mmho	—	1872	—
Igss	Gate Leakage Current	Vds = 0V, Vgs = -4.5V	µA	-30	-0.8	—
NF	Noise Figure[1]	f = 2 GHz	dB	—	1	—
		f = 900 MHz	dB	—	—	—
G	Gain[1]	f = 2 GHz	dB	13.5	15	16.5
		f = 900 MHz	dB	—	16.6	—
OIP3	Output 3rd Order Intercept Point[1,2]		f = 2 GHz	dBm	43	45.5 —
		f = 900 MHz	dBm	—	42	—
P1dB	Output 1dB Compressed[1]	f = 2 GHz	dBm	27.5	29	—
		f = 900 MHz	dBm	—	27.3	—
PAE	Power Added Efficiency[1]	f = 2 GHz	%	50	65	—
		f = 900 MHz	%	—	49	—
ACLR	Adjacent Channel Leakage Power Ratio[1,3]	Offset BW = 5 MHz	dBc	—	63.9	—
		Offset BW = 10 MHz	dBc	—	64.1	—

Notes:
1. Measurements at 2 GHz obtained using production test board described in Figure 2 while measurement at 0.9GHz obtained from load pull tuner.
2. i) 2 GHz OIP3 test condition: F1 = 2.0 GHz, F2 = 2.01 GHz and Pin = -5 dBm per tone.
   ii) 900 MHz OIP3 test condition: F1 = 900 MHz, F2 = 910 MHz and Pin = -5dBm per tone.
3. ACLR test spec is based on 3GPP TS 25.141 V5.3.1 (2002-06)
   - Test Model 1
   - Active Channels: PCCPCH + SCH + CPICH + PICH + SCCPCH + 64 DPCH (SF=128)
   - Freq = 2140 MHz
   - Pin = -5 dBm
   - Channel Integrate Bandwidth = 3.84 MHz
4. Use proper bias, board, heatsinking and derating designs to ensure max channel temperature is not exceeded. See absolute max ratings and application note for more details.

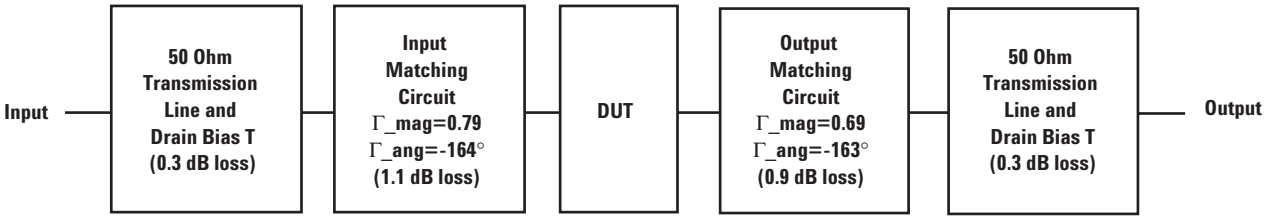


Figure 6. Block diagram of the 2 GHz production test board used for NF, Gain, OIP3 , P1dB and PAE measurements at 2 GHz. This circuit achieves a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

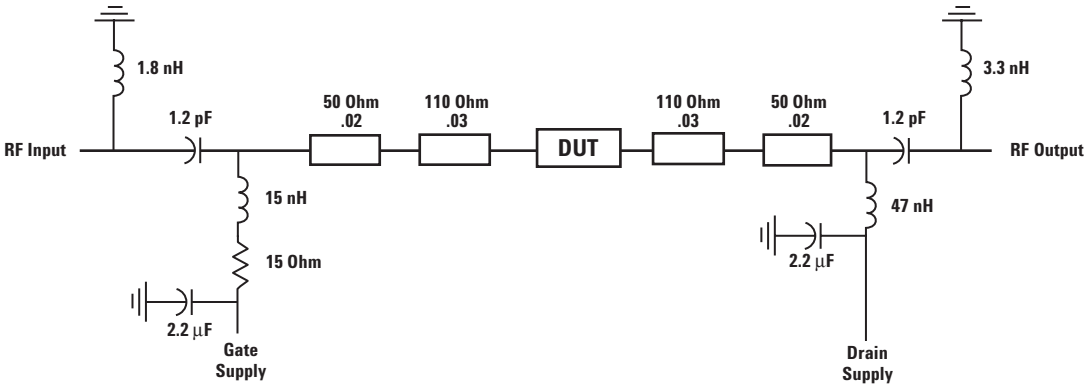


Figure 7. Simplified schematic of production test board. Primary purpose is to show 15 Ohm series resistor placement in gate supply. Transmission line tapers, tee intersections, bias lines and parasitic values are not shown.

Gamma Load and Source at Optimum OIP3 and P1dB Tuning Conditions

The device's optimum OIP3 and P1dB measurements were determined using a load pull system at 4.5V 280 mA and 4.5V 400 mA quiesent bias respectively:

Typical Gammas at Optimum OIP3 at 4.5V 280 mA

	Optimized for maximum OIP3 at 4.5V 280 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	46.42	16.03	26.67	45.80	0.305 < -140	0.577 < 162
2.0	45.50	15.07	28.93	50.30	0.806 < -179.2	0.511 < 164
2.4	44.83	12.97	29.03	45.70	0.756 < -167	0.589 < -168
3.9	43.97	6.11	27.33	33.90	0.782 < -162	0.524 < -153

Typical Gammas at Optimum P1dB at 4.5V 280mA

	Optimized for maximum P1dB at 4.5V 280 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	39.29	20.90	30.49	41.00	0.859 < 165	0.757 < 179
2.0	41.79	14.72	30.60	45.30	0.76 < -171	0.691 < -168
2.4	42.37	11.25	30.24	39.70	0.745 < -166	0.694 < -161
3.9	42.00	5.63	28.26	25.80	0.759 < -159	0.708 < -149

Typical Gammas at Optimum OIP3 at 4.5V 400 mA

	Optimized for maximum OIP3 at 4.5V 400 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	49.15	16.85	27.86	44.20	0.5852 < -135.80	0.4785 < 177.00
2.0	48.18	14.72	29.36	48.89	0.7267 < -175.37	0.7338 < 179.56
2.4	47.54	12.47	29.10	46.83	0.6155 < -171.71	0.5411 < -172.02
3.9	45.44	8.05	28.49	37.02	0.7888 < -148.43	0.5247 < -145.84

Typical Gammas at Optimum P1dB at 4.5V 400 mA

	Optimized for maximum P1dB at 4.5V 400 mA					
Freq (GHz)	**OIP3**	**Gain**	**P1dB**	**PAE**	**Gamma Source**	**Gamma Load**
0.9	41.78	21.84	31.23	49.97	0.7765 < 168.50	0.7589 < -175.09
2.0	43.28	14.83	31.03	44.78	0.8172 < -175.74	0.8011 < -165.75
2.4	42.46	11.90	30.66	41.00	0.8149 < -163.78	0.8042 < -161.79
3.9	42.94	7.70	29.56	33.06	0.8394 < -151.21	0.7826 < -149.00

ATF-501P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3 at 4.5V 280 mA

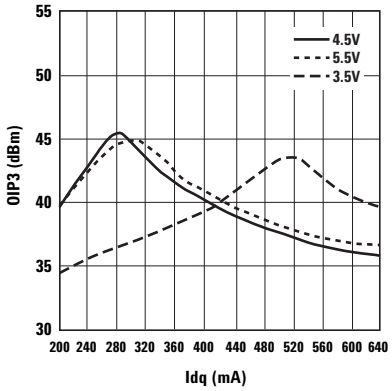


Figure 8. OIP3 vs. Idq and Vds at 2 GHz.

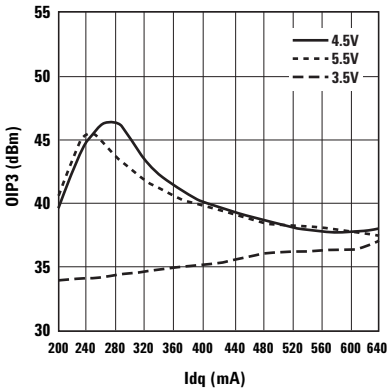


Figure 9. OIP3 vs. Idq and Vds at 0.9 GHz.

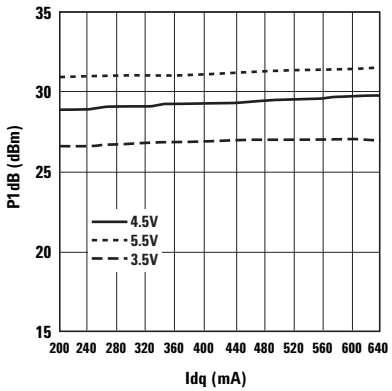


Figure 10. P1dB vs. Idq and Vds at 2 GHz.

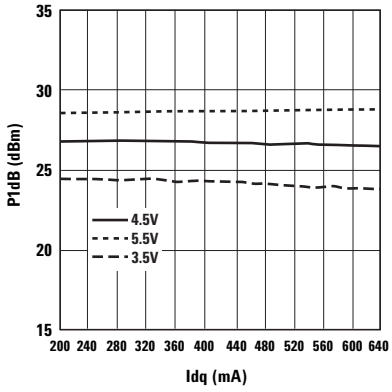


Figure 11. P1dB vs. Idq and Vds at 0.9 GHz.

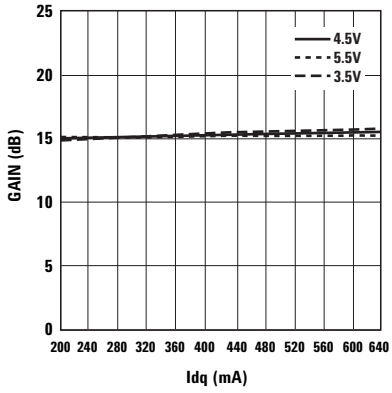


Figure 12. Gain vs. Idq and Vds at 2 GHz.

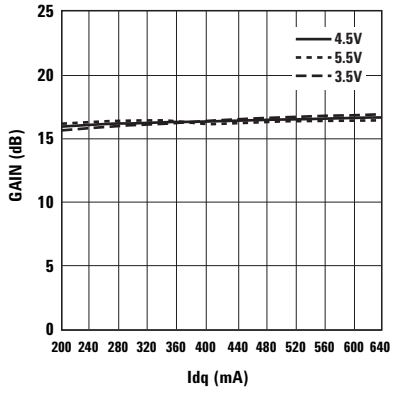


Figure 13. Gain vs. Idq and Vds at 0.9 GHz.

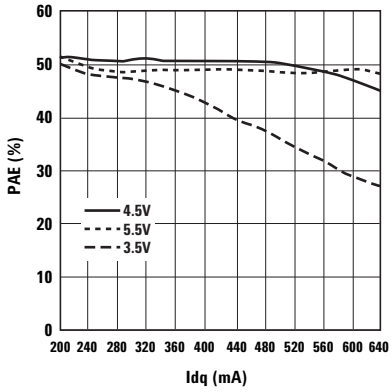


Figure 14. PAE vs. Idq and Vds at 2 GHz.

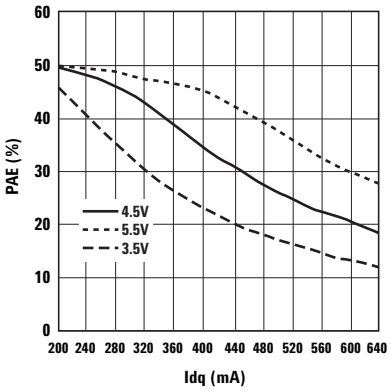


Figure 15. PAE vs. Idq and Vds at 0.9 GHz.

ATF-501P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal P1dB at 4.5V 280 mA

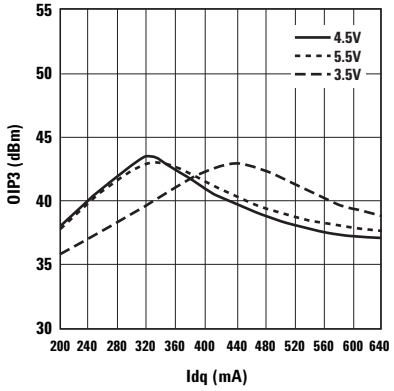


Figure 16. OIP3 vs. Idq and Vds at 2 GHz.

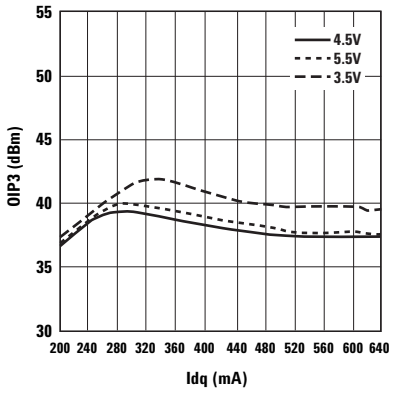


Figure 17. OIP3 vs. Idq and Vds at 0.9 GHz.

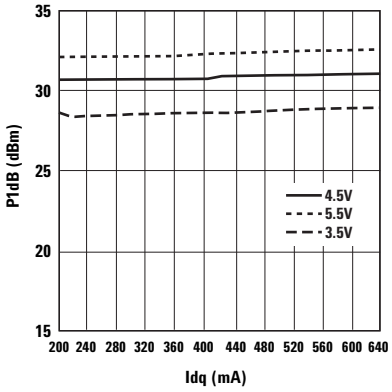


Figure 18. P1dB vs. Idq and Vds at 2 GHz.

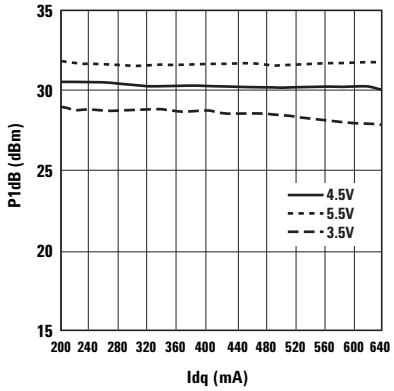


Figure 19. P1dB vs. Idq and Vds at 0.9 GHz.

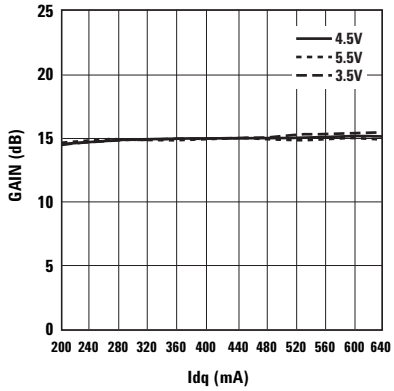


Figure 20. Gain vs. Idq and Vds at 2 GHz.

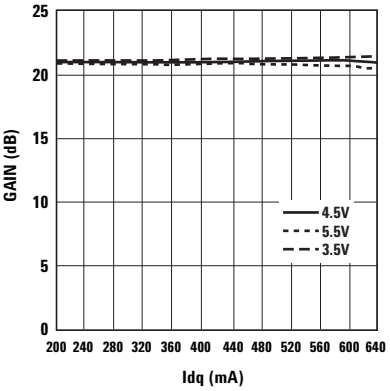


Figure 21. Gain vs. Idq and Vds at 0.9 GHz.

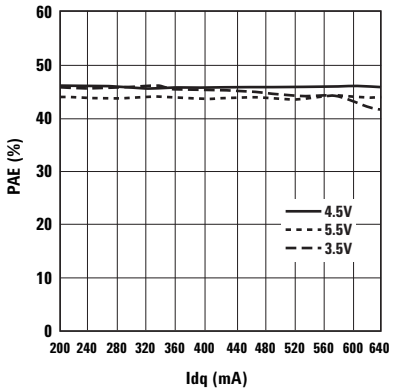


Figure 22. PAE vs. Idq and Vds at 2 GHz.

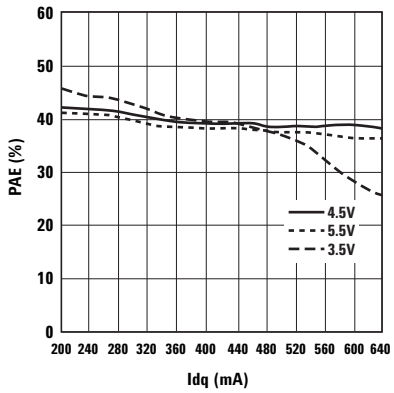


Figure 23. PAE vs. Idq and Vds at 0.9 GHz.

ATF-501P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimum OIP3 at 4.5V 280 mA

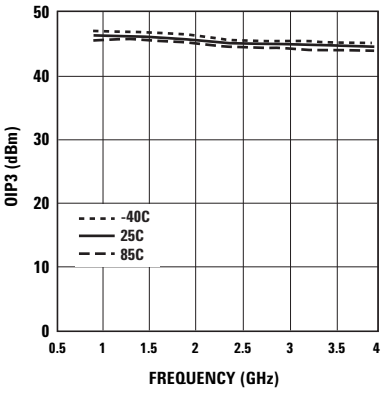


Figure 24. OIP3 vs. Temperature and Frequency at Optimal OIP3.

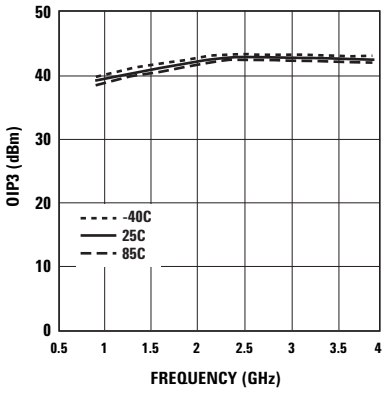


Figure 25. OIP3 vs. Temperature and Frequency at Optimal P1dB.

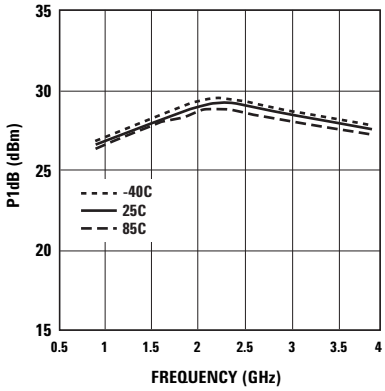


Figure 26. P1dB vs. Temperature and Frequency at Optimal OIP3.

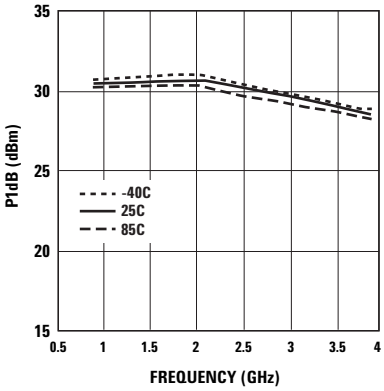


Figure 27. P1dB vs. Temperature and Frequency at Optimal P1dB.

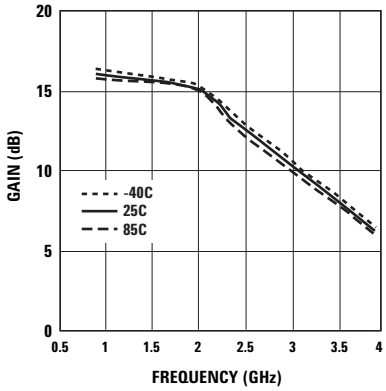


Figure 28. Gain vs. Temperature and Frequency at Optimal OIP3.

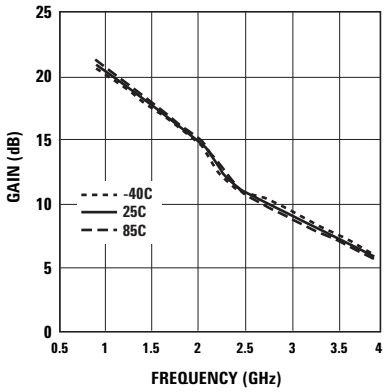


Figure 29. Gain vs. Temperature and Frequency at Optimal P1dB.

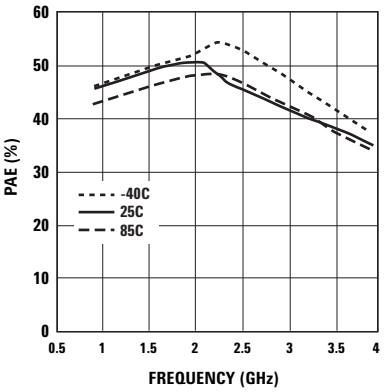


Figure 30. PAE vs. Temperature and Frequency at Optimal OIP3.

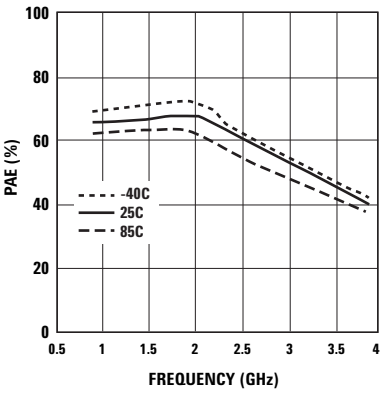


Figure 31. PAE vs. Temperature and Frequency at Optimal P1dB.

ATF-501P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3 at 4.5V 400 mA

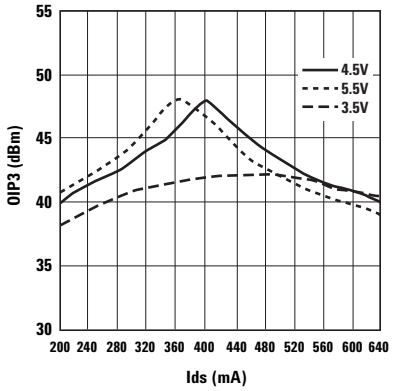


Figure 32. OIP3 vs. Ids and Vds at 2 GHz.

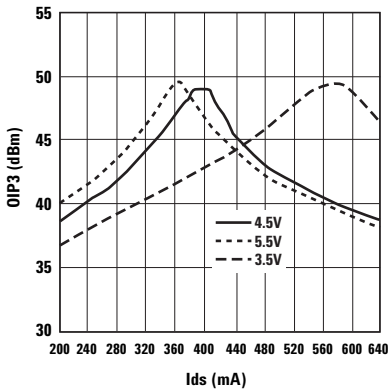


Figure 33. OIP3 vs. Ids and Vds at 900 MHz.

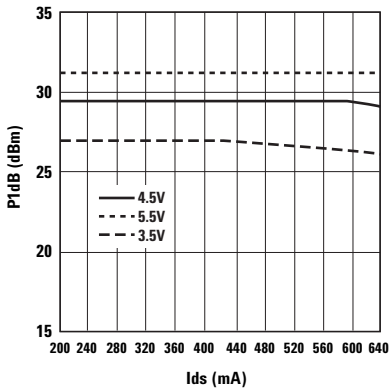


Figure 34. P1dB vs. Ids and Vds at 2 GHz.

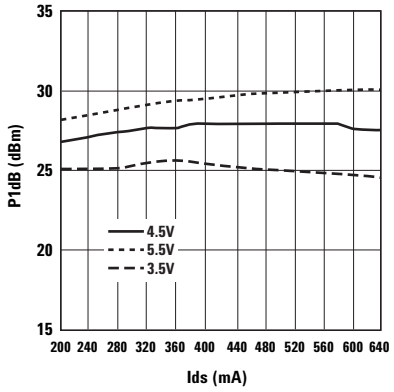


Figure 35. P1dB vs. Ids and Vds at 900 MHz.

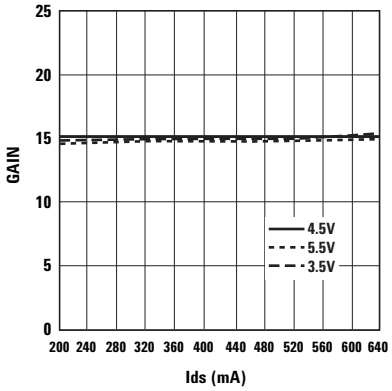


Figure 36. Gain vs. Ids and Vds at 2 GHz.

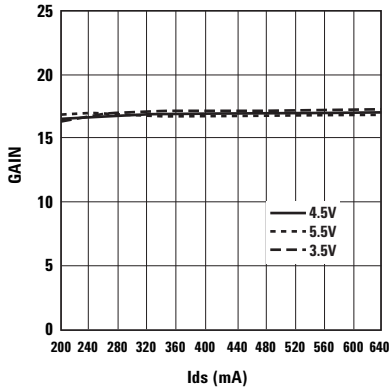


Figure 37. Gain vs. Ids and Vds at 900 MHz.

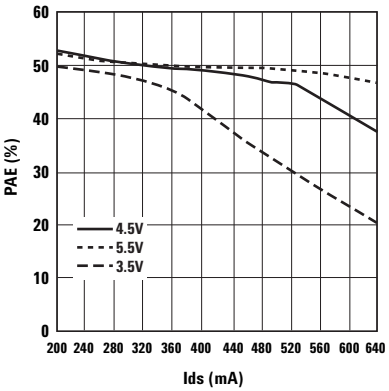


Figure 38. PAE vs. Ids and Vds at 2 GHz.

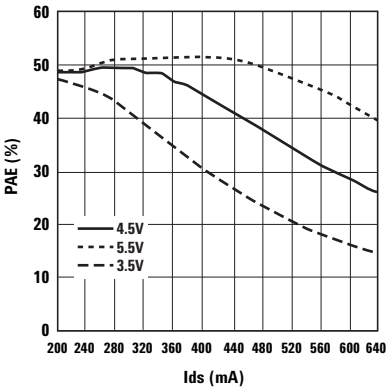


Figure 39. PAE vs. Ids and Vds at 900 MHz.

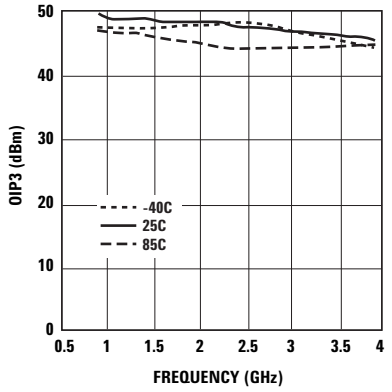


Figure 40. OIP3 vs. Temperature and Frequency at optimum OIP3.

Note:
Bias current (Ids) for the above charts are quiescent conditions.
Actual level may increase or decrease depending on amount of RF drive.

ATF-501P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal OIP3 at 4.5V 400 mA

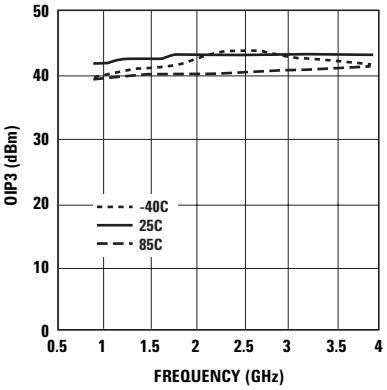


Figure 41. OIP3 vs. Temperature and Frequency at optimum P1dB.

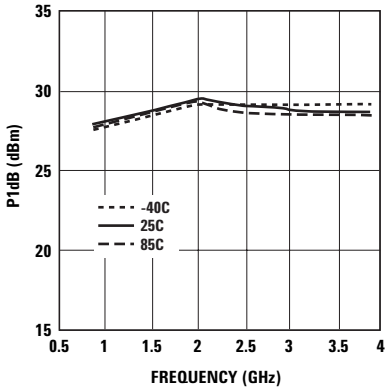


Figure 42. P1dB vs. Temperature and Frequency at optimum OIP3.

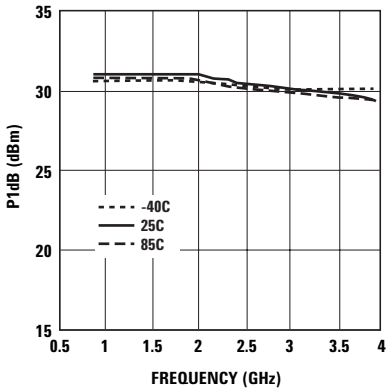


Figure 43. P1dB vs. Temperature and Frequency at optimum P1dB.

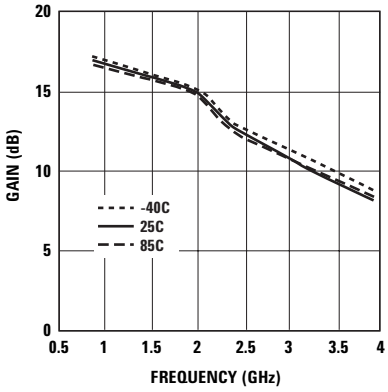


Figure 44. Gain vs. Temperature and Frequency at optimum OIP3.

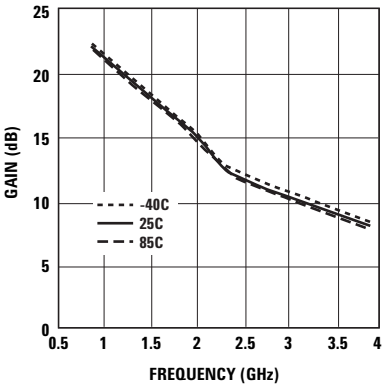


Figure 45. Gain vs. Temperature and Frequency at optimum P1dB.

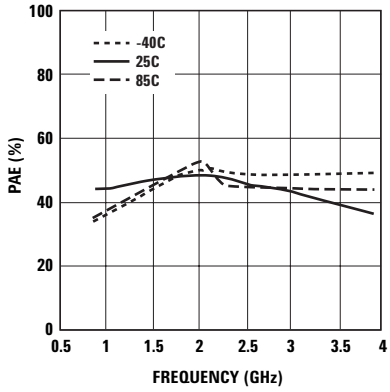


Figure 46. PAE vs. Temperature and Frequency at optimum OIP3.

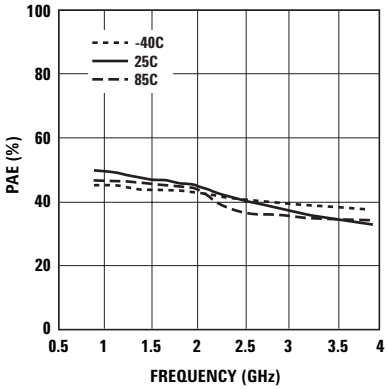


Figure 47. PAE vs. Temperature and Frequency at optimum P1dB.

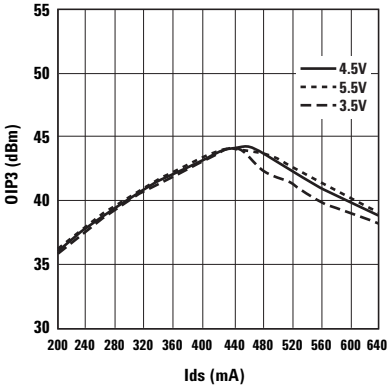


Figure 48. OIP3 vs. Ids and Vds at 2 GHz.

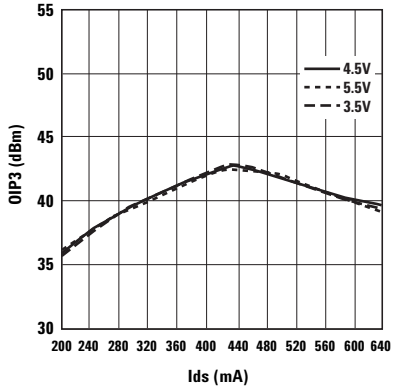


Figure 49. OIP3 vs. Ids and Vds at 900 MHz.

Note:
Bias current (Ids) for the above charts are quiescent conditions.
Actual level may increase or decrease depending on amount of RF drive.

ATF-501P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal P1dB at 4.5V 400 mA

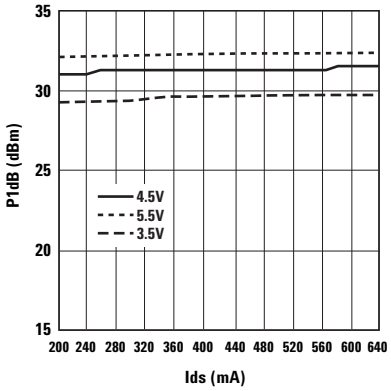


Figure 50. P1dB vs. Ids and Vds at 2 GHz.

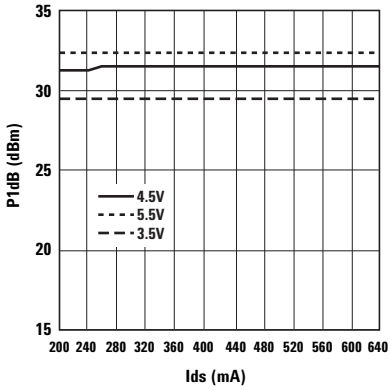


Figure 51. P1dB vs. Ids and Vds at 900 MHz.

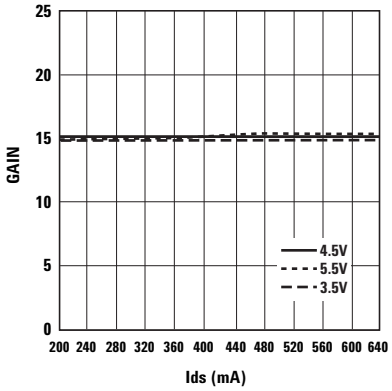


Figure 52. Gain vs. Ids and Vds at 2 GHz.

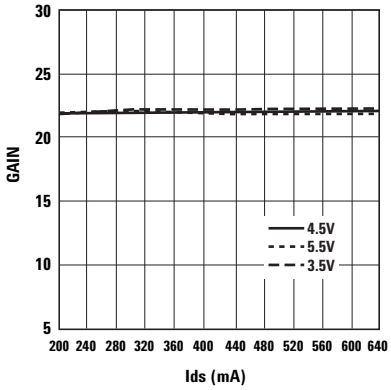


Figure 53. Gain vs. Ids and Vds at 900 MHz.

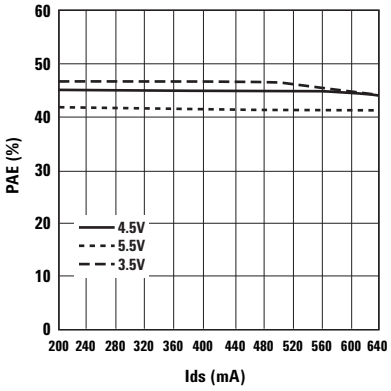


Figure 54. PAE vs. Ids and Vds at 2 GHz.

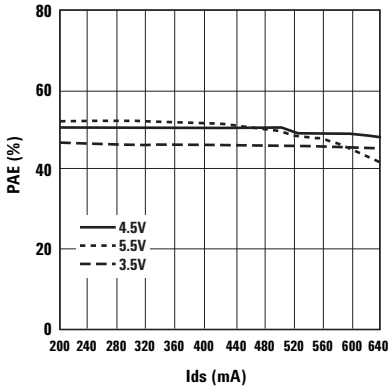


Figure 55. PAE vs. Ids and Vds at 900 MHz.

Note:
Bias current (Ids) for the above charts are quiescent conditions.
Actual level may increase or decrease depending on amount of RF drive.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 4.5V, I_{DS} = 280 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.915	-132.3	31.6	37.990	112.2	-38.4	0.012	29.3	0.647	-160.6	35.0	0.173
0.2	0.911	-156.2	26.2	20.324	99.9	-37.7	0.013	24.0	0.689	-171.1	31.9	0.314
0.3	0.910	-165.4	22.8	13.783	94.5	-37.1	0.014	24.5	0.699	-175.7	29.9	0.436
0.4	0.910	-170.9	20.3	10.342	91.1	-37.1	0.014	27.3	0.702	-178.5	28.7	0.569
0.5	0.908	-173.4	18.7	8.604	88.4	-36.5	0.015	29.6	0.691	-179.9	27.6	0.648
0.6	0.907	-176.1	17.1	7.194	86.1	-35.9	0.016	32.4	0.691	178.5	26.5	0.736
0.7	0.908	-178.5	15.8	6.167	84.1	-35.4	0.017	34.4	0.694	177.2	25.6	0.800
0.8	0.905	179.8	14.7	5.407	82.1	-34.9	0.018	36.3	0.695	175.2	24.8	0.871
0.9	0.909	178.2	13.6	4.799	80.3	-34.4	0.019	38.3	0.692	175.1	24.0	0.906
1	0.909	176.6	12.7	4.308	78.3	-34.0	0.020	39.9	0.692	173.9	23.3	0.953
1.5	0.902	170.5	9.1	2.859	70.3	-31.7	0.026	45.0	0.698	169.4	18.2	1.128
2	0.902	166.0	7.1	2.264	64.4	-30.5	0.030	46.9	0.700	165.6	16.0	1.209
2.5	0.901	165.0	6.6	2.134	63.1	-30.2	0.031	47.2	0.699	163.0	15.4	1.241
3	0.901	161.1	5.0	1.772	57.7	-28.9	0.036	47.4	0.697	159.1	13.8	1.278
4	0.898	155.0	3.0	1.412	49.3	-27.3	0.043	46.5	0.707	153.7	11.7	1.326
5	0.902	145.0	0.9	1.110	37.6	-24.7	0.058	43.5	0.699	146.8	9.7	1.272
6	0.893	134.9	-0.9	0.902	22.6	-22.9	0.072	35.6	0.697	145.3	7.8	1.286
7	0.899	125.8	-3.3	0.687	9.0	-22.2	0.078	27.3	0.652	134.1	5.7	1.394
8	0.895	115.6	-4.4	0.604	-1.1	-20.8	0.091	22.0	0.646	117.4	4.2	1.463
9	0.898	105.5	-5.3	0.542	-13.0	-19.6	0.105	12.3	0.641	115.5	3.2	1.447
10	0.886	95.5	-5.9	0.505	-20.2	-18.9	0.114	9.7	0.695	104.5	2.5	1.455
11	0.868	84.7	-6.6	0.469	-29.7	-17.6	0.132	0.5	0.742	91.3	1.6	1.431
12	0.862	74.0	-8.0	0.398	-40.8	-17.4	0.135	-6.3	0.735	88.1	-0.1	1.661
13	0.847	64.5	-7.9	0.403	-47.5	-16.0	0.159	-12.3	0.766	78.4	-0.1	1.491
14	0.844	55.6	-8.5	0.377	-58.4	-15.3	0.171	-21.3	0.800	68.9	-0.3	1.397
15	0.837	47.4	-9.0	0.354	-67.2	-14.6	0.187	-30.1	0.797	65.6	-1.1	1.414
16	0.824	39.9	-9.7	0.327	-72.0	-14.2	0.194	-36.8	0.763	51.5	-2.3	1.608
17	0.821	31.6	-9.8	0.323	-82.7	-13.4	0.215	-44.6	0.786	38.9	-2.4	1.488
18	0.805	24.6	-10.5	0.298	-90.1	-12.5	0.237	-51.8	0.781	29.5	-3.5	1.575

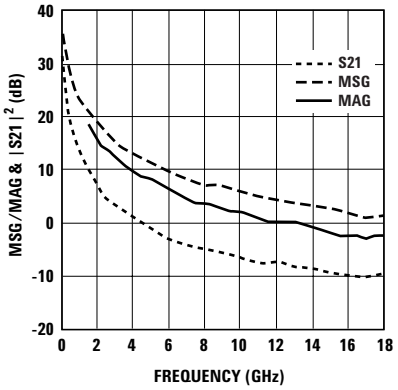


Figure 56. MSG/MAG & $|S21|^2$ vs. Frequency at 4.5V 280mA.

Notes:

1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 4.5V, I_{DS} = 200 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.922	-131.5	31.1	35.978	112.6	-37.7	0.013	28.9	0.664	-159.8	34.4	0.142
0.2	0.914	-155.7	25.7	19.290	100.1	-36.5	0.015	22.4	0.709	-170.7	31.1	0.274
0.3	0.914	-165.2	22.3	13.088	94.7	-36.5	0.015	22.5	0.719	-175.4	29.4	0.390
0.4	0.911	-170.5	19.8	9.814	91.4	-35.9	0.016	24.9	0.722	-178.4	27.9	0.510
0.5	0.911	-173.3	18.3	8.176	88.6	-35.4	0.017	26.8	0.713	-179.9	26.8	0.577
0.6	0.912	-176.0	16.7	6.834	86.4	-34.9	0.018	29.3	0.713	178.6	25.8	0.653
0.7	0.910	-178.3	15.4	5.861	84.3	-34.4	0.019	31.3	0.716	177.2	24.9	0.725
0.8	0.910	179.9	14.2	5.141	82.3	-34.4	0.019	33.0	0.718	175.5	24.3	0.801
0.9	0.913	178.4	13.2	4.558	80.5	-34.0	0.020	34.9	0.712	175.0	23.6	0.840
1	0.910	176.8	12.2	4.092	78.7	-33.6	0.021	36.6	0.714	173.8	22.9	0.903
1.5	0.904	170.5	8.7	2.718	70.5	-31.4	0.027	41.7	0.721	169.0	18.3	1.077
2	0.905	166.1	6.7	2.153	64.9	-30.2	0.031	44.2	0.721	165.2	16.0	1.161
2.5	0.905	165.2	6.1	2.027	63.7	-29.9	0.032	44.5	0.719	162.5	15.4	1.188
3	0.906	161.1	4.5	1.684	58.3	-28.6	0.037	44.9	0.715	158.5	13.7	1.227
4	0.905	154.9	2.6	1.354	50.3	-27.1	0.044	44.3	0.725	152.9	11.8	1.262
5	0.904	145.1	0.4	1.053	38.5	-24.7	0.058	41.6	0.716	145.7	9.5	1.271
6	0.899	134.9	-1.3	0.863	23.9	-22.9	0.072	34.1	0.712	144.1	7.7	1.263
7	0.905	126.0	-3.6	0.661	10.5	-22.2	0.078	26.0	0.660	132.9	5.6	1.371
8	0.902	115.8	-4.6	0.587	0.3	-20.8	0.091	20.8	0.654	116.3	4.2	1.423
9	0.900	106.4	-5.6	0.527	-11.1	-19.6	0.105	11.1	0.649	114.4	3.0	1.451
10	0.894	95.9	-6.1	0.498	-17.7	-18.9	0.114	8.4	0.700	103.4	2.6	1.412
11	0.882	84.9	-7.0	0.448	-26.8	-17.7	0.130	-0.9	0.746	90.5	1.6	1.407
12	0.873	74.3	-8.1	0.393	-38.8	-17.5	0.133	-7.5	0.738	87.3	0.1	1.614
13	0.856	64.6	-8.1	0.393	-45.4	-16.1	0.156	-13.1	0.768	77.8	-0.1	1.492
14	0.853	56.0	-8.4	0.380	-55.0	-15.6	0.166	-21.4	0.800	68.4	-0.2	1.399
15	0.837	47.4	-8.8	0.361	-64.1	-14.8	0.182	-29.6	0.799	65.2	-1.0	1.439
16	0.829	40.6	-9.2	0.345	-72.0	-14.4	0.190	-35.9	0.763	51.1	-1.8	1.556
17	0.828	32.7	-9.5	0.336	-80.5	-13.4	0.213	-43.3	0.787	38.5	-2.0	1.449
18	0.807	26.1	-10.2	0.310	-88.2	-12.5	0.236	-50.5	0.782	29.1	-3.2	1.542

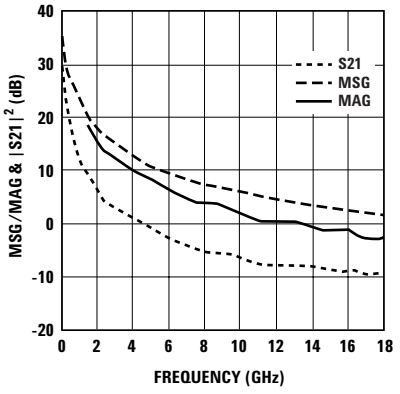


Figure 57. MSG/MAG & $|S21|^2$ vs. Frequency at 4.5V 200mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 4.5V, I_{DS} = 360 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.911	-132.8	31.6	38.110	112.4	-39.2	0.011	30.3	0.649	-162.1	35.4	0.200
0.2	0.910	-156.5	26.2	20.415	100.0	-38.4	0.012	24.9	0.692	-171.8	32.3	0.340
0.3	0.911	-165.8	22.8	13.848	94.6	-37.7	0.013	26.2	0.701	-176.2	30.3	0.472
0.4	0.913	-171.1	20.3	10.397	91.3	-37.7	0.013	28.9	0.704	-178.9	29.0	0.600
0.5	0.907	-173.7	18.7	8.640	88.5	-36.5	0.015	31.8	0.693	179.7	27.6	0.679
0.6	0.910	-176.3	17.2	7.232	86.2	-35.9	0.016	34.5	0.694	178.2	26.6	0.747
0.7	0.910	-178.6	15.8	6.200	84.2	-35.9	0.016	36.8	0.696	176.9	25.9	0.838
0.8	0.906	179.7	14.7	5.431	82.2	-35.4	0.017	38.8	0.697	175.6	25.0	0.914
0.9	0.913	178.0	13.7	4.826	80.3	-34.9	0.018	40.6	0.695	174.8	24.3	0.930
1	0.907	176.4	12.7	4.328	78.4	-34.0	0.020	42.3	0.694	173.7	23.4	0.984
1.5	0.904	170.3	9.2	2.878	70.4	-32.0	0.025	47.0	0.698	169.4	18.2	1.154
2	0.906	165.9	7.1	2.275	64.5	-30.5	0.030	48.7	0.702	165.5	16.1	1.193
2.5	0.904	164.8	6.6	2.146	63.2	-30.2	0.031	49.0	0.701	162.8	15.5	1.231
3	0.907	160.9	5.0	1.783	57.9	-28.9	0.036	49.0	0.699	159.0	14.0	1.246
4	0.906	154.7	3.1	1.424	49.4	-27.3	0.043	47.7	0.708	153.6	12.0	1.275
5	0.903	144.8	0.9	1.114	37.7	-24.7	0.058	44.2	0.701	146.7	9.7	1.268
6	0.896	134.7	-0.8	0.907	22.7	-22.7	0.073	36.2	0.699	145.1	7.9	1.256
7	0.903	125.6	-3.2	0.691	8.9	-22.2	0.078	27.9	0.654	134.0	5.9	1.355
8	0.903	115.0	-4.3	0.612	-1.0	-20.7	0.092	22.4	0.647	117.3	4.6	1.375
9	0.891	105.6	-5.3	0.544	-13.3	-19.5	0.106	12.8	0.642	115.4	2.9	1.495
10	0.885	94.9	-6.0	0.504	-20.0	-18.8	0.115	10.2	0.697	104.4	2.4	1.462
11	0.873	84.3	-6.7	0.465	-28.4	-17.5	0.133	0.9	0.743	91.3	1.6	1.416
12	0.866	74.0	-7.9	0.403	-41.1	-17.3	0.137	-5.8	0.735	87.9	0.1	1.607
13	0.849	64.3	-7.8	0.406	-47.3	-15.9	0.161	-12.1	0.768	78.3	0.0	1.464
14	0.849	55.7	-8.4	0.379	-57.9	-15.2	0.174	-21.3	0.801	68.8	-0.2	1.361
15	0.841	46.6	-9.0	0.353	-69.0	-14.5	0.189	-30.3	0.800	65.5	-0.9	1.376
16	0.828	39.0	-9.4	0.337	-73.1	-14.2	0.196	-37.1	0.763	51.4	-2.0	1.547
17	0.817	31.0	-9.8	0.322	-83.0	-13.2	0.218	-45.1	0.787	38.7	-2.4	1.491
18	0.809	23.9	-10.3	0.304	-92.7	-12.4	0.240	-52.4	0.783	29.3	-3.2	1.513

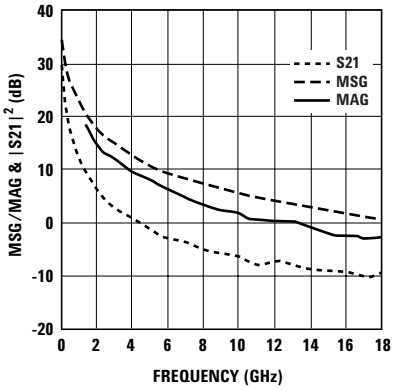


Figure 58. MSG/MAG & $|S21|^2$ vs. Frequency at 4.5V 360mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 3.5V, I_{DS} = 280 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.923	-133.9	30.6	34.047	111.6	-38.4	0.012	28.8	0.716	-164.7	34.5	0.166
0.2	0.922	-157.1	25.2	18.161	99.7	-37.7	0.013	23.8	0.759	-173.4	31.5	0.301
0.3	0.920	-166.1	21.8	12.313	94.5	-37.1	0.014	25.0	0.767	-177.3	29.4	0.427
0.4	0.920	-171.3	19.3	9.220	91.4	-37.1	0.014	27.5	0.770	-179.8	28.2	0.549
0.5	0.915	-173.9	17.7	7.674	88.7	-35.9	0.016	30.0	0.760	178.8	26.8	0.622
0.6	0.917	-176.5	16.2	6.429	86.6	-35.4	0.017	32.9	0.761	177.2	25.8	0.697
0.7	0.917	-178.9	14.8	5.511	84.6	-34.9	0.018	34.8	0.762	175.8	24.9	0.761
0.8	0.915	179.6	13.6	4.813	82.8	-34.9	0.018	37.2	0.760	175.0	24.3	0.843
0.9	0.918	177.7	12.7	4.302	81.0	-34.4	0.019	38.8	0.764	173.7	23.5	0.877
1	0.913	176.4	11.7	3.850	79.1	-33.6	0.021	40.5	0.759	172.4	22.6	0.930
1.5	0.913	170.4	8.1	2.555	72.0	-31.4	0.027	45.6	0.759	168.1	18.1	1.070
2	0.913	166.1	6.1	2.025	66.3	-30.2	0.031	47.1	0.763	163.9	15.9	1.139
2.5	0.910	164.8	5.6	1.912	65.1	-29.9	0.032	47.6	0.762	161.0	15.2	1.181
3	0.913	160.9	4.0	1.588	60.4	-28.6	0.037	47.5	0.758	156.7	13.6	1.206
4	0.906	154.6	2.1	1.276	52.2	-26.9	0.045	45.9	0.762	150.9	11.5	1.261
5	0.910	144.7	0.1	1.012	41.6	-24.4	0.060	42.4	0.754	143.3	9.4	1.226
6	0.903	134.6	-1.6	0.827	27.2	-22.5	0.075	34.3	0.742	141.3	7.5	1.239
7	0.907	125.4	-3.9	0.636	14.0	-22.0	0.079	25.3	0.674	130.1	5.3	1.402
8	0.903	115.2	-4.9	0.570	5.1	-20.6	0.093	19.8	0.669	113.5	3.9	1.448
9	0.897	105.5	-5.6	0.522	-7.0	-19.4	0.107	9.9	0.666	112.0	2.8	1.484
10	0.889	94.8	-6.0	0.499	-14.5	-18.8	0.115	7.0	0.709	100.9	2.4	1.458
11	0.880	84.2	-6.4	0.477	-23.6	-17.7	0.131	-2.4	0.754	88.2	1.9	1.378
12	0.870	73.4	-7.7	0.411	-33.8	-17.6	0.132	-9.1	0.745	85.0	0.3	1.614
13	0.847	63.8	-7.5	0.421	-41.1	-16.3	0.153	-14.5	0.770	75.9	0.1	1.519
14	0.839	55.1	-8.0	0.397	-52.2	-15.8	0.163	-22.5	0.801	66.5	-0.1	1.458
15	0.816	47.3	-8.2	0.390	-63.9	-15.0	0.178	-30.0	0.795	63.4	-0.8	1.495
16	0.808	39.8	-9.2	0.345	-70.3	-14.6	0.186	-35.9	0.755	49.5	-2.3	1.727
17	0.794	32.3	-9.0	0.354	-81.5	-13.5	0.211	-43.3	0.787	36.6	-2.1	1.538
18	0.769	26.0	-9.7	0.329	-91.7	-12.6	0.234	-50.7	0.777	27.7	-3.2	1.632

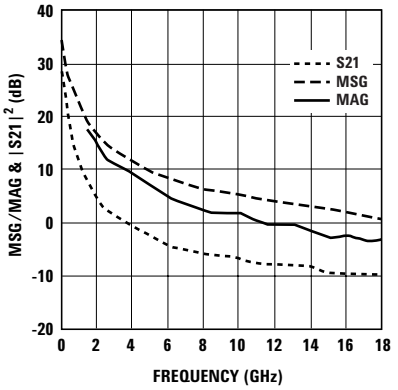


Figure 59. MSG/MAG & $|S21|^2$ vs. Frequency at 3.5V 280mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 3.5V, I_{DS} = 200 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.924	-132.7	30.5	33.400	112.1	-37.1	0.014	28.4	0.703	-162.3	33.8	0.150
0.2	0.919	-156.5	25.0	17.862	99.9	-36.5	0.015	22.1	0.749	-172.1	30.8	0.269
0.3	0.918	-165.7	21.7	12.118	94.6	-36.5	0.015	22.7	0.757	-176.5	29.1	0.390
0.4	0.918	-171.0	19.2	9.080	91.4	-35.9	0.016	24.6	0.760	-179.2	27.5	0.496
0.5	0.918	-173.6	17.6	7.556	88.7	-35.4	0.017	26.4	0.751	179.4	26.5	0.559
0.6	0.915	-176.2	16.0	6.328	86.5	-34.9	0.018	29.3	0.752	177.7	25.5	0.651
0.7	0.915	-178.5	14.7	5.422	84.5	-34.4	0.019	31.3	0.753	176.3	24.6	0.717
0.8	0.914	179.8	13.5	4.739	82.7	-34.0	0.020	33.2	0.752	175.3	23.7	0.777
0.9	0.919	178.0	12.5	4.232	80.8	-33.6	0.021	35.1	0.755	174.1	23.0	0.806
1	0.916	176.7	11.6	3.788	79.0	-33.2	0.022	36.7	0.750	172.8	22.4	0.870
1.5	0.912	170.5	8.0	2.515	71.5	-31.4	0.027	42.0	0.750	168.3	18.2	1.057
1.9	0.911	166.0	6.0	1.991	65.8	-29.9	0.032	44.3	0.755	165.0	15.8	1.126
2	0.910	164.9	5.5	1.882	64.7	-29.6	0.033	44.7	0.753	164.2	15.2	1.157
2.4	0.911	160.9	3.9	1.562	59.7	-28.6	0.037	45.0	0.750	161.3	13.5	1.215
3	0.909	154.7	2.0	1.255	51.5	-26.9	0.045	43.9	0.754	157.0	11.5	1.244
4	0.911	144.8	-0.1	0.988	40.4	-24.4	0.060	41.0	0.746	151.3	9.3	1.225
5	0.902	134.8	-1.8	0.813	25.9	-22.6	0.074	33.3	0.735	143.7	7.4	1.255
6	0.904	125.5	-4.1	0.624	12.7	-22.0	0.079	24.6	0.669	141.8	5.0	1.438
7	0.904	115.6	-5.1	0.555	3.9	-20.6	0.093	19.3	0.664	130.6	3.8	1.455
8	0.901	105.6	-5.9	0.509	-8.3	-19.4	0.107	9.5	0.662	113.9	2.7	1.466
9	0.897	95.4	-6.4	0.477	-14.5	-18.8	0.115	6.6	0.705	112.3	2.3	1.437
10	0.880	84.1	-6.9	0.450	-23.9	-17.7	0.130	-3.0	0.751	101.2	1.5	1.429
11	0.872	73.7	-8.1	0.393	-34.0	-17.6	0.132	-9.7	0.742	88.5	0.0	1.646
12	0.849	64.2	-7.8	0.408	-42.5	-16.4	0.152	-14.9	0.767	85.3	0.0	1.539
13	0.841	55.5	-8.2	0.391	-53.2	-15.8	0.162	-22.8	0.798	76.2	-0.2	1.465
14	0.820	47.1	-8.5	0.377	-63.5	-15.1	0.176	-29.9	0.793	66.8	-1.0	1.527
15	0.809	39.3	-9.0	0.354	-69.5	-14.7	0.185	-35.9	0.754	63.6	-2.1	1.708
16	0.794	32.7	-9.1	0.350	-84.1	-13.6	0.210	-43.1	0.785	49.8	-2.1	1.543
17	0.770	25.8	-9.6	0.332	-89.0	-12.6	0.234	-50.5	0.776	36.9	-3.1	1.634
18	0.766	21.5	-9.2	0.346	-99.8	-11.5	0.266	-60.7	0.797	28.0	-2.6	1.394

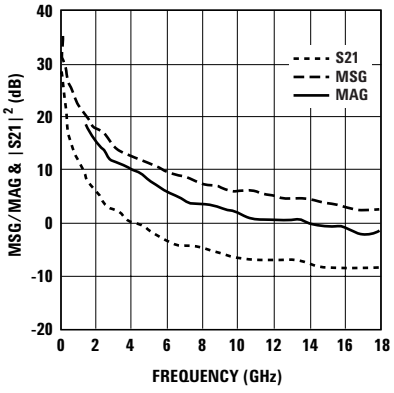


Figure 60. MSG/MAG & $|S21|^2$ vs. Frequency at 3.5V 200mA.

Notes:

1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 3.5V, I_{DS} = 360 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.919	-134.2	30.8	34.576	111.7	-39.2	0.011	29.6	0.722	-166.1	35.0	0.191
0.2	0.920	-157.3	25.3	18.445	99.7	-38.4	0.012	25.5	0.763	-174.1	31.9	0.336
0.3	0.921	-166.4	21.9	12.499	94.6	-37.7	0.013	26.7	0.771	-177.8	29.8	0.460
0.4	0.918	-171.4	19.4	9.372	91.5	-37.7	0.013	30.0	0.773	179.8	28.6	0.599
0.5	0.915	-174.0	17.8	7.792	88.8	-36.5	0.015	32.7	0.763	178.6	27.2	0.665
0.6	0.916	-176.7	16.3	6.537	86.6	-35.9	0.016	35.7	0.765	176.9	26.1	0.744
0.7	0.916	-178.9	15.0	5.596	84.7	-35.4	0.017	37.9	0.765	175.6	25.2	0.809
0.8	0.914	179.4	13.8	4.888	83.1	-34.9	0.018	40.0	0.764	174.9	24.3	0.871
0.9	0.919	178.1	12.8	4.370	81.1	-34.4	0.019	41.8	0.768	173.4	23.6	0.892
1	0.914	176.2	11.8	3.911	79.3	-34.0	0.020	43.0	0.762	172.2	22.9	0.963
1.5	0.912	170.2	8.3	2.596	72.2	-31.7	0.026	47.8	0.761	168.1	18.0	1.103
2	0.914	165.8	6.3	2.059	66.7	-30.2	0.031	49.2	0.766	163.8	15.9	1.142
2.5	0.910	164.7	5.8	1.940	65.6	-29.9	0.032	49.3	0.765	160.9	15.2	1.185
3	0.912	160.8	4.2	1.618	60.7	-28.6	0.037	49.0	0.761	156.6	13.6	1.210
4	0.913	154.4	2.3	1.296	52.9	-26.9	0.045	47.3	0.765	150.8	11.8	1.221
5	0.908	144.7	0.2	1.023	42.0	-24.4	0.060	43.2	0.756	143.0	9.4	1.236
6	0.903	134.5	-1.5	0.844	27.9	-22.5	0.075	34.8	0.745	141.1	7.6	1.233
7	0.906	125.5	-3.8	0.647	15.0	-21.9	0.080	25.7	0.676	129.9	5.3	1.392
8	0.904	115.1	-4.7	0.582	5.9	-20.6	0.093	20.3	0.670	113.3	4.1	1.430
9	0.902	105.3	-5.5	0.532	-6.4	-19.4	0.107	10.3	0.666	111.6	3.1	1.433
10	0.893	95.0	-5.8	0.513	-13.3	-18.8	0.115	7.5	0.710	100.7	2.7	1.416
11	0.881	84.1	-6.5	0.474	-22.0	-17.7	0.131	-1.9	0.756	88.2	1.9	1.388
12	0.873	73.6	-7.6	0.417	-32.9	-17.5	0.133	-8.5	0.746	84.9	0.5	1.577
13	0.847	63.9	-7.5	0.424	-40.6	-16.2	0.154	-13.9	0.772	75.7	0.2	1.507
14	0.844	55.4	-7.8	0.407	-52.7	-15.7	0.165	-22.0	0.802	66.3	0.1	1.407
15	0.827	47.4	-8.2	0.389	-63.7	-14.9	0.180	-29.7	0.793	63.2	-0.7	1.457
16	0.818	40.2	-8.9	0.357	-67.9	-14.6	0.187	-35.8	0.759	49.4	-1.9	1.637
17	0.799	32.9	-9.0	0.353	-81.4	-13.5	0.211	-43.1	0.786	36.5	-2.0	1.526
18	0.780	26.7	-9.3	0.344	-90.7	-12.5	0.236	-50.4	0.777	27.6	-2.7	1.549

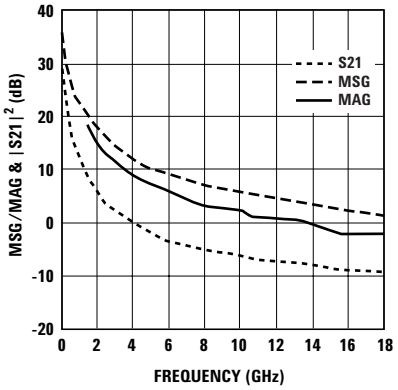


Figure 61. MSG/MAG & $|S21|^2$ vs. Frequency at 3.5V 360mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 5.5V, I_{DS} = 280 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.914	-131.5	31.8	39.087	112.6	-38.4	0.012	29.6	0.618	-158.7	35.1	0.172
0.2	0.912	-155.7	26.4	20.961	100.1	-37.7	0.013	23.9	0.661	-170.0	32.1	0.307
0.3	0.914	-165.2	23.1	14.228	94.5	-37.1	0.014	24.1	0.670	-174.9	30.1	0.420
0.4	0.913	-170.5	20.6	10.678	91.1	-37.1	0.014	26.7	0.674	-177.9	28.8	0.550
0.5	0.909	-173.3	19.0	8.871	88.3	-36.5	0.015	29.0	0.662	-179.3	27.7	0.638
0.6	0.910	-176.0	17.4	7.417	86.0	-35.9	0.016	31.7	0.663	179.2	26.7	0.715
0.7	0.911	-178.2	16.1	6.365	83.9	-35.4	0.017	34.3	0.666	177.8	25.7	0.782
0.8	0.908	-179.8	14.9	5.577	81.8	-34.9	0.018	36.0	0.667	176.3	24.9	0.850
0.9	0.913	178.4	13.9	4.956	79.9	-34.4	0.019	38.0	0.664	175.7	24.2	0.878
1	0.907	176.7	13.0	4.446	78.0	-34.0	0.020	39.4	0.664	174.5	23.5	0.958
1.5	0.903	170.5	9.4	2.951	69.6	-32.0	0.025	44.5	0.672	170.1	18.4	1.141
2	0.905	166.2	7.4	2.331	63.5	-30.5	0.030	46.4	0.674	166.5	16.3	1.182
2.5	0.903	165.2	6.8	2.197	62.1	-30.2	0.031	47.0	0.674	164.0	15.7	1.222
3	0.903	161.0	5.2	1.822	56.7	-29.1	0.035	47.3	0.672	160.3	14.0	1.284
4	0.900	154.7	3.3	1.455	47.9	-27.3	0.043	46.7	0.685	155.2	12.0	1.307
5	0.902	145.0	1.1	1.129	35.9	-24.9	0.057	43.8	0.679	148.6	9.8	1.278
6	0.895	134.9	-0.8	0.916	20.6	-23.0	0.071	36.2	0.681	147.0	8.0	1.271
7	0.903	125.8	-3.2	0.695	6.8	-22.3	0.077	28.3	0.648	135.8	6.1	1.340
8	0.898	115.4	-4.2	0.616	-3.5	-20.8	0.091	22.9	0.641	119.2	4.5	1.401
9	0.898	105.8	-5.3	0.546	-16.3	-19.6	0.105	13.3	0.636	117.2	3.3	1.416
10	0.884	95.4	-6.0	0.499	-23.2	-18.9	0.114	10.9	0.694	106.2	2.4	1.459
11	0.871	84.6	-6.8	0.458	-31.5	-17.6	0.132	1.6	0.741	92.7	1.6	1.420
12	0.864	74.2	-8.3	0.386	-43.6	-17.3	0.137	-5.2	0.731	89.5	-0.2	1.655
13	0.849	64.8	-8.3	0.385	-49.9	-15.8	0.162	-11.5	0.768	79.6	-0.3	1.479
14	0.854	56.1	-8.7	0.366	-60.4	-15.2	0.174	-20.9	0.804	70.2	-0.2	1.332
15	0.841	47.7	-9.6	0.330	-68.9	-14.4	0.191	-29.9	0.807	66.7	-1.3	1.385
16	0.834	40.0	-10.0	0.317	-73.5	-14.1	0.198	-37.0	0.768	52.4	-2.3	1.536
17	0.824	31.9	-10.2	0.310	-83.2	-13.2	0.219	-45.0	0.792	39.7	-2.5	1.466
18	0.813	24.7	-10.7	0.291	-88.9	-12.4	0.240	-52.2	0.788	30.0	-3.5	1.533

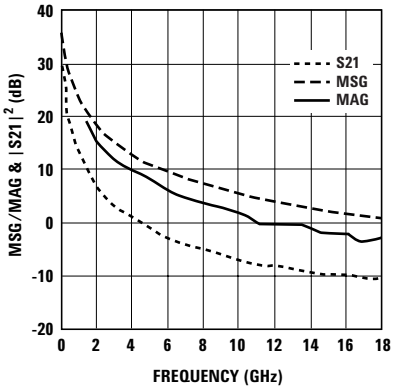


Figure 62. MSG/MAG & $|S21|^2$ vs. Frequency at 5.5V 280mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 5.5V, I_{DS} = 200 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.921	-130.1	31.8	38.725	113.1	-37.7	0.013	29.6	0.615	-156.5	34.7	0.145
0.2	0.914	-155.0	26.4	20.822	100.3	-37.1	0.014	22.8	0.659	-168.9	31.7	0.274
0.3	0.914	-164.6	23.0	14.136	94.7	-36.5	0.015	22.7	0.669	-174.1	29.7	0.385
0.4	0.913	-170.1	20.5	10.611	91.3	-36.5	0.015	24.9	0.673	-177.3	28.5	0.510
0.5	0.909	-172.9	18.9	8.824	88.4	-35.4	0.017	26.8	0.662	-178.9	27.2	0.576
0.6	0.909	-175.7	17.4	7.375	86.0	-35.4	0.017	29.4	0.662	179.6	26.4	0.672
0.7	0.909	-178.1	16.0	6.329	83.9	-34.9	0.018	31.3	0.665	178.2	25.5	0.739
0.8	0.908	-179.7	14.9	5.549	81.8	-34.4	0.019	32.9	0.667	176.5	24.7	0.798
0.9	0.911	178.5	13.8	4.922	80.0	-34.0	0.020	35.3	0.662	176.0	23.9	0.843
1	0.909	176.8	12.9	4.418	78.0	-33.6	0.021	36.4	0.664	174.8	23.2	0.897
1.5	0.905	170.8	9.3	2.933	69.4	-31.7	0.026	41.7	0.673	170.3	18.8	1.079
2	0.907	166.3	7.3	2.322	63.4	-30.5	0.030	44.3	0.674	166.6	16.5	1.153
2.5	0.903	165.3	6.8	2.182	62.1	-30.2	0.031	44.5	0.673	164.1	15.7	1.208
3	0.906	161.2	5.2	1.815	56.5	-28.9	0.036	45.1	0.671	160.4	14.2	1.226
4	0.903	155.0	3.2	1.447	47.8	-27.3	0.043	44.7	0.684	155.3	12.1	1.273
5	0.904	145.1	1.0	1.123	35.9	-24.9	0.057	42.3	0.678	148.7	9.9	1.257
6	0.899	135.2	-0.8	0.909	20.3	-23.0	0.071	35.1	0.681	147.2	8.2	1.235
7	0.904	126.2	-3.2	0.693	6.5	-22.4	0.076	27.4	0.647	136.0	6.2	1.332
8	0.901	115.6	-4.3	0.608	-4.0	-20.9	0.090	22.2	0.640	119.4	4.6	1.386
9	0.896	106.2	-5.4	0.536	-15.9	-19.7	0.104	12.6	0.634	117.5	3.1	1.459
10	0.891	95.4	-6.1	0.497	-23.9	-18.9	0.113	10.2	0.692	106.3	2.6	1.408
11	0.877	85.0	-7.0	0.446	-32.3	-17.7	0.131	1.0	0.739	92.9	1.5	1.403
12	0.871	74.4	-8.3	0.386	-42.5	-17.4	0.135	-5.8	0.730	89.7	-0.1	1.625
13	0.851	64.9	-8.2	0.387	-49.0	-15.9	0.160	-11.8	0.767	79.8	-0.3	1.480
14	0.850	56.2	-8.8	0.364	-60.0	-15.3	0.172	-21.0	0.803	70.5	-0.3	1.364
15	0.839	48.0	-9.5	0.335	-67.9	-14.5	0.188	-29.9	0.805	66.9	-1.3	1.403
16	0.834	39.7	-10.2	0.309	-72.5	-14.2	0.195	-36.8	0.768	52.7	-2.5	1.585
17	0.827	32.2	-10.2	0.309	-82.4	-13.3	0.216	-44.6	0.792	39.9	-2.5	1.472
18	0.814	24.4	-10.5	0.298	-89.4	-12.5	0.238	-51.8	0.790	30.2	-3.2	1.510

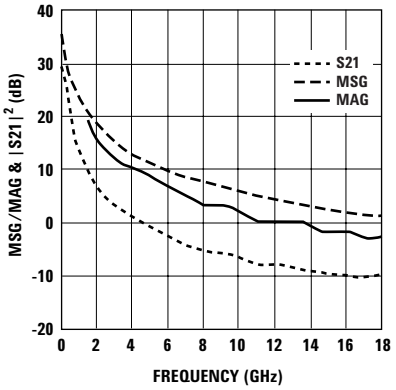


Figure 63. MSG/MAG & $|S21|^2$ vs. Frequency at 5.5V 200mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-501P8 Typical Scattering Parameters, V_{DS} = 5.5V, I_{DS} = 360 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG	K
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	factor
0.1	0.904	-132.0	31.8	38.785	113.0	-39.2	0.011	29.8	0.619	-159.9	35.5	0.198
0.2	0.910	-156.2	26.4	20.860	100.3	-38.4	0.012	24.8	0.662	-170.6	32.4	0.338
0.3	0.912	-165.4	23.0	14.161	94.7	-37.7	0.013	25.5	0.672	-175.3	30.4	0.459
0.4	0.912	-170.7	20.5	10.635	91.2	-37.1	0.014	27.8	0.675	-178.2	28.8	0.571
0.5	0.907	-173.5	18.9	8.834	88.4	-36.5	0.015	30.5	0.663	-179.5	27.7	0.666
0.6	0.909	-176.1	17.4	7.399	86.1	-35.9	0.016	33.4	0.664	178.9	26.7	0.741
0.7	0.909	-178.3	16.0	6.337	83.9	-35.4	0.017	35.7	0.666	177.6	25.7	0.808
0.8	0.907	179.9	14.9	5.557	81.9	-35.4	0.017	37.6	0.668	176.2	25.1	0.901
0.9	0.909	178.4	13.9	4.942	80.0	-34.9	0.018	39.7	0.665	175.5	24.4	0.943
1	0.906	176.7	12.9	4.429	78.0	-34.4	0.019	41.2	0.665	174.3	23.7	1.008
1.5	0.904	170.5	9.4	2.941	69.7	-32.0	0.025	46.2	0.672	170.1	18.4	1.150
2	0.904	166.1	7.3	2.325	63.6	-30.8	0.029	47.9	0.676	166.5	16.2	1.225
2.5	0.900	165.1	6.8	2.191	62.2	-30.2	0.031	48.4	0.675	163.9	15.5	1.254
3	0.905	161.0	5.2	1.817	56.6	-29.1	0.035	48.6	0.674	160.2	14.0	1.278
4	0.900	155.0	3.3	1.456	48.2	-27.5	0.042	47.4	0.686	155.1	12.0	1.329
5	0.904	144.9	1.1	1.130	35.7	-24.9	0.057	44.4	0.680	148.5	9.9	1.267
6	0.897	134.8	-0.8	0.913	20.7	-23.0	0.071	36.8	0.683	146.9	8.0	1.264
7	0.902	125.7	-3.2	0.695	7.3	-22.3	0.077	28.9	0.649	135.8	6.0	1.359
8	0.899	115.5	-4.3	0.609	-3.7	-20.8	0.091	23.4	0.643	119.1	4.5	1.402
9	0.893	105.9	-5.3	0.544	-16.0	-19.6	0.105	13.8	0.636	117.1	3.1	1.470
10	0.886	95.4	-6.0	0.499	-23.1	-18.9	0.114	11.7	0.696	106.1	2.4	1.447
11	0.867	85.0	-6.8	0.455	-31.7	-17.5	0.133	2.3	0.743	92.6	1.4	1.439
12	0.871	75.0	-8.2	0.389	-43.4	-17.2	0.138	-4.6	0.732	89.3	0.0	1.589
13	0.854	65.6	-8.2	0.387	-49.9	-15.7	0.164	-11.0	0.769	79.4	-0.2	1.436
14	0.855	56.8	-8.9	0.360	-61.2	-15.1	0.176	-20.4	0.805	70.0	-0.3	1.323
15	0.845	48.1	-9.6	0.330	-68.7	-14.3	0.192	-29.6	0.806	66.4	-1.3	1.371
16	0.842	40.7	-10.0	0.315	-72.5	-14.0	0.199	-36.7	0.769	52.1	-2.2	1.502
17	0.833	32.6	-10.2	0.309	-82.1	-13.2	0.220	-44.6	0.792	39.4	-2.4	1.436
18	0.826	25.5	-10.5	0.299	-87.9	-12.3	0.242	-51.8	0.789	29.7	-3.1	1.457

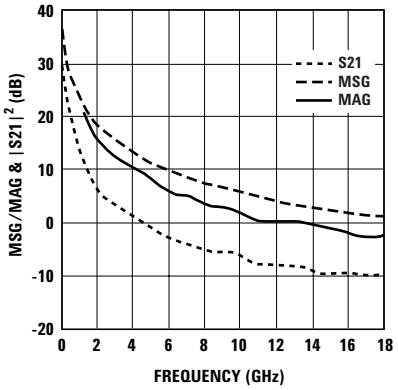


Figure 64. MSG/MAG & $|S21|^2$ vs. Frequency at 5.5V 360mA.

Notes:
1. S parameter is measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

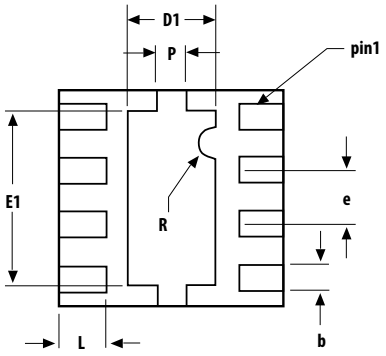
Device Models

Refer to Avago's Web Site
www.Avagotech.com/view/rf

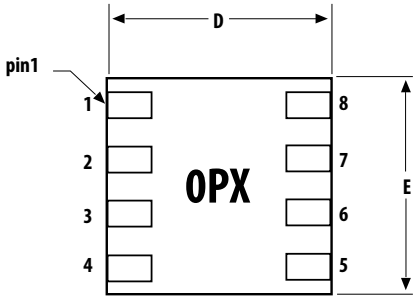
Ordering Information

Part Number	No. of Devices	Container
ATF-501P8-TR1	3000	7″ Reel
ATF-501P8-TR2	10000	13″Reel
ATF-501P8-BLK	100	antistatic bag

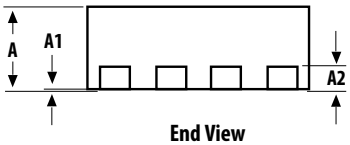
2 x 2 LPCC (JEDEC DFP-N) Package Dimensions



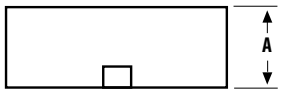
Bottom View



Top View



End View

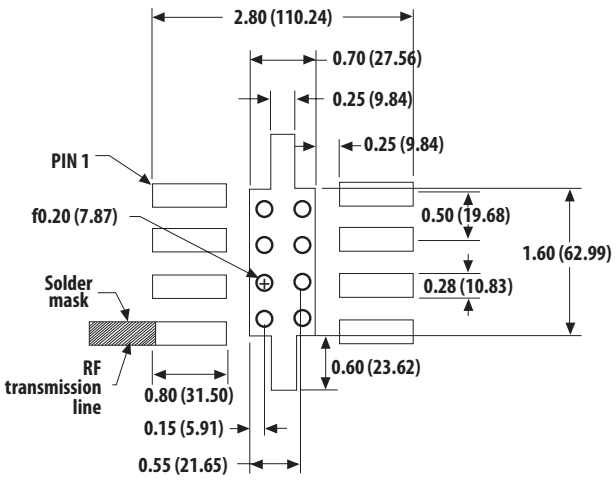


End View

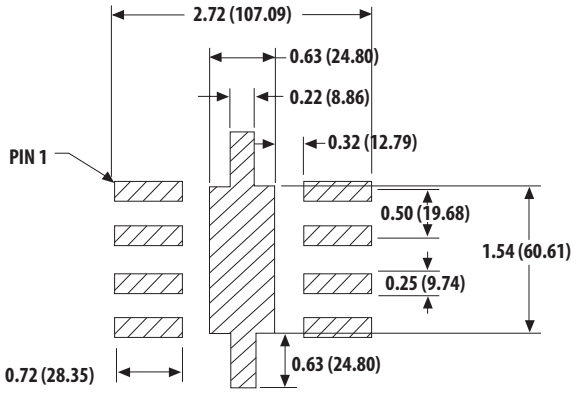
	DIMENSIONS		
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.203 REF	0.203 REF	0.203 REF
b	0.225	0.25	0.275
D	1.9	2.0	2.1
D1	0.65	0.80	0.95
E	1.9	2.0	2.1
E1	1.45	1.6	1.75
e	0.50 BSC	0.50 BSC	0.50 BSC
P	0.2	0.25	0.3
L		0.4 REF	

DIMENSIONS ARE IN MILLIMETERS

PCB Land Pattern and Stencil Design



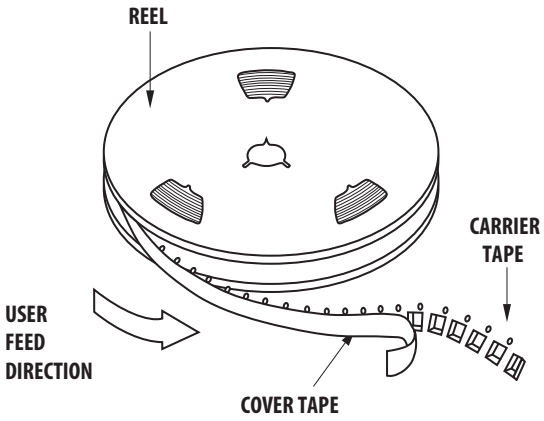
PCB Land Pattern (top view)

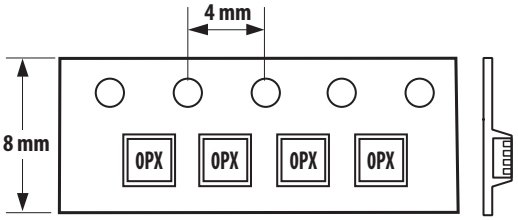


Stencil Layout (top view)

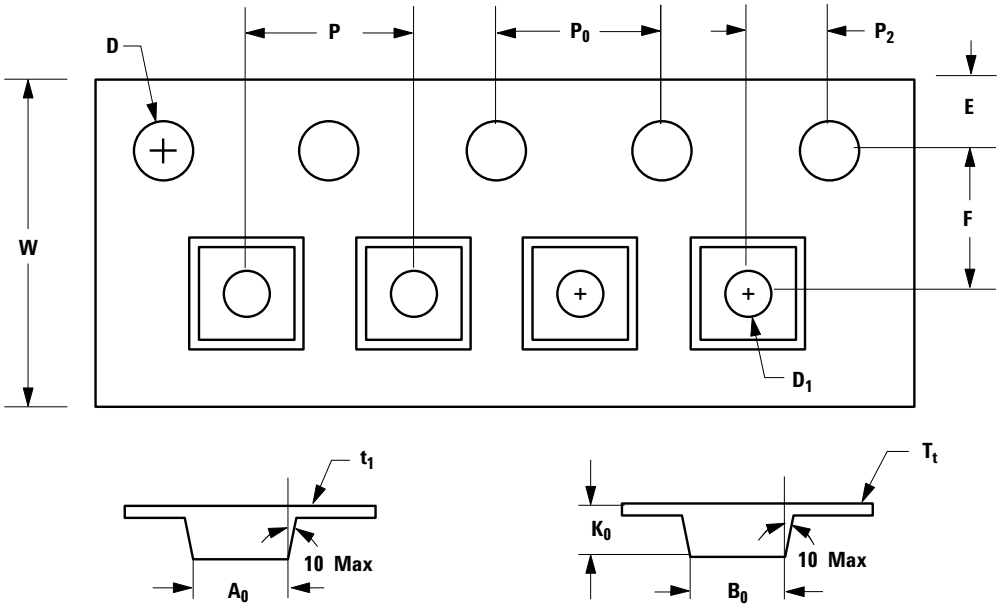
Notes:
Typical stencil thickness is 5 mils.
Measurements are in millimeters (mils).

Device Orientation





Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH	A_0	2.30 ± 0.05	0.091 ± 0.004
	WIDTH	B_0	2.30 ± 0.05	0.091 ± 0.004
	DEPTH	K_0	1.00 ± 0.05	0.039 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 8.00 – 0.10	0.315 ± 0.012 0.315 ± 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1846EN - March 27, 2009

ATF-531P8

High Linearity Enhancement Mode[1] Pseudomorphic HEMT in 2x2 mm² LPCC[3] Package

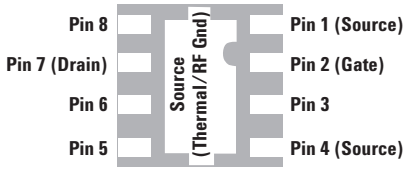
Data Sheet

Description

Avago Technologies' ATF-531P8 is a single-voltage high linearity, low noise E-pHEMT housed in an 8-lead JEDEC-standard leadless plastic chip carrier (LPCC[3]) package. The device is ideal as a high linearity, low-noise, medium-power amplifier. Its operating frequency range is from 50 MHz to 6 GHz.

The thermally efficient package measures only 2 mm x 2 mm x 0.75 mm. Its backside metalization provides excellent thermal dissipation as well as visual evidence of solder reflow. The device has a Point MTTF of over 300 years at a mounting temperature of +85°C. All devices are 100% RF & DC tested.

Pin Connections and Package Marking



Bottom View

Top View

Note:
Package marking provides orientation and identification:
"3P" = Device Code
"x" = Date code indicates the month of manufacture.

Features

- Single voltage operation
- High linearity and gain
- Low noise figure
- Excellent uniformity in product specifications
- Small package size: 2.0 x 2.0 x 0.75 mm
- Point MTTF > 300 years[2]
- MSL-1 and lead-free
- Tape-and-reel packaging option available

Specifications

2 GHz; 4V, 135 mA (Typ.)

- 38 dBm output IP3
- 0.6 dB noise figure
- 20 dB gain
- 10.7 dB LFOM[4]
- 24.5 dBm output power at 1 dB gain compression

Applications

- Front-end LNA Q1 and Q2 driver or pre-driver amplifier for Cellular/PCS and WCDMA wireless infrastructure
- Driver amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-pHEMT for other high linearity applications

Notes:
1. Enhancement mode technology employs a single positive V_{gs}, eliminating the need of negative gate voltage associated with conventional depletion mode devices.
2. Refer to reliability datasheet for detailed MTTF data.
3. Conforms to JEDEC reference outline MO229 for DRP-N
4. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

ATF-531P8 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain–Source Voltage[2]	V	7
V_{GS}	Gate–Source Voltage[2]	V	-7 to 1
V_{GD}	Gate Drain Voltage[2]	V	-7 to 1
I_{DS}	Drain Current[2]	mA	300
I_{GS}	Gate Current	mA	20
P_{diss}	Total Power Dissipation[3]	W	1
$P_{in\ max.}$	RF Input Power	dBm	+24
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{ch_b}	Thermal Resistance[4]	°C/W	63

Notes:
1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Board (package belly) temperature T_B is 25°C. Derate 16 mW/°C for T_B > 87°C.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. Device can safely handle +24 dBm RF Input Power provided IGS is limited to 20mA. IGS at P1dB drive level is bias circuit dependent.

Product Consistency Distribution Charts at 2 GHz, 4V, 135 mA[5,6]

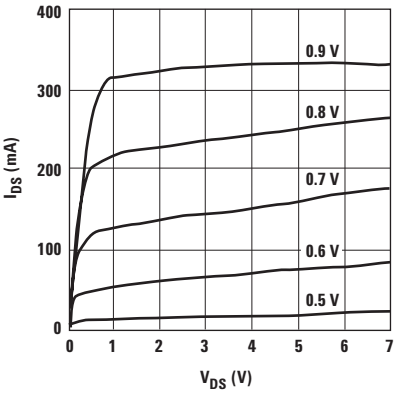


Figure 1. Typical I-V Curves (V_{GS} = 0.1 per step).

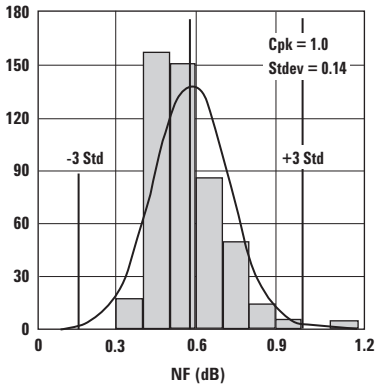


Figure 2. NF Nominal = 0.6, USL = 1.0.

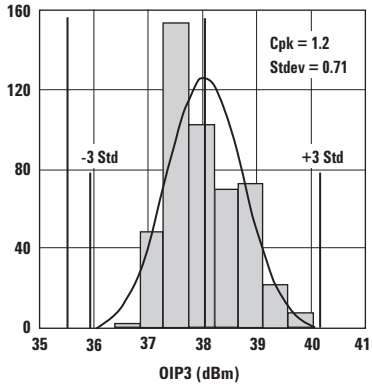


Figure 3. OIP3 LSL = 35.5, Nominal = 38.1.

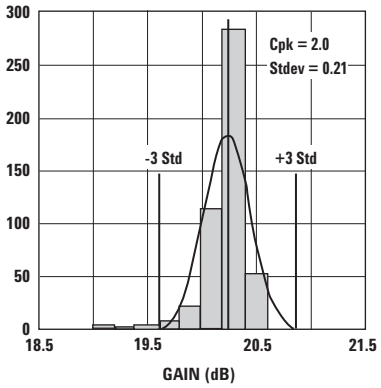


Figure 4. Small Signal Gain LSL = 18.5, Nominal = 20.2 dB, USL = 21.5.

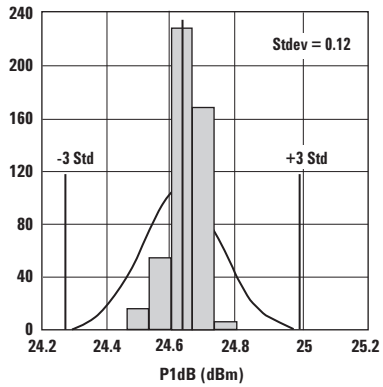


Figure 5. P1dB Nominal = 24.6.

Notes:
5. Distribution data sample size is 500 samples taken from 5 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements are made on production test board, which represents a trade-off between optimal OIP3, NF and VSWR. Circuit losses have been de-embedded from actual measurements.

ATF-531P8 Electrical Specifications

T_A = 25°C, DC bias for RF parameters is Vds = 4V and Ids = 135 mA unless otherwise specified.

Symbol	Parameter and Test Condition		Units	Min.	Typ.	Max.
Vgs	Operational Gate Voltage	Vds = 4V, Ids = 135 mA	V	—	0.68	—
Vth	Threshold Voltage	Vds = 4V, Ids = 8 mA	V	—	0.3	—
Idss	Saturated Drain Current	Vds = 4V, Vgs = 0V	µA	—	3.7	—
Gm	Transconductance	Vds = 4.5V, Gm = ΔIdss/ΔVgs; ΔVgs = Vgs1 - Vgs2 Vgs1 = 0.6V, Vgs2 = 0.55V	mmho	—	650	—
Igss	Gate Leakage Current	Vds = 0V, Vgs = -4V	µA	-10	-0.34	—
NF	Noise Figure[1]	f = 2 GHz f = 900 MHz	dB dB	— —	0.6 0.6	1 —
G	Gain[1]	f = 2 GHz f = 900 MHz	dB dB	18.5 —	20 25	21.5 —
OIP3	Output 3rd Order Intercept Point[1,2]	f = 2 GHz f = 900 MHz	dBm dBm	35.5 —	38 37	— —
P1dB	Output 1dB Compressed[1]	f = 2 GHz f = 900 MHz	dBm dBm	— —	24.5 23	— —
PAE	Power Added Efficiency	f = 2 GHz f = 900 MHz	% %	— —	57 45	— —
ACLR	Adjacent Channel Leakage Power Ratio[1,3]	Offset BW = 5 MHz Offset BW = 10 MHz	dBc dBc	— —	-68 -64	— —

Notes:

1. Measurements obtained using production test board described in Figure 6.
2. F1 = 2.00 GHz, F2 = 2.01 GHz and Pin = -10 dBm per tone.
3. ACLR test spec is based on 3GPP TS 25.141 V5.3.1 (2002-06)
   - Test Model 1
   - Active Channels: PCCPCH + SCH + CPICH + PICH + SCCPCH + 64 DPCH (SF=128)
   - Freq = 2140 MHz
   - Pin = -5 dBm
   - Chan Integ Bw = 3.84 MHz

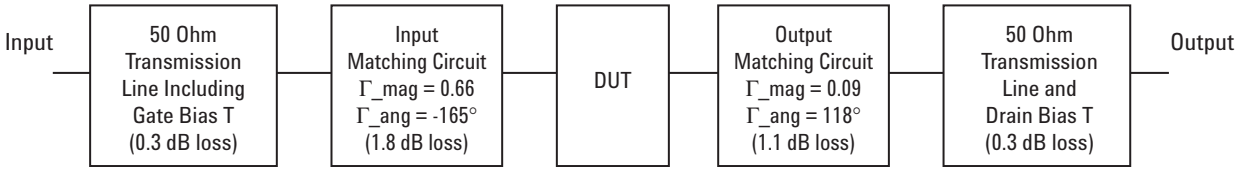


Figure 6. Block diagram of the 2 GHz production test board used for NF, Gain, OIP3 , P1dB and PAE and ACLR measurements. This circuit achieves a trade-off between optimal OIP3, NF and VSWR. Circuit losses have been de-embedded from actual measurements.

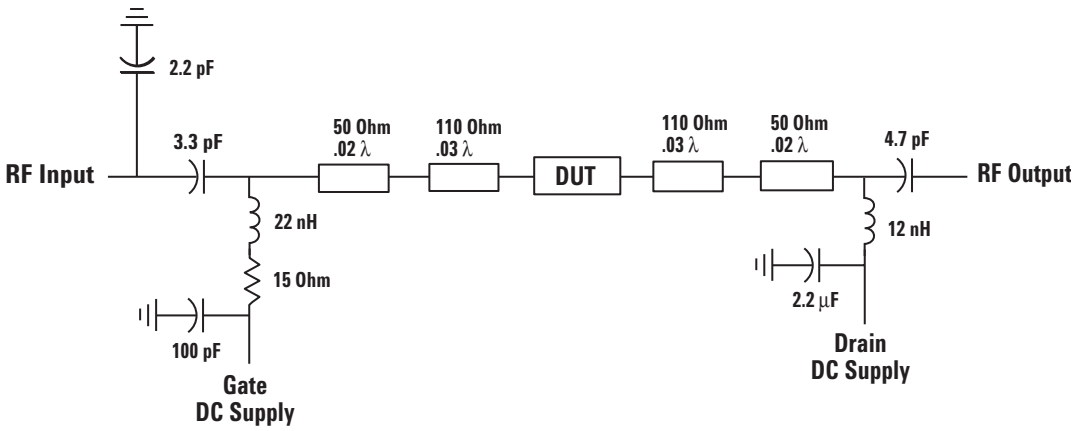


Figure 7. Simplified schematic of production test board. Primary purpose is to show 15 Ohm series resistor placement in gate supply. Transmission line tapers, tee intersections, bias lines and parasitic values are not shown.

Gamma Load and Source at Optimum OIP3 Tuning Conditions

The device's optimum OIP3 measurements were determined using a Maury load pull system at 4V, 135 mA quiesent bias. The gamma load and source over frequency are shown in the table below:

Freq	Gamma Source		Gamma Load		OIP3	Gain	P1dB	PAE
(GHz)	Mag	Ang	Mag	Ang	(dBm)	(dB)	(dBm)	(%)
0.9	0.616	-37.1	0.249	130.0	40.3	16.5	23.4	43.2
2.0	0.310	34.5	0.285	168.3	41.5	13.4	24.8	51.9
3.9	0.421	167.5	0.437	-161.6	41.5	10.5	24.7	42.8
5.8	0.402	-162.8	0.418	-134.1	41.0	7.9	24.7	36.6

ATF-531P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3

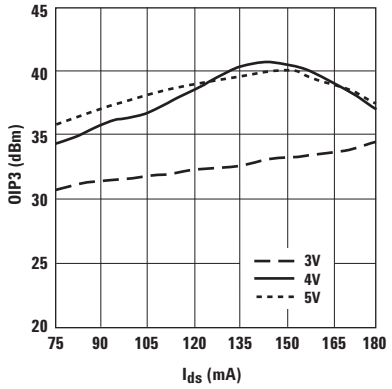


Figure 8. OIP3 vs. I_{ds} and V_{ds} at 900 MHz.

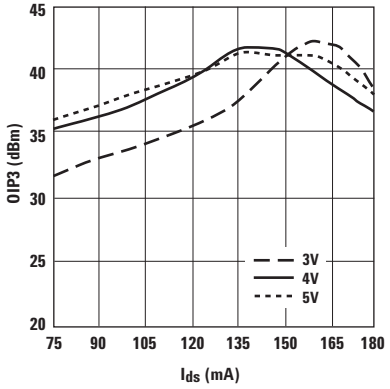


Figure 9. OIP3 vs. I_{ds} and V_{ds} at 2 GHz.

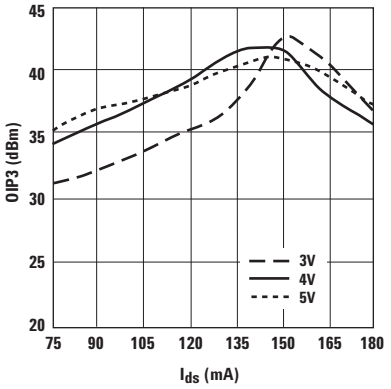


Figure 10. OIP3 vs. I_{ds} and V_{ds} at 3.9 GHz.

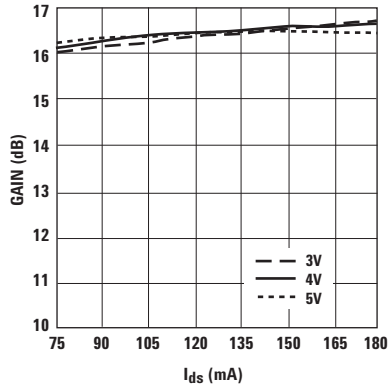


Figure 11. Small Signal Gain vs. I_{ds} and V_{ds} at 900 MHz.

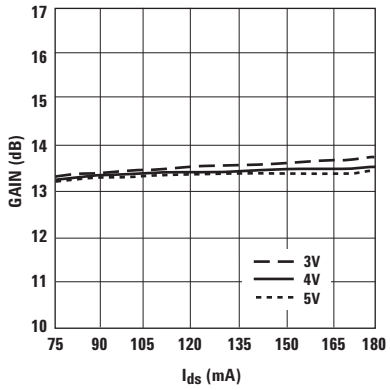


Figure 12. Small Signal Gain vs. I_{ds} and V_{ds} at 2 GHz.

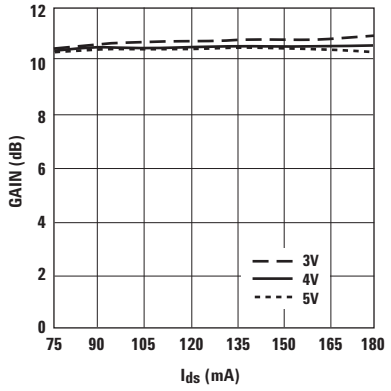


Figure 13. Small Signal Gain vs. I_{ds} and V_{ds} at 3.9 GHz.

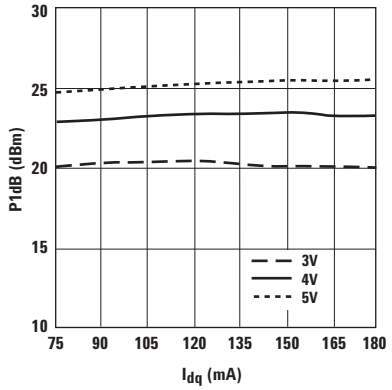


Figure 14. P1dB vs. I_{dq} and V_{ds} at 900 MHz.

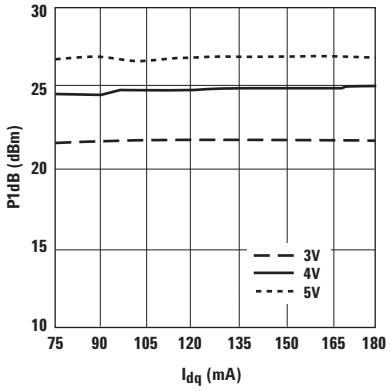


Figure 15. P1dB vs. I_{dq} and V_{ds} at 2 GHz.

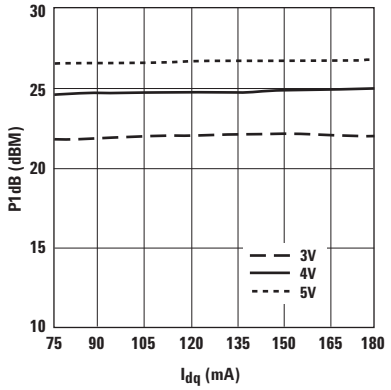


Figure 16. P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase or decrease depending on amount of RF drive. The objective of load pull is to optimize OIP3 and therefore may trade-off Small Signal Gain, P1dB and VSWR.

ATF-531P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal OIP3

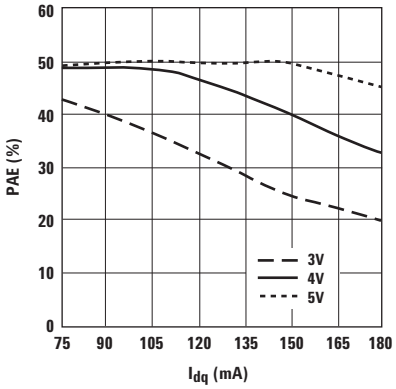


Figure 17. PAE vs. I_{dq} and V_{ds} at 900 MHz.

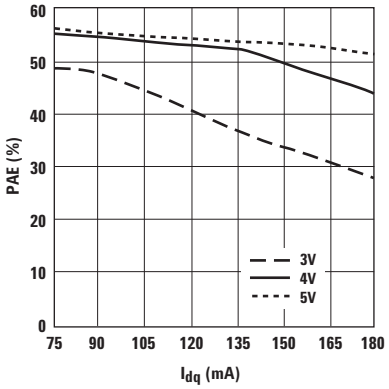


Figure 18. PAE vs. I_{dq} and V_{ds} at 2 GHz.

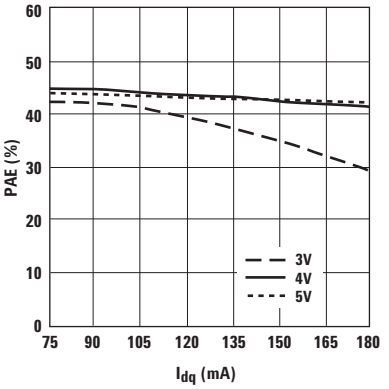


Figure 19. PAE vs. I_{dq} and V_{ds} at 3.9 GHz.

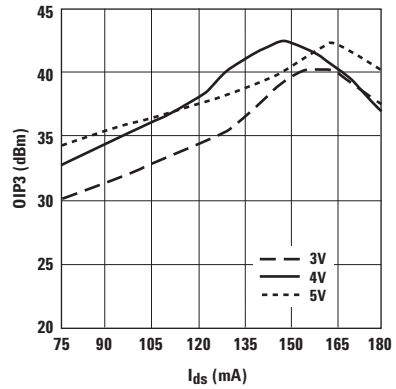


Figure 20. OIP3 vs. I_{ds} and V_{ds} at 5.8 GHz.

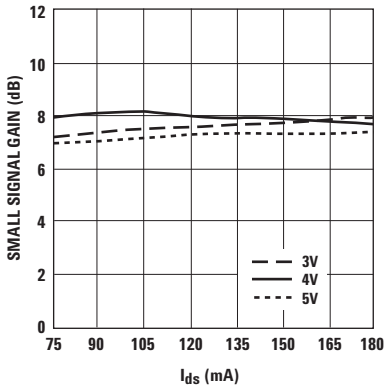


Figure 21. Small Signal Gain vs. I_{ds} and V_{ds} at 5.8 GHz.

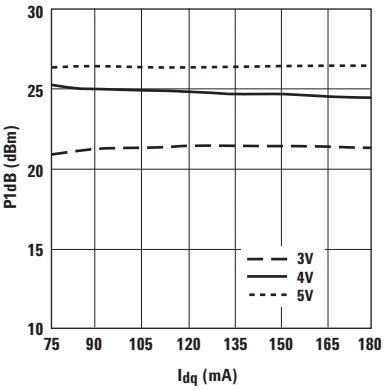


Figure 22. P1dB vs. I_{dq} and V_{ds} at 5.8 GHz.

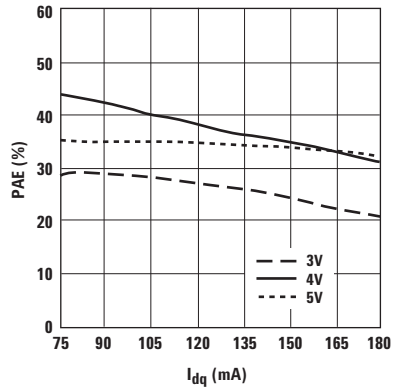


Figure 23. PAE vs. I_{dq} and V_{ds} at 5.8 GHz.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase or decrease depending on amount of RF drive. The objective of load pull is to optimize OIP3 and therefore may trade-off Small Signal Gain, P1dB and VSWR.

ATF-531P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3, continued

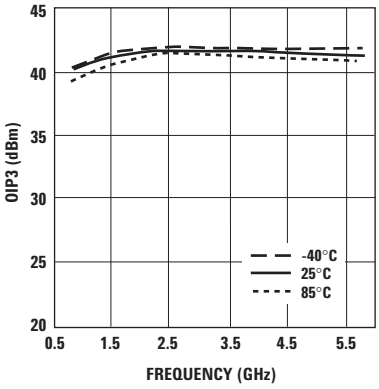


Figure 24. OIP3 vs. Temp and Freq. (Tuned for optimal OIP3 at 4V, 135 mA)

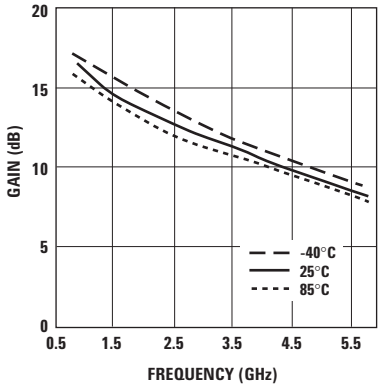


Figure 25. Small Signal Gain vs. Temp and Freq. (Tuned for optimal OIP3 at 4V, 135 mA)

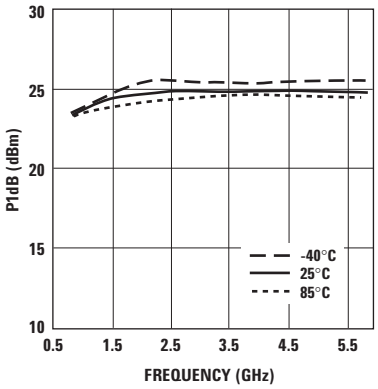


Figure 26. P1dB vs. Temp and Freq. (Tuned for optimal OIP3 at 4V, 135 mA)

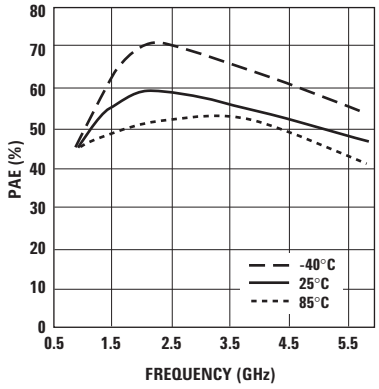


Figure 27. PAE vs. Temp and Freq. (Tuned for optimal OIP3 at 4V, 135 mA)

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase or decrease depending on amount of RF drive. The objective of load pull is to optimize OIP3 and therefore may trade-off Small Signal Gain, P1dB and VSWR.

ATF-531P8 Typical Scattering Parameters at 25°C, $V_{DS} = 4V$, $I_{DS} = 180$ mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.626	-59.4	33.20	45.702	154.5	-40.00	0.010	62.6	0.410	-44.4	36.60
0.2	0.704	-97.4	31.41	37.192	135.8	-35.92	0.016	48.8	0.384	-79.2	33.66
0.3	0.761	-119.4	29.53	29.950	123.5	-34.42	0.019	39.1	0.370	-101.8	31.98
0.4	0.794	-133.8	27.78	24.477	114.8	-33.56	0.021	33.7	0.360	-117.6	30.67
0.5	0.815	-142.5	26.32	20.693	108.9	-32.77	0.023	30.0	0.355	-127.1	29.54
0.6	0.824	-149.6	24.99	17.760	103.9	-32.77	0.023	27.4	0.351	-135.5	28.88
0.7	0.834	-155.1	23.82	15.516	99.9	-32.40	0.024	25.8	0.349	-141.9	28.11
0.8	0.840	-159.7	22.76	13.742	96.6	-32.40	0.024	24.6	0.349	-146.9	27.58
0.9	0.845	-163.3	21.83	12.346	93.6	-32.04	0.025	24.2	0.349	-151.1	26.94
1	0.848	-166.4	20.96	11.164	91.0	-32.04	0.025	23.8	0.347	-154.3	26.50
1.5	0.854	-177.7	17.59	7.579	80.6	-31.37	0.027	23.5	0.344	-165.8	24.48
1.9	0.857	175.9	15.60	6.024	73.9	-30.75	0.029	24.4	0.344	-171.2	23.17
2	0.853	174.4	15.36	5.863	72.6	-30.46	0.030	24.9	0.335	-171.8	22.91
2.4	0.853	168.9	13.79	4.894	66.5	-29.90	0.032	25.8	0.339	-176.8	21.85
3	0.855	161.6	11.83	3.902	57.9	-29.12	0.035	26.6	0.337	177.0	19.60
4	0.858	150.8	9.27	2.906	44.6	-27.74	0.041	26.5	0.356	168.5	16.23
5	0.864	140.7	7.20	2.292	31.6	-26.56	0.047	24.3	0.378	160.6	14.19
6	0.871	131.7	5.48	1.879	19.4	-25.35	0.054	21.2	0.402	152.4	12.69
7	0.869	123.5	4.04	1.593	7.5	-24.29	0.061	17.4	0.427	144.6	11.18
8	0.880	115.2	2.73	1.370	-4.3	-23.35	0.068	12.6	0.449	136.1	10.39
9	0.883	106.8	1.77	1.226	-16.1	-22.27	0.077	7.0	0.465	127.4	9.70
10	0.884	95.7	0.70	1.084	-29.0	-21.41	0.085	-0.8	0.489	116.6	8.70
11	0.874	85.1	-0.34	0.962	-41.6	-20.63	0.093	-8.8	0.505	106.0	7.20
12	0.874	74.1	-1.39	0.852	-52.8	-19.91	0.101	-16.6	0.544	97.2	6.30
13	0.877	63.3	-2.52	0.748	-64.5	-19.49	0.106	-24.6	0.596	85.9	5.46
14	0.884	57.9	-3.64	0.658	-74.6	-19.02	0.112	-31.9	0.638	74.7	4.95
15	0.894	46.8	-4.81	0.575	-85.4	-18.71	0.116	-39.8	0.662	65.9	4.29
16	0.896	43.3	-5.66	0.521	-93.6	-18.49	0.119	-47.8	0.699	56.1	4.06
17	0.898	31.9	-7.25	0.434	-102.6	-18.49	0.119	-55.1	0.748	47.7	2.82
18	0.918	20.8	-8.61	0.371	-110.5	-18.94	0.113	-62.6	0.718	39.3	1.75

Typical Noise Parameters at 25°C, $V_{DS} = 4V$, $I_{DS} = 180$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.50	0.20	166.00	0.041	28.26
0.9	0.59	0.25	169.00	0.044	24.27
1	0.60	0.35	171.00	0.036	24.15
1.5	0.72	0.40	173.00	0.039	21.14
2	0.81	0.57	-173.50	0.029	20.07
2.4	0.90	0.61	-167.70	0.033	18.73
3	1.01	0.63	-163.50	0.041	16.91
3.5	1.10	0.67	-158.20	0.054	15.86
3.9	1.13	0.70	-153.90	0.068	15.12
5	1.34	0.72	-142.70	0.139	13.08
5.8	1.48	0.75	-135.40	0.229	12.04
6	1.58	0.76	-133.30	0.278	11.82
7	1.68	0.80	-125.00	0.470	10.69
8	1.89	0.84	-116.10	0.860	9.97
9	2.15	0.82	-106.90	1.170	8.96
10	2.34	0.85	-95.10	2.010	8.09

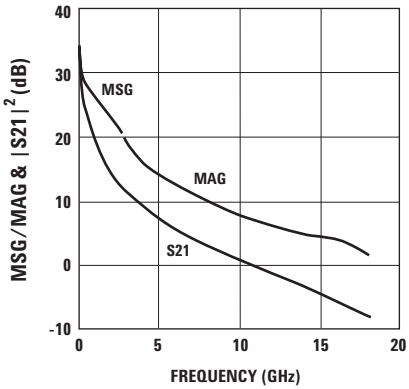


Figure 28. MSG/MAG & $|S21|^2$ (dB) @ 4V, 180 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-531P8 Typical Scattering Parameters, $V_{DS} = 4V$, $I_{DS} = 135$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.812	-56.4	34.07	50.547	151.8	-38.42	0.012	62.6	0.449	-49.1	36.25
0.2	0.820	-94.6	31.95	39.582	132.2	-34.89	0.018	45.8	0.425	-85.0	33.42
0.3	0.834	-117.3	29.87	31.147	120.2	-33.15	0.022	36.5	0.397	-108.1	31.51
0.4	0.842	-132.4	27.99	25.104	111.8	-32.40	0.024	30.5	0.385	-123.7	30.20
0.5	0.846	-141.4	26.46	21.036	106.3	-32.04	0.025	27.0	0.379	-132.5	29.25
0.6	0.849	-148.7	25.08	17.954	101.6	-31.70	0.026	24.8	0.375	-140.4	28.39
0.7	0.853	-154.4	23.88	15.628	97.9	-31.70	0.026	23.2	0.372	-146.4	27.79
0.8	0.853	-159.0	22.80	13.809	94.8	-31.37	0.027	22.4	0.372	-151.0	27.09
0.9	0.855	-162.7	21.85	12.376	92.0	-31.37	0.027	21.7	0.371	-154.9	26.61
1	0.857	-166.0	20.97	11.186	89.6	-31.37	0.027	21.2	0.369	-157.9	26.17
1.5	0.857	-177.3	17.58	7.568	79.7	-30.75	0.029	21.4	0.366	-168.7	24.17
1.9	0.857	176.2	15.57	6.007	73.3	-30.17	0.031	21.7	0.366	-174.2	22.87
2	0.853	174.7	15.34	5.847	72.0	-29.90	0.032	22.5	0.347	-174.8	22.62
2.4	0.852	169.2	13.77	4.879	66.0	-29.37	0.034	23.0	0.351	-179.7	21.57
3	0.853	161.7	11.80	3.889	57.6	-28.64	0.037	24.1	0.358	174.2	20.22
4	0.857	150.8	9.24	2.896	44.6	-27.54	0.042	23.9	0.375	165.7	16.28
5	0.861	140.9	7.18	2.285	31.8	-26.38	0.048	22.2	0.396	157.8	14.11
6	0.866	131.6	5.45	1.873	19.7	-25.19	0.055	18.6	0.417	149.6	12.50
7	0.867	123.5	4.02	1.589	7.9	-24.29	0.061	15.1	0.440	141.8	11.10
8	0.875	115.1	2.72	1.367	-3.8	-23.22	0.069	10.4	0.459	133.4	10.16
9	0.877	106.9	1.76	1.224	-15.3	-22.16	0.078	4.8	0.474	124.8	9.40
10	0.884	95.6	0.71	1.085	-28.2	-21.31	0.086	-2.6	0.496	114.1	8.69
11	0.889	85.3	-0.34	0.962	-41.0	-20.63	0.093	-10.7	0.511	103.7	7.93
12	0.872	73.9	-1.33	0.858	-51.7	-19.91	0.101	-18.3	0.548	95.1	6.24
13	0.878	63.6	-2.48	0.752	-64.0	-19.58	0.105	-26.2	0.600	84.0	5.55
14	0.886	57.6	-3.57	0.663	-73.7	-19.02	0.112	-33.3	0.640	73.1	5.05
15	0.902	47.2	-4.66	0.585	-84.8	-18.79	0.115	-42.0	0.663	64.4	4.93
16	0.902	43.7	-5.56	0.527	-91.3	-18.49	0.119	-49.2	0.698	54.7	4.37
17	0.895	32.1	-6.99	0.447	-101.9	-18.49	0.119	-56.7	0.746	46.5	2.93
18	0.932	20.6	-8.75	0.365	-109.6	-18.94	0.113	-63.9	0.716	38.2	2.36

Typical Noise Parameters, $V_{DS} = 4V$, $I_{DS} = 135$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.18	0.20	166.00	0.014	28.57
0.9	0.26	0.25	169.00	0.018	24.42
1	0.35	0.35	171.00	0.021	24.32
1.5	0.40	0.40	173.00	0.021	21.25
2	0.51	0.47	177.20	0.022	19.35
2.4	0.56	0.51	-174.50	0.022	17.66
3	0.60	0.56	-169.30	0.023	16.37
3.5	0.73	0.60	-162.90	0.030	15.09
3.9	0.83	0.66	-157.60	0.040	14.82
5	1.03	0.68	-145.50	0.085	12.76
5.8	1.15	0.72	-137.10	0.140	11.55
6	1.20	0.72	-135.20	0.160	11.31
7	1.34	0.78	-126.70	0.300	10.55
8	1.57	0.83	-117.00	0.630	9.81
9	1.78	0.82	-107.90	0.880	8.86
10	1.83	0.85	-95.70	1.460	8.17

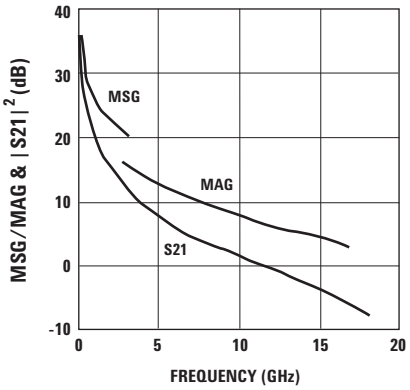


Figure 29. MSG/MAG & $|S21|^2$ (dB) @ 4V, 135 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-531P8 Typical Scattering Parameters, $V_{DS} = 4V$, $I_{DS} = 75$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.930	-51.3	33.70	48.399	152.3	-37.08	0.014	63.6	0.524	-45.7	35.39
0.2	0.889	-88.3	31.65	38.230	132.6	-32.77	0.023	46.8	0.467	-80.7	32.21
0.3	0.876	-111.6	29.58	30.121	120.6	-31.37	0.027	36.1	0.436	-103.2	30.48
0.4	0.867	-127.3	27.71	24.294	112.2	-30.75	0.029	29.5	0.415	-119.1	29.23
0.5	0.862	-137.0	26.18	20.379	106.6	-30.46	0.030	25.9	0.405	-128.4	28.32
0.6	0.858	-144.7	24.81	17.405	101.9	-30.17	0.031	23.1	0.397	-136.8	27.49
0.7	0.857	-151.0	23.62	15.165	98.2	-29.90	0.032	21.1	0.392	-143.2	26.76
0.8	0.856	-156.0	22.54	13.404	95.0	-29.90	0.032	19.9	0.390	-148.2	26.22
0.9	0.854	-160.0	21.59	12.005	92.2	-29.63	0.033	18.3	0.387	-152.3	25.61
1	0.857	-163.5	20.72	10.859	89.8	-29.63	0.033	18.2	0.384	-155.6	25.17
1.5	0.853	-175.7	17.33	7.351	79.8	-29.12	0.035	16.3	0.380	-167.2	23.22
1.9	0.853	177.6	15.33	5.839	73.3	-28.87	0.036	16.5	0.379	-173.2	22.10
2	0.848	176.2	15.09	5.681	72.0	-28.64	0.037	16.7	0.360	-173.8	21.86
2.4	0.846	170.3	13.52	4.742	66.0	-28.18	0.039	17.0	0.363	-179.0	20.85
3	0.848	162.4	11.55	3.780	57.5	-27.74	0.041	17.0	0.369	174.6	19.65
4	0.850	151.6	8.98	2.813	44.3	-26.94	0.045	16.7	0.385	165.7	16.29
5	0.853	141.4	6.93	2.220	31.5	-25.85	0.051	15.4	0.405	157.5	13.90
6	0.861	132.3	5.22	1.824	19.4	-25.04	0.056	12.9	0.426	149.2	12.31
7	0.861	123.8	3.78	1.546	7.5	-24.01	0.063	9.8	0.447	141.3	10.85
8	0.868	115.6	2.50	1.334	-4.3	-23.22	0.069	5.5	0.467	132.8	9.85
9	0.873	107.1	1.51	1.190	-15.9	-22.16	0.078	0.4	0.481	124.1	9.15
10	0.875	95.8	0.50	1.059	-28.8	-21.41	0.085	-6.6	0.501	113.3	8.19
11	0.881	85.6	-0.57	0.937	-41.2	-20.63	0.093	-13.8	0.515	102.9	7.40
12	0.871	74.2	-1.56	0.836	-52.5	-20.00	0.100	-21.4	0.553	94.5	6.12
13	0.873	63.7	-2.65	0.737	-63.9	-19.66	0.104	-28.8	0.604	83.4	5.28
14	0.885	57.0	-3.80	0.646	-74.0	-19.17	0.110	-36.3	0.644	72.5	4.89
15	0.891	47.0	-4.72	0.581	-85.2	-18.79	0.115	-43.7	0.666	63.7	4.38
16	0.912	43.7	-5.76	0.515	-93.5	-18.56	0.118	-51.7	0.700	54.2	5.43
17	0.895	32.2	-7.15	0.439	-102.3	-18.49	0.119	-58.5	0.748	46.0	2.90
18	0.933	21.2	-8.66	0.369	-110.5	-19.02	0.112	-65.8	0.718	37.8	2.74

Typical Noise Parameters, $V_{DS} = 4V$, $I_{DS} = 75$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.15	0.10	130.00	0.016	27.97
0.9	0.20	0.15	135.00	0.019	23.50
1	0.22	0.20	143.00	0.019	23.02
1.5	0.30	0.30	148.00	0.022	20.07
2	0.36	0.35	154.10	0.024	17.85
2.4	0.44	0.43	168.70	0.022	16.35
3	0.50	0.47	179.30	0.022	15.29
3.5	0.55	0.58	-170.80	0.019	14.11
3.9	0.63	0.60	-164.80	0.024	14.01
5	0.80	0.67	-150.90	0.050	11.92
5.8	0.90	0.72	-140.80	0.095	11.00
6	0.91	0.72	-139.50	0.100	10.56
7	1.14	0.71	-129.10	0.180	9.80
8	1.24	0.74	-119.90	0.285	9.31
9	1.49	0.74	-109.70	0.460	8.41
10	1.61	0.76	-97.30	0.720	7.73

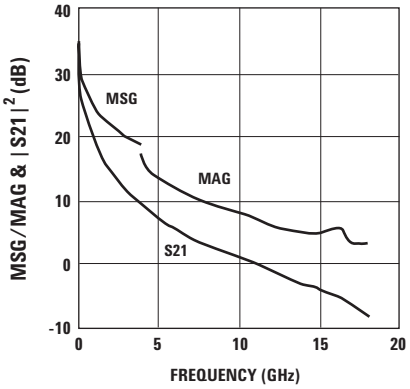


Figure 30. MSG/MAG & $|S21|^2$ (dB) @ 4V, 75 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-531P8 Typical Scattering Parameters, $V_{DS} = 5V$, $I_{DS} = 135$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.805	-56.0	34.11	50.734	152.1	-39.17	0.011	62.6	0.468	-45.2	36.64
0.2	0.815	-94.0	32.03	39.967	132.6	-34.89	0.018	46.6	0.419	-79.7	33.46
0.3	0.831	-116.9	29.97	31.517	120.5	-33.56	0.021	36.3	0.387	-102.0	31.76
0.4	0.839	-131.7	28.10	25.418	112.1	-32.77	0.023	30.7	0.364	-117.9	30.43
0.5	0.844	-140.9	26.58	21.322	106.4	-32.40	0.024	27.2	0.354	-127.0	29.49
0.6	0.846	-148.3	25.20	18.207	101.8	-32.04	0.025	24.9	0.346	-135.4	28.62
0.7	0.850	-154.0	24.00	15.852	98.0	-31.70	0.026	23.3	0.342	-141.6	27.85
0.8	0.852	-158.7	22.93	14.014	94.8	-31.70	0.026	22.3	0.339	-146.5	27.32
0.9	0.855	-162.5	21.98	12.559	92.0	-31.70	0.026	21.6	0.337	-150.5	26.84
1	0.854	-165.6	21.10	11.351	89.6	-31.37	0.027	20.9	0.335	-153.9	26.24
1.5	0.855	-177.1	17.71	7.681	79.5	-31.06	0.028	21.1	0.331	-165.0	24.38
1.9	0.857	176.3	15.71	6.099	73.0	-30.46	0.030	22.3	0.331	-170.4	23.08
2	0.851	174.9	15.46	5.931	71.7	-30.17	0.031	22.3	0.336	-170.9	22.82
2.4	0.851	169.4	13.89	4.946	65.6	-29.63	0.033	23.3	0.315	-175.8	21.76
3	0.852	161.8	11.92	3.943	57.1	-29.12	0.035	24.3	0.323	178.2	19.82
4	0.857	151.1	9.35	2.935	43.9	-27.74	0.041	24.4	0.343	169.9	16.43
5	0.859	141.0	7.30	2.318	30.9	-26.56	0.047	22.8	0.367	162.1	14.19
6	0.870	131.8	5.57	1.899	18.5	-25.51	0.053	19.7	0.391	154.0	12.82
7	0.867	123.6	4.11	1.605	6.5	-24.44	0.060	16.3	0.417	146.2	11.24
8	0.877	115.6	2.80	1.381	-5.2	-23.48	0.067	11.8	0.440	137.7	10.41
9	0.881	106.7	1.82	1.233	-17.0	-22.38	0.076	6.1	0.458	129.1	9.75
10	0.885	95.6	0.75	1.090	-30.1	-21.41	0.085	-1.3	0.482	118.1	8.94
11	0.892	85.2	-0.30	0.966	-42.9	-20.72	0.092	-9.1	0.500	107.5	8.31
12	0.875	74.2	-1.33	0.858	-54.3	-20.00	0.100	-17.0	0.540	98.6	6.52
13	0.883	63.8	-2.49	0.751	-65.9	-19.66	0.104	-24.8	0.593	87.1	5.87
14	0.886	57.9	-3.58	0.662	-76.4	-19.09	0.111	-31.8	0.636	75.8	5.23
15	0.913	47.4	-4.78	0.577	-86.8	-18.71	0.116	-40.3	0.660	66.8	6.01
16	0.908	43.1	-5.81	0.512	-94.4	-18.56	0.118	-47.8	0.699	57.0	4.78
17	0.891	32.2	-6.99	0.447	-105.1	-18.49	0.119	-54.9	0.747	48.4	2.98
18	0.928	20.6	-8.64	0.370	-112.1	-18.86	0.114	-62.6	0.717	39.9	2.41

Typical Noise Parameters, $V_{DS} = 5V$, $I_{DS} = 135$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.45	0.20	154.00	0.037	28.85
0.9	0.48	0.32	160.00	0.032	25.13
1	0.50	0.35	166.00	0.030	24.43
1.5	0.55	0.40	170.00	0.030	21.26
2	0.65	0.46	177.40	0.030	19.38
2.4	0.70	0.49	-175.10	0.032	17.90
3	0.77	0.55	-168.90	0.031	16.33
3.5	0.84	0.58	-162.60	0.037	15.23
3.9	0.90	0.62	-158.20	0.043	14.60
5	1.06	0.66	-145.80	0.085	12.66
5.8	1.20	0.69	-137.30	0.140	11.60
6	1.19	0.69	-135.40	0.150	11.38
7	1.40	0.77	-126.50	0.320	10.55
8	1.52	0.81	-117.90	0.550	9.84
9	1.75	0.82	-107.50	0.890	9.05
10	1.88	0.85	-95.60	1.530	8.29

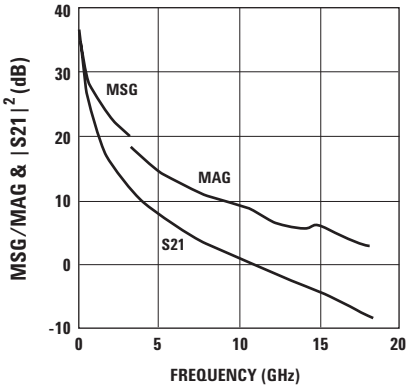


Figure 31. MSG/MAG & $|S21|^2$ (dB) @ 5V, 135 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-531P8 Typical Scattering Parameters, $V_{DS} = 3V$, $I_{DS} = 135$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.823	-57.1	33.96	49.888	151.3	-37.72	0.013	62.6	0.427	-55.1	35.84
0.2	0.826	-95.6	31.82	38.989	131.6	-33.98	0.020	45.7	0.418	-92.8	32.90
0.3	0.842	-118.2	29.66	30.415	119.6	-32.77	0.023	36.0	0.421	-115.9	31.21
0.4	0.846	-133.1	27.75	24.416	111.4	-32.04	0.025	30.1	0.420	-130.7	29.90
0.5	0.851	-142.0	26.21	20.452	105.9	-31.70	0.026	26.8	0.419	-139.0	28.96
0.6	0.850	-149.2	24.83	17.443	101.4	-31.37	0.027	24.4	0.419	-146.4	28.10
0.7	0.855	-154.9	23.62	15.178	97.7	-31.37	0.027	22.9	0.419	-151.9	27.50
0.8	0.856	-159.5	22.55	13.405	94.7	-31.06	0.028	22.1	0.420	-156.1	26.80
0.9	0.859	-163.2	21.59	12.012	92.0	-31.06	0.028	21.4	0.421	-159.7	26.32
1	0.857	-166.3	20.71	10.853	89.6	-30.75	0.029	21.1	0.419	-162.6	25.73
1.5	0.857	-177.7	17.32	7.342	79.9	-30.46	0.030	21.0	0.418	-172.9	23.89
1.9	0.858	175.8	15.31	5.828	73.6	-29.90	0.032	21.6	0.418	-178.2	22.60
2	0.855	174.4	15.08	5.676	72.3	-29.37	0.034	22.1	0.410	-179.1	22.23
2.4	0.855	168.8	13.51	4.738	66.4	-29.12	0.035	22.6	0.403	176.0	21.32
3	0.854	161.4	11.54	3.774	58.2	-28.40	0.038	22.8	0.409	169.8	19.97
4	0.858	150.7	8.98	2.812	45.3	-27.13	0.044	22.7	0.423	161.0	16.15
5	0.860	140.4	6.92	2.219	32.8	-26.02	0.050	20.7	0.440	152.8	13.82
6	0.868	131.4	5.21	1.821	21.0	-24.88	0.057	17.2	0.457	144.4	12.31
7	0.866	123.2	3.79	1.547	9.4	-23.88	0.064	13.4	0.475	136.6	10.81
8	0.877	114.8	2.52	1.337	-2.0	-22.85	0.072	8.5	0.490	128.0	10.00
9	0.876	106.3	1.57	1.198	-13.7	-21.83	0.081	2.6	0.502	119.3	9.09
10	0.880	95.1	0.56	1.066	-26.0	-21.11	0.088	-5.0	0.519	108.7	8.20
11	0.883	84.7	-0.46	0.948	-38.2	-20.35	0.096	-12.9	0.530	98.4	7.31
12	0.874	73.6	-1.51	0.840	-49.6	-19.83	0.102	-20.7	0.566	90.7	6.06
13	0.878	62.9	-2.56	0.745	-61.1	-19.41	0.107	-28.5	0.613	79.7	5.32
14	0.884	56.9	-3.54	0.665	-71.0	-18.94	0.113	-35.9	0.652	69.3	4.87
15	0.906	46.7	-4.70	0.582	-80.8	-18.71	0.116	-43.9	0.670	60.8	4.76
16	0.907	42.9	-5.61	0.524	-88.0	-18.49	0.119	-51.4	0.704	51.6	4.29
17	0.893	32.2	-6.80	0.457	-99.8	-18.42	0.120	-58.7	0.747	43.7	2.90
18	0.925	20.7	-8.38	0.381	-107.2	-18.86	0.114	-66.3	0.717	35.8	2.20

Typical Noise Parameters, $V_{DS} = 3V$, $I_{DS} = 135$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.25	0.20	166.00	0.020	28.47
0.9	0.30	0.25	169.00	0.022	24.36
1	0.30	0.35	171.00	0.018	24.24
1.5	0.36	0.40	173.00	0.019	21.17
2	0.45	0.46	176.80	0.020	19.30
2.4	0.52	0.52	-174.70	0.021	18.08
3	0.66	0.56	-169.80	0.025	16.26
3.5	0.70	0.62	-162.80	0.028	15.33
3.9	0.87	0.65	-157.90	0.042	14.62
5	1.02	0.67	-145.70	0.082	12.52
5.8	1.13	0.71	-136.80	0.140	11.53
6	1.24	0.73	-135.10	0.175	11.40
7	1.34	0.82	-126.20	0.380	10.57
8	1.58	0.83	-116.90	0.645	9.67
9	1.78	0.81	-107.50	0.870	8.59
10	1.88	0.83	-95.40	1.350	7.76

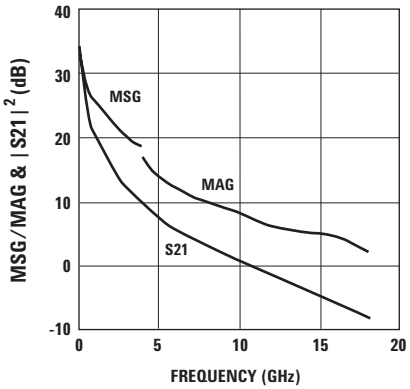


Figure 32. MSG/MAG & $|S21|^2$ (dB) @ 3V, 135 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

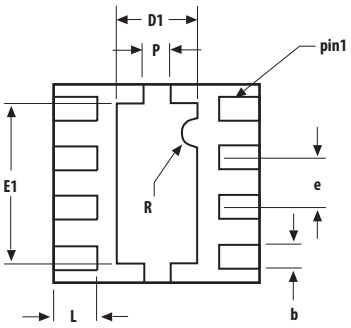
Device Models

Refer to Avago Technologies' Web Site
www.avagotech.com/rf

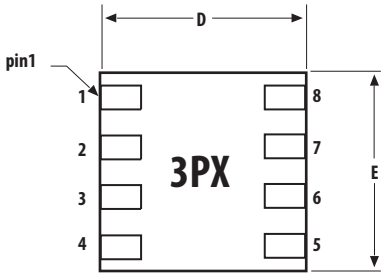
Ordering Information

Part Number	No. of Devices	Container
ATF-531P8-TR1	3000	7″ Reel
ATF-531P8-TR2	10000	13″Reel
ATF-531P8-BLK	100	antistatic bag

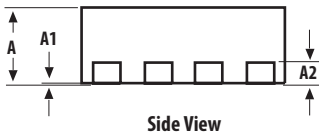
2 x 2 LPCC (JEDEC DFP-N) Package Dimensions



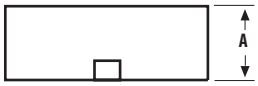
Bottom View



Top View



Side View

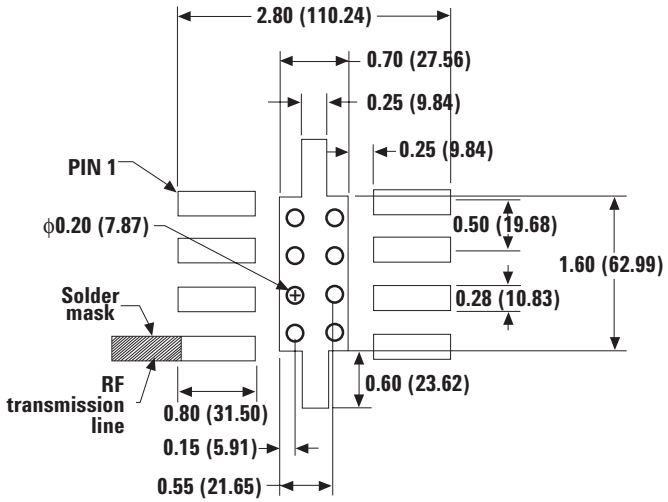


End View

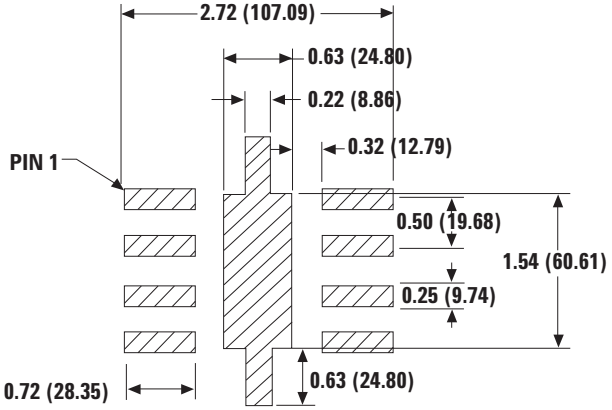
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.203 REF	
b	0.225	0.25	0.275
D	1.9	2.0	2.1
D1	0.65	0.80	0.95
E	1.9	2.0	2.1
E1	1.45	1.6	1.75
e		0.50 BSC	
P	0.20	0.25	0.30
L	0.35	0.40	0.45

DIMENSIONS ARE IN MILLIMETERS

PCB Land Pattern and Stencil Design

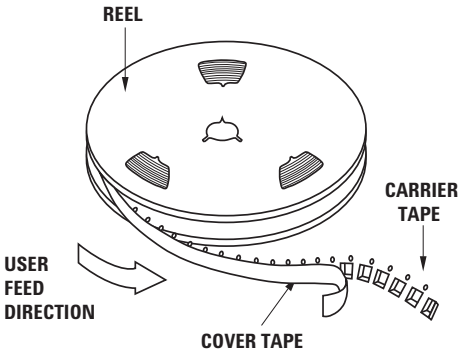


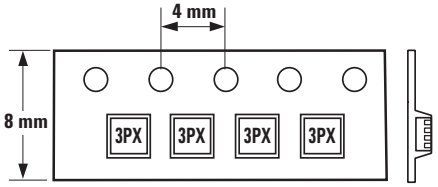
PCB Land Pattern (top view)



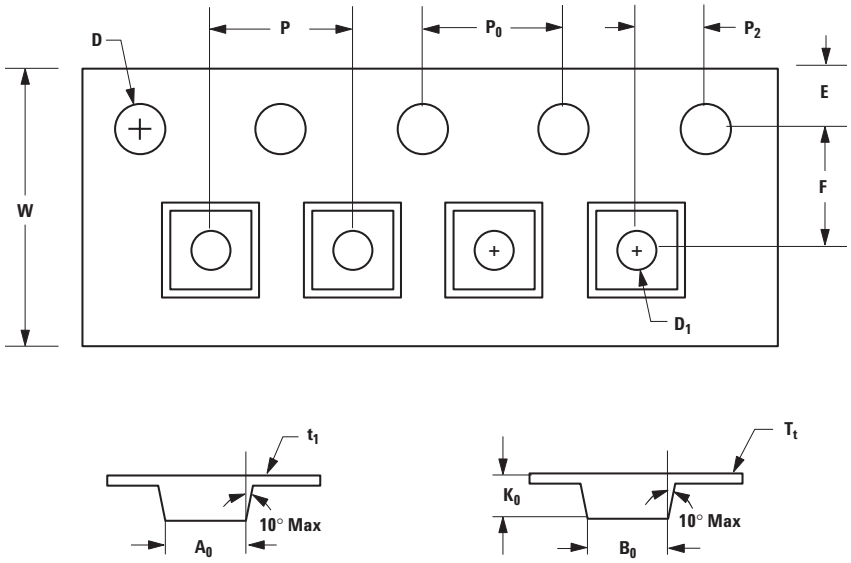
Stencil Layout (top view)

Device Orientation





Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH	A_0	2.30 ± 0.05	0.091 ± 0.004
	WIDTH	B_0	2.30 ± 0.05	0.091 ± 0.004
	DEPTH	K_0	1.00 ± 0.05	0.039 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 8.00 – 0.10	0.315 ± 0.012 0.315 ± 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

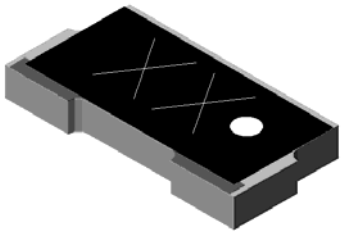
For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0845EN - August 26, 2008

Model D10AAXXZ4

RF Power

Surface Mount Attenuator
7 Watts



Description

The D10AAXXZ4 is high performance Alumina (Al2O3) surface mount attenuator intended as a lower cost alternative to Aluminum Nitride (AlN) and Beryllium Oxide (BeO). The attenuator is well suited to all cellular frequency bands such as; AMPS, GSM, DCS, PCS, PHS and UMTS. The high power handling makes the part ideal for inter-stage matching, directional couplers, and for use in isolators.

Features:

- **RoHS compliant**
- **Lowest Cost**
- **True Surface Mount**
- **Alumina Ceramic**
- **Non-Nichrome Resistive Element**
- **Low VSWR**
- **100% Tested**

General Specifications

Resistive Element	Thick film
Substrate	Alumina Ceramic
Terminal Finish	Matte Tin over Sulfamate Nickel
Operating Temperature	-55 to +125°C (see chart)

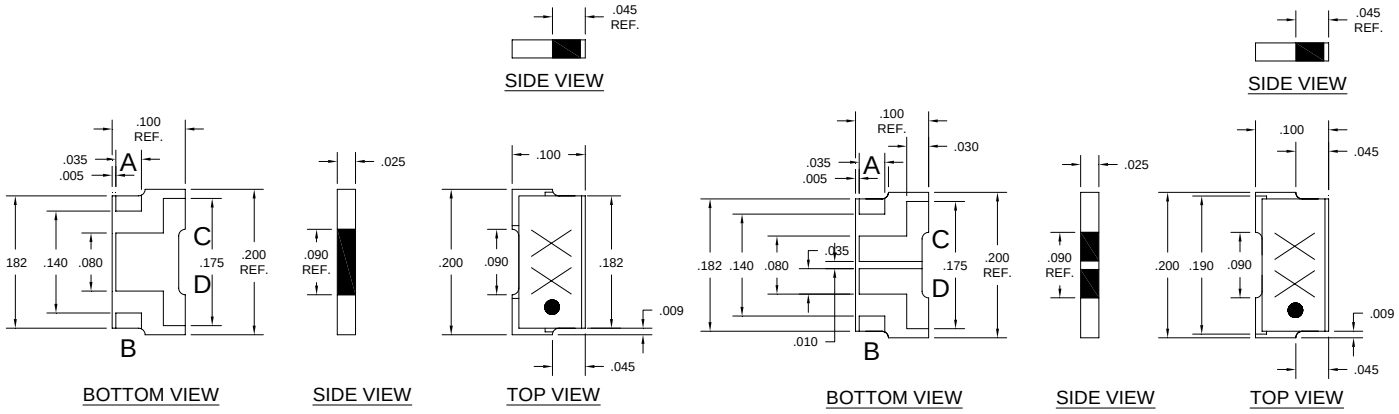
Tolerance is ±0.010", unless otherwise specified. Designed to meet of exceed applicable portions of MIL-E-5400. All dimensions in inches.

Electrical Specifications

Attenuation Value:	1 – 6, 9, 10, 20 & 30dB
Power:	7 Watts
Frequency Range:	DC – 3.0 GHz
V.S.W.R.:	<1.25:1

Specification based on unit properly installed using suggested mounting instructions and a 50 ohm nominal impedance. **Specifications subject to change.**

Outline Drawing



FOR PART NUMBERS D10AA9Z4 AND D10AA10Z4

FOR PART NUMBERS D10AA20Z4 AND D10AA30Z4

Dimensions given in inches.

Rev. 6/24/05

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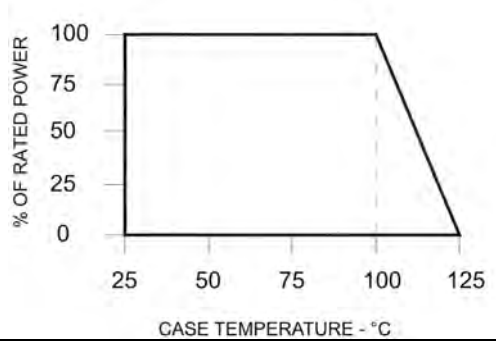
Model D10AAXXZ4

RF Power

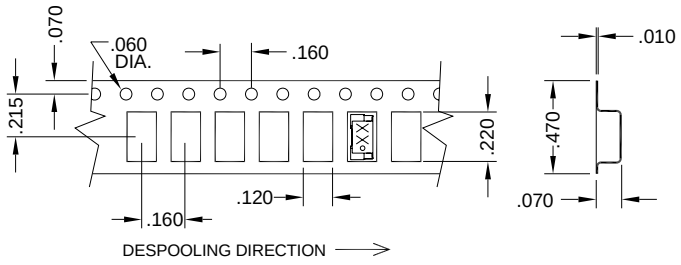
Specifications:

PART NUMBER	ATTENUATION(dB)	TOL. (±dB)	POWER (WATTS)	VSWR	FREQ (GHZ)
D10AA1Z4	1	0.30	7	1.25:1	3.0
D10AA2Z4	2	0.30	7	1.25:1	3.0
D10AA3Z4	3	0.30	7	1.25:1	3.0
D10AA4Z4	4	0.30	7	1.25:1	3.0
D10AA5Z4	5	0.30	7	1.25:1	3.0
D10AA6Z4	6	0.30	7	1.25:1	3.0
D10AA9Z4	9	0.25	7	1.25:1	3.0
D10AA10Z4	10	0.25	7	1.25:1	3.0
D10AA20Z4	20	0.50	7	1.25:1	3.0
D10AA30Z4	30	1.50	7	1.25:1	3.0

Power De-rating:

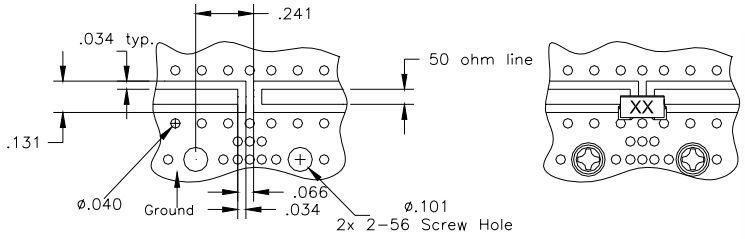


Tape & Reel:

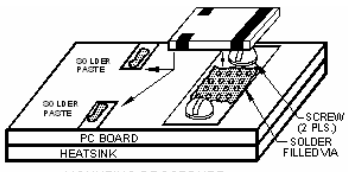


Dimension given in inches.

Mounting Footprint and Procedure:



Dimension given in inches.
For best thermal performance the PCB should be placed with thermal joint compound to the heat sink.



MOUNTING PROCEDURE

1. DRILL THERMAL VIAS THROUGH PCB AND FILL WITH SOLDER, SUCH AS Sn96.
2. SOLDER PART IN PLACE USING Sn96 TYPE SOLDER WITH A CONTROLLED TEMPERATURE IRON (260°C)
3. TO ENSURE GOOD THERMAL CONNECTIVITY TO HEAT SINK, DRILL AND TAP HEATSINK AND MOUNT PCB BOARD TO HEATSINK USING SCREWS.

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Model D10AAXXZ4

Material Declaration **D10AAXXZ4** **Matte Tin Finish**

Material	Weight			
	(lbs)	(g)	(PPM)	CAS Number
Alumina	5.889E-05	2.671E-02	7.496E+05	1344-28-1
Diethylene Glycol Ethyl Ether Acetate	2.212E-07	1.004E-04	2.818E+03	1121-52
Dipropylene Glycol Monomethyl Ether	2.976E-7	1.350E-04	3.789E+03	3459-09-48
Epoxy resin and polymers	1.323E-06	6.000E-04	1.684E+4	1002
Matte Tin	1.381E-06	6.262E-04	1.758E+04	7440-31-5
Nickel	8.416E-07	3.817E-04	1.071E+04	7440-02-0
Polymer	6.507E-07	2.952E-04	8.285E+03	
Propylene Glycol Monomethyl Ethere Acetate	1.775E-07	8.050E-05	2.259E+03	1086-56
Ruthenium	1.618E-06	7.341E-04	2.060E+04	12036-10-1
Silicon Oxide	7.490E-07	3.397E-04	9.534E+03	10097-28-6
Silver Alloy	1.062E-05	4.816E-03	1.352E+05	7440-22-4

Total Weight Calculated	7.855E-05	3.563E-02
Total Weight Measured	7.932E-05	3.598E-02

The values presented above are estimates at the current revision, and it is derived from vendor supplied data. While Anaren strives for accurate reporting, due to product and process variations at both Anaren and our suppliers, the quoted values are our best estimates only, and not measured absolute values. Product specifications are subject to change without notice.

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ECP200D

2 Watt, High Linearity InGaP HBT Amplifier

Product Features

- 400 – 2300 MHz
- 18 dB Gain @ 900 MHz
- +33 dBm P1dB
- +51 dBm Output IP3
- +5V Single Positive Supply
- Lead-free/green/RoHS-compliant 16pin 4mm QFN package

Applications

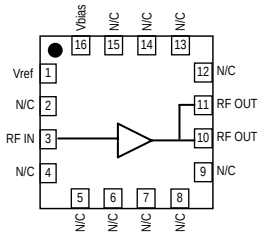
- Final stage amplifiers for Repeaters
- Mobile Infrastructure

Product Description

The ECP200D is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrowband-tuned application circuits with up to +51 dBm OIP3 and +33 dBm of compressed 1dB power. It is housed in an industry standard in a lead-free/ green/RoHS-compliant 16-pin 4x4mm QFN surface-mount package. All devices are 100% RF and DC tested.

The ECP200D is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. An internal active bias allows the ECP200D to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G base stations.

Functional Diagram



Function	Pin No.
Vref	1
RF Input	3
RF Output	10, 11
Vbias	16
GND	Backside Paddle
N/C or GND	2, 4-9, 12-15

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	400		2300
Test Frequency	MHz		2140	
Gain	dB	9	10	
Input Return Loss	dB		20	
Output Return Loss	dB		6.8	
P1dB	dBm	+32	+33.2	
Output IP3 (2)	dBm	+47	+48	
IS-95A Channel Power @ -45 dBc ACPR, 1960 MHz	dBm		+27.5	
wCDMA Channel Power @ -45 dBc ACLR, 2140 MHz	dBm		+25.3	
Noise Figure	dB		7.7	
Operating Current Range, Icc (3)	mA	700	800	900
Device Voltage, Vcc	V		+5	

1. Test conditions unless otherwise noted: 25 ºC, +5V Vsupply, 2140 MHz, in tuned application circuit.
2. 3OIP measured with two tones at an output power of +17 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8. It is expected that the current can increase by an additional 200 mA at P1dB. Pin 1 is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will pull 22mA of current when used with a series bias resistor of R1=15Ω. (ie. total device current typically will be 822 mA.)

Typical Performance (4)

Parameter	Units	Typical		
Frequency	MHz	900	1960	2140
S21 – Gain	dB	18	11	10
S11 – Input R.L.	dB	-18	-19	-20
S22 – Output R.L.	dB	-11	-6.8	-6.8
P1dB	dBm	+33	+33.4	+33.2
Output IP3	dBm	+49	+51	+48
IS-95A Channel Power @ -45 dBc ACPR	dBm	+27	+27.5	
wCDMA Channel Power @ -45 dBc ACLR	dBm			+25.3
Noise Figure	dB	8.0	7.3	7.7
Device Bias (3)		+5 V @ 800 mA		

4. Typical parameters reflect performance in a tuned application circuit at +25 °C.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power (continuous)	+28 dBm
Device Voltage	+8 V
Device Current	1400 mA
Device Power	8 W
Thermal Resistance, Rth	17.5°C/W
Junction Temperature	+200°C

Operation of this device above any of these parameters may cause permanent damage.

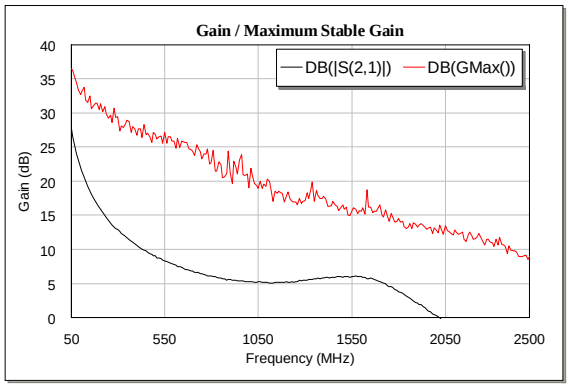
Ordering Information

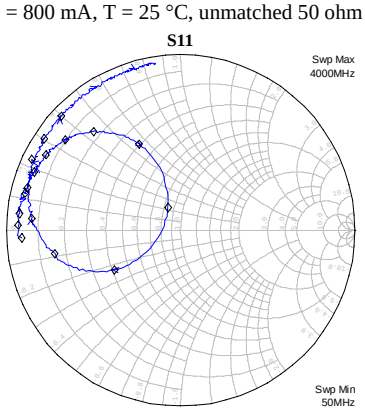
Part No.	Description
ECP200D-G	2 Watt, High Linearity InGaP HBT Amplifier (lead-free/green/RoHS-compliant 16-pin 4x4mm QFN package)
ECP200D-PCB900	900 MHz Evaluation Board
ECP200D-PCB1960	1960 MHz Evaluation Board
ECP200D-PCB2140	2140 MHz Evaluation Board

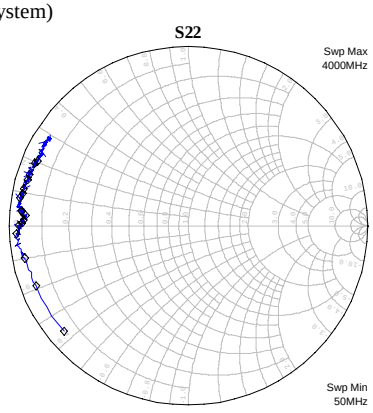
Standard tape / reel size = 1000 pieces on a 7” reel

Typical Device Data

S-Parameters (V_{CC} = +5 V, I_{CC} = 800 mA, T = 25 °C, unmatched 50 ohm system)







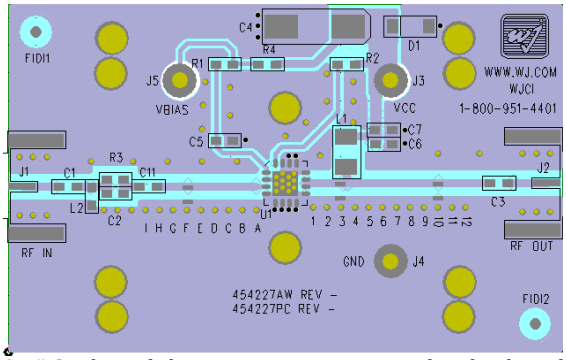
Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increments.

S-Parameters (V_{CC} = +5 V, I_{CC} = 800 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.80	-177.34	27.72	107.79	-45.30	19.06	-0.81	-139.65
100	-0.60	178.13	22.13	96.85	-43.21	11.92	-0.79	-158.43
200	-0.64	174.02	16.20	89.13	-44.86	-4.05	-0.62	-168.80
400	-0.76	166.66	10.54	80.79	-42.84	6.99	-0.35	-177.29
600	-0.89	158.43	7.75	72.52	-44.05	2.89	-0.47	179.92
800	-1.08	150.86	6.09	64.42	-43.61	-7.72	-0.66	179.00
1000	-1.54	141.98	5.29	54.50	-42.64	-4.97	-0.73	177.98
1200	-2.48	131.55	5.24	41.62	-39.25	-33.49	-0.82	176.35
1400	-5.25	115.96	5.83	20.85	-39.43	-52.73	-0.58	175.10
1600	-16.57	118.86	6.03	-9.41	-37.39	-100.38	-0.58	174.84
1800	-7.12	-149.33	3.81	-47.41	-39.26	-126.48	-0.42	170.66
2000	-2.68	-169.62	0.37	-72.56	-40.69	-169.19	-0.52	169.04
2200	-1.34	175.50	-3.32	-89.96	-45.63	-163.76	-0.53	167.35
2400	-0.80	164.47	-6.81	-102.05	-50.41	149.05	-0.61	164.01
2600	-0.49	154.67	-9.46	-112.59	-48.80	157.02	-0.62	162.14
2800	-0.53	146.29	-12.22	-121.23	-50.62	69.74	-0.68	157.85
3000	-0.50	136.44	-14.55	-128.37	-49.46	79.86	-0.77	156.81

Device S-parameters are available for download from the website at: http://www.wj.com

Application Circuit PC Board Layout



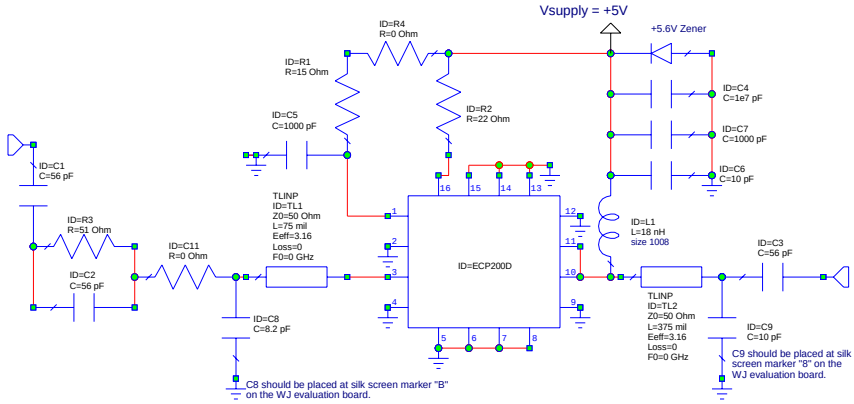
Circuit Board Material: .014” Getek, single layer, 1 oz copper, Microstrip line details: width = .026”, spacing = .026”
The silk screen markers ‘A’, ‘B’, ‘C’, etc. and ‘1’, ‘2’, ‘3’, etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050” increments.

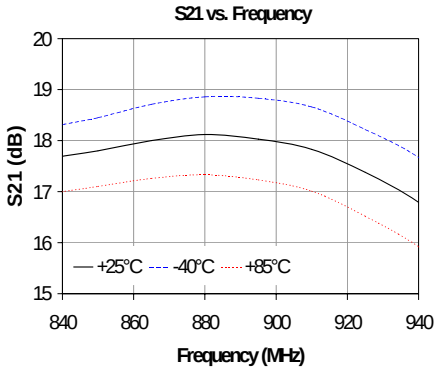
900 MHz Application Circuit (ECP200D-PCB900)

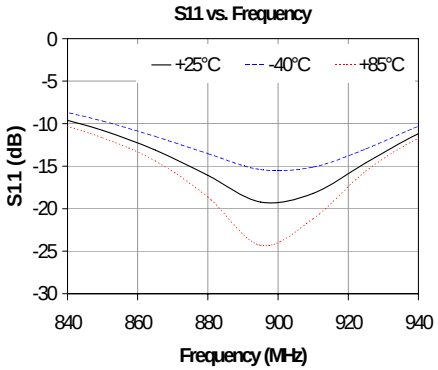
Typical RF Performance at 25 °C

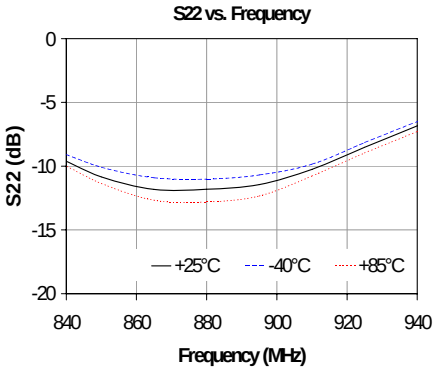
Frequency	900 MHz
S21 – Gain	18 dB
S11 – Input Return Loss	-18 dB
S22 – Output Return Loss	-11 dB
Output P1dB	+33 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+49 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+27 dBm
Noise Figure	8.0 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	800 mA

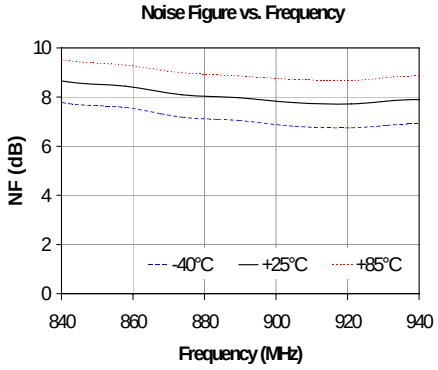
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

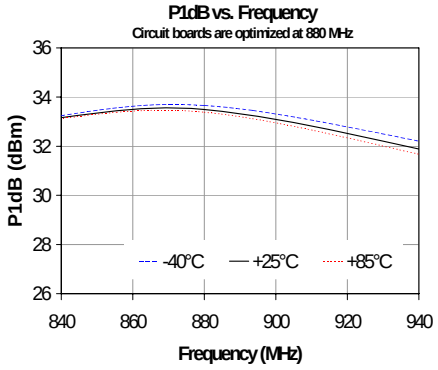


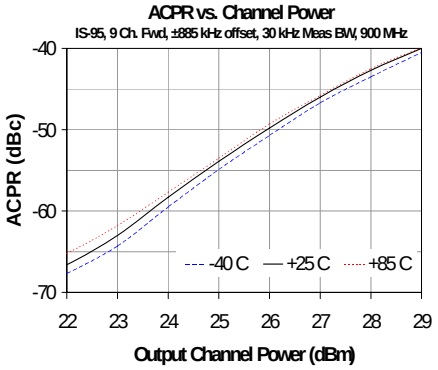


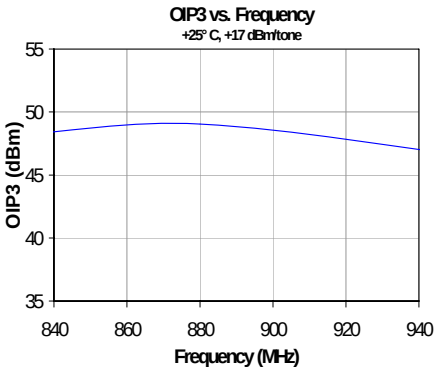


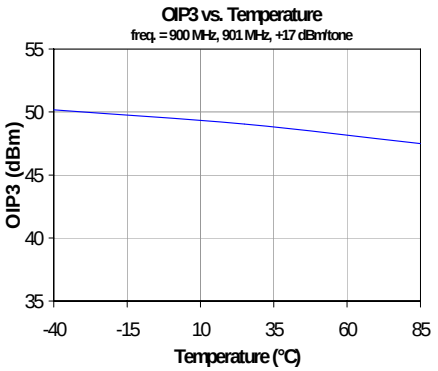


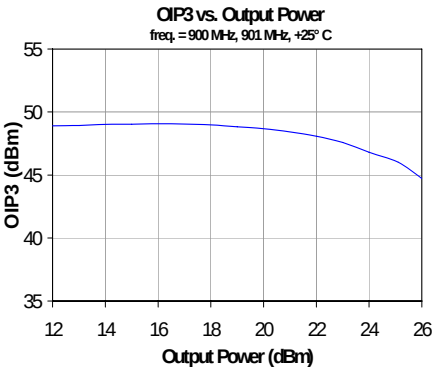












ECP200D

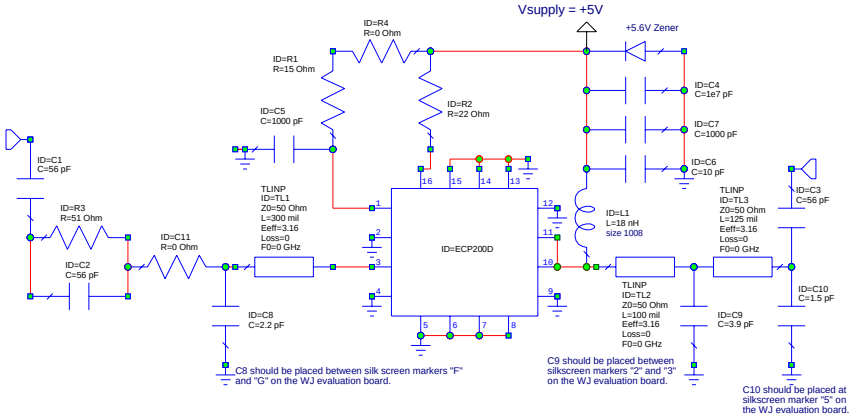
2 Watt, High Linearity InGaP HBT Amplifier

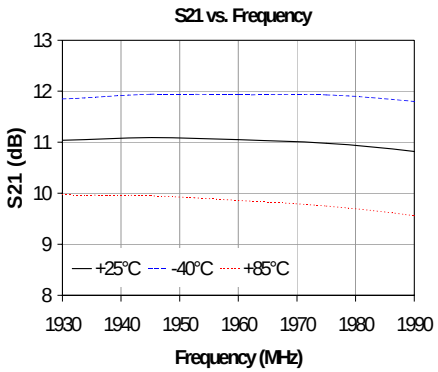
1960 MHz Application Circuit (ECP200D-PCB1960)

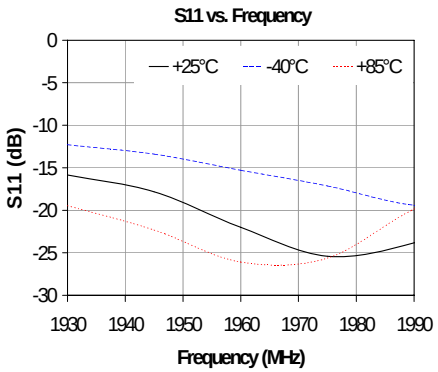
Typical RF Performance at 25 °C

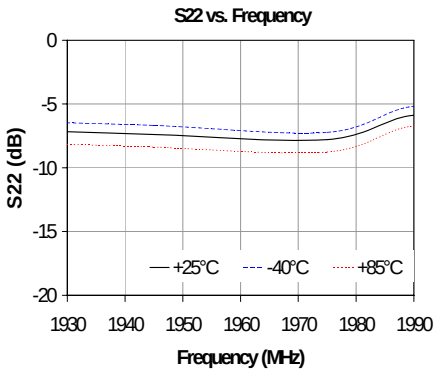
Frequency	1960 MHz
S21 – Gain	11 dB
S11 – Input Return Loss	-20 dB
S22 – Output Return Loss	-6.8 dB
Output P1dB	+33.4 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+51 dBm
Channel Power (@-45 dBc ACPR, IS-95 9 channels fwd)	+27.5 dB
Noise Figure	7.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	800 mA

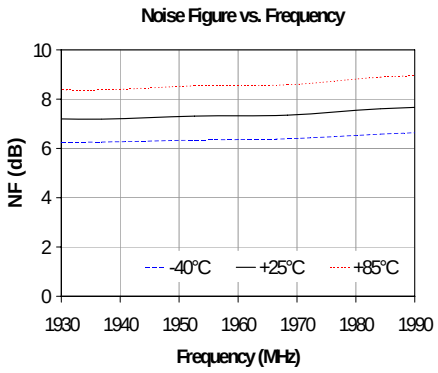
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

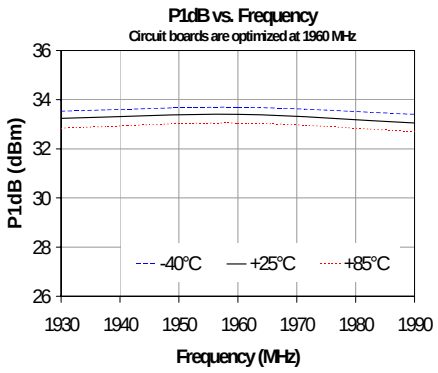


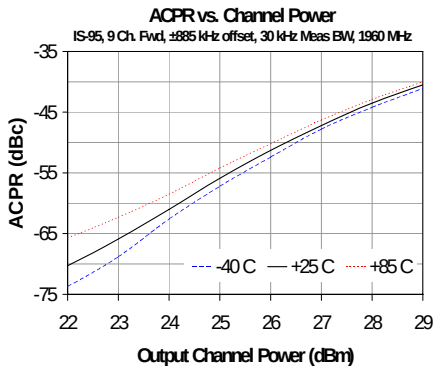


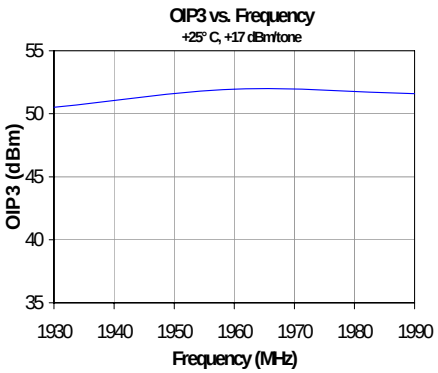


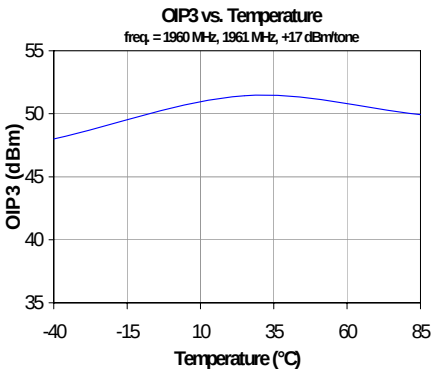


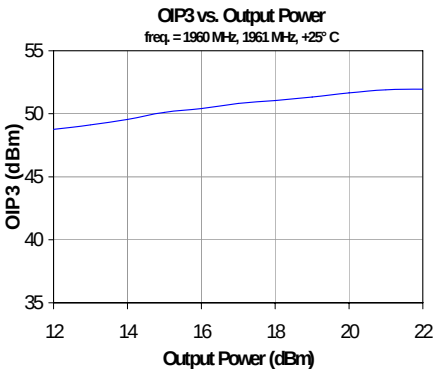










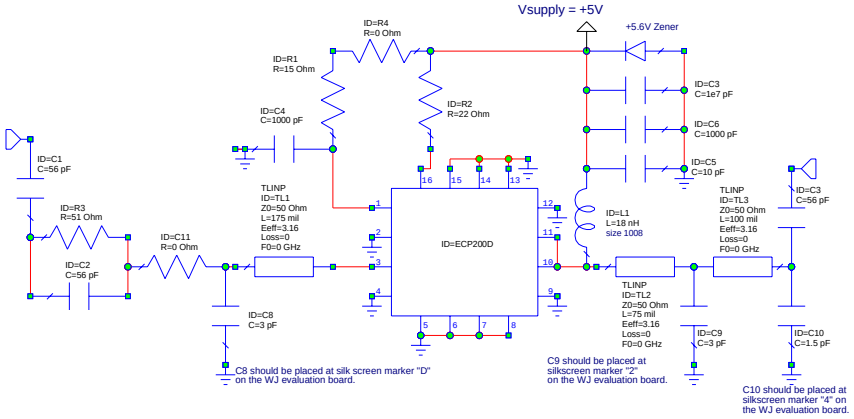


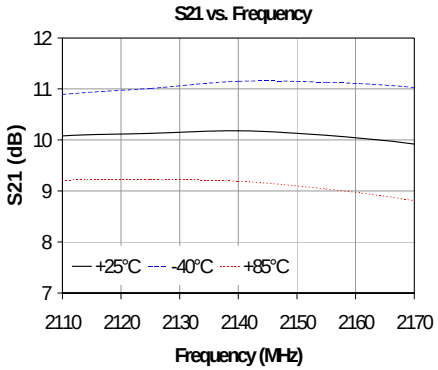
2140 MHz Application Circuit (ECP200D-PCB2140)

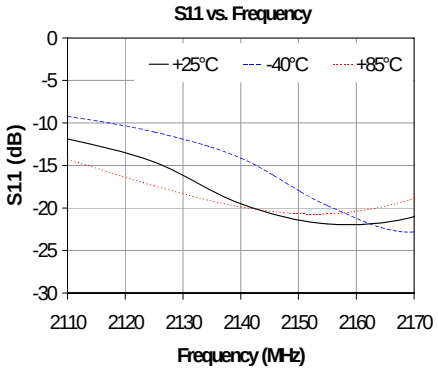
Typical RF Performance at 25 °C

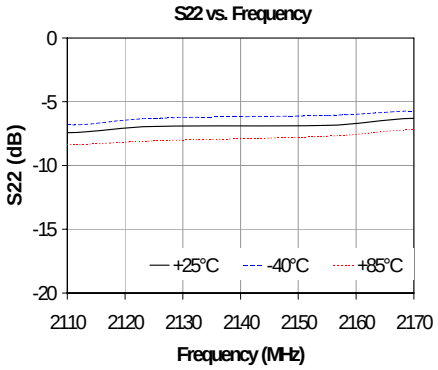
Frequency	2140 MHz
S21 – Gain	10 dB
S11 – Input Return Loss	-20 dB
S22 – Output Return Loss	-6.8 dB
Output P1dB	+33.2 dBm
Output IP3 (+17 dBm / tone, 1 MHz spacing)	+48 dBm
W-CDMA Channel Power (@ -45 dBc ACLR)	+25.3 dBm
Noise Figure	7.7 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	800 mA

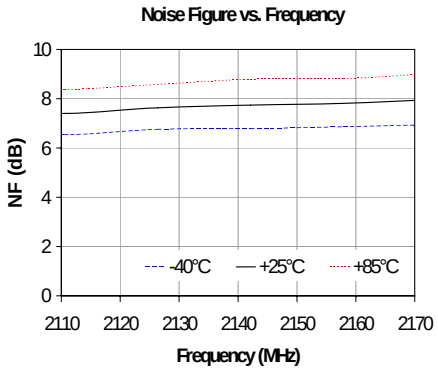
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

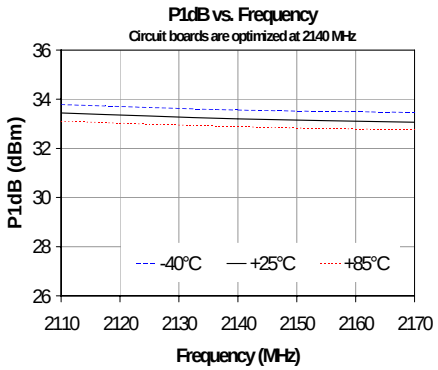


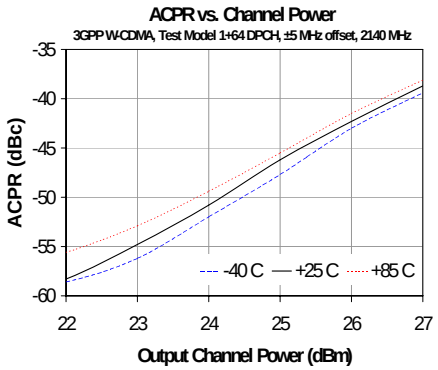


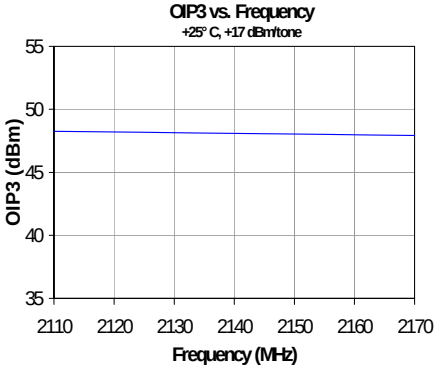


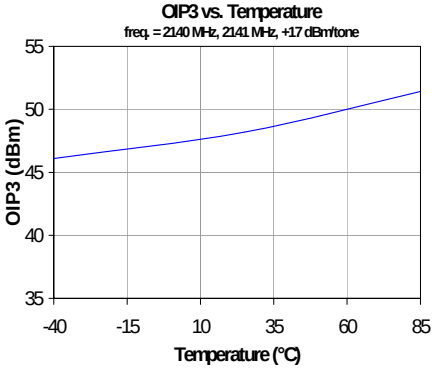


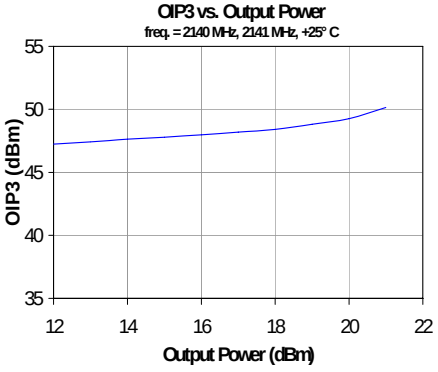








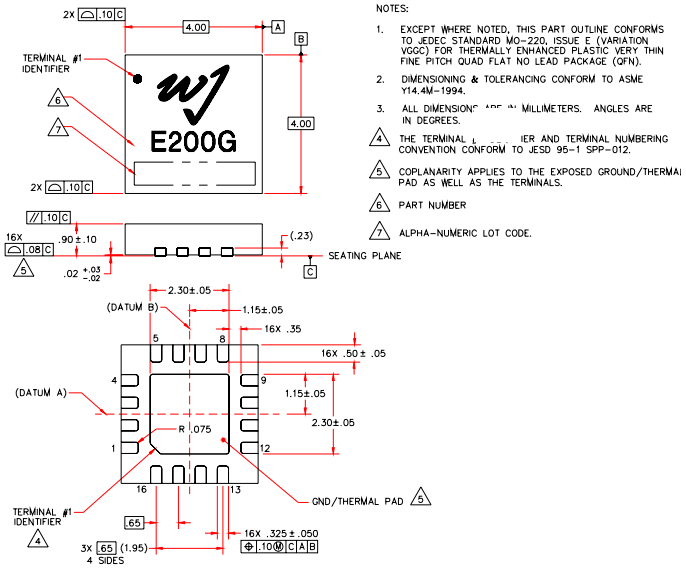




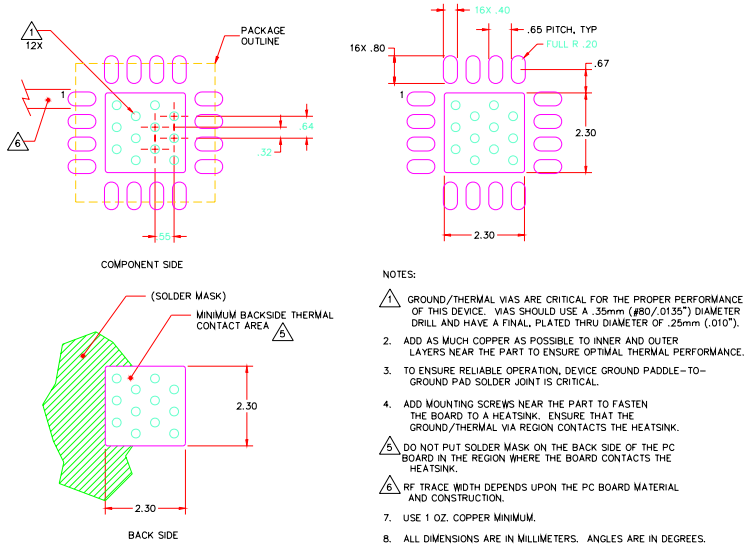
ECP200D-G Mechanical Information

This package is lead-free/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

Outline Drawing



Land Pattern



Product Marking

The component will be marked with an "E200G" designator with an alphanumeric lot code on the top surface of the package. The obsolete tin-lead package is marked with an "ECP200D" designator followed by an alphanumeric lot code.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes between 500 and 1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 2 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

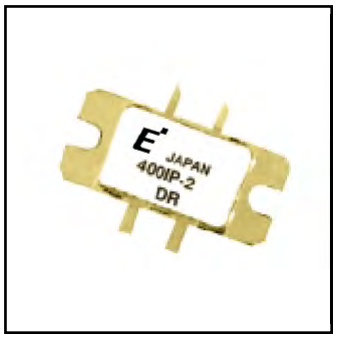
1. A heatsink underneath the area of the PCB for the mounted device is highly recommended for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

FLL400IP-2

L-Band Medium & High Power GaAs FET

FEATURES

- Push-Pull Configuration
- High Power Output: 35W (Typ.)
- High PAE: 44% (Typ.)
- Broad Frequency Range: 800 to 2000 MHz.
- Suitable for class A operation at 10V and class AB operation at 12V



DESCRIPTION

The FLL400IP-2 is a 35 Watt GaAs FET that employs a push-pull design which offers ease of matching, greater consistency and a broader bandwidth for high power L-band amplifiers. This product is targeted to reduce the size and complexity of highly linear, high power base station transmitting amplifiers. This new product is uniquely suited for use in PCS/PCN base station amplifiers as it offers high gain, long term reliability and ease of use.

APPLICATIONS

- Solid State Base-Station Power Amplifier.
- PCS/PCN Communication Systems.

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta=25°C)

Parameter	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	Tc = 25°C	107	W
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		+175	°C

Eudyna recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 12 volts.
2. The forward and reverse gate currents should not exceed 54.4 and -17.4 mA respectively with gate resistance of 25Ω.
3. The operating channel temperature (T_{ch}) should not exceed 145°C.

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

Item	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS}=0V	-	12	16	A
Transconductance	gm	V_{DS} = 5V, I_{DS}=7.2A	-	6000	-	mS
Pinch-Off Voltage	V_p	V_{DS} = 5V, I_{DS}=720mA	-1.0	-2.0	-3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	I_{GS} = -720µA	-5	-	-	V
Output Power at 1 dB G.C.P.	P_{1dB}	V_{DS} = 12V f=1.96GHz I_{DS} = 2A	44.5	45.5	-	dBm
Power Gain at 1 dB G.C.P.	G_{1dB}		9.0	10.0	-	dB
Drain Current	I_{DSR}		-	6.0	8.0	A
Power-Added Efficiency	η_{add}		-	44	-	%
Output Power at 1 dB G.C.P.	P_{1dB}	V_{DS} = 10V f=1.96GHz I_{DS} = 2A	-	44.5	-	dBm
Power Gain at 1 dB G.C.P.	G_{1dB}		-	10.0	-	dB
Thermal Resistance	R_{th}	Channel to Case	-	1.0	1.4	°C/W

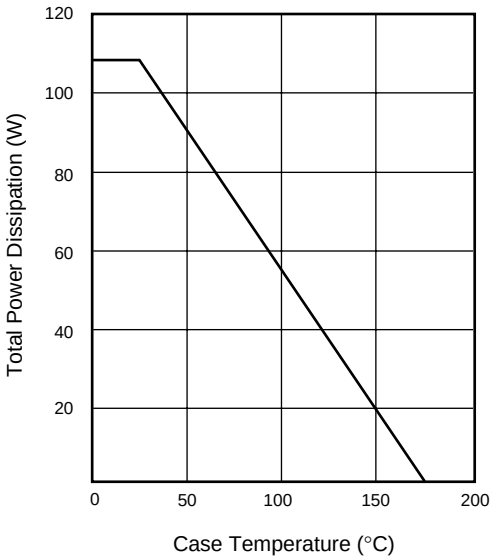
CASE STYLE: IP

G.C.P.: Gain Compression Point

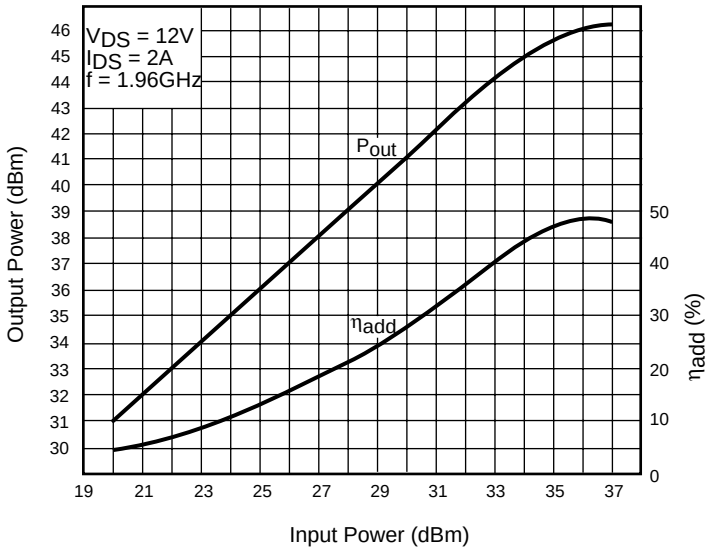
Eudyna

Edition 1.6
December 1999

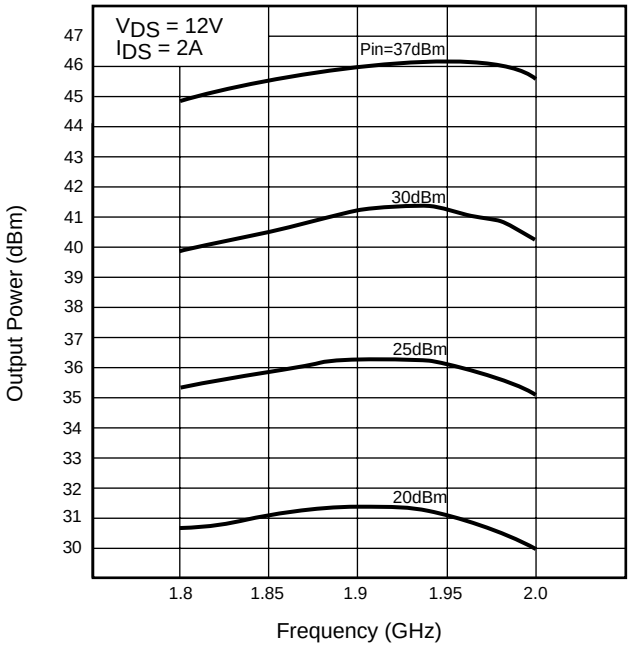
POWER DERATING CURVE



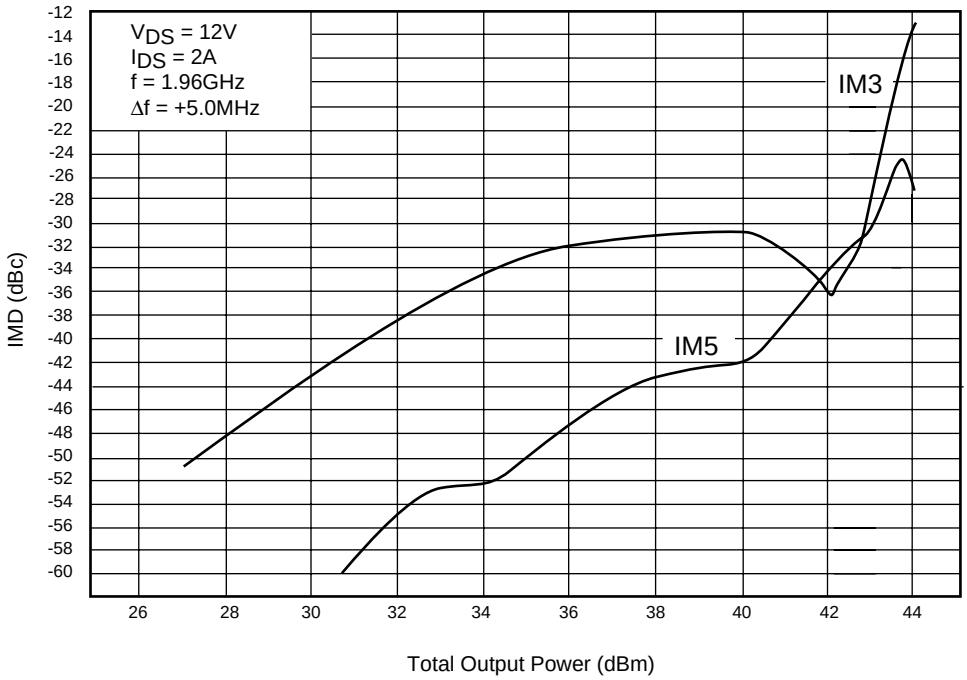
OUTPUT POWER & ηadd vs. INPUT POWER



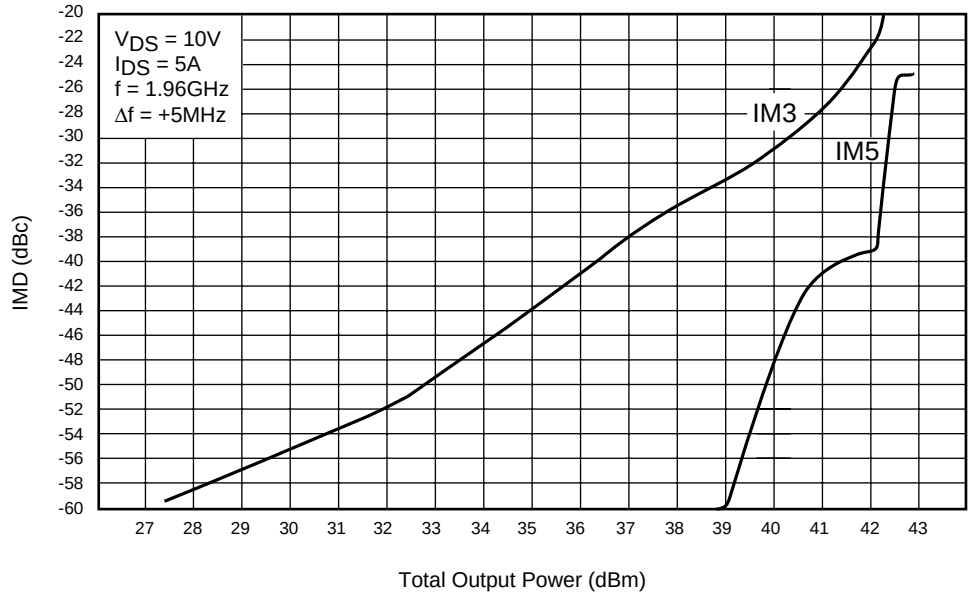
OUTPUT POWER vs. FREQUENCY



OUTPUT POWER vs. IMD

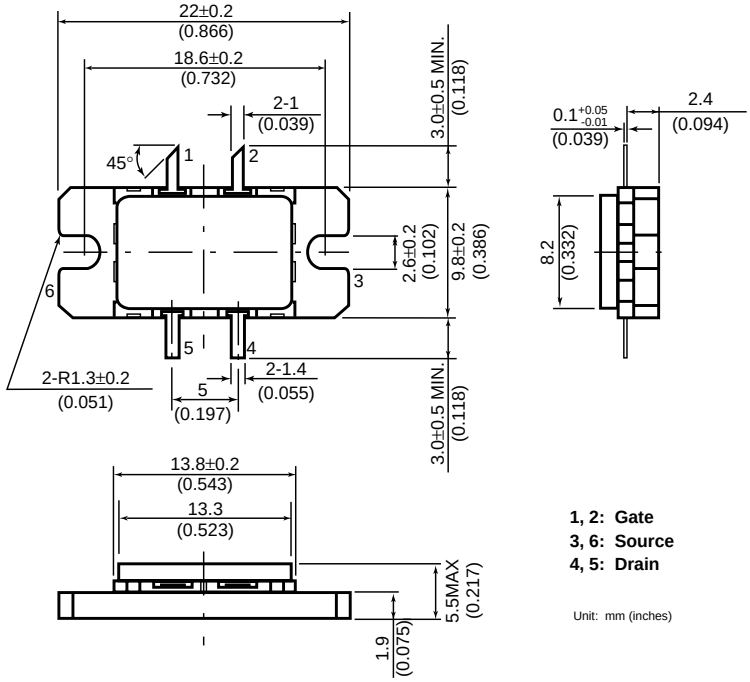


OUTPUT POWER vs. IMD



Case Style "IP"

Metal-Ceramic Hermetic Package



FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21360-4E

ASSP

Single Serial Input PLL Frequency Synthesizer On-chip 2.0 GHz Prescaler

MB15E05SL

■ DESCRIPTION

The Fujitsu MB15E05SL is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.0 GHz prescaler. The 2.0 GHz prescaler has a dual modulus division ratio of 64/65 or 128/129 enabling pulse swallowing operation.

The supply voltage range is between 2.4 V and 3.6 V. The MB15E05SL uses the latest BiCMOS process, as a result the supply current is typically 3.0 mA at 2.7 V. A refined charge pump supplies well-balanced output currents of 1.5 mA and 6 mA. The charge pump current is selectable by serial data.

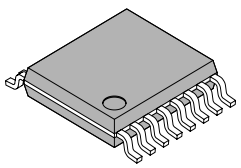
MB15E05SL is ideally suited for wireless mobile communications, such as GSM (Global System for Mobile Communications) and PCS.

■ FEATURES

- High frequency operation: 2.0 GHz max
- Low power supply voltage: V_{CC} = 2.4 to 3.6 V
- Ultra Low power supply current: I_{CC} = 3.0 mA typ. (V_{CC} = Vp = 2.7 V, Ta = +25°C, in locking state)
  I_{CC} = 3.5 mA typ. (V_{CC} = Vp = 3.0 V, Ta = +25°C, in locking state)
- Direct power saving function: Power supply current in power saving mode
  Typ. 0.1 µA (V_{CC} = Vp = 3.0 V, Ta = +25°C), Max. 10 µA (V_{CC} = Vp = 3.0 V)
- Dual modulus prescaler: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Software selectable charge pump current
- On-chip phase control for phase comparator
- Operating temperature: Ta = –40 to +85°C
- Pin compatible with MB15E05, MB15E05L

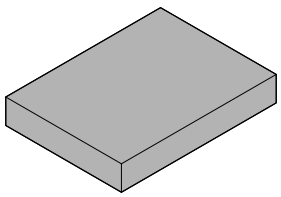
■ PACKAGES

16-pin plastic SSOP



(FPT-16P-M05)

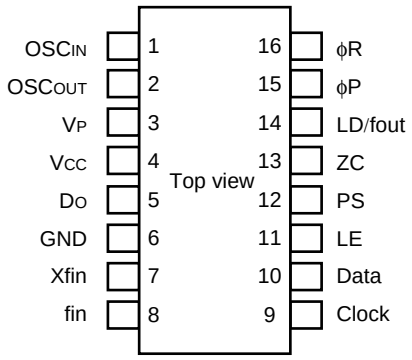
16-pad plastic BCC



(LCC-16P-M06)

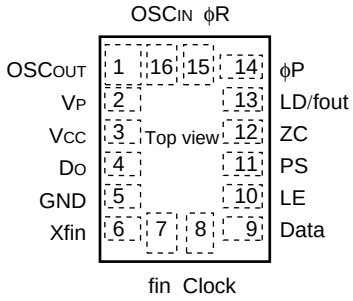
■ PIN ASSIGNMENTS

16-pin SSOP



(FPT-16P-M05)

16-pad BCC

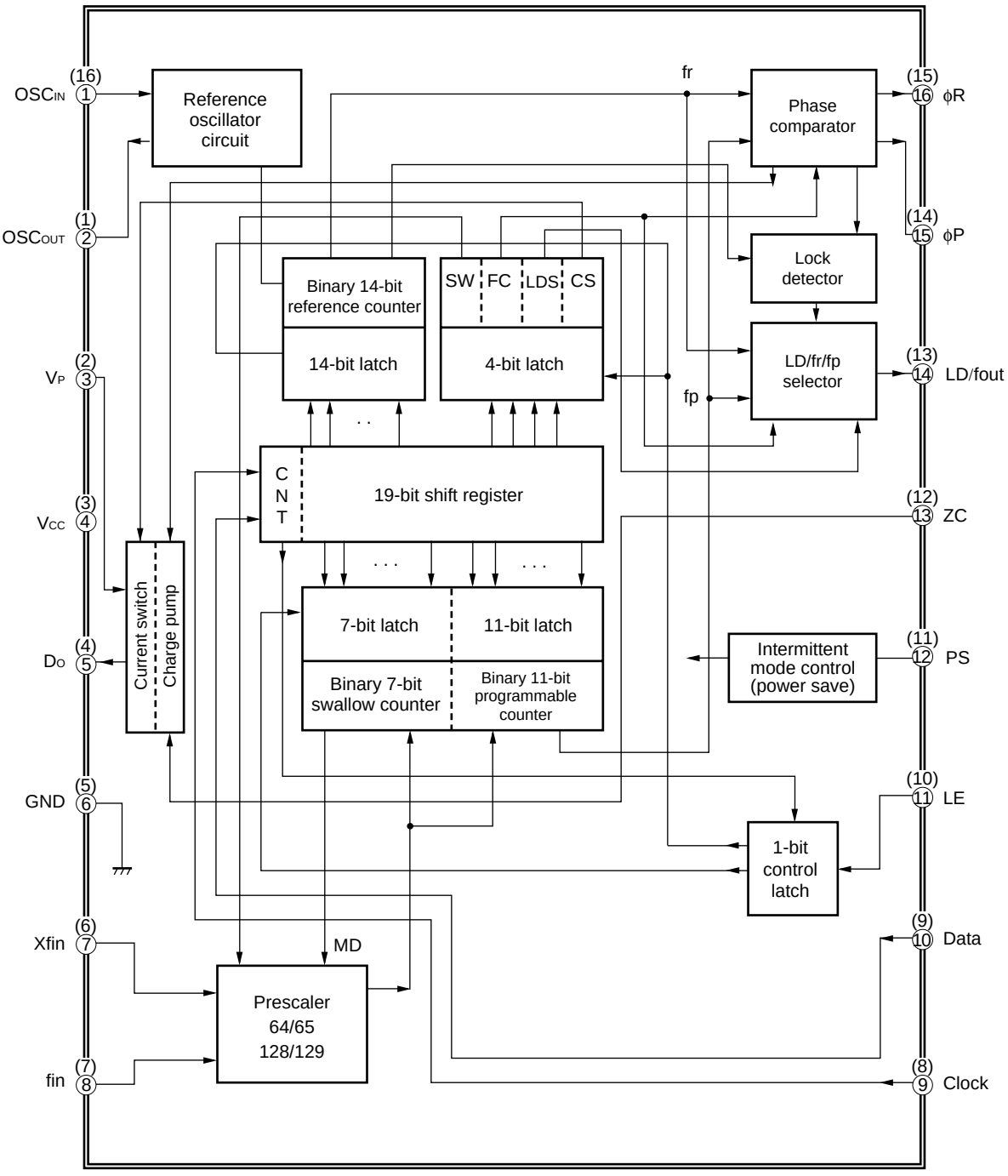


(LCC-16P-M06)

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Descriptions
SSOP	BCC			
1	16	OSC_{IN}	I	Programmable reference divider input. Connection to a TCXO.
2	1	OSC_{OUT}	O	Oscillator output.
3	2	V_P	–	Power supply voltage input for the charge pump.
4	3	V_{CC}	–	Power supply voltage input.
5	4	D_O	O	Charge pump output. Phase of the charge pump can be selected via programming of the FC bit.
6	5	GND	–	Ground.
7	6	Xfin	I	Prescaler complementary input, which should be grounded via a capacitor.
8	7	fin	I	Prescaler input. Connection to an external VCO should be done via AC coupling.
9	8	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	9	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.)
11	10	LE	I	Load enable signal input. (Open is prohibited.) When LE is set high, the data in the shift register is transferred to a latch according to the control bit in the serial data.
12	11	PS	I	Power saving mode control. This pin must be set at “L” at Power-ON. (Open is prohibited.) PS = “H”; Normal mode PS = “L”; Power saving mode
13	12	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = “H”; Normal Do output. ZC = “L”; Do becomes high impedance.
14	13	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout). The output signal is selected via programming of the LDS bit. LDS = “H”; outputs fout (fr/fp monitoring output) LDS = “L”; outputs LD (“H” at locking, “L” at unlocking.)
15	14	ϕP	O	Phase comparator N-channel open drain output for an external charge pump. Phase can be selected via programming of the FC bit.
16	15	ϕR	O	Phase comparator CMOS output for an external charge pump. Phase can be selected via programming of the FC bit.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit	Remark
			Min.	Max.		
Power supply voltage	V_{CC}	–	–0.5	4.0	V	
	V_P	–	V_{CC}	6.0	V	
Input voltage	V_I	–	–0.5	V_{CC} +0.5	V	
Output voltage	V_O	Except Do	GND	V_{CC}	V	
	V_O	Do	GND	V_P	V	
Storage temperature	Tstg	–	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.4	3.0	3.6	V	
	V_P	V_{CC}	–	5.5	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

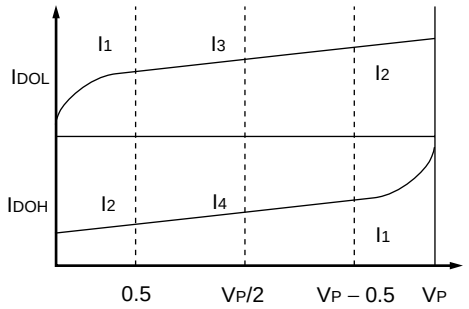
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.4 to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
Power supply current*1		I_{CC}	fin = 2000 MHz, V_{CC} = V_P = 2.7 V (V_{CC} = V_P = 3.0 V)		–	3.0 (3.5)	–	mA
Power saving current		I_{PS}	ZC = "H" or open		–	0.1*2	10	µA
Operating frequency	fin	f_{IN}	–		100	–	2000	MHz
	OSC_{IN}	fosc	–		3	–	40	MHz
Input sensitivity	fin*3	Pfin	50 Ω system (Refer to the measurement circuit.)		–15	–	+2	dBm
	OSC_{IN}*3	V_{OSC}	–		0.5	–	V_{CC}	Vp-p
"H" level input voltage	Data, Clock, LE, PS, ZC	V_{IH}	–		$V_{CC} \times 0.7$	–	–	V
"L" level input voltage		V_{IL}	–		–	–	$V_{CC} \times 0.3$	
"H" level input current	Data, Clock, LE, PS	I_{IH}*4	–		–1.0	–	+1.0	µA
"L" level input current		I_{IL}*4	–		–1.0	–	+1.0	
"H" level input current	OSC_{IN}	I_{IH}	–		0	–	+100	µA
"L" level input current		I_{IL}*4	–		–100	–	0	
"H" level input current	ZC	I_{IH}*4	–		–1.0	–	+1.0	µA
"L" level input current		I_{IL}*4	Pull up input		–100	–	0	
"L" level output voltage	ϕP	V_{OL}	Open drain output		–	–	0.4	V
"H" level output voltage	ϕR, LD/fout	V_{OH}	V_{CC} = V_P = 3.0 V, I_{OH} = –1 mA		V_{CC} – 0.4	–	–	V
"L" level output voltage		V_{OL}	V_{CC} = V_P = 3.0 V, I_{OL} = 1 mA		–	–	0.4	
"H" level output voltage	Do	V_{DOH}	V_{CC} = V_P = 3.0 V, I_{DOH} = –0.5 mA		V_P – 0.4	–	–	V
"L" level output voltage		V_{DOL}	V_{CC} = V_P = 3.0 V, I_{DOL} = 0.5 mA		–	–	0.4	
High impedance cutoff current	Do	I_{OFF}	V_{CC} = V_P = 3.0 V, V_{OFF} = 0.5 V to V_P – 0.5 V		–	–	2.5	nA
"L" level output current	ϕP	I_{OL}	Open drain output		1.0	–	–	mA
"H" level output current	ϕR, LD/fout	I_{OH}	–		–	–	–1.0	mA
"L" level output current		I_{OL}	–		1.0	–	–	
"H" level output current	Do	I_{DOH}*4	V_{CC} = 3 V, V_P = 3 V, V_{DO} = V_P/2, Ta = +25°C	CS bit = "H"	–	–6.0	–	mA
				CS bit = "L"	–	–1.5	–	
"L" level output current		I_{DOL}		CS bit = "H"	–	6.0	–	
				CS bit = "L"	–	1.5	–	
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT}*5	V_{DO} = V_P/2		–	3	–	%
	vs V_{DO}	I_{DOVD}*6	0.5 V ≤ V_{DO} ≤ V_P – 0.5 V		–	10	–	%
	vs Ta	I_{DOTA}*7	– 40°C ≤ Ta ≤ +85°C		–	10	–	%

*1: Conditions; fosc = 12 MHz, Ta = +25°C, in locking state.
*2: $V_{CC} = V_P = 3.0$ V, fosc = 12.8 MHz, Ta = +25°C, in power saving mode
*3: AC coupling. 1000 pF capacitor is connected under the condition of min. operating frequency.
*4: The symbol "–" (minus) means direction of current flow.
*5: $V_{CC} = V_P = 3.0$ V, Ta = +25°C $(|I_3| - |I_4|) / [(|I_3| + |I_4|) /2] \times 100(\%)$
*6: $V_{CC} = V_P = 3.0$ V, Ta = +25°C $[(|I_2| - |I_1|) /2] / [(|I_1| + |I_2|) /2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
*7: $V_{CC} = V_P = 3.0$ V, $V_{DO} = V_P/2$ $(|I_{DO(+85°C)} - I_{DO(-40°C)}| /2) / (|I_{DO(+85°C)} + I_{DO(-40°C)}| /2) \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})



■ FUNCTIONAL DESCRIPTION

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)
- M : Preset divide ratio of modulus prescaler (64 or 128)

2. Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, stored data is latched according to the control bit data as follows:

Table 1. Control Bit

Control bit (CNT)	Destination of serial data
H	For the programmable reference divider
L	For the programmable divider

(1) Shift Register Configuration

Programmable Reference Counter

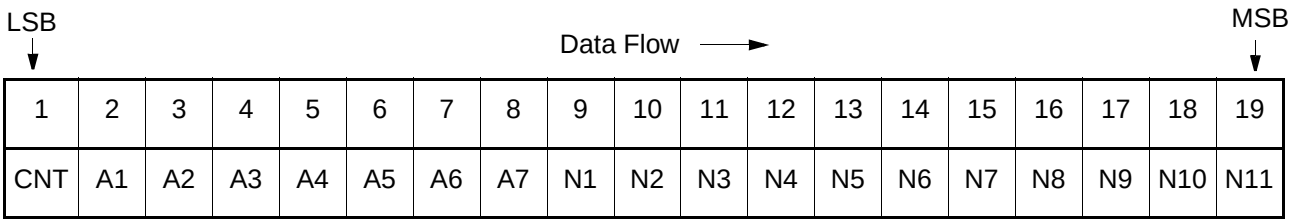
LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS	CS

CNT	: Control bit	[Table 1]
R1 to R14	: Divide ratio setting bit for the programmable reference counter (3 to 16,383)	[Table 2]
SW	: Divide ratio setting bit for the prescaler (64/65 or 128/129)	[Table 5]
FC	: Phase control bit for the phase comparator	[Table 8]
LDS	: LD/f_{OUT} signal select bit	[Table 7]
CS	: Charge pump current select bit	[Table 6]

Note: Start data input with MSB first.

Programmable Counter



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT : Control bit [Table 1]
N1 to N11: Divide ratio setting bits for the programmable counter (3 to 2,047) [Table 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table 4]

Note: Data input with MSB first.

Table 2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio(R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Binary 11-bit Programmable Counter Data Setting

Divide ratio(N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 4. Binary 7-bit Swallow Counter Data Setting

Divide ratio(A)	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Table 5. Prescaler Data Setting

SW	Prescaler divide ratio
H	64/65
L	128/129

Table 6. Charge Pump Current Setting

CS	Current value
H	±6.0 mA
L	±1.5 mA

Table 7. LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

(2) Relation between the FC Input and Phase Characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (fout) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ϕR, and ϕP is shown below.

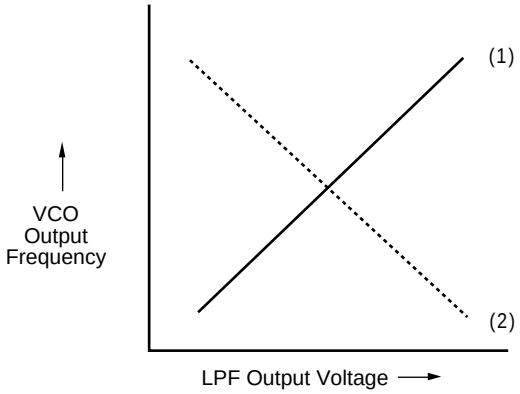
Table 8. FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	D_O	ϕR	ϕP	LD/fout	D_O	ϕR	ϕP	LD/fout
$fr > f_P$	H	L	L	fout = fr	L	H	Z*	fout = fp
$fr < f_P$	L	H	Z*		H	L	L	
$fr = f_P$	Z*	L	Z*		Z*	L	Z*	

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

- When the LPF and VCO characteristics are similar to (1), set FC bit high.
- When the VCO characteristics are similar to (2), set FC bit low.



3. Do Output Control

Table 9. ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

4. Power Saving Mode (Intermittent Mode Control Circuit)

Table 10. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the signal PLL, the lock detector, LD, remains high, indicating a locked condition.

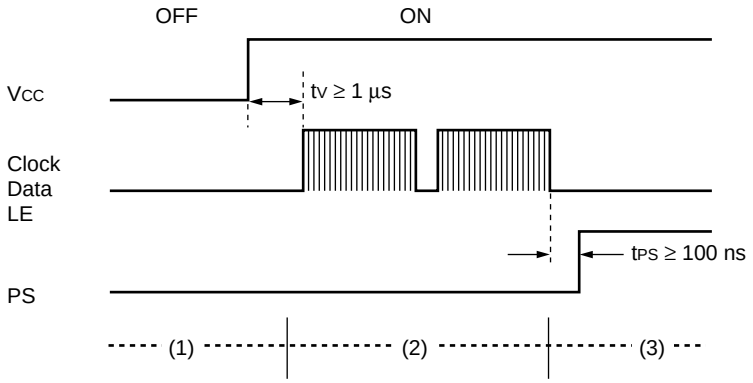
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

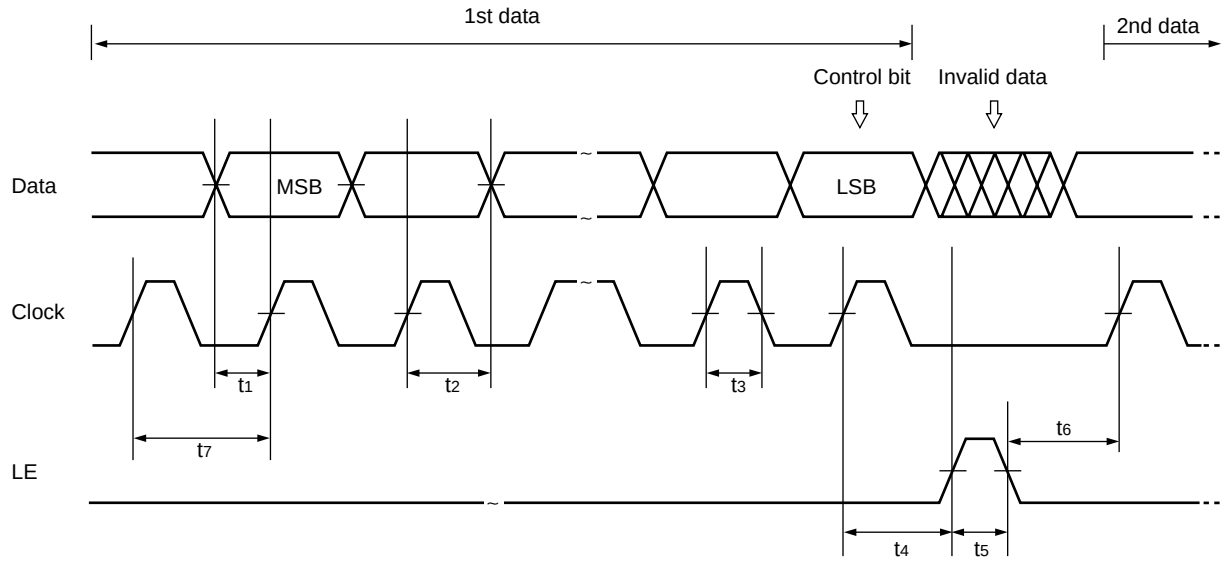
Note: When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 µs.

Note: • PS pin must be set “L” for Power-ON.



(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2$ V).
(3) Release power saving mode (PS: “L” → “H”) 100 ns later after setting serial data.

■ SERIAL DATA INPUT TIMING



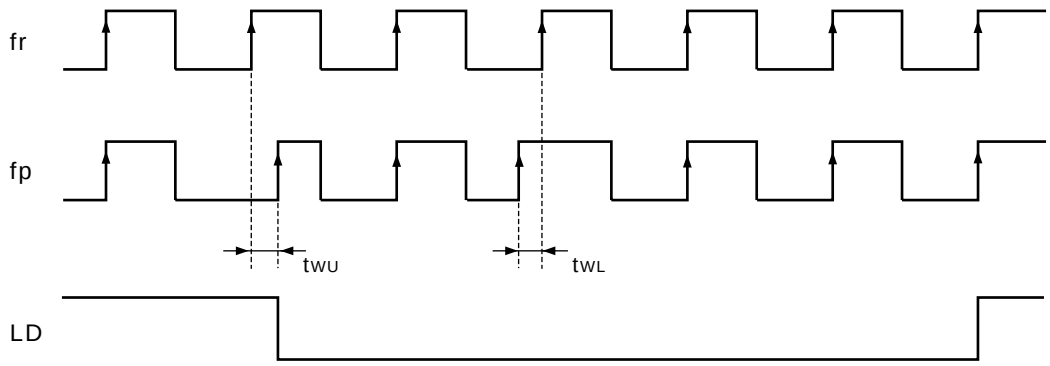
On the rising edge of the clock, one bit of data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t_1	20	–	–	ns
t_2	20	–	–	ns
t_3	30	–	–	ns
t_4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	100	–	–	ns
t_6	20	–	–	ns
t_7	100	–	–	ns

Note: LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM

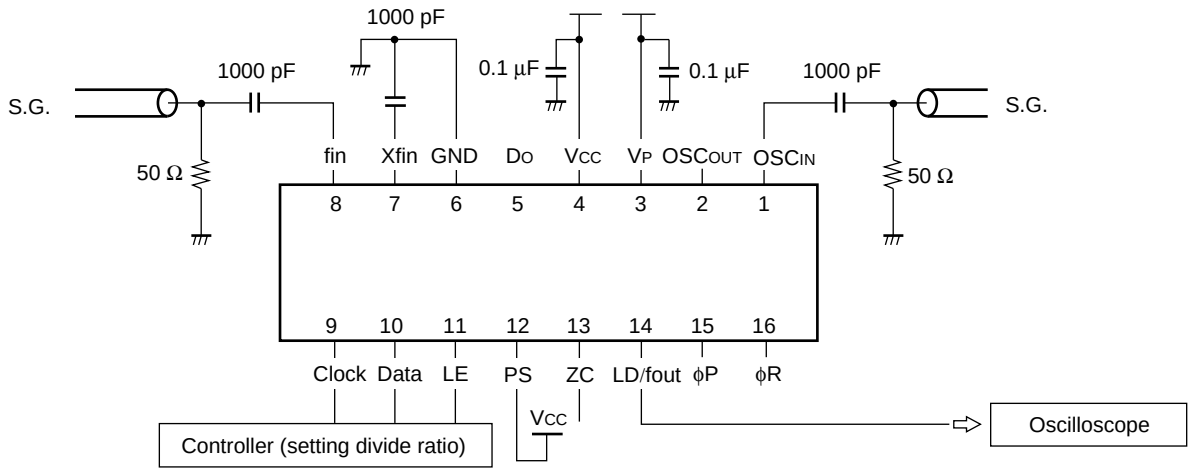


[FC = “H”]

[FC = “L”]

Notes:
- Phase error detection range: -2π to $+2\pi$
- Pulses on Do signal during locked state are output to prevent dead zone.
- LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency.
  $t_{WU} \geq 2/fosc$ (s) (e. g. $t_{WU} \geq 156.3$ ns, fosc = 12.8 MHz)
  $t_{WU} \leq 4/fosc$ (s) (e. g. $t_{WL} \leq 312.5$ ns, fosc = 12.8 MHz)
- LD becomes high during the power saving mode (PS = “L”).

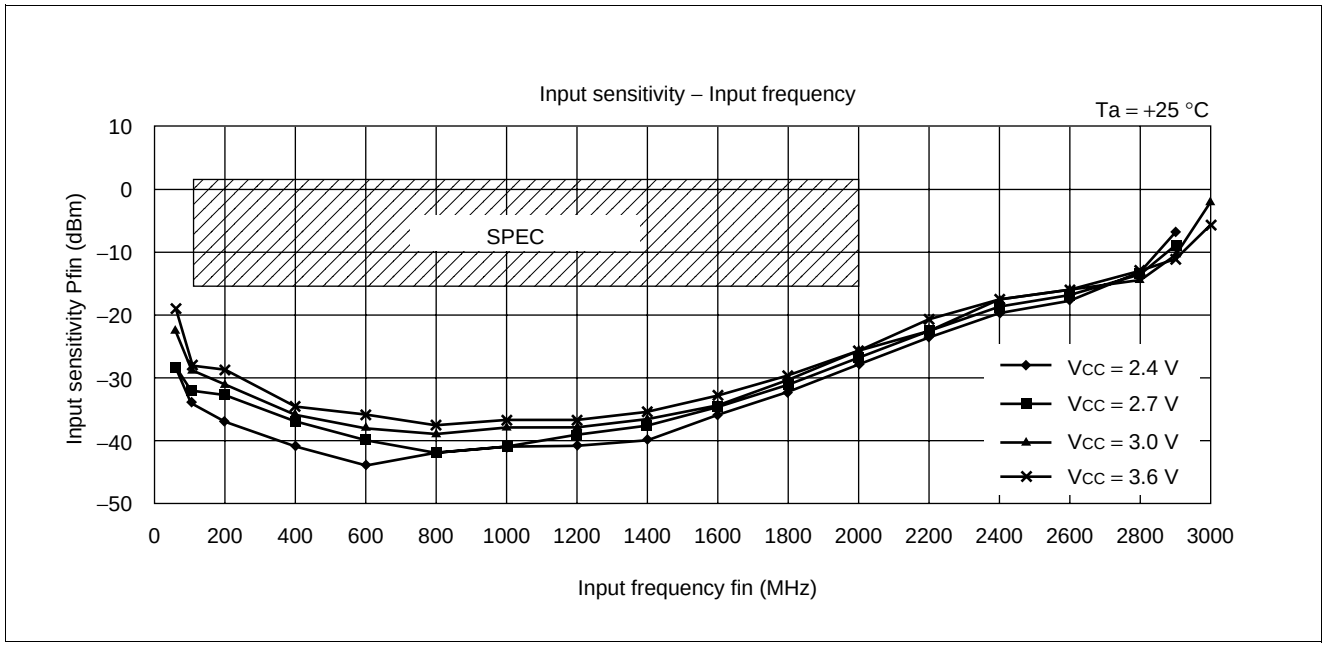
■ MEASURMENT CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})



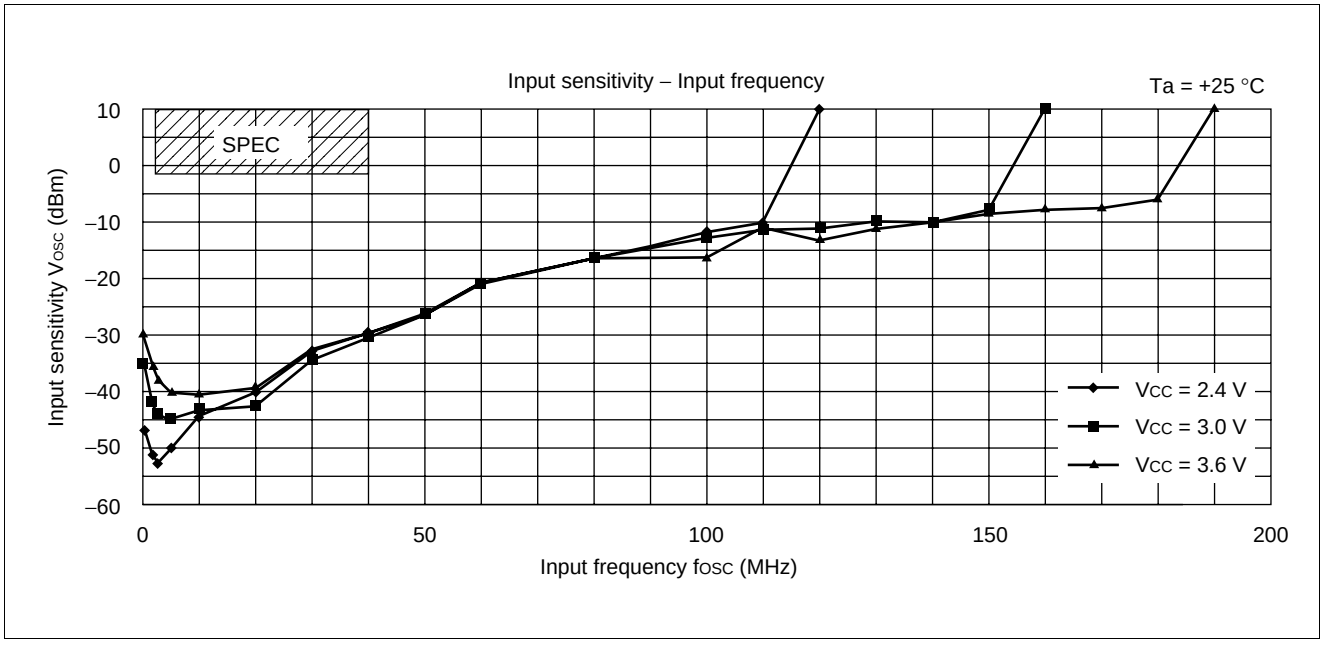
Note: SSOP-16

■ TYPICAL CHARACTERISTICS

1. fin input sensitivity

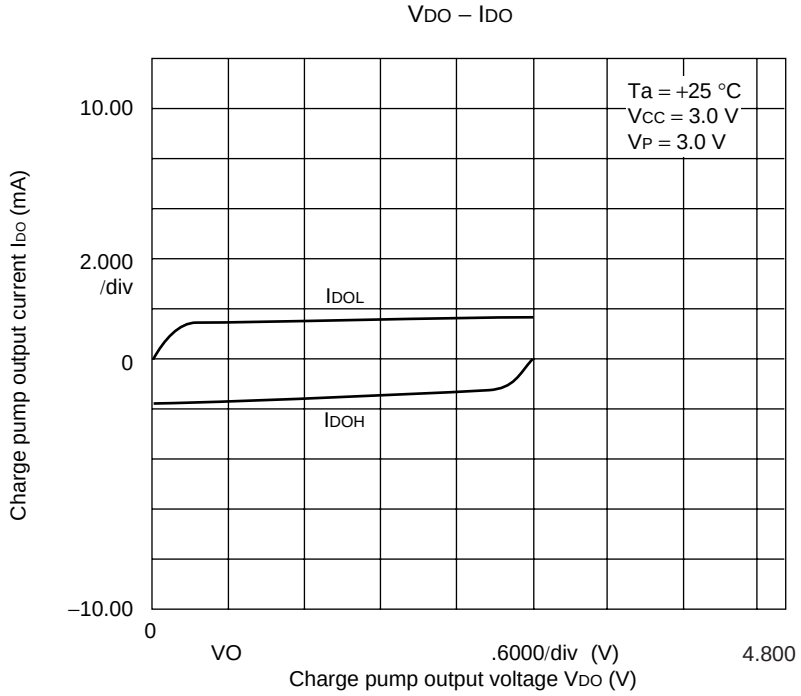


2. OSC_{IN} input sensitivity

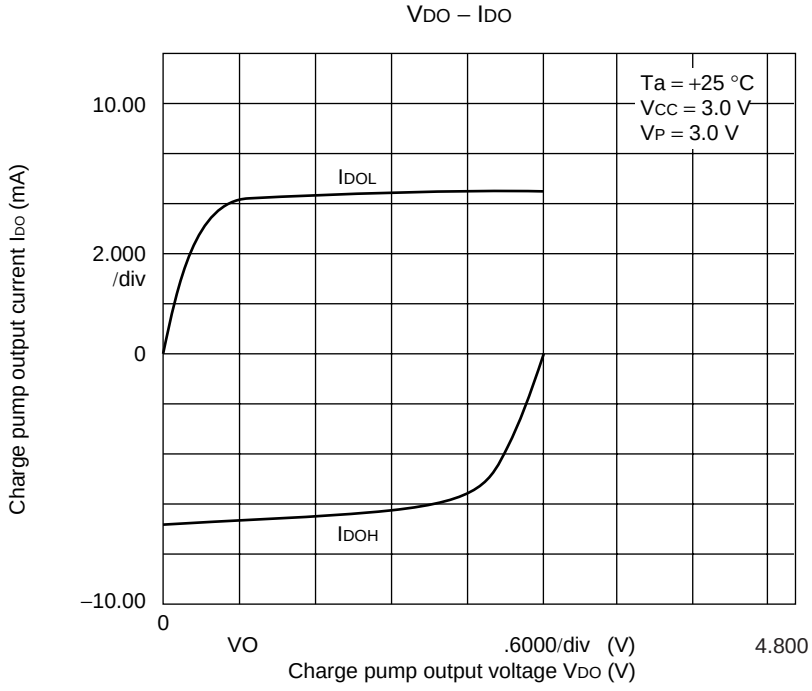


3. Do output current

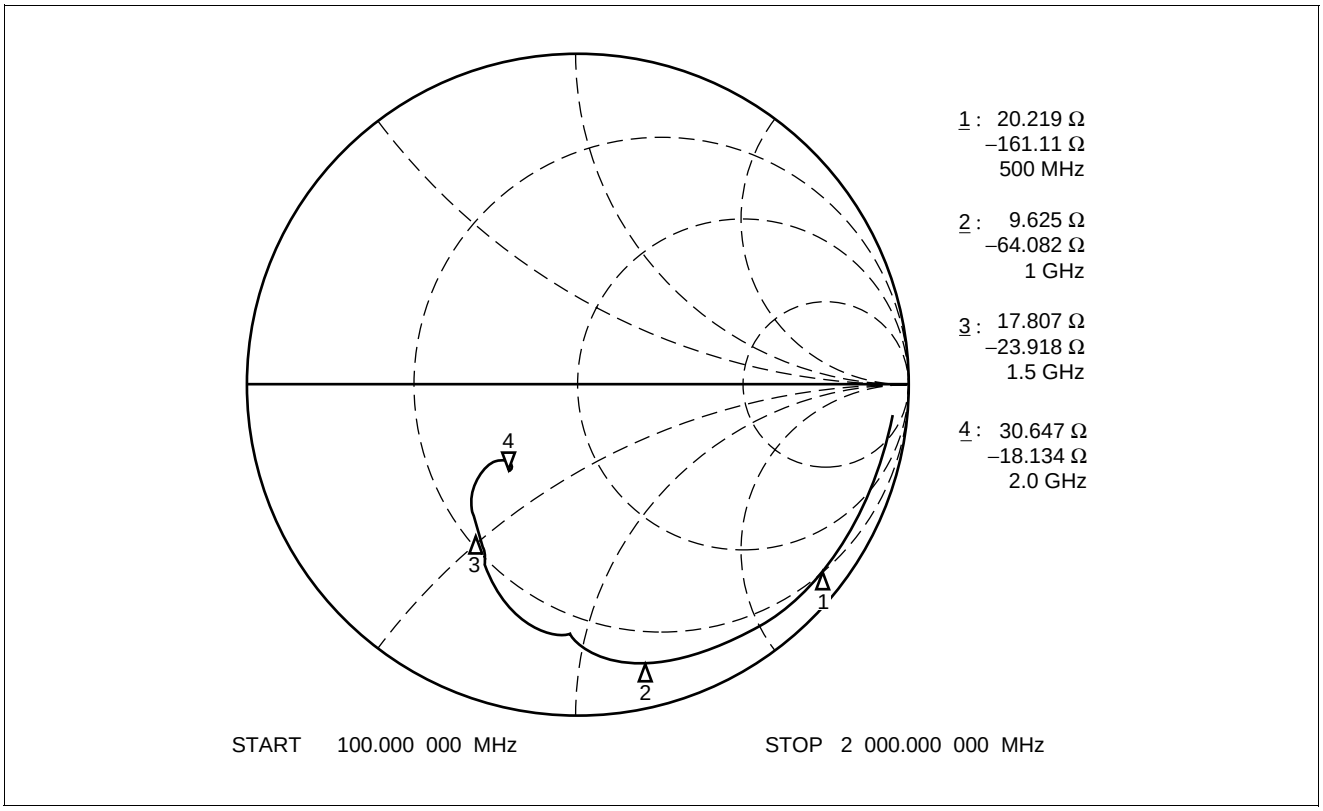
1.5 mA mode



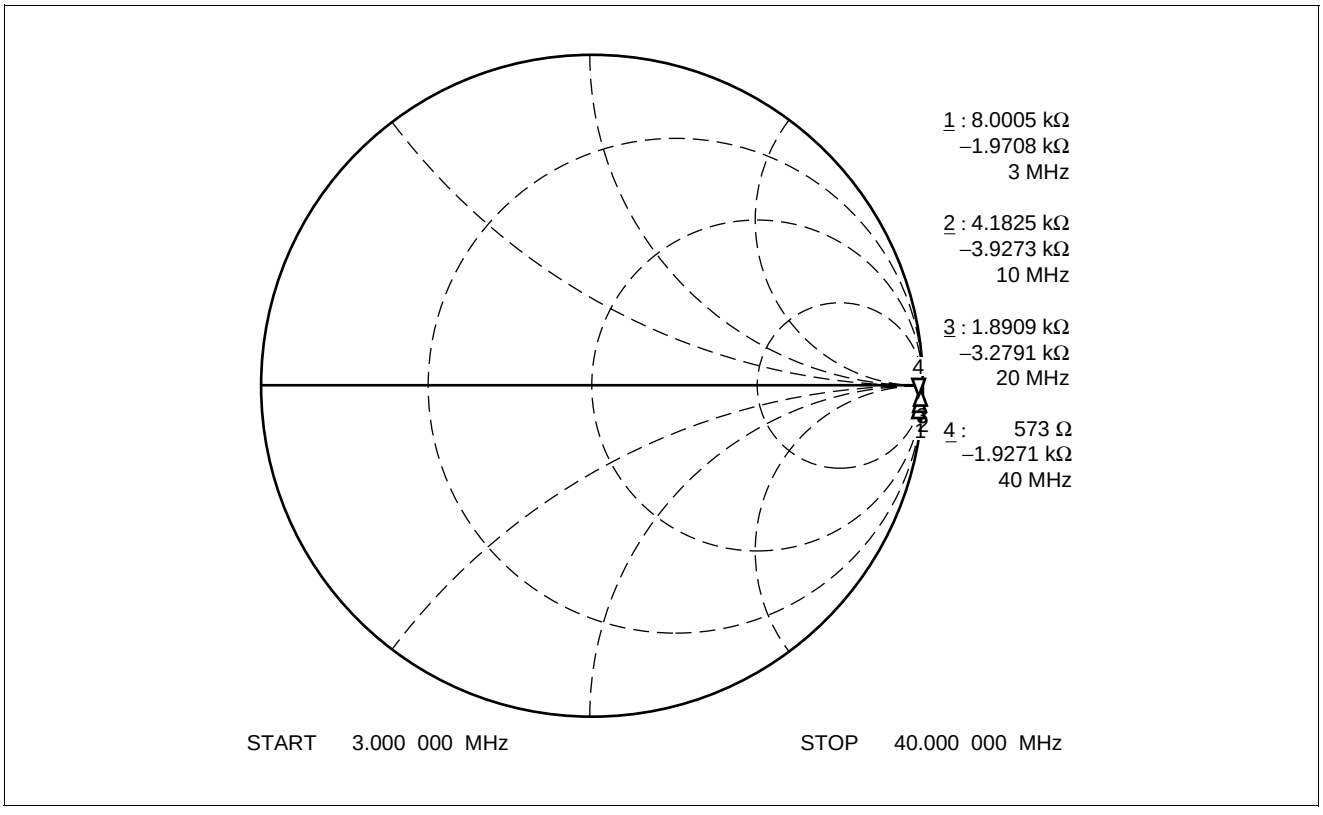
6.0 mA mode



4. fin input impedance

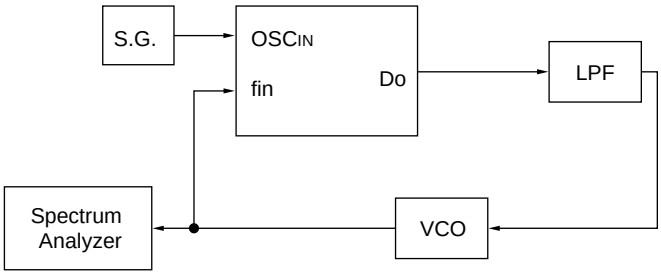


5. OSC_{IN} input impedance



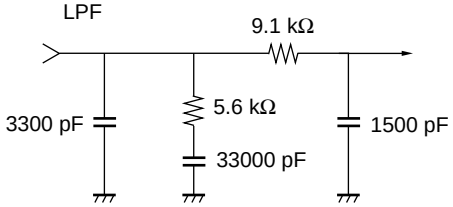
■ REFERENCE INFORMATION

Test Circuit

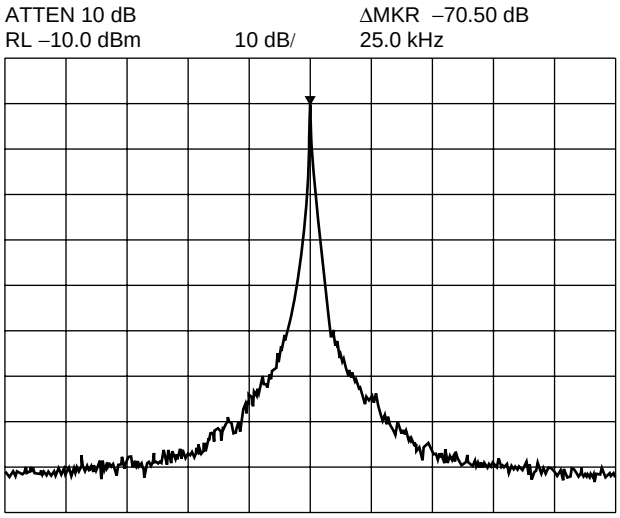


f_{VCO} = 1607 MHz
K_V = 28 MHz/V
fr = 25 kHz
f_{OSC} = 14.4 MHz
V_{CC} = V_P = 3.0 V
V_{VCO} = 2.1 V
Ta = +25 °C
CP : 6 mA mode

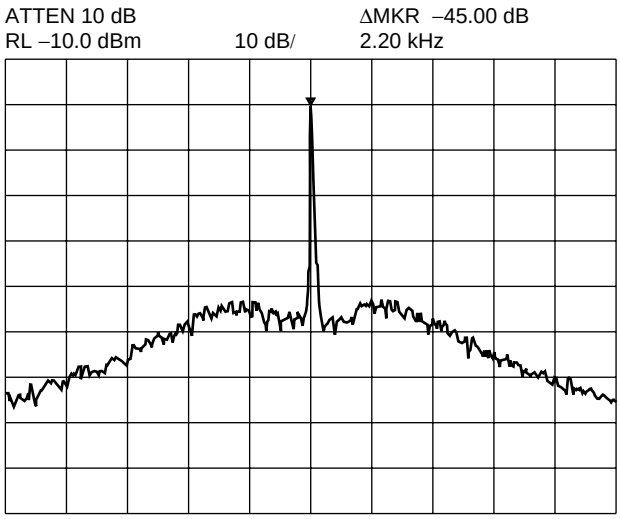
LPF



PLL Reference Leakage



PLL Phase Noise



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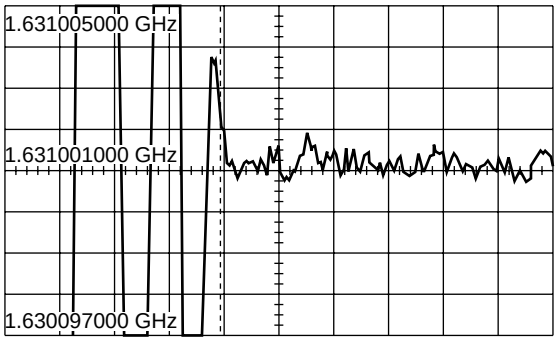
PLL Lock Up time

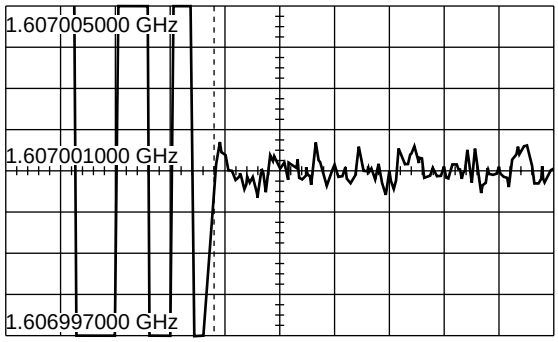
1607 MH→1631 MHz within ± 1 kHz
Lch→Hch 1.46 ms



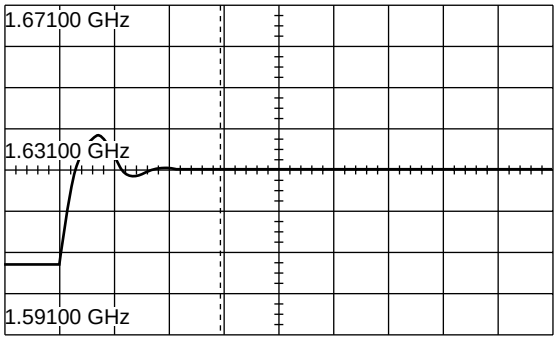
500.0 µs/div

PLL Lock Up time

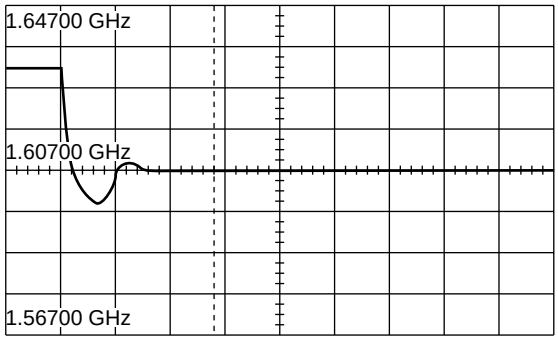
1631 MH→1607 MHz within ± 1 kHz
Hch→Lch 1.37 ms



500.0 µs/div

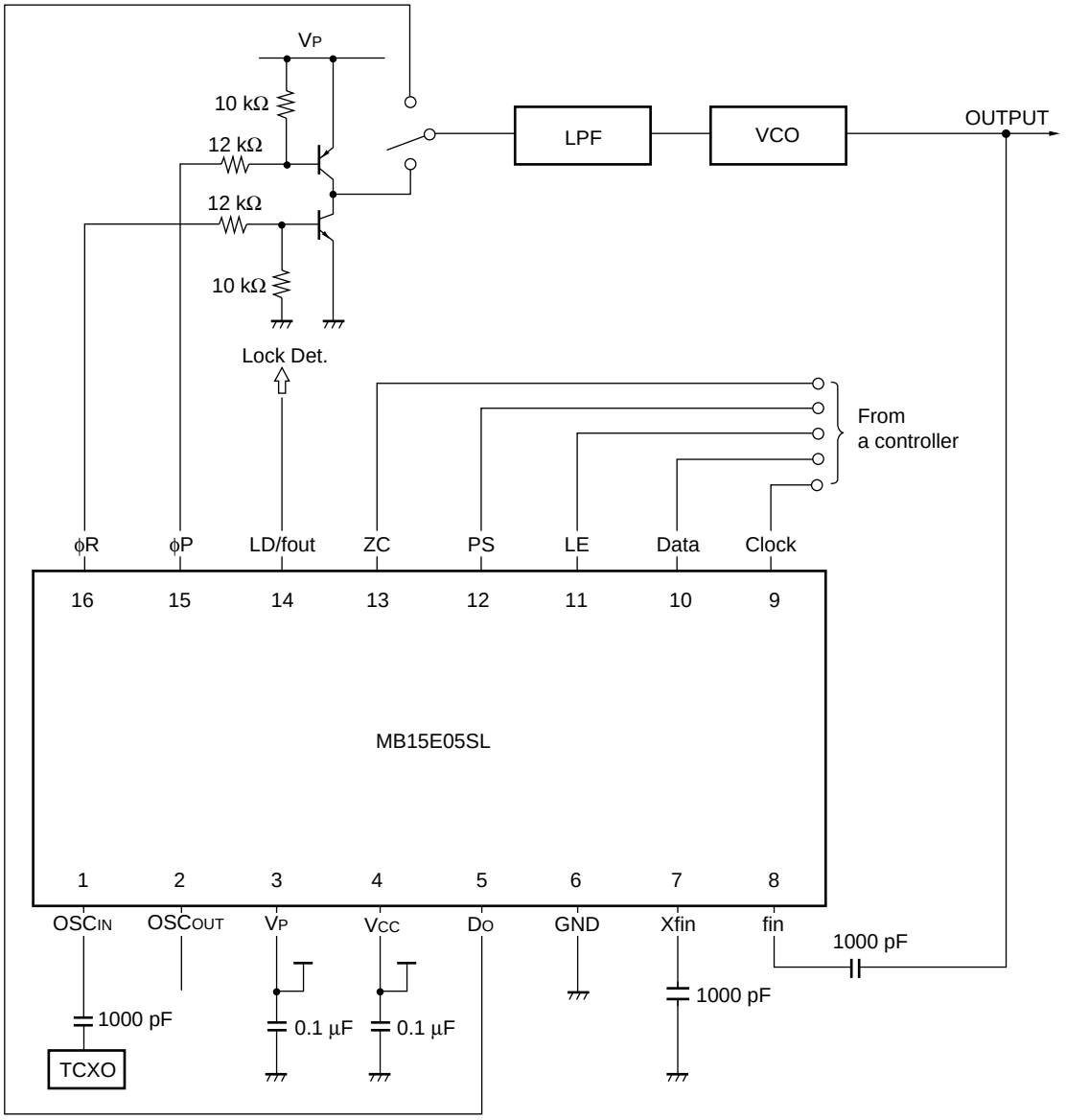


500.0 µs/div



500.0 µs/div

■ APPLICATION EXAMPLE



V_P: 5.5 V Max

Notes:
- SSOP-16
- In case of using a crystal resonator, it is necessary to optimize matching between the crystal and this LSI, and perform detailed system evaluation. It is recommended to consult with a supplier of the crystal resonator. (Reference oscillator circuit provides its own bias, feedback resistor is 100 kΩ (typ).)

■ USAGE PRECAUTIONS

To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting device into or removing device from a socket.
-Protect leads with a conductive sheet when transporting a board-mounted device.

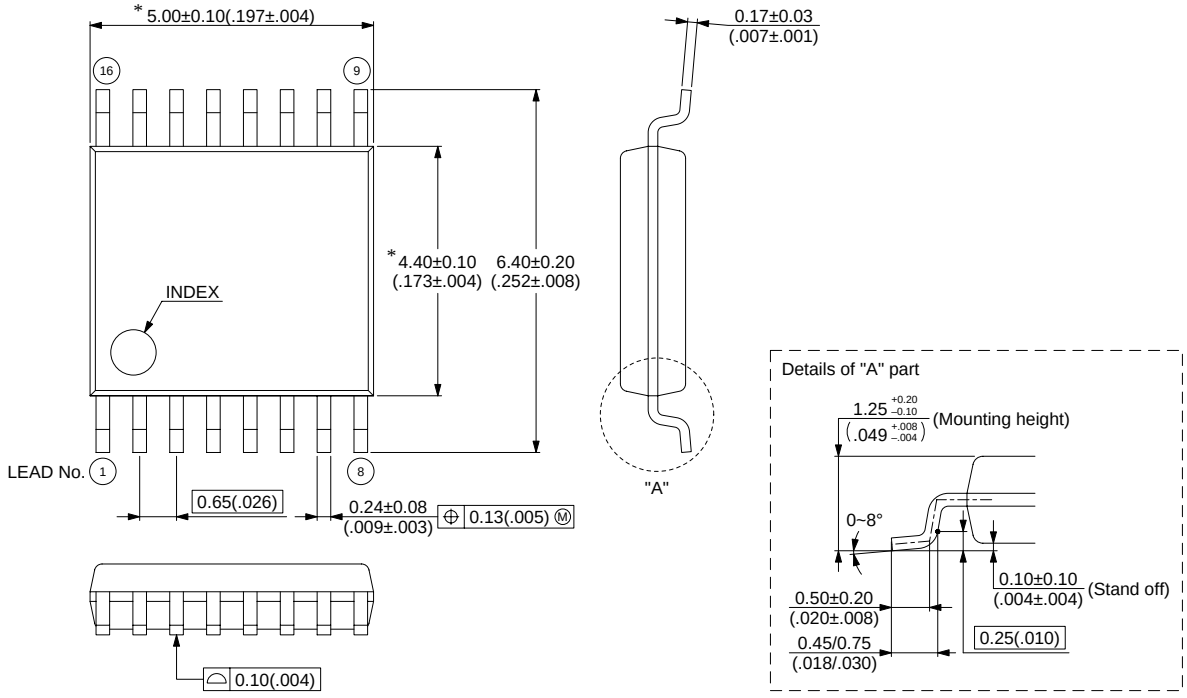
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E05SLPFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15E05SLPV1	16-pad, Plastic BCC (LCC-16P-M06)	

■ PACKAGE DIMENSIONS

16-pin, Plastic SSOP
(FPT-16P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

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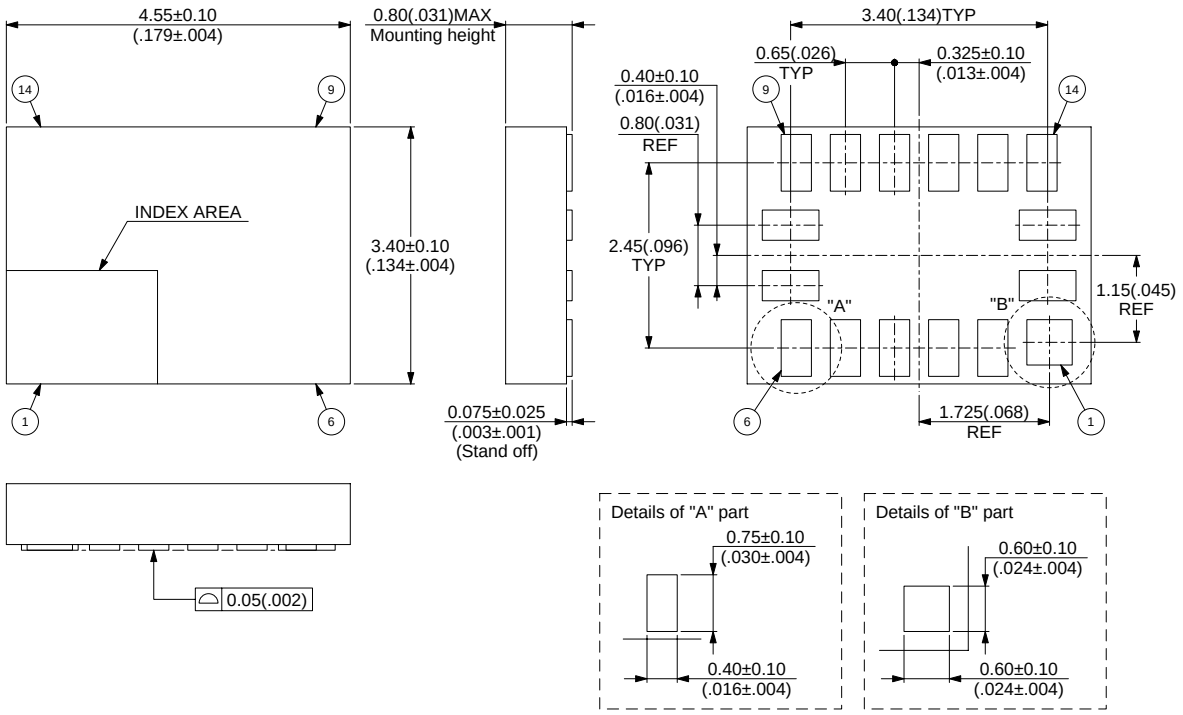
16-pad plastic BCC
(LCC-16P-M06)



Dimensions in mm (inches)

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MGA-62563
Current-Adjustable, Low Noise Amplifier

Data Sheet

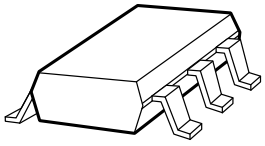
Description

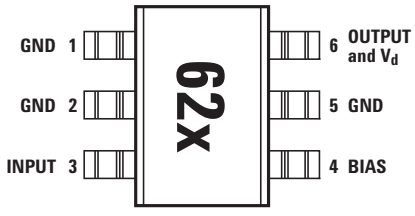
Avago's MGA-62563 is an economical, easy-to-use GaAs MMIC amplifier that offers excellent linearity and low noise figure for applications from 0.1 to 3.5 GHz. Packaged in an miniature SOT-363 package, it requires half the board space of a SOT-143 package.

One external resistor is used to set the bias current taken by the device over a wide range. This allows the designer to use the same part in several circuit positions and tailor the linearity performance (and current consumption) to suit each position.

The output of the amplifier is matched to 50Ω (below 2:1 VSWR) across the entire bandwidth and only requires minimum input matching. The amplifier allows a wide dynamic range by offering a 0.9 dB NF coupled with a +32.9 dBm Output IP3. The circuit uses state-of-the-art E-pHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3V power supply, while internal feedback ensures stability (K>1) over all frequencies.

Pin Connections and Package Marking





Note:

Package marking provides orientation and identification:

"62" = Device Code

"x" = Date code indicates the month of manufacture.

Features

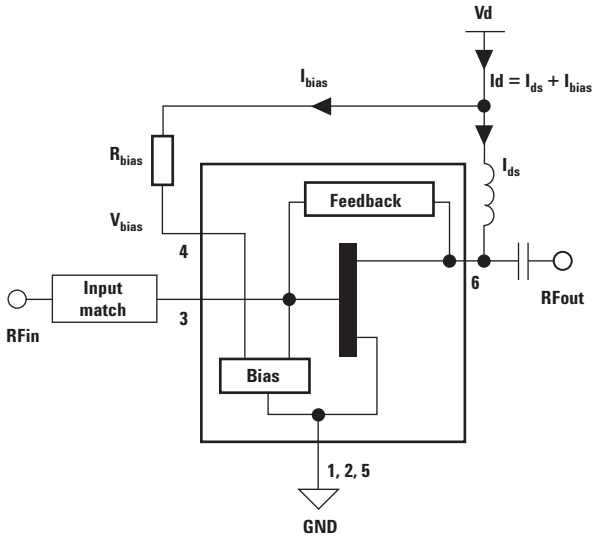
- Single +3V supply
- High linearity
- Low noise figure
- Miniature package
- Unconditionally stable

Specifications

at 500 MHz; 3V, 60 mA (Typ.)

- 0.9 dB noise figure
- 32.9 dBm OIP3
- 22 dB gain
- 17.8 dBm P_{1dB}

Simplified Schematic



MGA-62563 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_d	Device Voltage (pin 6)[2]	V	6
I_d	Device Current (pin 6)[2]	mA	100
P_{in}	CW RF Input Power (pin 3)[3]	dBm	21
I_{ref}	Bias Reference Current (pin 4)	mA	12
P_{diss}	Total Power Dissipation[4]	mW	600
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{ch_b}	Thermal Resistance[5]	°C/W	97

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Bias is assumed at DC quiescent conditions.
3. With the DC (typical bias) and RF applied to the device at board temperature T_B = 25°C.
4. Total dissipation power is referred to board (package belly) temperature T_B = 85°C, P_{diss} is required to derate at 10 mW/°C for T_B > 85°C.
5. Thermal resistance measured using 150°C Liquid Crystal Measurement method.

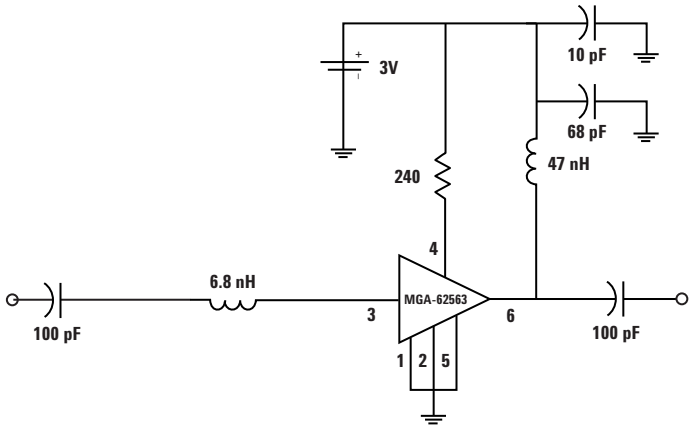


Figure 1. Test circuit of the 0.5 GHz production test board used for NF, Gain and OIP3 measurements. This circuit achieves a trade-off between optimal NF, Gain, OIP3 and input return loss. Circuit losses have been de-embedded from actual measurements.

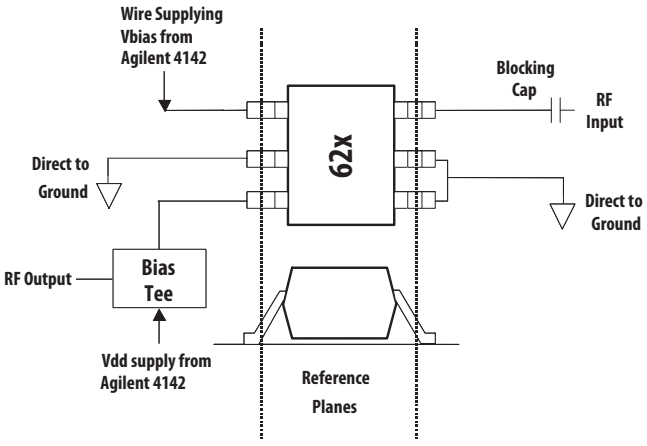


Figure 1b. A diagram showing the connection to the DUT during an S and Noise parameter measurement using an automated tuner system.

Product Consistency Distribution Charts at 3V, 0.5 GHz, $R_{bias} = 240\Omega$[1]

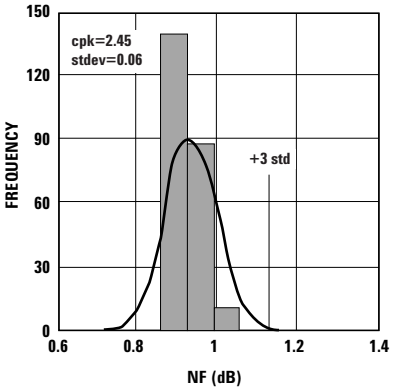


Figure 2. NF @ 2 GHz 3V 60 mA. USL=1.4, Nominal=0.93.

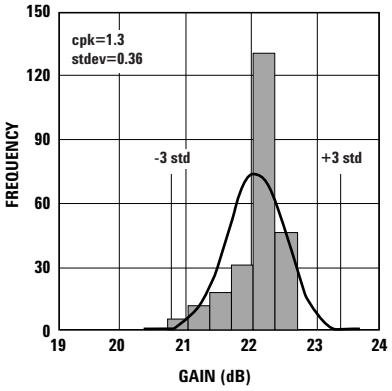


Figure 3. Gain @ 2 GHz 3V 60 mA. LSL =20.4, Nominal = 22, USL = 23.4

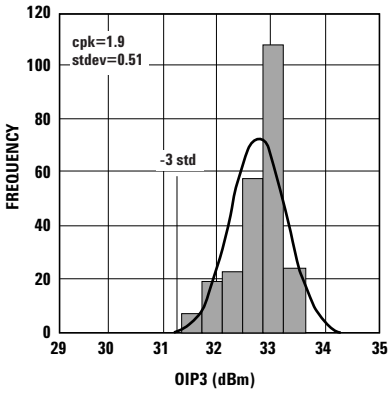


Figure 4. OIP3 @ 2 GHz 3V 60 mA. LSL=30, Nominal=32.9.

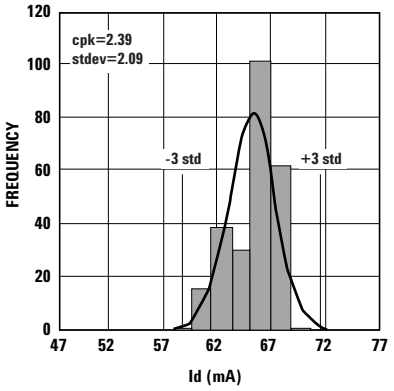


Figure 5. Id @ 3V. LSL = 47, Nominal = 62, USL = 77

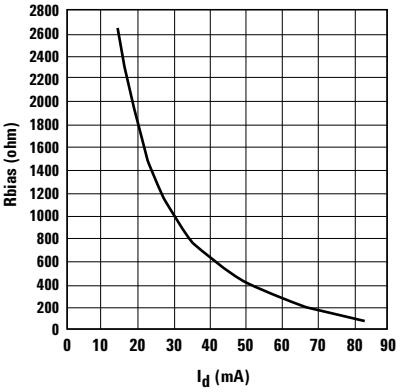


Figure 6. Rbias vs. I_d (3V supply).

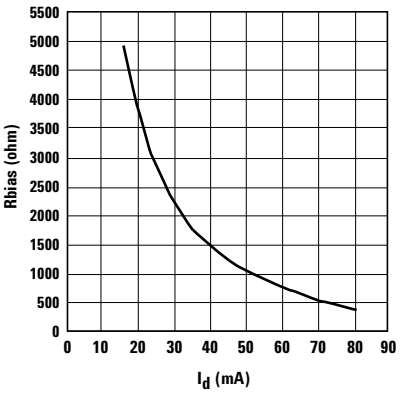


Figure 7. Rbias vs. I_d (5V supply).

Note:

1. Measured on the production test circuit

MGA-62563 Electrical Specifications

T_C = 25°C, Z_O = 50Ω, V_d = 3V (unless otherwise specified)

Symbol	Parameters and Test Conditions	Freq	Units	Min.	Typ.	Max.	Std Dev
Id[1,2]	Device Current		mA	47	62	77	2.09
NF_{test} [1,2]	Noise Figure in test circuit [1]	f = 0.5 GHz	dB		0.93	1.4	0.06
G_{test} [1,2]	Associated Gain in test circuit[1]	f = 0.5 GHz	dB	20.4	22	23.4	0.36
$OIP3_{test}$ [1,2]	Ouput 3rd Order Intercept in test circuit[1]	f = 0.5 GHz	dBm	30	32.9		0.51
$NF_{50ý}$[3]	Noise Figure in 50Ω system	f = 0.1 GHz	dB		1.1		
		f = 0.2 GHz			1.0		
		f = 0.5 GHz			0.8		
		f = 1.0 GHz			0.9		0.06
		f = 1.5 GHz			1.0		
		f = 2.0 GHz			1.2		
		f = 2.5 GHz			1.3		
		f = 3.0 GHz			1.5		
$\|S_{21}\|^2_{50ý}$ [3]	Associated Gain in 50Ω system	f = 0.1 GHz	dB		23.5		
		f = 0.2 GHz			23		
		f = 0.5 GHz			22		
		f = 1.0 GHz			20		0.36
		f = 1.5 GHz			17		
		f = 2.0 GHz			15.5		
		f = 2.5 GHz			14		
		f = 3.0 GHz			13		
$OIP3_{50ý}$[3]	Output 3rd Order Intercept Point in 50Ω system	f = 0.1 GHz	dBm		34.7		
		f = 0.2 GHz			34.7		
		f = 0.5 GHz			34.8		
		f = 1.0 GHz			33.5		0.51
		f = 1.5 GHz			33		
		f = 2.0 GHz			32.3		
		f = 2.5 GHz			32		
		f = 3.0 GHz			31		
$P1dB_{50ý}$[3]	Output Power at 1dB Gain Compression in 50Ω system	f = 0.1 GHz	dBm		18		
		f = 0.2 GHz			18		
		f =0.5 GHz			18		
		f = 1.0 GHz			17.6		
		f = 1.5 GHz			17.6		
		f = 2.0 GHz			17.7		
		f = 2.5 GHz			17.9		
		f = 3.0 GHz			17.7		

Notes:

1. Guaranteed specifications are 100% tested in the production test circuit as shown in Figure 1, the typical value is based on measurement of at least 500 parts from three non-consecutive wafer lots during initial characterization of this product.
2. Circuit achieved a trade-off between optimal NF, Gain, OIP3 and input return loss.
3. Parameter quoted at 50Ω is based on measurement of selected typical parts tested on a 50Ω input and output test fixture.

MGA-62563 Typical Performance, $V_d = 3V$, $I_{ds} = 60$ mA at 50Ω Input and Output

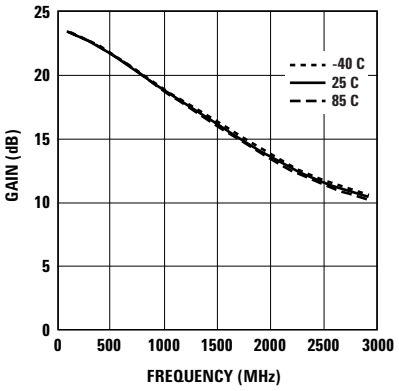


Figure 8. Gain vs. Frequency (3V 60 mA).

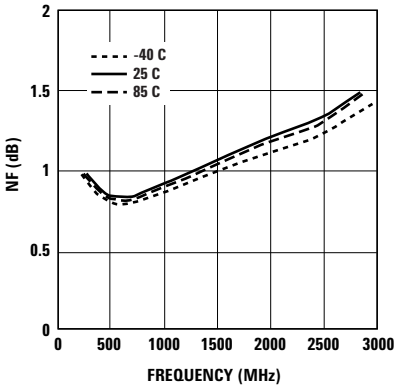


Figure 9. NF vs. Frequency (3V 60 mA).

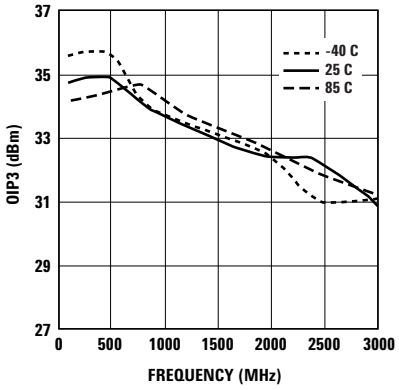


Figure 10. OIP3 vs. Frequency (3V 60 mA).

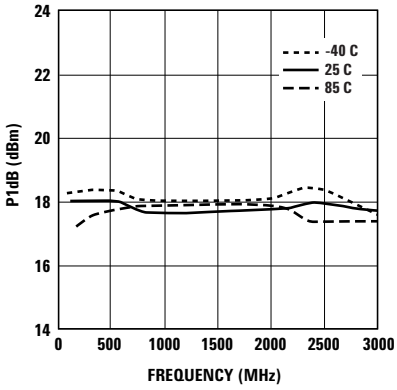


Figure 11. P1dB vs. Frequency (3V 60 mA).

MGA-62563 Typical Performance, $V_d = 3V$, $I_{ds} = 30$ mA at 50Ω Input and Output

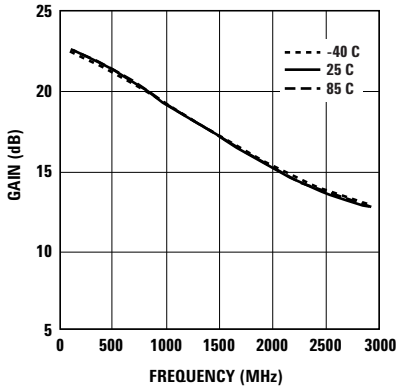


Figure 12. Gain vs. Frequency (3V 30 mA).

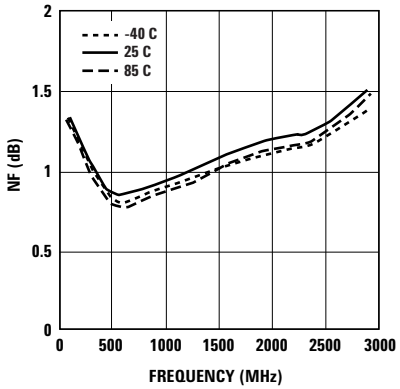


Figure 13. NF vs. Frequency (3V 30 mA).

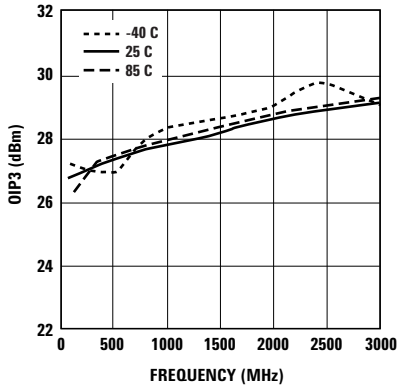


Figure 14. OIP3 vs. Frequency (3V 30 mA).

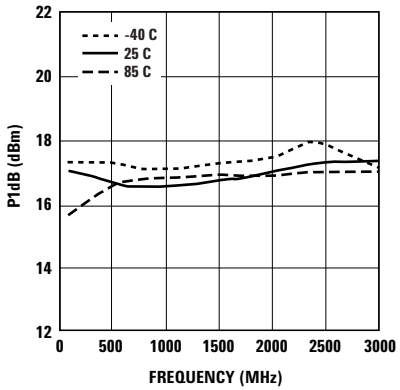


Figure 15. P1dB vs. Frequency (3V 30 mA).

MGA-62563 Typical Performance, $V_d = 5V$, $I_{ds} = 60$ mA at 50Ω Input and Output

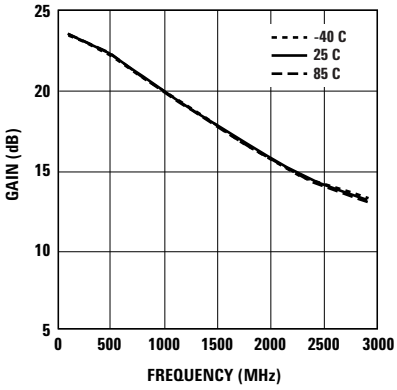


Figure 16. Gain vs. Frequency (5V 60 mA).

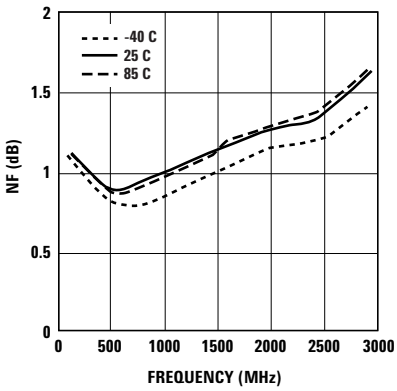


Figure 17. NF vs. Frequency (5V 60 mA).

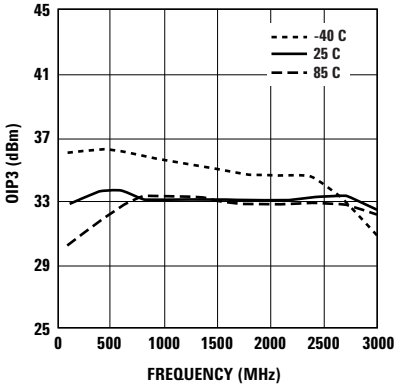


Figure 18. OIP3 vs. Frequency (5V 60 mA).

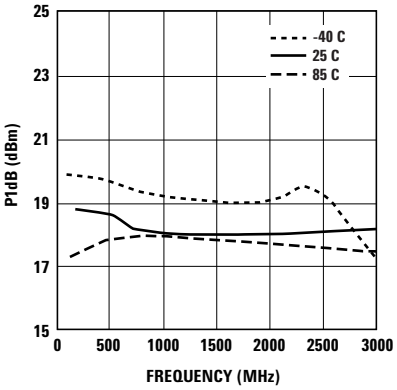


Figure 19. P1dB vs. Frequency (5V 60 mA).

MGA-62563 Typical Performance, $V_d = 5V$, $I_{ds} = 30$ mA at 50Ω Input and Output

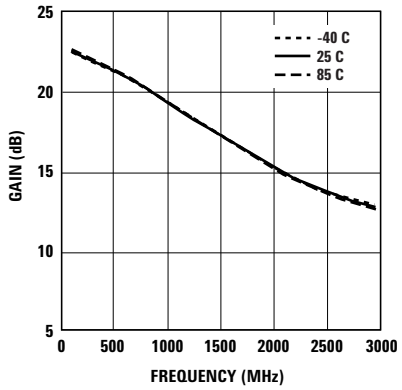


Figure 20. Gain vs. Frequency (5V 30 mA).

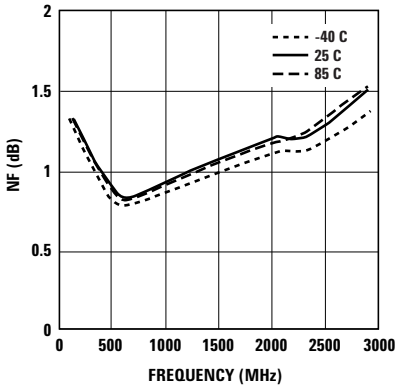


Figure 21. NF vs. Frequency (5V 30 mA).

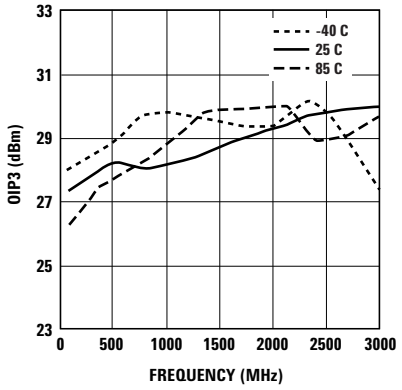


Figure 22. OIP3 vs. Frequency (5V 30 mA).

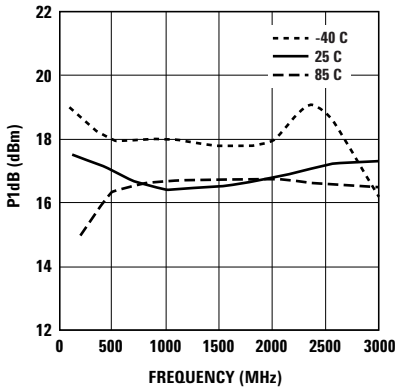


Figure 23. P1dB vs. Frequency (5V 30 mA).

MGA-62563 Typical Performance, Freq=0.5 GHz, T_C=25°C at 50Ω Input and Output

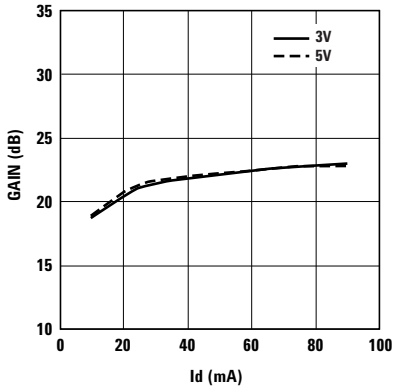


Figure 24. Gain vs. Id (500 MHz).

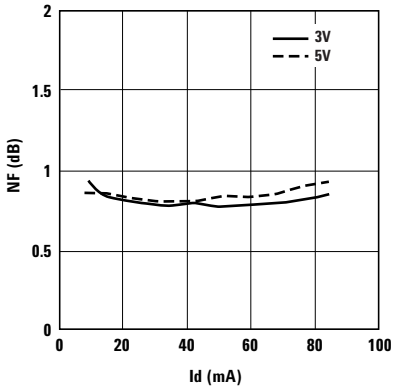


Figure 25. NF vs. Id (500 MHz).

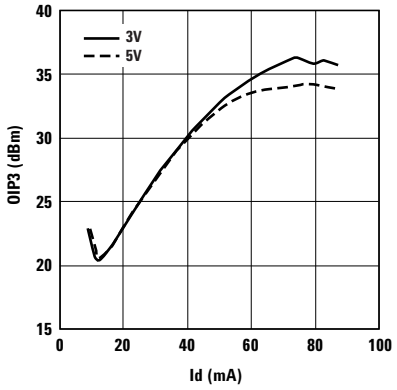


Figure 26. OIP3 vs. Id (500 MHz).

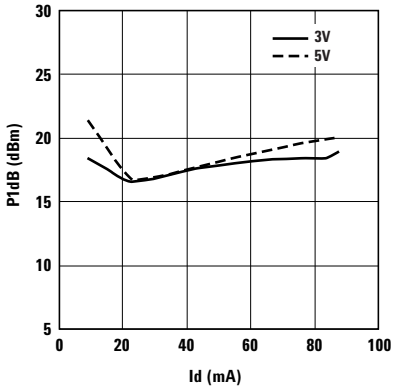


Figure 27. P1dB vs. Id (500 MHz).

MGA-62563 Typical Performance, Freq=0.1 GHz, T_C=25°C at 50Ω Input and Output

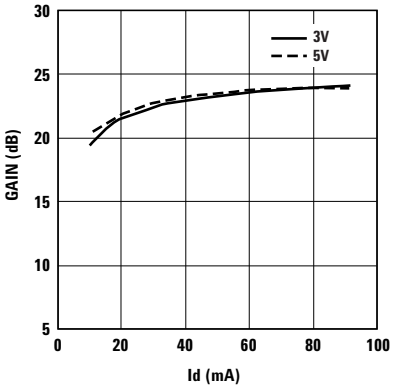


Figure 28. Gain vs. Id (100 MHz).

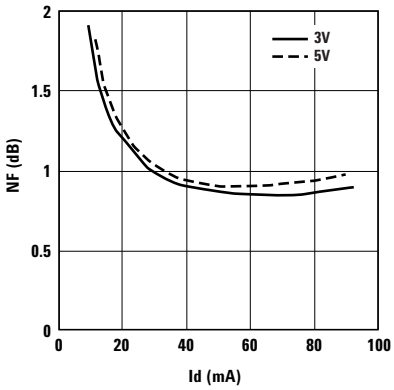


Figure 29. NF vs. Id (100 MHz).

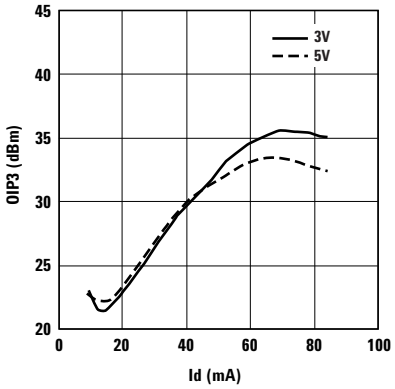


Figure 30. OIP3 vs. Id (100 MHz).

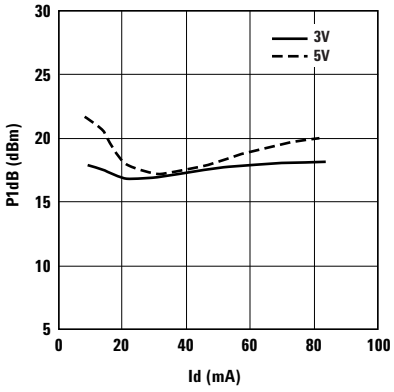


Figure 31. P1dB vs. Id (100 MHz).

MGA-62563 Typical Scattering Parameters, $T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 3V$, $I_{ds} = 60$ mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		K-factor
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	
0.1	0.185	-82.272	22.91	13.982	155.827	0.042	5.4	0.129	-164.437	1.09
0.2	0.187	-90.11	22.63	13.537	153.346	0.042	5.474	0.135	-168.363	1.1
0.3	0.193	-98.147	22.31	13.054	150.578	0.042	5.636	0.141	-172.09	1.12
0.4	0.203	-106.14	21.97	12.545	147.524	0.042	5.912	0.148	-175.737	1.15
0.5	0.217	-114.27	21.57	11.986	143.942	0.042	6.346	0.154	-179.503	1.17
0.6	0.233	-121.367	21.18	11.459	140.212	0.041	6.892	0.159	177.105	1.22
0.7	0.252	-127.882	20.78	10.945	136.065	0.041	7.583	0.163	173.986	1.25
0.8	0.272	-133.795	20.39	10.457	131.465	0.041	8.43	0.167	171.256	1.27
0.9	0.295	-138.842	20.02	10.021	126.434	0.041	9.417	0.171	168.886	1.3
1	0.317	-143.232	19.66	9.611	121.342	0.042	10.645	0.173	167.409	1.3
1.1	0.34	-147.643	19.26	9.179	116.107	0.042	12.083	0.175	166.393	1.32
1.2	0.358	-151.668	18.87	8.78	111.387	0.042	13.52	0.177	165.719	1.35
1.3	0.371	-154.625	18.48	8.397	106.965	0.043	14.99	0.172	164.894	1.36
1.4	0.378	-156.903	18.1	8.035	102.832	0.044	16.437	0.163	164.215	1.38
1.5	0.385	-159.101	17.71	7.684	98.886	0.045	17.798	0.153	164.02	1.4
1.6	0.392	-161.727	17.32	7.349	95.185	0.046	19.056	0.144	163.07	1.42
1.7	0.397	-164.752	16.92	7.015	91.424	0.048	20.227	0.132	162.822	1.42
1.8	0.4	-167.685	16.55	6.72	88.093	0.049	21.207	0.122	162.927	1.44
1.9	0.4	-170.686	16.19	6.446	84.931	0.051	22.085	0.113	163.177	1.44
2	0.4	-173.615	15.84	6.195	81.892	0.052	22.821	0.104	163.203	1.47
2.5	0.401	171.986	14.29	5.184	67.423	0.063	24.202	0.059	160.575	1.46
3	0.391	153.64	12.93	4.432	53.871	0.074	22.323	0.029	162.52	1.46
3.5	0.418	141.02	11.87	3.923	39.725	0.088	16.919	0.024	14.44	1.37
4	0.461	127.008	10.81	3.472	26.244	0.099	11.289	0.043	17.922	1.32
4.5	0.548	119.58	9.83	3.1	11.923	0.108	4.074	0.083	3.197	1.22
5	0.615	105.771	8.73	2.733	-1.958	0.119	-3.141	0.057	18.181	1.14
5.5	0.674	97.228	7.69	2.425	-13.281	0.126	-10.835	0.026	-8.344	1.05
6	0.701	85.967	7.26	2.308	-24.509	0.131	-17.126	0.096	123.432	1.01
6.5	0.698	77.659	6.44	2.099	-35.324	0.138	-24.617	0.165	105.103	1.06
7	0.69	66.448	6.33	2.072	-47.318	0.145	-31.049	0.259	92.547	1.06
7.5	0.677	55.492	5.55	1.895	-59.77	0.15	-39.087	0.284	78.001	1.14
8	0.673	45.318	5.18	1.816	-68.839	0.157	-45.822	0.294	70.774	1.14
9	0.718	26.713	4.61	1.701	-88.8	0.167	-62.304	0.323	48.33	1.07
10	0.778	15.285	4.14	1.61	-104.215	0.168	-76.006	0.364	24.415	0.99

Typical Noise Parameters at 25°C,

$T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 3V$, $I_{ds} = 60$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	NF@50Ω
GHz	dB	Mag.	Ang.		dB
0.5	0.79	0.08	57.8	0.12	0.8
1	0.65	0.07	168.2	0.07	0.65
1.5	0.76	0.12	-176.7	0.07	0.77
2	0.87	0.13	149.3	0.08	0.89
2.5	0.93	0.16	-179	0.08	0.97
3	0.96	0.23	-164.8	0.08	1.06
3.5	1.11	0.24	-150	0.09	1.22
4	1.28	0.27	-142.7	0.11	1.43
4.5	1.36	0.33	-133.7	0.12	1.61
5	1.44	0.38	-123	0.15	1.79
5.5	1.47	0.43	-114	0.19	1.97
6	1.63	0.45	-103.6	0.25	2.2
6.5	1.69	0.5	-94.5	0.34	2.47
7	1.77	0.54	-85.3	0.43	2.71
7.5	1.94	0.58	-75.1	0.57	3.08
8	2.07	0.6	-64.9	0.77	3.42
8.5	2.25	0.64	-54.6	1	3.89
9	2.4	0.67	-45.9	1.28	4.31
9.5	2.25	0.75	-39.2	1.6	4.77
10	2.44	0.74	-34	1.91	5.14

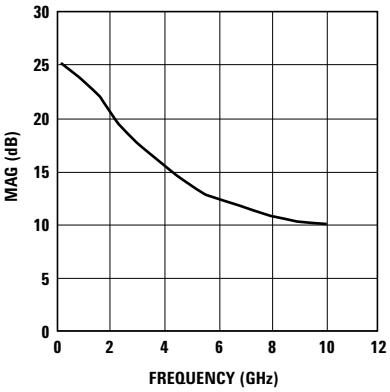


Figure 32. MAG vs. Frequency.

MGA-62563 Typical Scattering Parameters, $T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 3V$, $I_{ds} = 30$ mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		K-factor
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	
0.1	0.229	-64.839	21.81	12.314	156.524	0.049	5.851	0.088	-127.44	1.06
0.2	0.225	-72.068	21.54	11.942	153.986	0.049	5.688	0.093	-135.628	1.08
0.3	0.224	-80.018	21.24	11.537	151.158	0.049	5.569	0.1	-143.242	1.09
0.4	0.227	-88.494	20.91	11.11	148.033	0.049	5.526	0.108	-150.147	1.11
0.5	0.234	-97.66	20.54	10.643	144.386	0.048	5.588	0.116	-156.622	1.15
0.6	0.246	-106.065	20.17	10.202	140.583	0.048	5.738	0.125	-161.903	1.17
0.7	0.261	-113.999	19.8	9.774	136.408	0.048	6.002	0.133	-166.307	1.19
0.8	0.28	-121.285	19.43	9.369	131.811	0.048	6.379	0.141	-169.879	1.22
0.9	0.302	-127.551	19.1	9.012	126.834	0.048	6.887	0.15	-172.861	1.23
1	0.324	-133.004	18.77	8.676	121.818	0.049	7.629	0.158	-174.888	1.23
1.1	0.348	-138.366	18.4	8.322	116.64	0.049	8.559	0.166	-176.589	1.24
1.2	0.367	-143.111	18.05	7.993	111.957	0.049	9.506	0.174	-178.07	1.26
1.3	0.38	-146.63	17.69	7.669	107.573	0.05	10.548	0.174	-179.151	1.27
1.4	0.39	-149.336	17.33	7.356	103.466	0.051	11.645	0.168	-179.685	1.28
1.5	0.399	-151.941	16.97	7.052	99.534	0.052	12.668	0.162	-179.868	1.29
1.6	0.407	-154.928	16.6	6.758	95.851	0.053	13.646	0.156	179.214	1.31
1.7	0.413	-158.278	16.21	6.466	92.108	0.054	14.581	0.148	179.163	1.33
1.8	0.416	-161.47	15.86	6.207	88.778	0.055	15.393	0.141	179.311	1.35
1.9	0.418	-164.666	15.51	5.965	85.613	0.057	16.142	0.134	179.509	1.36
2	0.417	-167.751	15.18	5.744	82.561	0.058	16.791	0.128	179.436	1.38
2.5	0.422	177.274	13.71	4.848	67.999	0.068	18.161	0.089	176.954	1.4
3	0.412	158.337	12.41	4.174	54.232	0.079	16.464	0.062	176.77	1.42
3.5	0.442	144.969	11.39	3.71	39.961	0.092	11.54	0.015	130.879	1.35
4	0.486	129.994	10.34	3.287	26.316	0.102	6.16	0.028	68.898	1.32
4.5	0.573	121.597	9.35	2.935	11.973	0.111	-0.792	0.063	24.183	1.21
5	0.638	107.123	8.25	2.585	-2.051	0.122	-7.727	0.057	50.418	1.13
5.5	0.696	98.232	7.18	2.285	-13.425	0.128	-15.159	0.026	55.253	1.05
6	0.721	86.681	6.73	2.169	-24.666	0.131	-21.346	0.124	119.497	1
6.5	0.713	78.214	5.85	1.961	-35.535	0.139	-28.725	0.191	103.907	1.06
7	0.704	66.96	5.7	1.927	-47.61	0.146	-34.963	0.287	91.799	1.06
7.5	0.687	55.912	4.88	1.753	-60.15	0.15	-42.644	0.31	77.221	1.16
8	0.68	45.807	4.47	1.673	-69.283	0.156	-49.076	0.318	69.627	1.18
9	0.725	27.162	3.85	1.558	-89.513	0.166	-65.125	0.343	47.128	1.1
10	0.787	15.674	3.34	1.469	-105.215	0.168	-78.788	0.382	23.467	1

Typical Noise Parameters at 25°C,

$T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 3V$, $I_{ds} = 30$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	NF@50Ω
GHz	dB	Mag.	Ang.		dB
0.5	0.76	0.07	92.8	0.1	0.77
1	0.66	0.06	149.8	0.08	0.67
1.5	0.79	0.09	167.2	0.07	0.8
2	0.86	0.14	142.8	0.08	0.88
2.5	0.91	0.15	167.5	0.08	0.95
3	0.94	0.23	-174.7	0.07	1.03
3.5	1.07	0.24	-159.3	0.08	1.17
4	1.21	0.27	-148.9	0.09	1.35
4.5	1.28	0.32	-140.7	0.11	1.51
5	1.39	0.36	-129.5	0.13	1.69
5.5	1.43	0.4	-119.9	0.17	1.85
6	1.58	0.42	-109.1	0.21	2.05
6.5	1.63	0.48	-100.3	0.28	2.31
7	1.68	0.53	-91	0.35	2.51
7.5	1.86	0.56	-80.2	0.48	2.87
8	1.96	0.59	-69.4	0.65	3.18
8.5	2.15	0.63	-58.6	0.85	3.61
9	2.26	0.64	-51.5	1.12	4.02
9.5	2.15	0.75	-42.4	1.4	4.49
10	2.32	0.74	-37.5	1.69	4.87

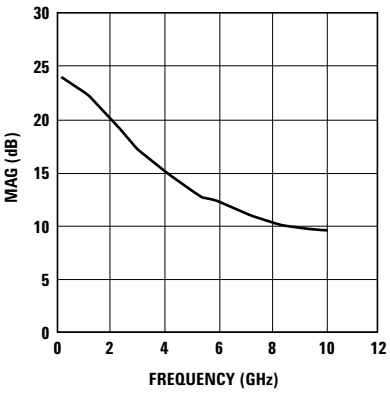


Figure 33. MAG vs. Frequency.

MGA-62563 Typical Scattering Parameters, $T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 3V$, $I_{ds} = 20$ mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		K-factor
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	
0.1	0.274	-53.949	20.92	11.121	157.035	0.054	5.715	0.094	-80.83	1.05
0.2	0.265	-60.28	20.67	10.806	154.512	0.054	5.383	0.09	-91.02	1.07
0.3	0.259	-67.514	20.39	10.459	151.71	0.054	5.086	0.089	-102.192	1.08
0.4	0.257	-75.557	20.08	10.093	148.613	0.054	4.833	0.091	-113.483	1.1
0.5	0.258	-84.672	19.72	9.687	144.952	0.054	4.637	0.095	-124.7	1.12
0.6	0.264	-93.431	19.37	9.304	141.158	0.054	4.525	0.101	-133.965	1.14
0.7	0.275	-102.057	19.02	8.932	137.004	0.054	4.504	0.109	-141.605	1.16
0.8	0.29	-110.18	18.67	8.581	132.446	0.054	4.576	0.118	-147.841	1.18
0.9	0.31	-117.309	18.35	8.271	127.543	0.054	4.783	0.129	-152.991	1.19
1	0.331	-123.571	18.04	7.983	122.588	0.054	5.195	0.139	-156.749	1.2
1.1	0.354	-129.682	17.71	7.679	117.464	0.054	5.763	0.15	-160.026	1.21
1.2	0.372	-134.998	17.38	7.396	112.827	0.054	6.374	0.16	-162.849	1.22
1.3	0.387	-138.974	17.04	7.11	108.473	0.055	7.105	0.163	-164.481	1.22
1.4	0.397	-142.056	16.69	6.828	104.388	0.055	7.939	0.16	-165.092	1.25
1.5	0.407	-145.03	16.33	6.555	100.473	0.056	8.736	0.157	-165.37	1.26
1.6	0.416	-148.334	15.97	6.289	96.786	0.057	9.514	0.152	-166.308	1.28
1.7	0.423	-151.951	15.6	6.025	93.017	0.058	10.294	0.146	-166.218	1.3
1.8	0.427	-155.37	15.25	5.789	89.657	0.059	10.984	0.141	-166.034	1.32
1.9	0.428	-158.764	14.91	5.568	86.471	0.06	11.651	0.137	-165.814	1.34
2	0.428	-161.995	14.59	5.365	83.402	0.062	12.246	0.132	-165.841	1.35
2.5	0.432	-177.573	13.16	4.549	68.702	0.07	13.701	0.098	-166.888	1.41
3	0.422	162.92	11.89	3.933	54.632	0.08	12.332	0.073	-164.868	1.45
3.5	0.453	148.816	10.89	3.503	40.096	0.092	7.985	0.024	-165.023	1.39
4	0.497	133.003	9.85	3.108	26.107	0.102	3.027	0.013	108.515	1.35
4.5	0.584	123.794	8.87	2.777	11.49	0.111	-3.486	0.044	23.417	1.24
5	0.648	108.792	7.8	2.455	-2.939	0.121	-9.998	0.044	61.186	1.15
5.5	0.705	99.614	6.75	2.174	-14.677	0.128	-17.142	0.019	83.666	1.05
6	0.729	87.836	6.32	2.07	-26.088	0.131	-23.178	0.129	125.118	1
6.5	0.719	79.179	5.46	1.875	-37.227	0.138	-30.431	0.194	108.15	1.06
7	0.709	67.879	5.33	1.847	-49.36	0.144	-36.508	0.289	94.828	1.06
7.5	0.69	56.687	4.54	1.686	-62.033	0.148	-43.977	0.312	79.896	1.17
8	0.682	46.564	4.15	1.613	-71.166	0.155	-50.351	0.321	72.003	1.19
9	0.725	27.786	3.57	1.508	-91.211	0.164	-66.308	0.344	49.405	1.11
10	0.791	15.826	3.07	1.424	-106.691	0.166	-79.9	0.382	25.395	1

Typical Noise Parameters at 25°C,

$T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 3V$, $I_{ds} = 20$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	NF@50Ω
GHz	dB	Mag.	Ang.		dB
0.5	0.83	0.1	83.2	0.11	0.85
1	0.71	0.06	133.5	0.08	0.71
1.5	0.81	0.09	151.9	0.07	0.82
2	0.88	0.15	133.2	0.08	0.91
2.5	0.93	0.16	160.2	0.08	0.97
3	0.98	0.23	179.7	0.07	1.07
3.5	1.1	0.24	-164.5	0.08	1.2
4	1.2	0.28	-154	0.09	1.36
4.5	1.29	0.33	-143.9	0.1	1.52
5	1.4	0.36	-132.8	0.12	1.71
5.5	1.46	0.4	-122.9	0.16	1.88
6	1.62	0.42	-112	0.21	2.1
6.5	1.68	0.47	-102.3	0.28	2.34
7	1.74	0.52	-92.9	0.35	2.56
7.5	1.92	0.55	-82.2	0.47	2.91
8	2.04	0.57	-71.5	0.65	3.23
8.5	2.22	0.61	-60	0.85	3.65
9	2.32	0.65	-52.5	1.13	4.09
9.5	2.2	0.75	-43.5	1.41	4.55
10	2.39	0.74	-38.6	1.71	4.94

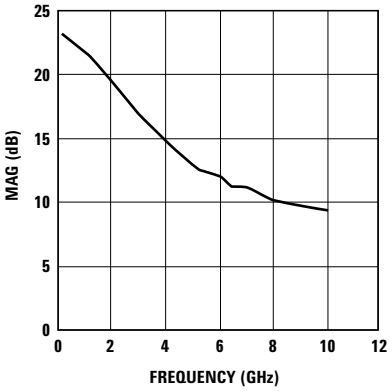


Figure 34. MAG vs. Frequency.

MGA-62563 Typical Scattering Parameters, $T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 5V$, $I_{ds} = 40$ mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		K-factor
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	
0.1	0.22	-62.539	22.22	12.911	155.715	0.046	2.6	0.041	-117.254	1.09
0.2	0.214	-69.644	21.94	12.502	153.158	0.045	2.081	0.038	-129.6	1.12
0.3	0.212	-77.541	21.62	12.057	150.317	0.045	1.608	0.038	-142.653	1.14
0.4	0.214	-86.029	21.28	11.588	147.183	0.044	1.201	0.039	-155.322	1.18
0.5	0.22	-95.298	20.89	11.075	143.514	0.043	0.89	0.041	-167.419	1.23
0.6	0.229	-103.863	20.5	10.59	139.683	0.043	0.698	0.043	-177.186	1.26
0.7	0.243	-112.001	20.1	10.12	135.429	0.042	0.643	0.045	174.82	1.31
0.8	0.259	-119.5	19.71	9.675	130.731	0.041	0.734	0.047	168.782	1.37
0.9	0.279	-125.972	19.35	9.281	125.639	0.041	1.042	0.048	164.393	1.4
1	0.299	-131.628	19	8.911	120.513	0.04	1.762	0.049	163.524	1.45
1.1	0.32	-137.177	18.61	8.521	115.245	0.039	2.85	0.048	164.901	1.51
1.2	0.336	-142.073	18.23	8.159	110.507	0.039	4.1	0.049	167.544	1.55
1.3	0.348	-145.665	17.84	7.801	106.06	0.039	5.603	0.043	170.928	1.59
1.4	0.356	-148.38	17.45	7.455	101.898	0.039	7.304	0.032	178.48	1.64
1.5	0.363	-150.989	17.05	7.121	97.936	0.039	9.091	0.024	-165.089	1.7
1.6	0.37	-154.012	16.65	6.8	94.219	0.039	10.88	0.019	-143.445	1.75
1.7	0.374	-157.396	16.23	6.481	90.464	0.04	12.735	0.02	-106.9	1.78
1.8	0.376	-160.639	15.85	6.2	87.131	0.04	14.442	0.027	-86.207	1.84
1.9	0.376	-163.914	15.47	5.939	83.969	0.041	16.084	0.035	-75.973	1.87
2	0.375	-167.082	15.12	5.699	80.94	0.042	17.612	0.043	-70.287	1.9
2.5	0.372	177.387	13.51	4.736	66.672	0.05	22.955	0.081	-58.59	1.9
3	0.356	158.01	12.14	4.047	53.37	0.059	24.196	0.112	-56.813	1.89
3.5	0.381	144.376	11.06	3.573	39.369	0.07	21.054	0.14	-52.546	1.75
4	0.423	129.789	10.03	3.175	25.905	0.08	17.196	0.146	-53.692	1.66
4.5	0.508	121.918	9.07	2.842	11.472	0.09	11.517	0.155	-54.803	1.49
5	0.576	107.907	8.06	2.528	-2.535	0.102	5.225	0.123	-67.978	1.35
5.5	0.639	99.362	7.06	2.255	-14.4	0.11	-2.316	0.122	-90.136	1.23
6	0.672	88.277	6.69	2.16	-25.888	0.122	-8.464	0.105	-150.094	1.1
6.5	0.672	79.728	5.92	1.976	-37.199	0.125	-15.947	0.121	162.804	1.18
7	0.668	68.454	5.81	1.953	-49.487	0.135	-22.415	0.187	127.855	1.15
7.5	0.657	57.275	5.12	1.803	-62.284	0.142	-30.896	0.213	108.129	1.22
8	0.655	47.003	4.75	1.728	-71.76	0.151	-38.436	0.231	98.412	1.2
9	0.704	28.227	4.24	1.629	-91.789	0.161	-55.934	0.261	73.264	1.09
10	0.772	16.7	3.85	1.558	-107.404	0.162	-68.84	0.298	44.421	0.98

Typical Noise Parameters at 25°C,

$T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 5V$, $I_{ds} = 40$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	NF@50Ω
GHz	dB	Mag.	Ang.		dB
0.5	0.75	0.05	89.7	0.1	0.75
1	0.67	0.06	157.9	0.08	0.67
1.5	0.78	0.1	174	0.07	0.79
2	0.87	0.13	147.1	0.08	0.9
2.5	0.95	0.15	174.2	0.08	0.98
3	0.98	0.22	-169.9	0.08	1.07
3.5	1.1	0.23	-153.6	0.09	1.2
4	1.25	0.26	-146.3	0.1	1.4
4.5	1.33	0.31	-138.5	0.12	1.54
5	1.42	0.36	-127.2	0.14	1.73
5.5	1.44	0.4	-117.8	0.18	1.88
6	1.61	0.43	-107.4	0.22	2.1
6.5	1.66	0.48	-97.8	0.3	2.36
7	1.7	0.53	-89.1	0.38	2.57
7.5	1.92	0.56	-78.4	0.51	2.94
8	2.03	0.58	-68.2	0.69	3.27
8.5	2.21	0.62	-57.2	0.91	3.7
9	2.34	0.65	-50.2	1.18	4.15
9.5	2.23	0.75	-41.6	1.48	4.64
10	2.43	0.75	-36.6	1.8	5.06

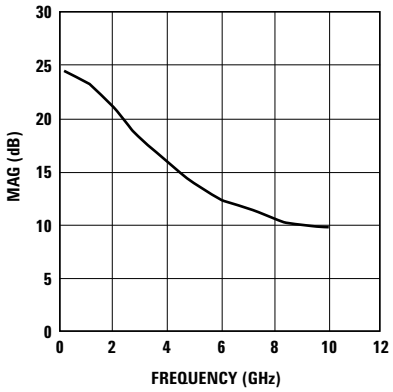


Figure 35. MAG vs. Frequency.

MGA-62563 Typical Scattering Parameters, $T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 5V$, $I_{ds} = 30$ mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		K-factor
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	
0.1	0.237	-58.467	21.8	12.306	156.126	0.048	2.335	0.051	-78.66	1.09
0.2	0.23	-65.183	21.53	11.928	153.564	0.048	1.765	0.045	-87.521	1.11
0.3	0.227	-72.749	21.23	11.518	150.716	0.047	1.228	0.039	-99.059	1.14
0.4	0.226	-81.026	20.89	11.082	147.575	0.047	0.749	0.036	-112.979	1.16
0.5	0.23	-90.235	20.51	10.603	143.898	0.046	0.336	0.033	-129.188	1.21
0.6	0.238	-98.902	20.13	10.153	140.036	0.046	0.043	0.033	-143.928	1.24
0.7	0.25	-107.258	19.75	9.716	135.78	0.045	-0.127	0.034	-156.168	1.28
0.8	0.265	-115.042	19.37	9.304	131.095	0.044	-0.173	0.036	-165.43	1.33
0.9	0.284	-121.835	19.03	8.94	126.04	0.043	-0.043	0.039	-171.896	1.38
1	0.304	-127.797	18.69	8.602	120.95	0.043	0.462	0.041	-173.502	1.4
1.1	0.325	-133.627	18.32	8.246	115.706	0.042	1.306	0.044	-172.856	1.46
1.2	0.342	-138.742	17.97	7.914	110.976	0.042	2.313	0.047	-171.524	1.48
1.3	0.354	-142.508	17.6	7.583	106.528	0.042	3.581	0.044	-166.973	1.52
1.4	0.363	-145.389	17.22	7.259	102.357	0.041	5.063	0.038	-156.713	1.6
1.5	0.371	-148.151	16.83	6.946	98.374	0.041	6.652	0.034	-141.923	1.64
1.6	0.378	-151.305	16.45	6.644	94.631	0.042	8.268	0.032	-127.89	1.66
1.7	0.383	-154.816	16.04	6.342	90.832	0.042	9.963	0.034	-108.748	1.72
1.8	0.386	-158.161	15.67	6.075	87.455	0.043	11.558	0.039	-95.871	1.74
1.9	0.386	-161.511	15.31	5.827	84.258	0.043	13.115	0.045	-87.243	1.8
2	0.385	-164.738	14.96	5.6	81.188	0.044	14.587	0.052	-81.336	1.83
2.5	0.383	179.495	13.41	4.684	66.72	0.051	19.968	0.083	-65.882	1.86
3	0.368	159.885	12.09	4.023	53.234	0.06	21.459	0.111	-61.634	1.85
3.5	0.393	145.917	11.05	3.568	39.154	0.071	18.676	0.136	-55.813	1.72
4	0.435	130.892	10.05	3.179	25.626	0.081	15.046	0.14	-56.384	1.62
4.5	0.52	122.592	9.11	2.854	11.264	0.09	9.563	0.148	-56.648	1.46
5	0.588	108.322	8.1	2.541	-2.66	0.102	3.467	0.117	-69.997	1.32
5.5	0.65	99.592	7.11	2.266	-14.387	0.11	-3.953	0.117	-92.334	1.2
6	0.682	88.363	6.72	2.167	-25.768	0.122	-10.031	0.106	-153.954	1.07
6.5	0.68	79.738	5.93	1.979	-36.871	0.125	-17.411	0.125	160.43	1.16
7	0.675	68.426	5.8	1.949	-49	0.134	-23.769	0.193	126.821	1.14
7.5	0.663	57.213	5.06	1.791	-61.602	0.141	-32.118	0.218	107.343	1.21
8	0.659	46.972	4.67	1.711	-70.948	0.15	-39.536	0.236	97.607	1.21
9	0.707	28.23	4.07	1.597	-90.845	0.16	-56.781	0.265	72.633	1.11
10	0.774	16.694	3.6	1.513	-106.409	0.161	-69.865	0.303	44.117	1

Typical Noise Parameters at 25°C,

$T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 5V$, $I_{ds} = 30$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	NF@50Ω
GHz	dB	Mag.	Ang.		dB
0.5	0.77	0.08	83.8	0.11	0.78
1	0.67	0.05	149.4	0.08	0.68
1.5	0.79	0.09	168.8	0.07	0.8
2	0.87	0.13	142.3	0.08	0.9
2.5	0.95	0.14	169.1	0.08	0.98
3	0.98	0.22	-173.6	0.08	1.06
3.5	1.09	0.23	-159.3	0.08	1.19
4	1.21	0.26	-148.7	0.1	1.35
4.5	1.29	0.31	-140.3	0.11	1.51
5	1.39	0.35	-129.6	0.13	1.68
5.5	1.42	0.39	-120.3	0.17	1.82
6	1.58	0.41	-109.2	0.21	2.03
6.5	1.62	0.47	-100	0.28	2.28
7	1.68	0.52	-90.7	0.35	2.49
7.5	1.88	0.55	-79.9	0.48	2.85
8	2	0.57	-69.8	0.65	3.17
8.5	2.17	0.62	-58.8	0.85	3.59
9	2.3	0.64	-51.3	1.12	4.03
9.5	2.25	0.72	-42.6	1.41	4.48
10	2.37	0.74	-37.8	1.7	4.91

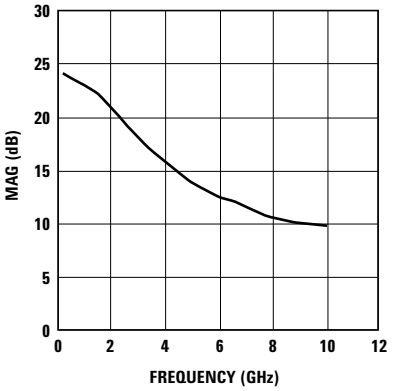


Figure 36. MAG vs. Frequency.

MGA-62563 Typical Scattering Parameters, $T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 5V$, $I_{ds} = 20$ mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		K-factor
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	
0.1	0.276	-50.781	20.99	11.213	156.884	0.053	3.086	0.093	-52.766	1.07
0.2	0.266	-56.676	20.74	10.894	154.329	0.053	2.41	0.083	-58.024	1.09
0.3	0.259	-63.497	20.46	10.544	151.483	0.052	1.753	0.074	-64.698	1.12
0.4	0.255	-71.17	20.15	10.174	148.356	0.052	1.131	0.065	-72.808	1.14
0.5	0.254	-80.022	19.79	9.763	144.671	0.051	0.542	0.058	-83.072	1.18
0.6	0.257	-88.677	19.44	9.375	140.845	0.051	0.052	0.052	-94.078	1.2
0.7	0.265	-97.315	19.08	8.997	136.657	0.05	-0.34	0.05	-105.431	1.24
0.8	0.277	-105.608	18.73	8.641	132.057	0.05	-0.641	0.05	-116.715	1.27
0.9	0.294	-113.01	18.41	8.327	127.118	0.049	-0.769	0.052	-126.861	1.31
1	0.313	-119.584	18.1	8.038	122.134	0.049	-0.568	0.056	-133.663	1.32
1.1	0.332	-125.983	17.77	7.732	117	0.048	-0.093	0.062	-138.752	1.36
1.2	0.349	-131.536	17.44	7.446	112.349	0.048	0.54	0.067	-142.695	1.38
1.3	0.362	-135.667	17.09	7.154	107.971	0.047	1.412	0.068	-141.888	1.43
1.4	0.371	-138.843	16.73	6.864	103.851	0.047	2.497	0.066	-137.128	1.47
1.5	0.38	-141.9	16.37	6.583	99.905	0.047	3.676	0.065	-131.552	1.51
1.6	0.389	-145.323	16	6.311	96.172	0.047	4.908	0.063	-126.926	1.55
1.7	0.394	-149.051	15.62	6.037	92.39	0.047	6.242	0.063	-119.49	1.6
1.8	0.397	-152.57	15.26	5.794	89.022	0.048	7.499	0.065	-113.329	1.62
1.9	0.397	-156.063	14.91	5.566	85.817	0.048	8.774	0.067	-107.935	1.68
2	0.396	-159.406	14.58	5.357	82.739	0.049	10.021	0.07	-103.352	1.7
2.5	0.395	-175.583	13.08	4.508	68.14	0.055	14.801	0.083	-84.66	1.78
3	0.38	164.391	11.79	3.888	54.386	0.063	16.272	0.102	-74.77	1.81
3.5	0.407	149.754	10.77	3.454	40.091	0.074	13.807	0.118	-63.62	1.7
4	0.449	133.82	9.76	3.075	26.308	0.083	10.436	0.118	-61.976	1.63
4.5	0.534	124.633	8.8	2.753	11.752	0.092	5.262	0.123	-58.73	1.47
5	0.6	109.771	7.78	2.448	-2.529	0.104	-0.451	0.093	-72.766	1.33
5.5	0.661	100.709	6.77	2.179	-14.499	0.111	-7.532	0.097	-96.992	1.22
6	0.692	89.216	6.37	2.083	-26.054	0.122	-13.423	0.102	-166.868	1.09
6.5	0.688	80.407	5.56	1.897	-37.379	0.125	-20.653	0.134	151.132	1.18
7	0.681	69.043	5.43	1.868	-49.653	0.134	-26.784	0.209	121.656	1.16
7.5	0.666	57.717	4.69	1.716	-62.476	0.141	-34.82	0.234	103.118	1.24
8	0.661	47.473	4.3	1.641	-71.899	0.149	-41.982	0.25	93.688	1.24
9	0.708	28.579	3.73	1.537	-92	0.159	-58.934	0.278	69.322	1.13
10	0.774	16.789	3.28	1.459	-107.719	0.161	-72.037	0.315	41.449	1.02

Typical Noise Parameters at 25°C,

$T_C = 25°C$, $Z_0 = 50\Omega$, $V_d = 5V$, $I_{ds} = 20$ mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	NF@50Ω
GHz	dB	Mag.	Ang.		dB
0.5	0.81	0.1	90	0.11	0.83
1	0.7	0.05	129.3	0.08	0.71
1.5	0.82	0.08	150.1	0.08	0.83
2	0.9	0.13	132.1	0.08	0.92
2.5	0.94	0.15	158.4	0.08	0.98
3	0.98	0.22	180	0.07	1.06
3.5	1.1	0.23	-165	0.08	1.19
4	1.19	0.27	-153.6	0.09	1.34
4.5	1.28	0.31	-144.2	0.1	1.49
5	1.39	0.35	-132.9	0.12	1.66
5.5	1.42	0.39	-122.5	0.16	1.81
6	1.58	0.4	-112	0.2	2.01
6.5	1.64	0.46	-102.7	0.27	2.26
7	1.7	0.51	-93.5	0.33	2.47
7.5	1.9	0.54	-82.5	0.45	2.82
8	1.99	0.57	-71.3	0.62	3.15
8.5	2.17	0.6	-60.2	0.82	3.54
9	2.3	0.63	-52.6	1.09	3.98
9.5	2.11	0.75	-44	1.36	4.45
10	2.41	0.73	-38.5	1.67	4.85

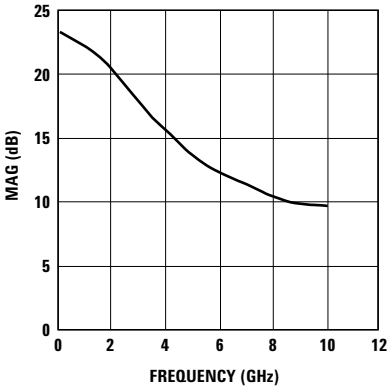


Figure 37. MAG vs. Frequency.

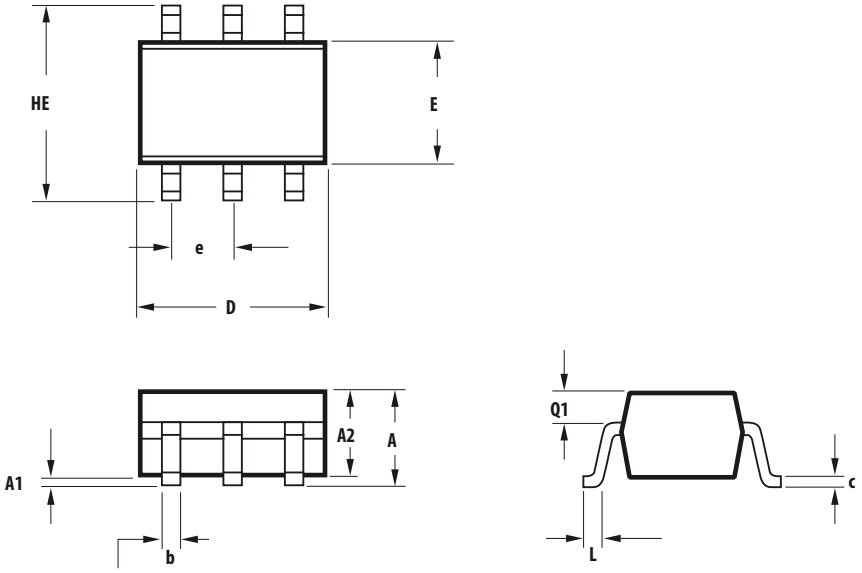
Refer to Avago Technologies Web Site for S-parameters at different biases. www.avagotech.com/view/rf

Device Models, Refer to Avago Technologies Web Site www.avagotech.com/view/rf

Ordering Information

Part Number	No. of Devices	Container
MGA-62563-TR1G	3000	7″ Reel
MGA-62563-TR2G	10000	13″Reel
MGA-62563-BLKG	100	antistatic bag

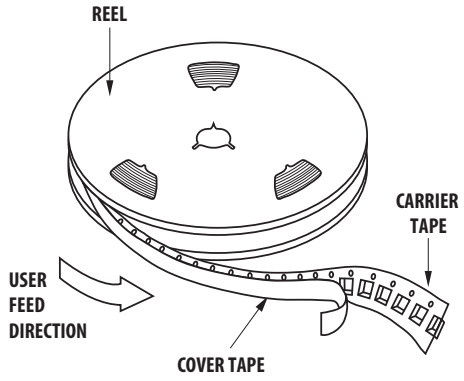
SOT-363/SC-70 (JEDEC DFP-N) Package Dimensions

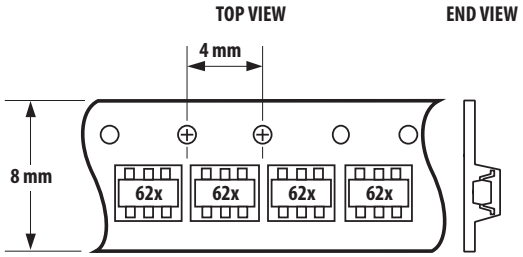


SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.650 BCS	
b	0.15	0.30
c	0.10	0.20
L	0.10	0.30

NOTES:
1. All dimensions are in mm.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to EIAJ SC70.
5. Die is facing up for mold and facing down for trim/form, ie: reverse trim/form.
6. Package surface to be mirror finish.

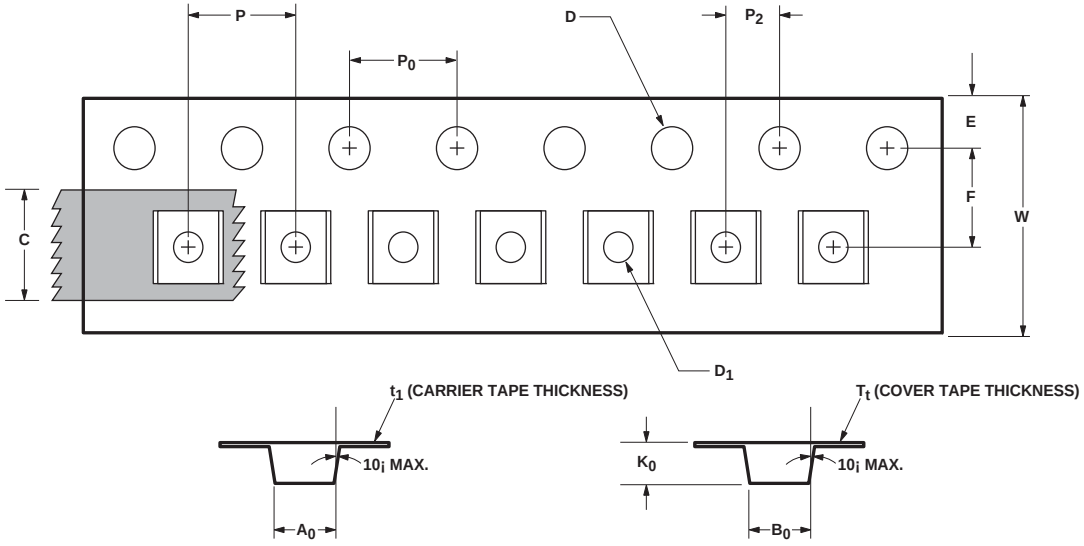
Device Orientation





(Package marking example orientation shown.)

Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30 - 0.10	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.40 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1237EN - August 5, 2011

MITSUBISHI ELECTRIC

< High-power GaAs FET (small signal gain stage) >

MGF0905A

L & S BAND / 2.5W
non - matched

DESCRIPTION

The MGF0905A, GaAs FET with an N-channel schottky gate, is designed for use L & S band amplifiers.

FEATURES

- High output power
  Po=34.0dBm(TYP.) @f=1.65GHz,Pin=26dBm
- High power gain
  Gp=8.0dB(TYP.) @f=1.65GHz,Pin=26dBm
- High power added efficiency
  P.A.E=40%(TYP.) @f=1.65GHz,Pin=26dBm

APPLICATION

- for L & S band power amplifiers

QUALITY

- GG

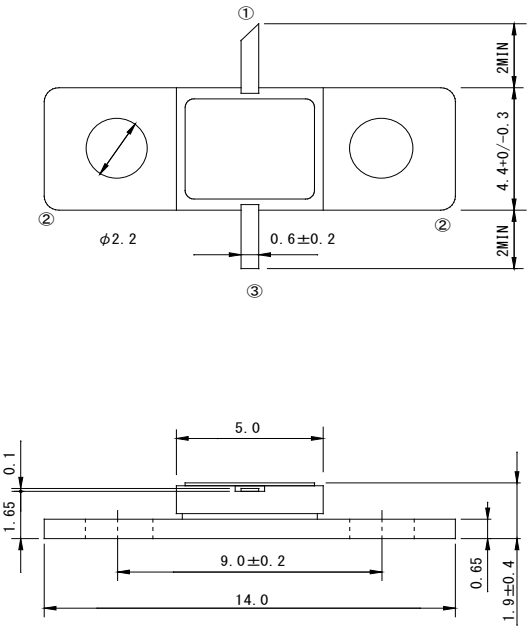
Packaging

- 4 inch Tray (25 pcs)

RECOMMENDED BIAS CONDITIONS

- Vds=8V • Ids=800mA • Rg=100Ω

OUTLINE DRAWING Unit : millimeters



GF-7

(1) GATE
(2) SOURCE (FLANGE)
(3) DRAIN

Absolute maximum ratings (Ta=25°C)

Symbol	Parameter	Ratings	Unit
VGDO	Gate to Drain Voltage	-17	V
VGSO	Gate to source voltage	-17	V
ID	Drain current	3200	mA
IGR	Reverse gate current	-10	mA
IGF	Forward gate current	21.5	mA
PT*1	Total power dissipation	14.3	W
Tch	Cannel temperature	175	°C
Tstg	Storage temperature	-65 to +175	°C

*1:Tc=25°C

Electrical characteristics (Ta=25°C)

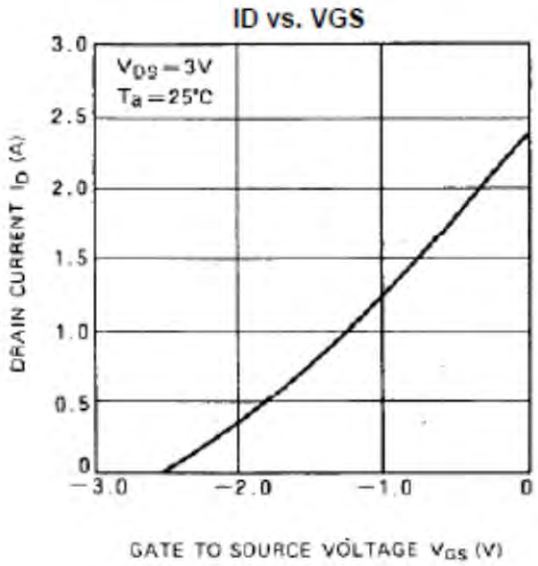
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
IDSS	Saturation drain current	VDS=3V. VGS=0V	1600	2450	3200	mA
gm	Transconductance	VDS=3V, ID=800mA	-	800	-	mS
VGS(off)	Gate to source cut-off voltage	VDS=3V,ID=10mA	-1	-3	-5	V
Po	Output power	VDS=8V,ID(RF off)=800mA	33	34	-	dBm
P.A.E	Power added efficiency	f=1.65GHz	-	40	-	%
ID	Drain Current	Pin=26dBm	-	650	-	mA
Rth(ch-c) *2	Thermal resistance	ΔVf method	-	-	10.5	°C/W

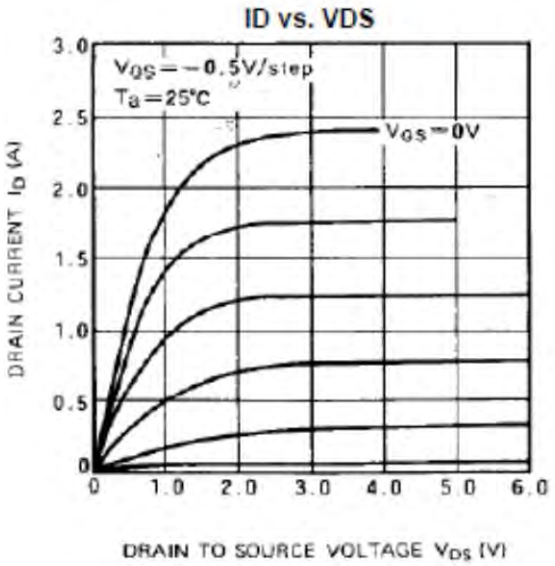
*2 :Channel-case

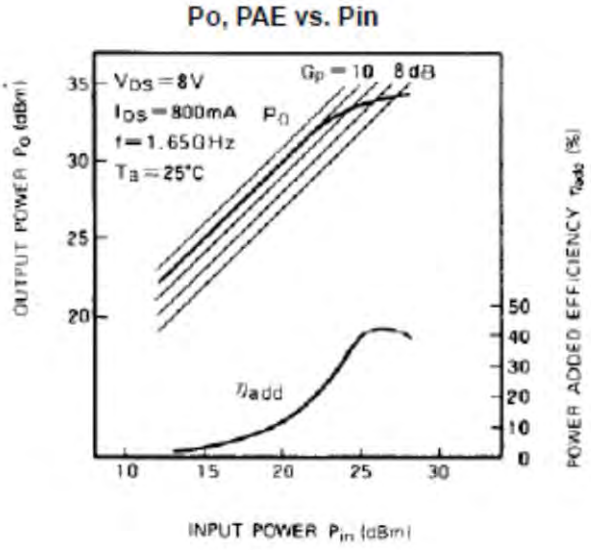
Publication Date : Dec., 2014
CSTG-16249

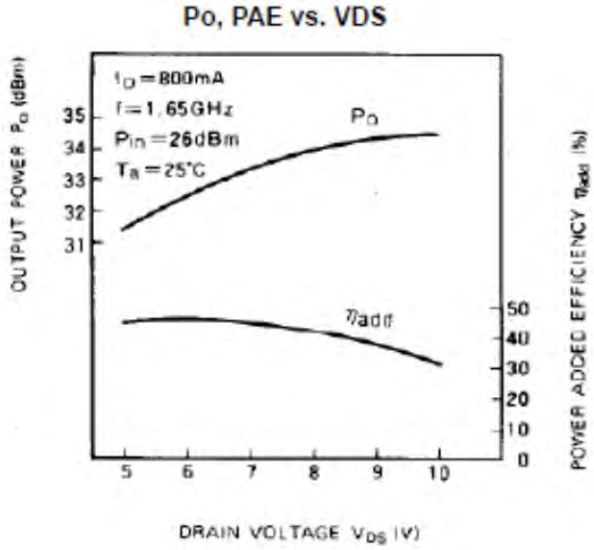
MITSUBISHI ELECTRIC CORPORATION

MGF0904A TYPICAL CHARACTERISTICS(Ta=25deg.C)

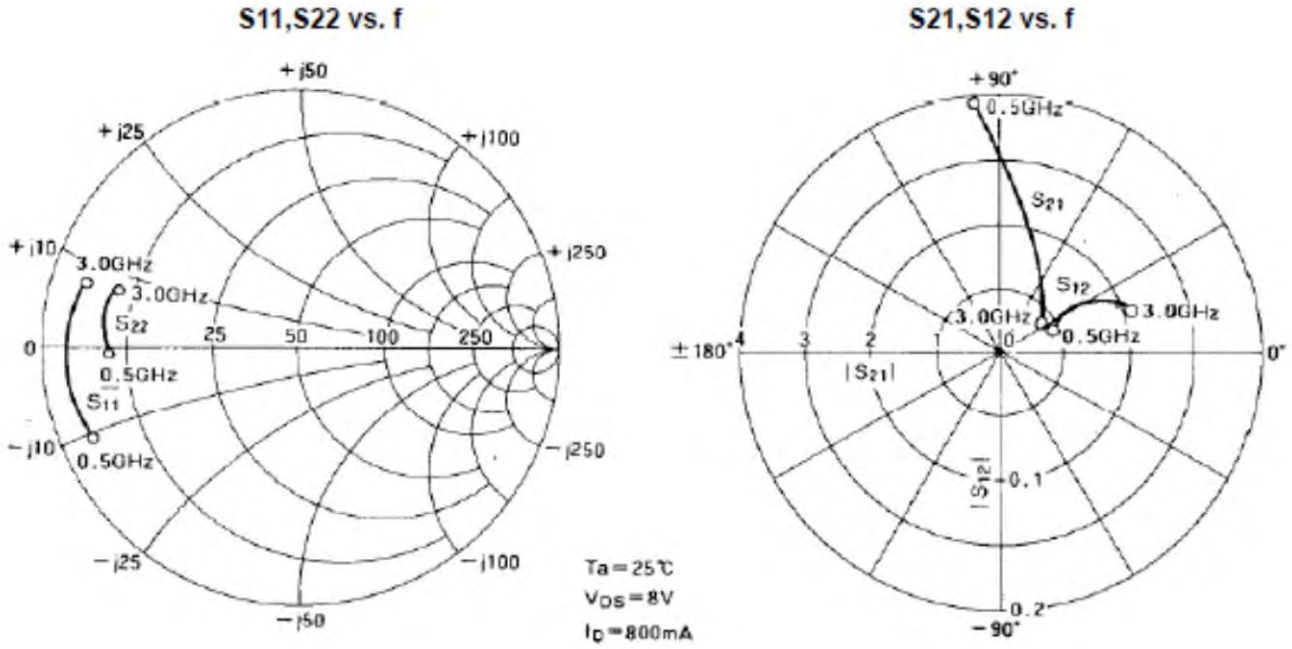








MGF0904A S-parameters(Ta=25deg.C , VDS=8(V), IDS=800(mA))



f (GHz)	S Parameters(Typ.)									
	S11		S21		S12		S22		K	MSG/MAG
	Magn.	Angle(deg.)	Magn.	Angle(deg.)	Magn.	Angle(deg.)	Magn.	Angle(deg.)	-	dB
0.5	0.861	-155.5	3.895	96.0	0.022	25.0	0.731	-179.0	0.806	22.5
1.0	0.887	-170.5	1.999	78.0	0.025	33.0	0.753	175.5	1.133	16.8
1.5	0.894	177.0	1.485	68.0	0.033	33.0	0.747	172.5	1.175	14.0
2.0	0.887	173.0	1.205	58.0	0.039	29.0	0.743	169.5	1.205	12.2
2.5	0.877	169.0	1.000	48.5	0.047	24.0	0.738	166.5	1.221	10.4
3.0	0.864	165.0	0.795	35.0	0.054	18.0	0.723	164.0	1.365	8.1

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CSTG-16249

MITSUBISHI ELECTRIC CORPORATION

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www.golledge.com

Golledge Electronics Ltd
Eaglewood Park, ILMINSTER
Somerset, TA19 9DQ, UK

SAW Filter 742.50MHz **Model: TA1016A**
Part No: MP03363 **Rev No: 1**

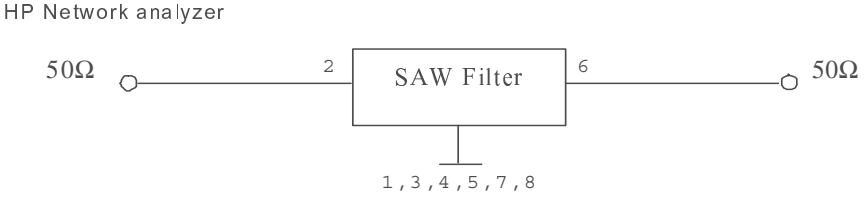
A. MAXIMUM RATING:

1. Input Power Level: 10dBm
2. DC Voltage: 3V
3. Operating Temperature: -30℃ to +85℃
4. Storage Temperature: -40℃ to +85℃

B. ELECTRICAL CHARACTERISTICS:

Item	Unit	Min.	Typ.	Max.	Note
Center Frequency Fc	MHz	-	742.5	-	-
Insertion loss (727 ~ 758MHz) IL	dB	-	2.3	4	-
Bandwidth @ -2.5dB	MHz	31	37	-	-
Amplitude Ripple (less than 2.0 dB in any 11MHz portion of the specified band)	dB	-	0.7	2.5	-
Attenuation (Reference level from 0dB)					
300 ~ 650MHz	dB	28	55	-	-
698 ~ 716MHz	dB	10	45	-	-
776 ~ 787MHz	dB	10	31	-	-
840 ~ 1050MHz	dB	28	49	-	-
Temperature Coefficient of Frequency	ppm/℃	-	-36	-	-

C. MEASUREMENT CIRCUIT:



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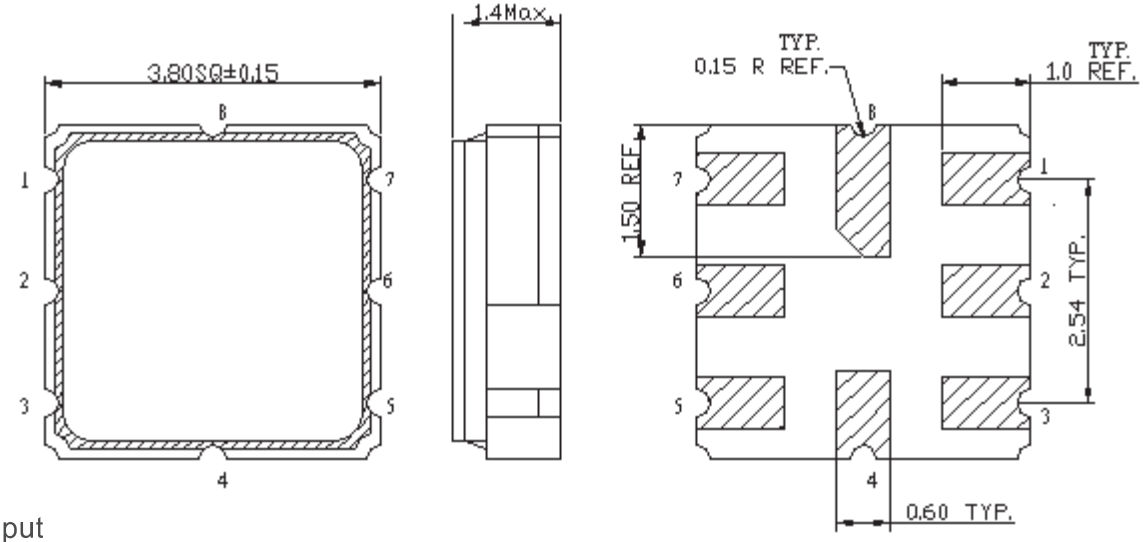
D. OUTLINE DRAWING:



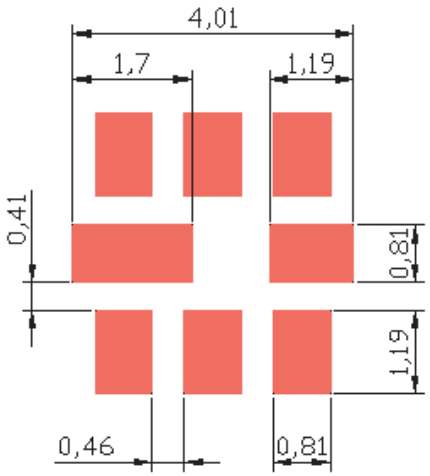
2: Input

6: Output

1, 3, 4, 5, 7, 8: Ground

Unit: mm

E. PCB FOOTPRINT:



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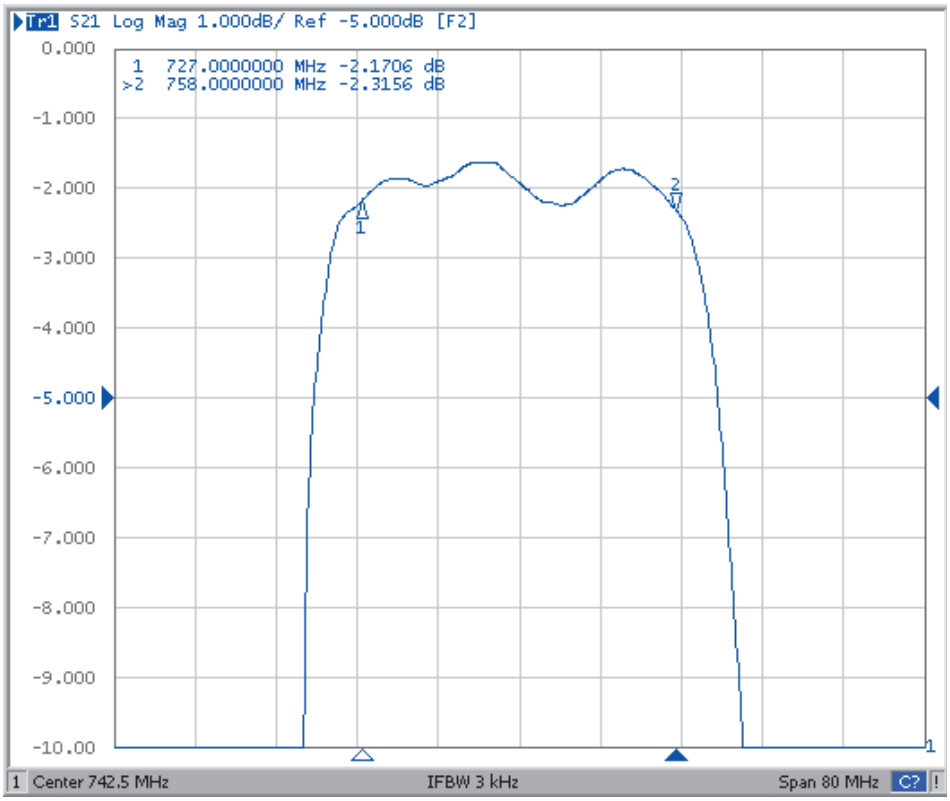
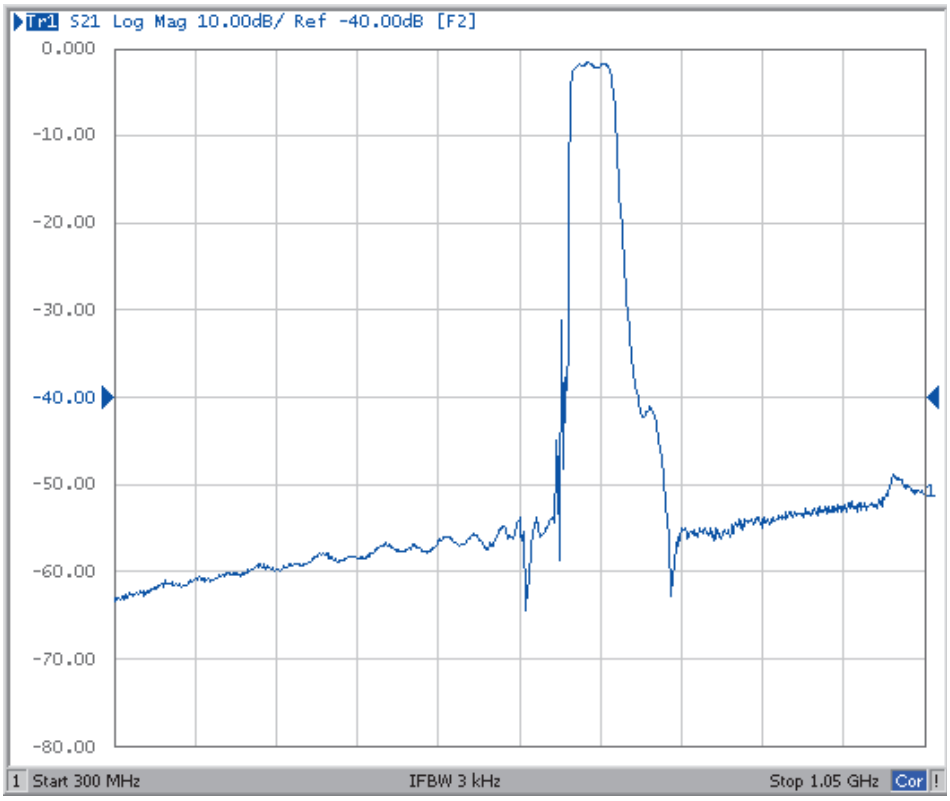
F. FREQUENCY CHARACTERISTICS:





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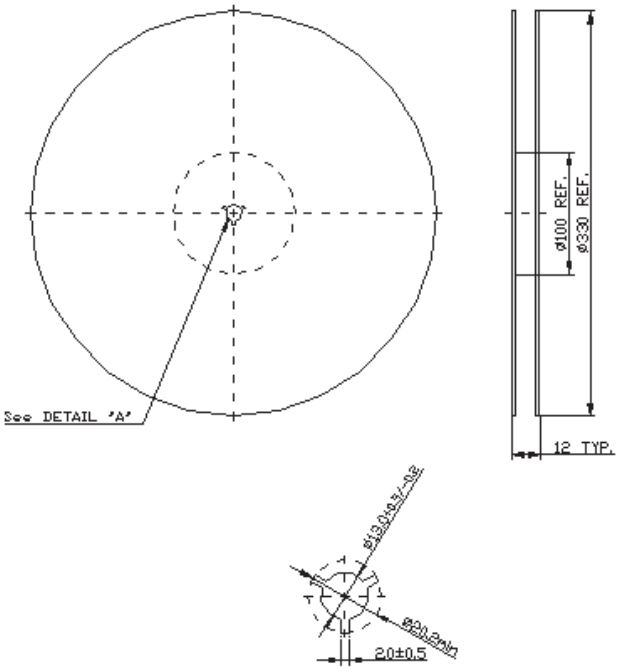
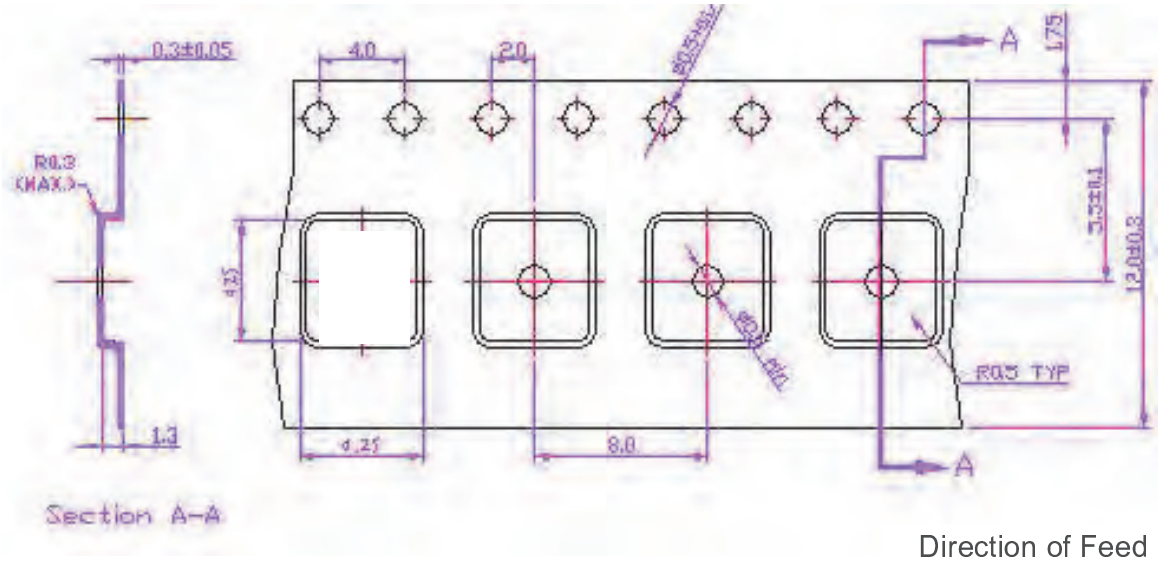
G. PACKING:

1. Reel Dimension

(Reel Count: 7” = 1000; 13” = 3000)



2. Tape Dimension



Direction of Feed

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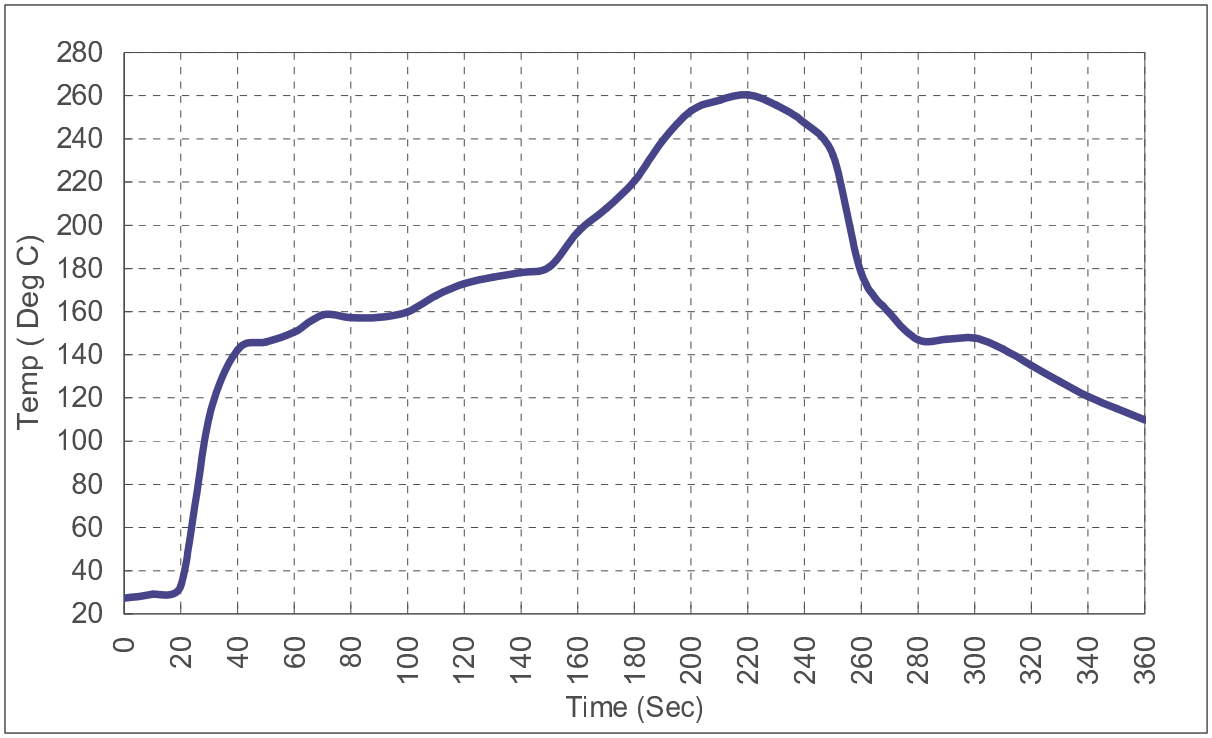
H. RECOMMENDED REFLOW PROFILE:



Temperature Compensated Crystal Oscillator

SAMSUNG ELECTRO-MECHANICS

Temperature Compensated Crystal Oscillator

■ INTRODUCTION

TCXO is abbreviation of Temperature Compensated Crystal Oscillator. TCXO is a reference oscillator in frequency synthesizers required highly accurate frequency stabilization, such as PLL in mobile phone and various telecommunication system. Generally, TCXO is divided into two types : discrete type and 1 chip IC type. discrete type TCXO is consisted of crystal, MLCC, oscillation IC, resistor, thermistor and PCB. 1 chip IC type TCXO is consisted of crystal, 1 chip IC, ceramic package.

■ FEATURE AND APPLICATION

● Feature

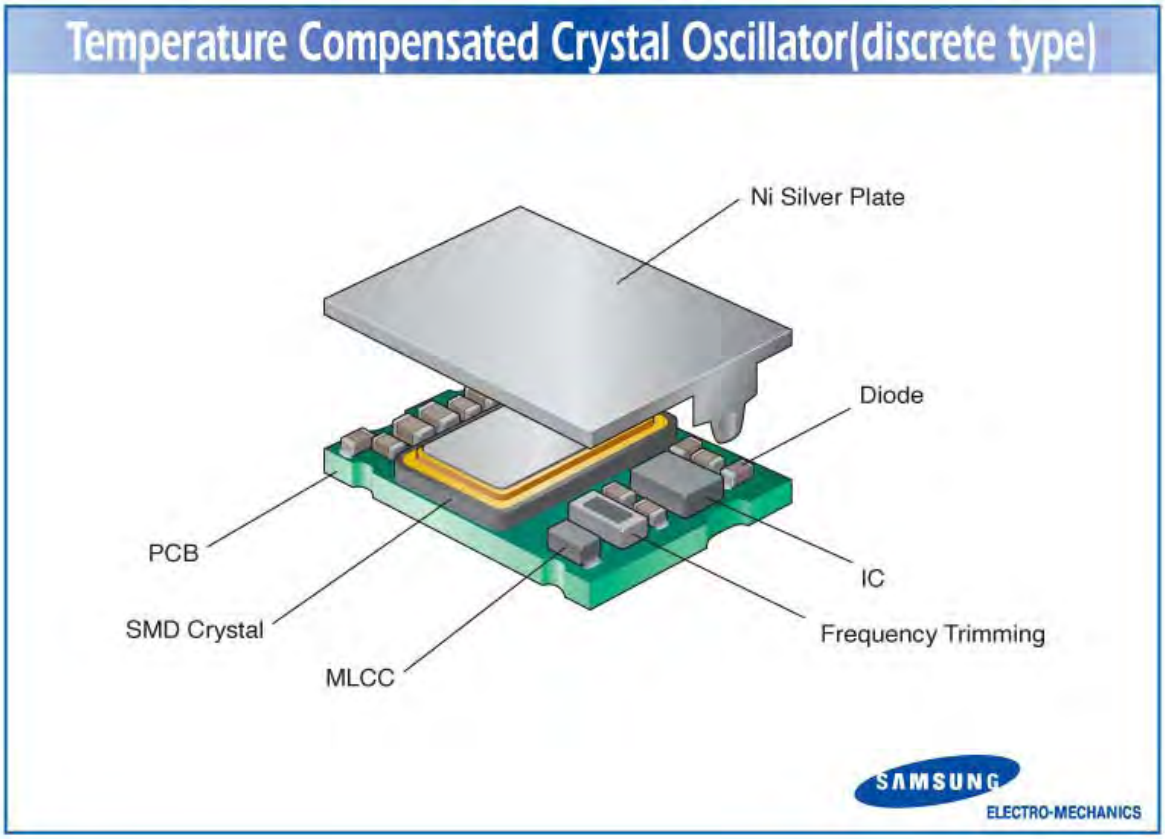
- Various products
- SMD type(leadless)
- Industry Standard Size
- AFC(Auto Function Control) function is available
- Highly accurate frequency stability
- Low power consumption
- Tape & Reel for Surface Mount Assembly

● Application

- GSM / GPRS / UMTS / W-CDMA : 13MHz, 26MHz
- PCS / CDMA / 1xEVDO : 19.2MHz, 19.68MHz
- PCS / CDMA (include GPS function) : 19.2MHz

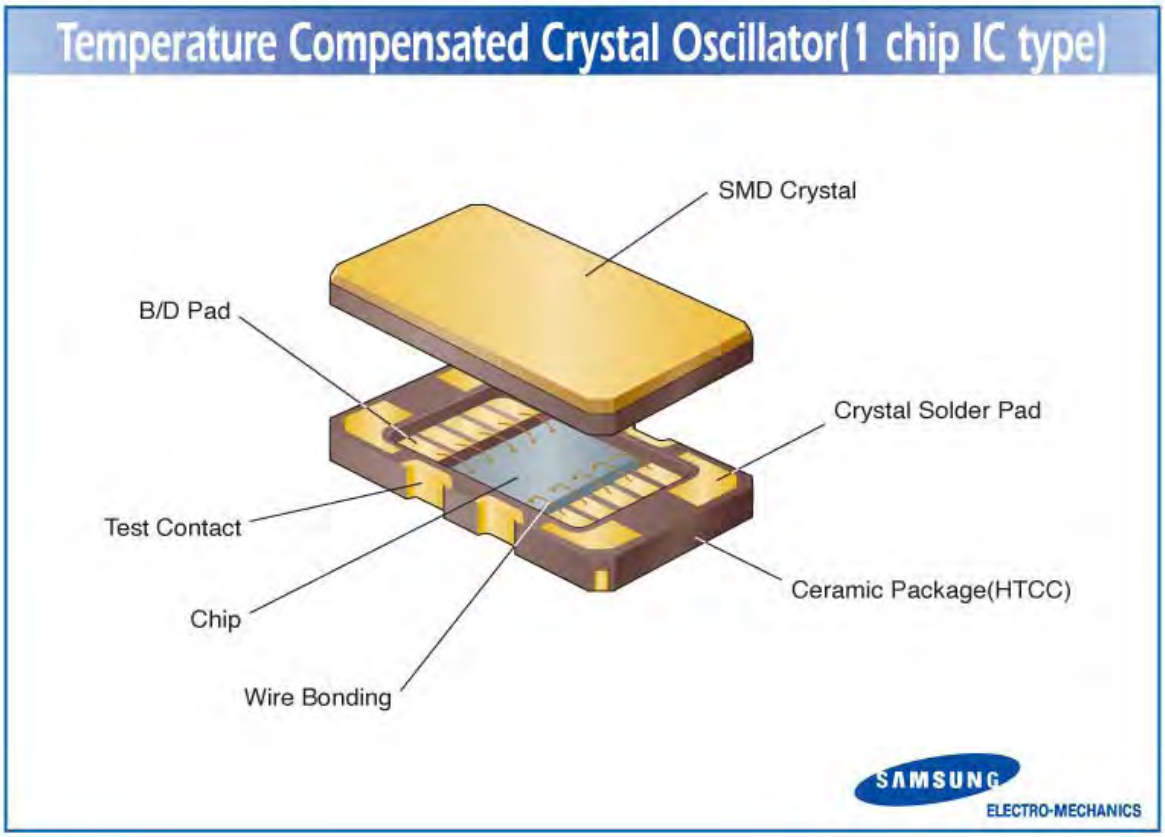
■ STRUCTURE

● **Discrete type (7x5, 5x3.2)**



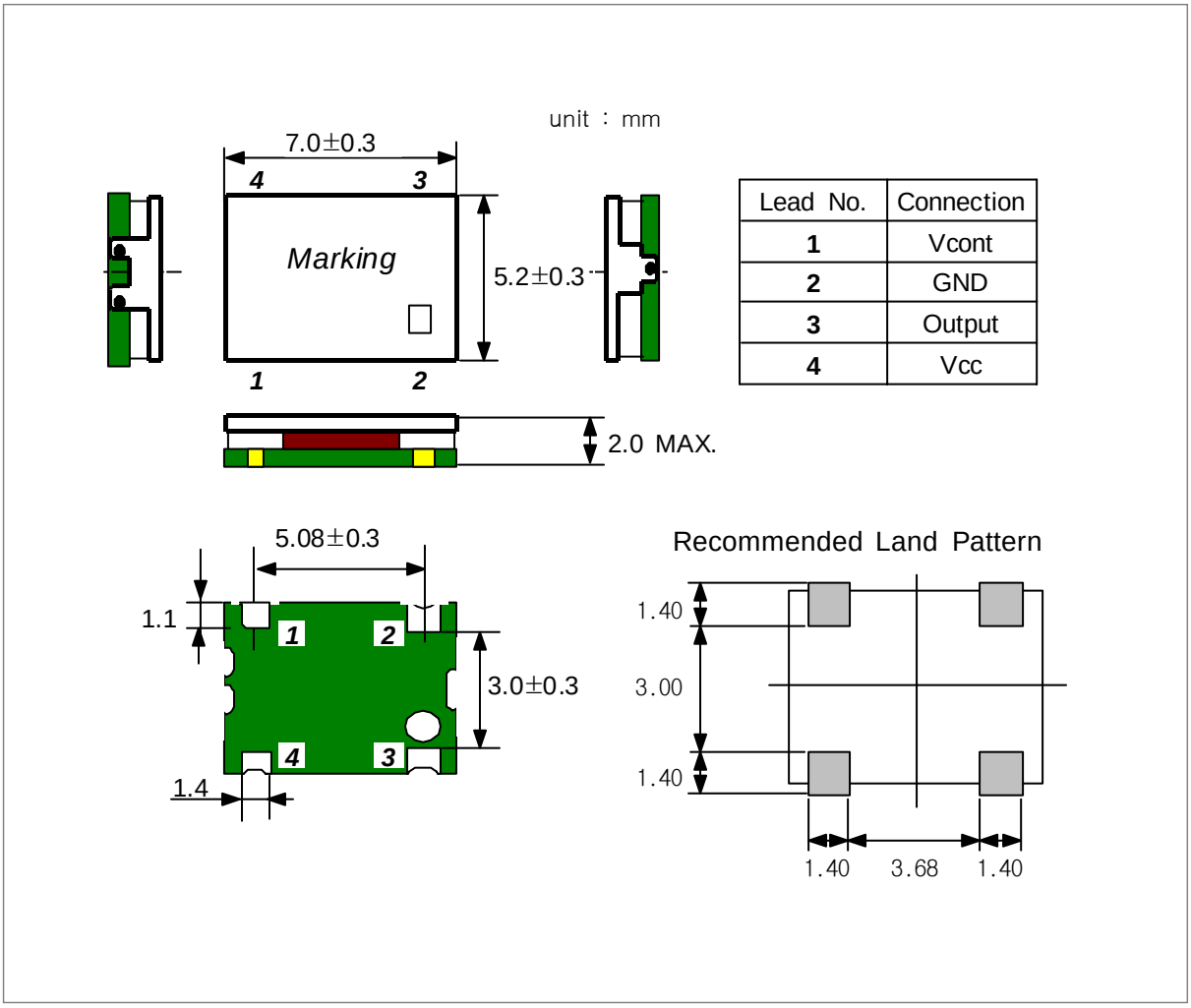
Temperature Compensated Crystal Oscillator

● **1 chip IC type (5x3.2, 4x2.5, 3.2x2.5)**



■ APPEARANCE AND DIMENSION

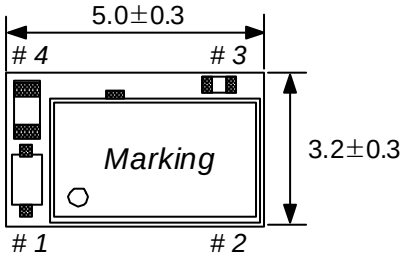
● 7x5 Discrete type



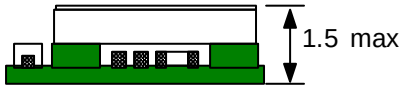
Lead No.	Connection
1	Vcont
2	GND
3	Output
4	Vcc

● **5x3.2 Discrete type**

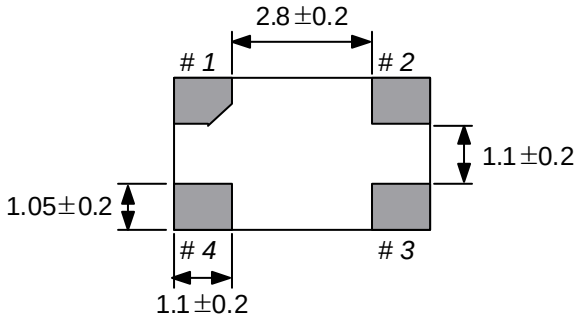
unit : mm

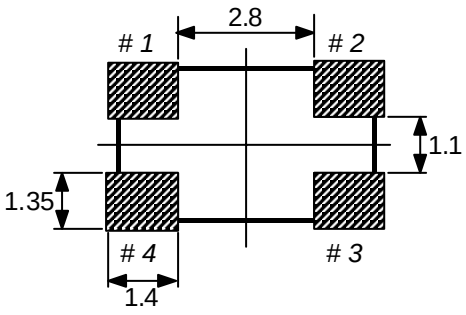


Lead No.	Connection
1	Vcont
2	GND
3	Output
4	Vcc



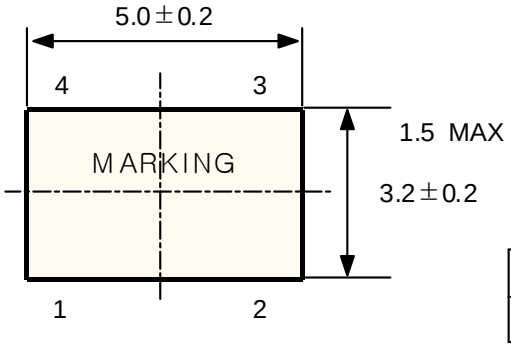
※ Recommended Land Pattern



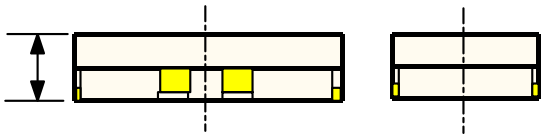


● **5x3.2 1 chip IC type**

Top View

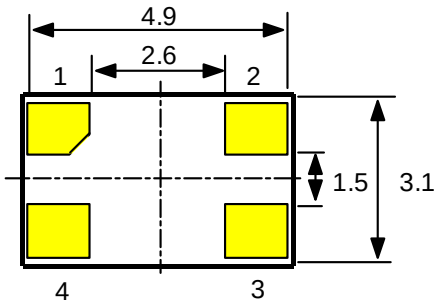


Side View

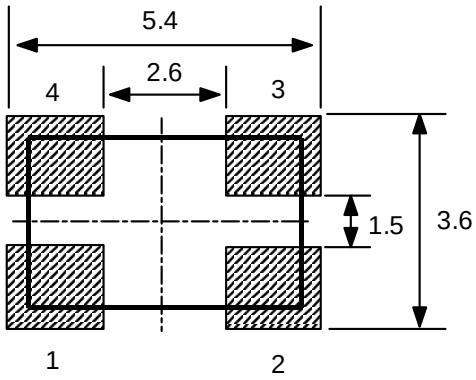


Lead No.	1	2	3	4
Connection	Vcont	GND	Output	Vcc

Bottom View

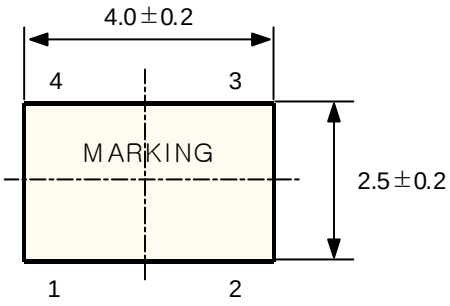


Recommended Land Pattern

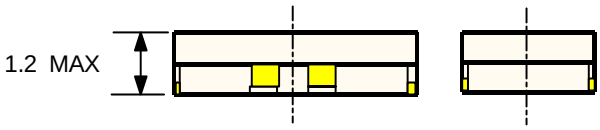


● **4x2.5 1 chip IC type**

Top View

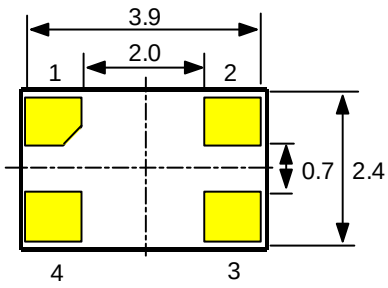


Side View

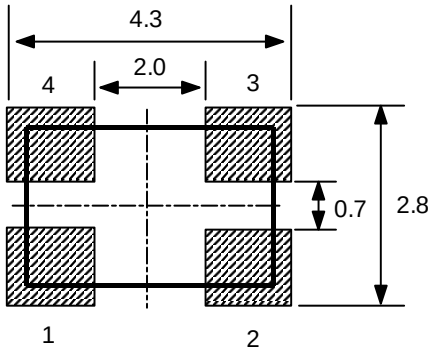


Lead No.	*1*	*2*	*3*	*4*
Connection	Vcont	GND	Output	Vcc

Bottom View

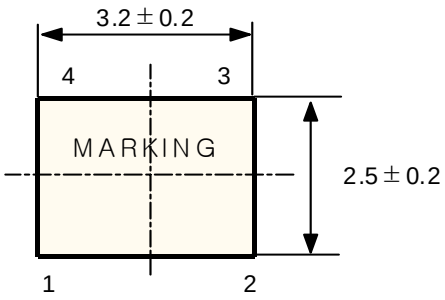


※ Recommended Land Pattern

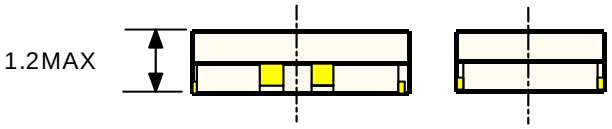


● **3.2x2.5 1 chip IC type**

Top View

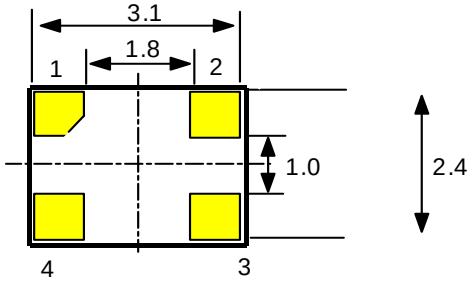


Side View

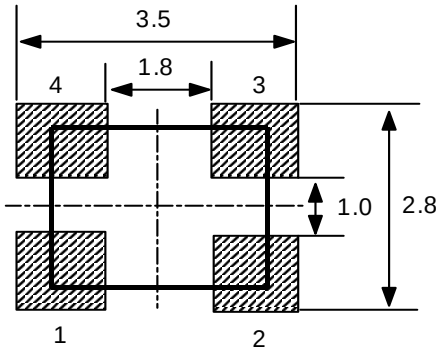


Lead No.	1	2	3	4
Connection	Vcont	GND	Output	Vcc

Bottom View



※ Recommended Land Pattern



■ PART NUMBERING

TO	B	1920	D	P	H	4	KR	A
❶	❷	❸	❹	❺	❻	❼	❽	❾

❶ Product Abbreviation
❷ Size
❸ Nominal Frequency
❹ Additional Function
❺ Operating Voltage
❻ Operating Temperature
❼ Pin Number
❽ Country Code
❾ User Serial Number

❶ Product Abbreviation

Abbreviation of Temperature Compensated Crystal Oscillator

❷ Size

Symbol	Size
U	11.4x9.6x2.6 mm
S	9.0x7.0x2.0 mm
A	7.0x5.2x2.0 mm / 7.0x5.0x2.0 mm
B	5.0x3.2x1.5 mm
F	4.0x2.5x1.5 mm
C	User Spec

❸ Nominal Frequency

EX) 1920 : 19.200000 MHz

❹ Additional Function

Symbol	Additional Function
N	No Additional Function
V	Voltage Controlled Method
D	Digital Temperature Compensation

❺ Operating Voltage

Symbol	Operating Voltage
A	3.0V
B	3.3V
C	4.0V
D	5.0V
P	2.8V

❻ Operating Temperature

Symbol	Operating Temperature
H	-30℃ ~ 80'C
I	-30℃ ~ 75'C
J	-30℃ ~ 70'C
K	-20℃ ~ 70'C
L	0℃ ~ 50'C
M	User Spec

❼ Pin Number

Symbol	Pin Number
4	4
6	6

❽ Country Code

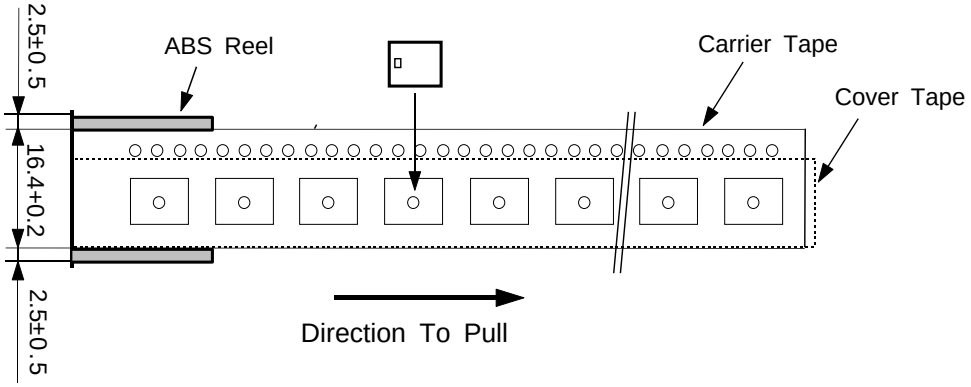
Symbol	Country
KR	Korea
US	United States of America
FR	France
DK	Denmark
DE	Germany

❾ User Serial Number

Give a character from A to Z in order of User Serial Number

■ PACKAGING

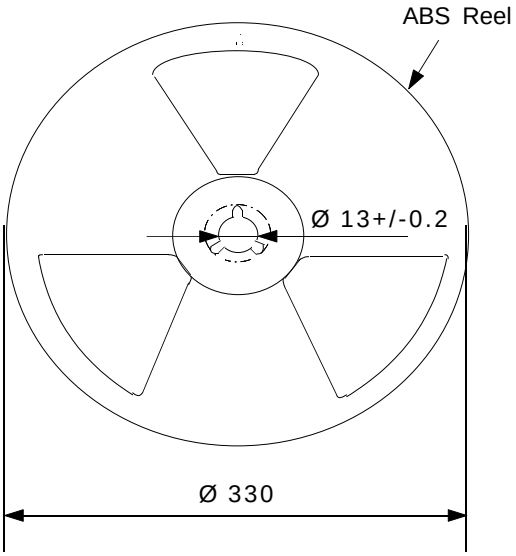
● 7x5 Discrete type

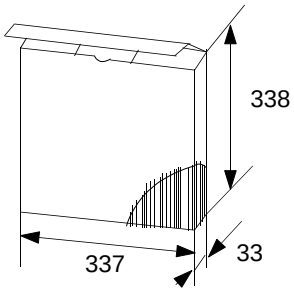


7-1. After inserting products into the carrier tape, and then it is rolled up to ABS reel under the shielding condition of carrier covering tape. Direction to pull is shown on the above drawings.

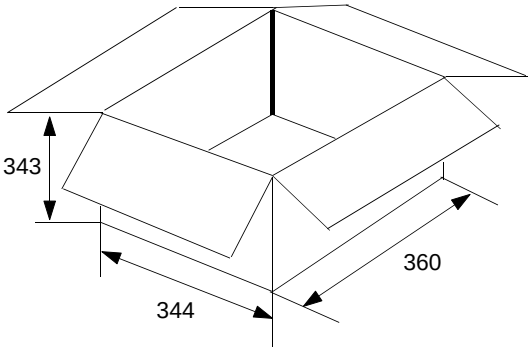
7-2. Both the end edge, 160㎜ of carrier tape will be shield without products.

7-3. Degree of detaching strength of carrier tape
(1) Angle : 165' ~ 185'
(2) Speed : 300mm/min (5mm/Sec.)
(3) Force : 20g ~ 70g



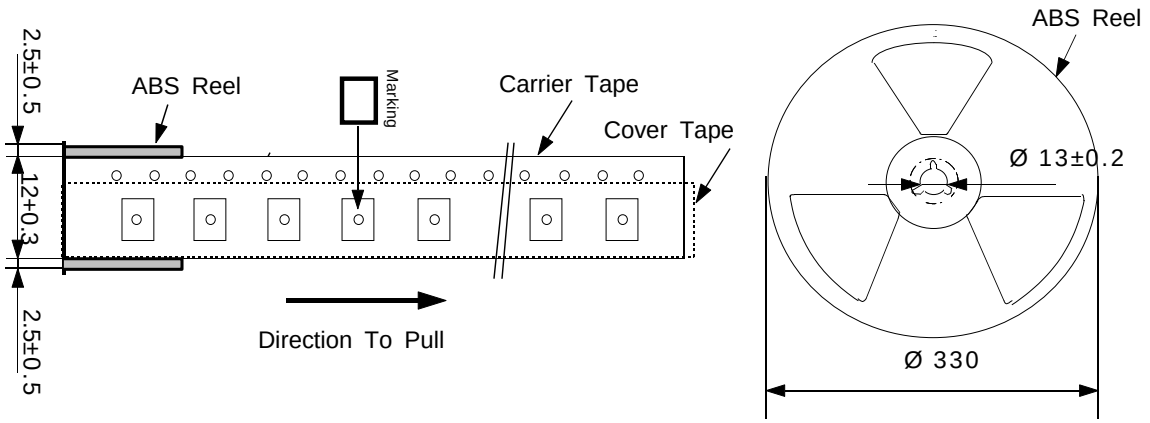


● Inner Box Packaging Quantity
: 1 reel / box (2,000 pcs / reel)

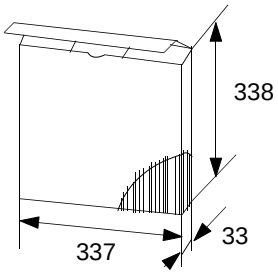


● Outer Box Packaging Quantity
: 20,000 pcs / box

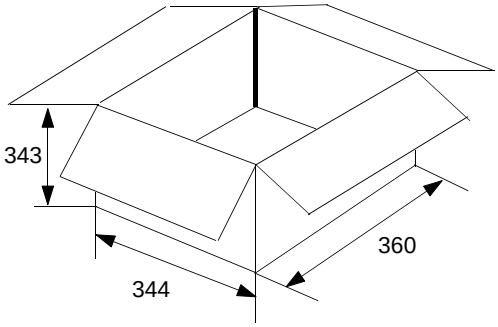
● **5x3.2 1 chip IC type, Discrete type**



1. After inserting products into the carrier tape, and then it is rolled up to ABS reel under the shielding condition of carrier covering tape. Direction to pull is shown on the above drawings .
2. Both the end edge, 160㎜ of carrier tape will be shield without products.
3. Degree of detaching strength of carrier tape
   (1) Angle : 165˚ ~ 185˚
   (2) Speed : 300mm/min (5mm/Sec.)
   (3) Force : 20g ~ 70g

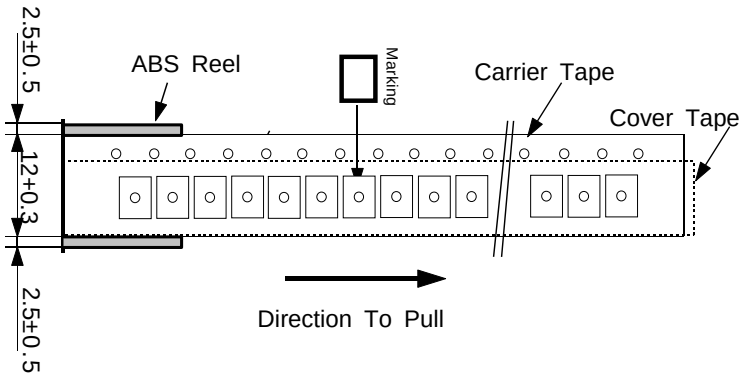


● Inner Box Packaging Quantity
: 1 reel / box (3,000 pcs / reel)

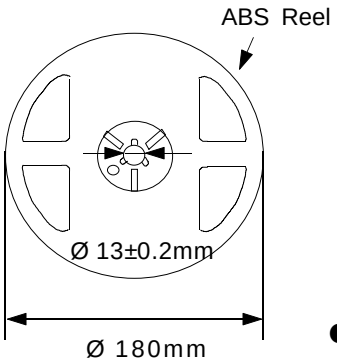


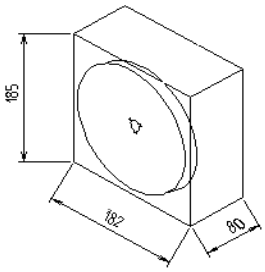
● Outer Box Packaging Quantity
: 30,000 pcs / box

● **4x2.5 1 chip IC type**

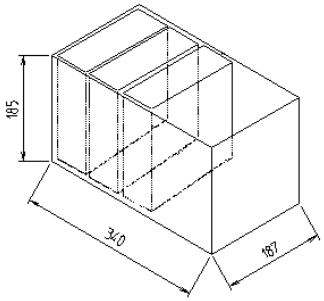


1. After inserting products into the carrier tape, and then it is rolled up to ABS reel under the shielding condition of carrier covering tape. Direction to pull is shown on the above drawings.
2. Both the end edge, 160㎜ of carrier tape will be shield without products.
3. Degree of detaching strength of carrier tape
   (1) Angle : 165° ~ 185°
   (2) Speed : 300mm/min (5mm/Sec.)
   (3) Force : 20g ~ 70g

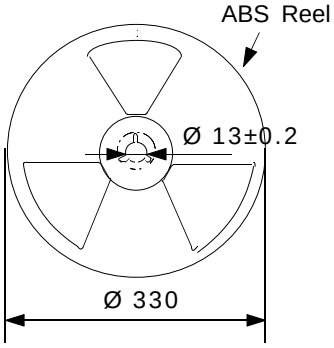


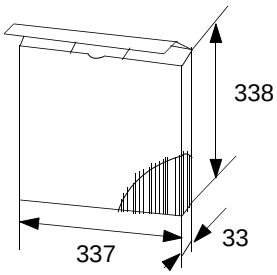


● Inner Box Packaging Quantity
: 5 reel / box (3,500 pcs / reel)

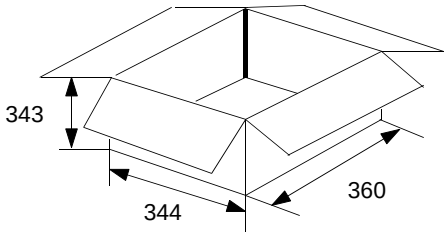


● Outer Box Packaging Quantity
: 70,000 pcs / box





● Inner Box Packaging Quantity
: 1 reel / box (9,000 pcs / reel)



● Outer Box Packaging Quantity
: 90,000 pcs / box

■ RELIABILITY TEST DATA

NO	ITEM	TEST CONDITION
1	High Temp. Storage	85+/-2'C, 96+/-2Hr
2	Low Temp. Storage	-40+/-2'C, 96+/-2Hr
3	High Temp. & High Humidity Storage	40'C, 90~95%RH, 96+/-2Hr
4	Thermal shock	-40'C/30min ~ 85'C/30min, 15cycles
5	Vibration	Frequency : 20~2000Hz Acceleration : 5G XYZ each direction × 30min
6	Drop	150cm, 120g Jig, onto concrete, each side(6), corner(1), total 7times
7	Solderability	230℃+/-5℃ for 10sec, more than 90% must be covered
8	Solder heat resistance	260+/-5℃ for 10sec

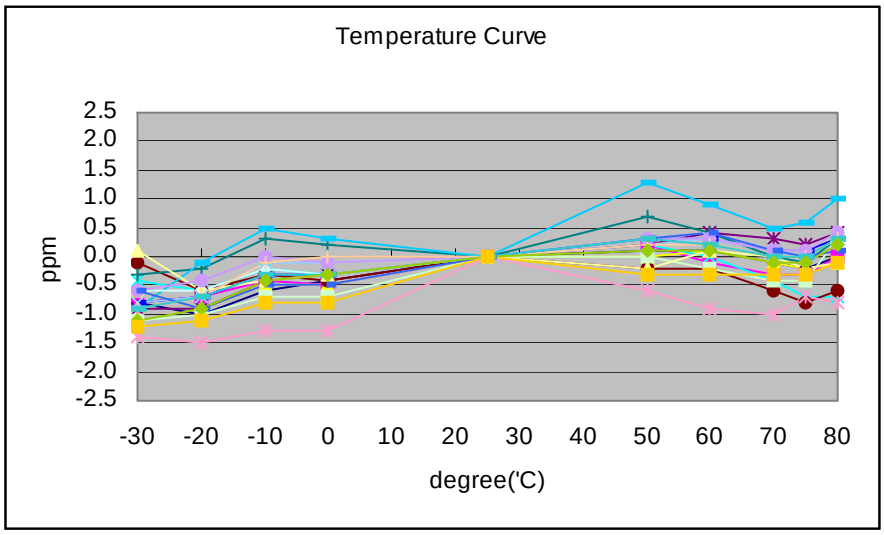
Note

1. Must be measured after 4~12hours at room temperature, humidity.
2. Frequency must be within initial value +/-2ppm.

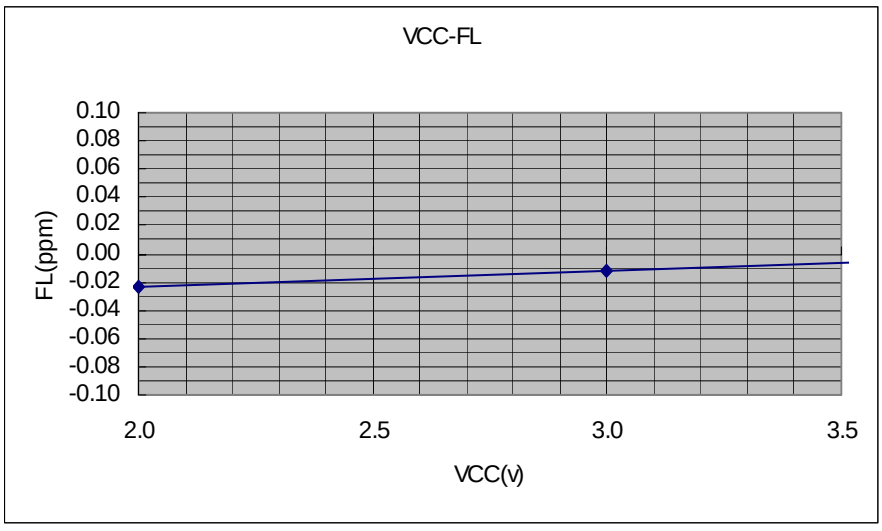
■ CHARACTERISTIC GRAPH

● ELECTRICAL CHARACTERISTICS

▶ TEMPERATURE CHARACTERISTICS CURVE

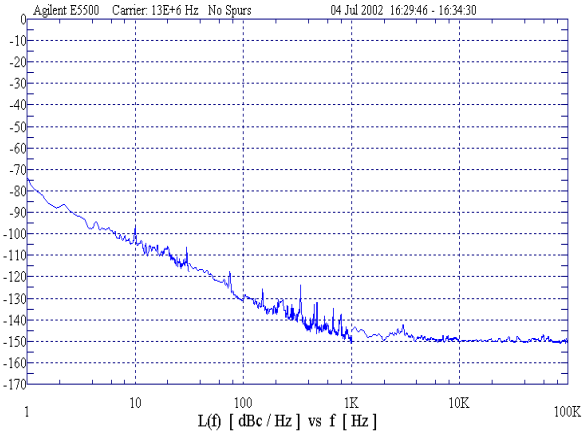


▶ PUSHING CHARACTERISTICS (SUPPLY VOLTAGE VARIATION)

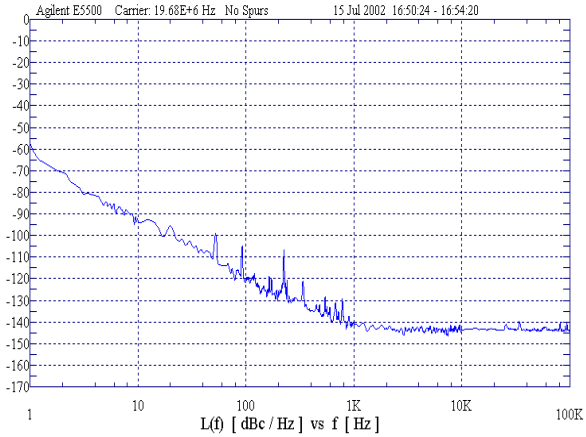


▶ PHASE NOISE (7x5 discrete type)

7052 13MHz (discrete type)

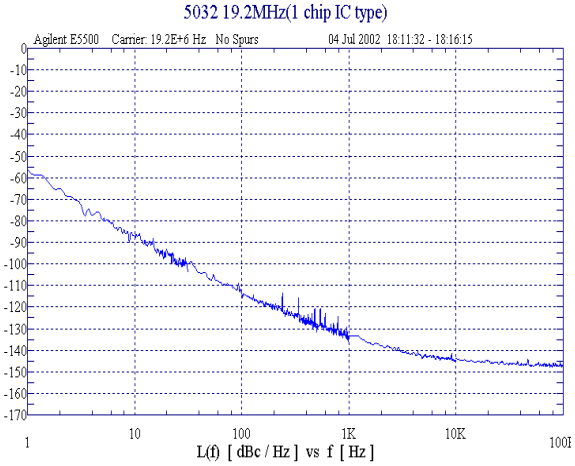


7052 19.68MHz (discrete type)

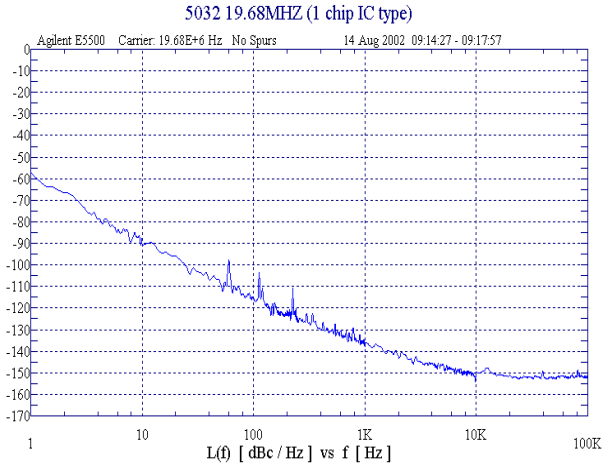


▶ PHASE NOISE (5x3.2 1 chip IC type)

5032 19.2MHz(1 chip IC type)

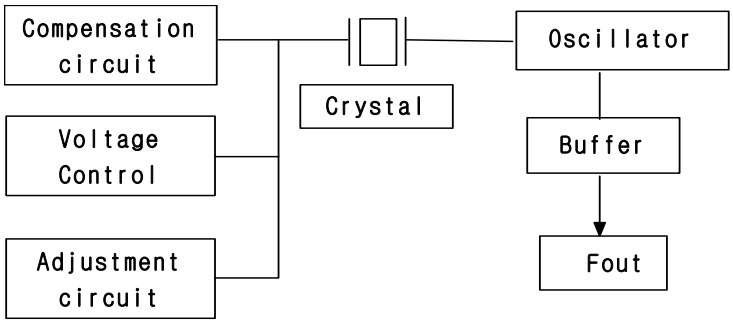


5032 19.68MHZ (1 chip IC type)

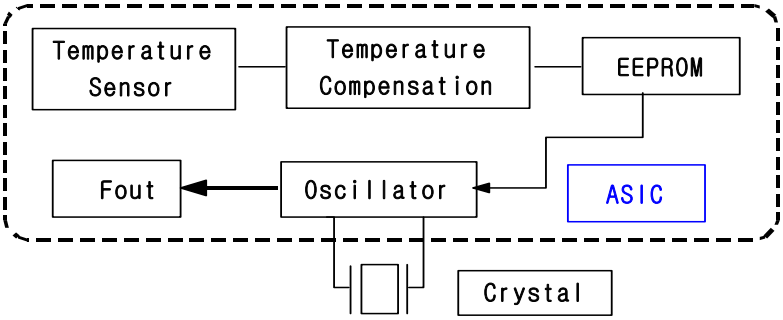


■ BLOCK DIAGRAM

● **Discrete type (7x5, 5x3.2)**



● **1 chip IC type (5x3.2, 4x2.5, 3.2x2.5)**



■ NOTICE

● Caution to handle / Storage

1. Storage
   Keep products at the room temperature (20±15℃), normal humidity (below 60% RH), recommend to use products within 6months after manufacturing, and in case of opening the product box, recommend to use products within 24 hours.

2. Static Electricity
   While handling, prevent to occur static electricity, and while moving, move products under doing - no static electricity.

3. Reflow
   Recommend to soldering according to recommended reflow condition.

4. Be cautious of products pin connection

Measurement condition

Ambient temperature:	23	°C
Input power level:	0	dBm
Terminating impedance:		
Input:	50	Ω
Output:	50	Ω

Characteristics

Remark:
The maximum attenuation in the pass band is defined as the insertion loss a_e. The nominal frequency f_N is fixed at 781,5 MHz without any tolerance or limit. The values of absolute attenuation a_{abs} are guaranteed for the whole operating temperature range. The frequency shift of the filter in the operating temperature range is included in the production tolerance scheme.

D a t a		**typ. value**		**tolerance / limit**		
Insertion loss (reference level)	a_e	1,6	dB	max.	3,0	dB
Nominal frequency	f_N	-			781,5	MHz
Passband	PB	-		f_N ±	5,5	MHz
Pass band ripple p-p		0,5	dB	max.	1,5	dB
Relative attenuation	a_{rel}					
734 MHz ... 757 MHz		37	dB	min.	25	dB
851 MHz ... 894 MHz		35	dB	min.	20	dB
Return loss within PB		16	dB	min.	10	dB
Input power level		-		max.	15**	dBm
Operating temperature range	OTR	-		- 25 °C ... + 85 °C		
Storage temperature range		-		- 40 °C ... + 85 °C		
Temperature coefficient of frequency	TC_f *	-39	ppm/K		-	

*) $\Delta f_C(Hz) = Tc_f(ppm/K) \times (T - T_o) \times f_{CAT}(MHz)$.
**) 25dBm short term in frequency range 734MHz…757MHz

Generated:

Checked / Approved:

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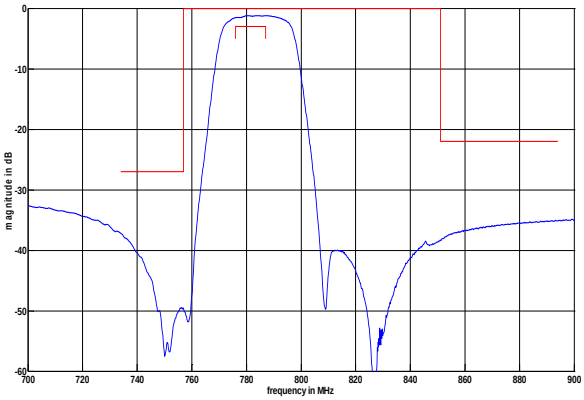
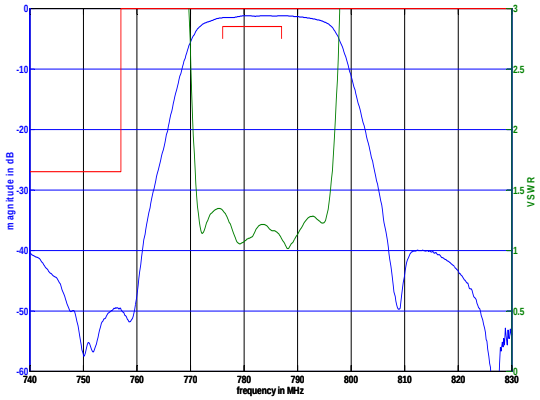
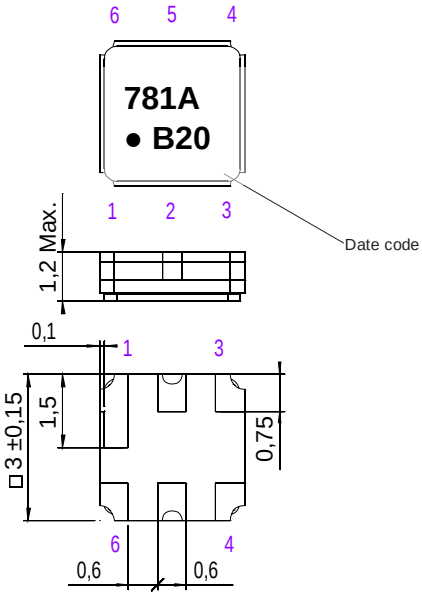
Filter characteristic





Construction and pin connection

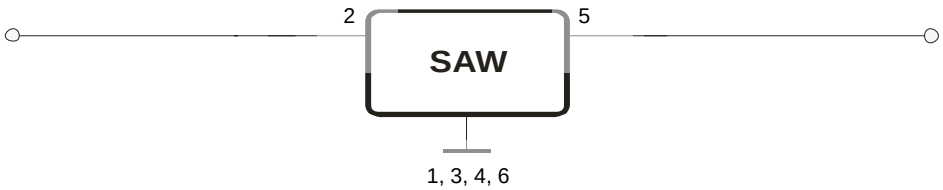
(All dimensions in mm)



1	Ground
2	Input
3	Ground
4	Ground
5	Output
6	Ground

Date code:	Year + week
B	2011
C	2012
D	2013
...	

50 Ω Test circuit



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Stability characteristics, reliability

After the following tests the filter shall meet the whole specification:

1. Shock:	500g, 1 ms, half sine wave, 3 shocks each plane; DIN IEC 68 T2 - 27
2. Vibration:	10 Hz to 500 Hz, 0,35 mm or g respectively, 1 octave per min, 10 cycles per plan, 3 plans; DIN IEC 68 T2 - 6
3. Change of temperature:	-55 °C to 125°C / 30 min. each / 10 cycles DIN IEC 68 part 2 – 14 Test N
4. Resistance to solder heat (reflow):	reflow possible: three times max.; for temperature conditions refer to the attached "Air reflow temperature conditions" on page 4;
5. ESD	ANSI/ESD S20.20-1999**,** class 1A for HBM

This filter is RoHS compliant (2002/95/EG, 2005/618/EG)

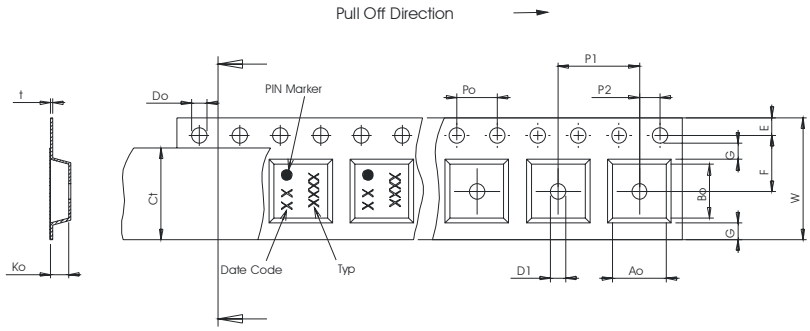
Packing

Tape & Reel: IEC 286 – 3, with exception of value for N and minimum bending radius;
tape type II, embossed carrier tape with top cover tape on the upper side;

max. pieces of filters per reel:	3000
reel of empty components at start:	min. 300 mm
reel of empty components at start including leader:	min. 500 mm
trailer:	min. 300 mm

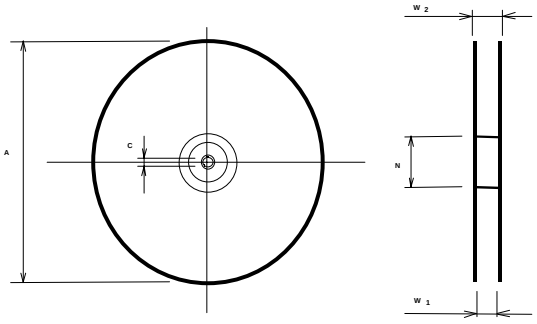
Tape (all dimensions in mm)

W	:	8,00 ± 0,3
Po	:	4,00 ± 0,1
Do	:	1,50 +0,1/-0
E	:	1,75 ± 0,1
F	:	3,50 ± 0,05
G(min)	:	0,75
P2	:	2,00 ± 0,05
P1	:	4,00 ± 0,1
D1(min)	:	1,50
Ao	:	3,25 ± 0,1
Bo	:	3,25 ± 0,1
Ct	:	5,3 ± 0,1



Reel (all dimensions in mm)

A	:	180
W1	:	8,4 +1,5/-0
W2(max)	:	14,4
N(min)	:	60
C	:	13,0 ± 0,2



The minimum bending radius is 45 mm.

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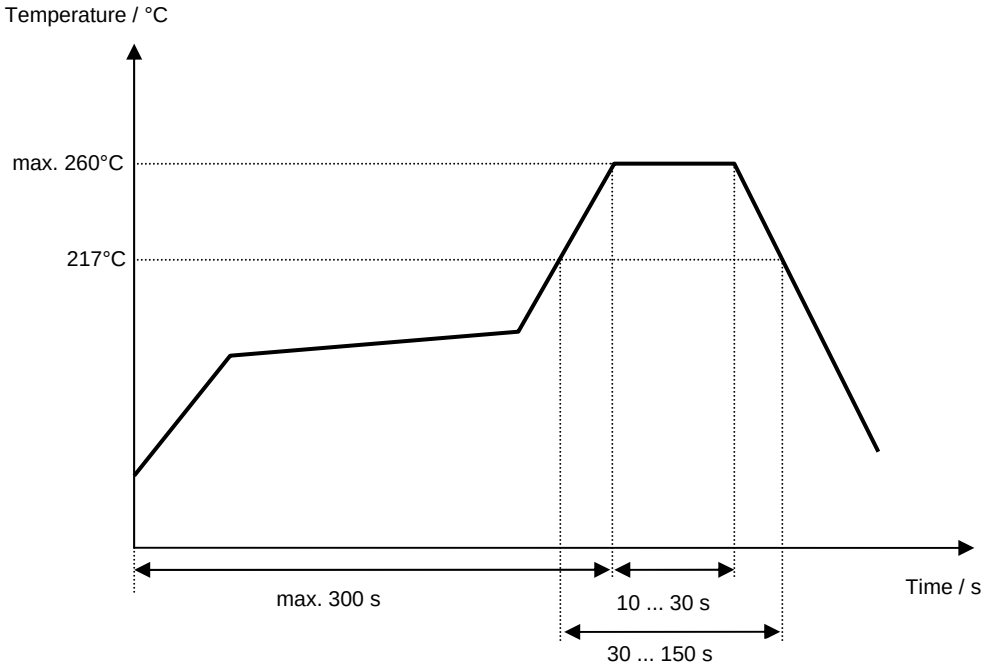
Air reflow temperature conditions

Conditions	**Exposure**
Average ramp-up rate (30°C to 217°C)	less than 3°C/second
> 100°C	between 300 and 600 seconds
> 150°C	between 240 and 500 seconds
> 217°C	between 30 and 150 seconds
Peak temperature	max. 260°C
Time within 5°C of actual peak temperature	between 10 and 30 seconds
Cool-down rate (Peak to 50°C)	less than 6°C/second
Time from 30°C to Peak temperature	no greater than 300 seconds

Chip-mount air reflow profile



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History

Version	Reason of Changes	Name	Date
1.0	- Generation of development specification	Strehl	04.08.2008
1.1	- Change construction	Strehl	12.08.2008
1.2	- add of typical values and filter characteristics	Pfeiffer	27.04.2009
2.0	- Adding additional stop band criteria @734MHz…757MHz - Adding short term input power level of 25dBm - Change of tape and reel orientation	S.Springfeldt	10.05.2011

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TEXAS INSTRUMENTS

TPS5430, TPS5431

SLVS632G – JANUARY 2006 – REVISED FEBRUARY 2015

TPS543x 3-A, Wide Input Range, Step-Down Converter

1 Features

- Wide Input Voltage Range:
  - TPS5430: 5.5 V to 36 V
  - TPS5431: 5.5 V to 23 V
- Up to 3-A Continuous (4-A Peak) Output Current
- High Efficiency up to 95% Enabled by 110-mΩ Integrated MOSFET Switch
- Wide Output Voltage Range: Adjustable Down to 1.22 V with 1.5% Initial Accuracy
- Internal Compensation Minimizes External Parts Count
- Fixed 500 kHz Switching Frequency for Small Filter Size
- Improved Line Regulation and Transient Response by Input Voltage Feed Forward
- System Protected by Overcurrent Limiting, Overvoltage Protection and Thermal Shutdown
- –40°C to 125°C Operating Junction Temperature Range
- Available in Small Thermally Enhanced 8-Pin SO PowerPAD™ Package

2 Applications

- Consumer: Set-top Box, DVD, LCD Displays
- Industrial and Car Audio Power Supplies
- Battery Chargers, High Power LED Supply
- 12-V/24-V Distributed Power Systems

3 Description

The TPS543x is a high-output-current PWM converter that integrates a low-resistance, high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V; an internally set slow-start circuit to limit inrush currents; and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 µA typically. Other features include an active-high enable, overcurrent limiting, over-voltage protection and thermal shutdown. To reduce design complexity and external component count, the TPS543x feedback loop is internally compensated. The TPS5431 is intended to operate from power rails up to 23 V. The TPS5430 regulates a wide variety of power sources including 24 V bus.

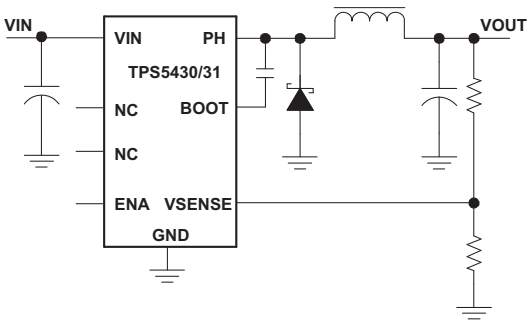
The TPS543x device is available in a thermally enhanced, easy to use 8-pin SOIC PowerPAD™ package. TI provides evaluation modules and the Designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

Device Information(1)

PART NUMBER	PACKAGE	INPUT VOLTAGE
TPS5430	HSOP (8)	5.5 V to 36 V
TPS5431		5.5 V to 23 V

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency vs Output Current

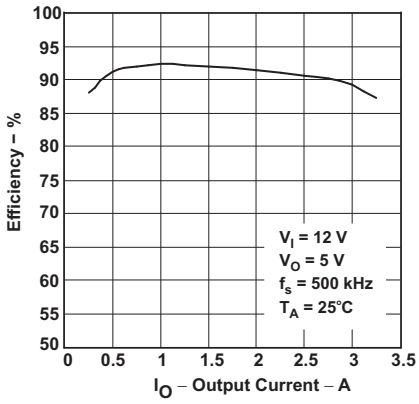


Table of Contents

4 Revision History

Changes from Revision F (December 2014) to Revision G — **Page**

- Fixed typo error TPS5430x to TPS513x ... 1

Changes from Revision E (September 2013) to Revision F — **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 3

Changes from Revision D (January 2013) to Revision E — **Page**

- Deleted SWIFT from the data sheet Title, Features, and Description ... 1

Changes from Revision C (November 2006) to Revision D — **Page**

- Replaced the DISSIPATION RATINGS with the THERMAL INFORMATION table ... 4

Changes from Revision B (August 2006) to Revision C — **Page**

- Changed the Efficiency vs Output Current graph ... 1
- Changed the FUNCTIONAL BLOCK DIAGRAM ... 9
- Added the Circuit Using Ceramic Output Filter Capacitors section ... 23

Changes from Revision A (March 2006) to Revision B — **Page**

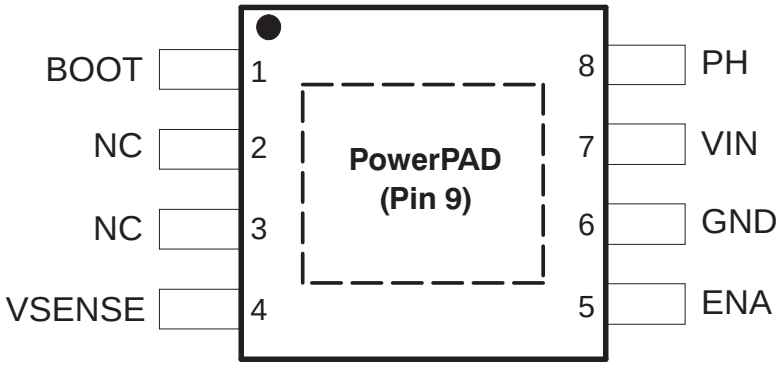
- Added Note 3 to the ABSOLUTE MAXIMUM RATINGS table ... 3

Changes from Original (January 2006) to Revision A **Page**

- Added Added device number TPS5431 1
- Changed Figure 17 21
- Added Figure 18 22

5 Pin Configuration and Functions

DDA PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	Boost capacitor for the high-side FET gate driver. Connect 0.01 µF low ESR capacitor from BOOT pin to PH pin.
NC	2, 3	—	Not connected internally.
VSENSE	4	I	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	I	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	—	Ground. Connect to PowerPAD.
VIN	7	—	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality, low ESR ceramic capacitor.
PH	8	I	Source of the high side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	—	GND pin must be connected to the exposed pad for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

				MIN	MAX	UNIT
V_I	Input voltage range	TPS5430	VIN	–0.3	40(3)	V
			PH (steady-state)	–0.6	40(3)	
		TPS5431	VIN	–0.3	25	
			PH (steady-state)	–0.6	25	
			ENA	–0.3	7	
			BOOT-PH	–0.3	10	
			VSENSE	–0.3	3	
			PH (transient < 10 ns)	–1.2		
I_O	Source current		PH		Internally Limited	
I_{lkg}	Leakage current		PH		10	µA
T_J	Operating virtual junction temperature range			–40	150	°C
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
VIN	Input voltage range	TPS5430	5.5	36	V
		TPS5431	5.5	23	
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)(2)(3)		TPS5430 TPS5431	UNIT
		DDA	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2-layer custom board) (4)	33	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (4-layer custom board) (5)	26	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	42.3	
ψ_{JT}	Junction-to-top characterization parameter	4.9	
ψ_{JB}	Junction-to-board characterization parameter	20.7	
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.4	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	0.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	20.8	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Maximum power dissipation may be limited by overcurrent protection
(3) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See *Thermal Calculations* in applications section of this data sheet for more information.
(4) Test boards conditions:
  (a) 3 in x 3 in, 2 layers, thickness: 0.062 inch.
  (b) 2 oz. copper traces located on the top and bottom of the PCB.
  (c) 6 thermal vias in the PowerPAD area under the device package.
(5) Test board conditions:
  (a) 3 in x 3 in, 4 layers, thickness: 0.062 inch.
  (b) 2 oz. copper traces located on the top and bottom of the PCB.
  (c) 2 oz. copper ground planes on the 2 internal layers.
  (d) 6 thermal vias in the PowerPAD area under the device package.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, VIN = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	µA
UNDERVOLTAGE LOCK OUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 3 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87%	89%		
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		6.6	8	10	ms
CURRENT LIMIT						
	Current limit		4	5	6	A
	Current limit hiccup time		13	16	20	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

6.6 Typical Characteristics

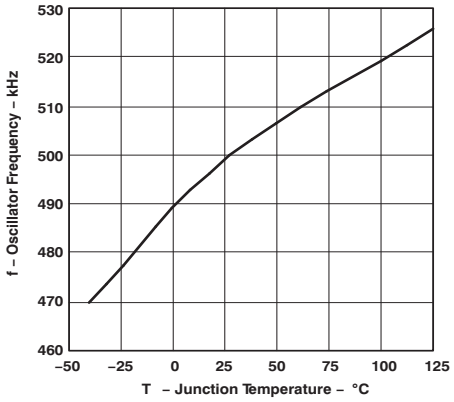


Figure 1. Oscillator Frequency vs. Junction Temperature

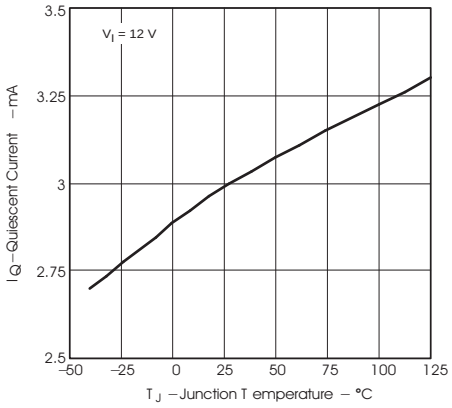


Figure 2. Non-Switching Quiescent Current vs. Junction Temperature

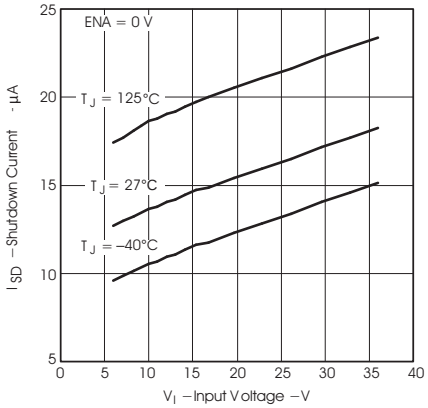


Figure 3. Shutdown Quiescent Current vs. Input Voltage

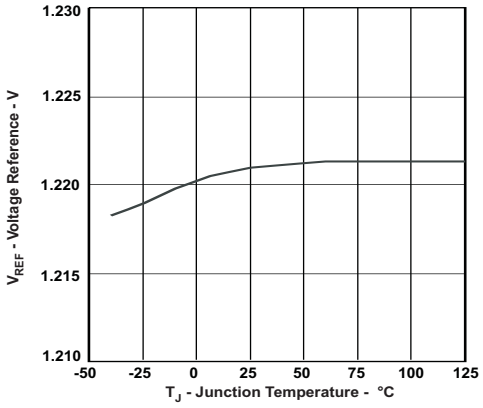


Figure 4. Voltage Reference vs. Junction Temperature

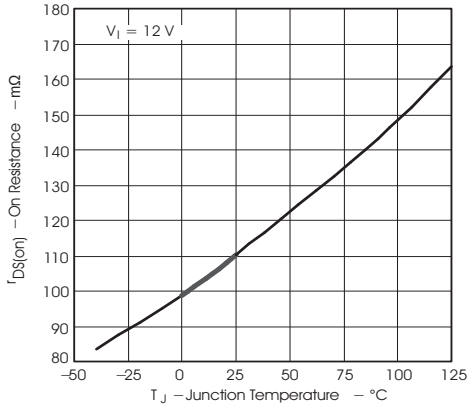


Figure 5. On Resistance vs. Junction Temperature

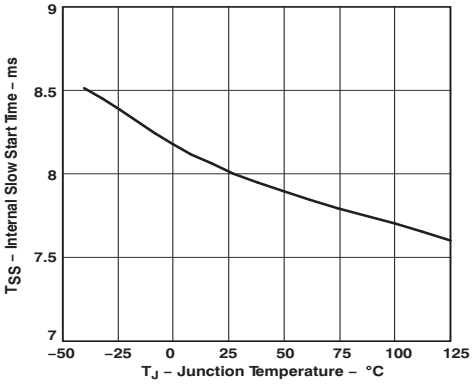


Figure 6. Internal Slow Start Time vs. Junction Temperature

Typical Characteristics (continued)

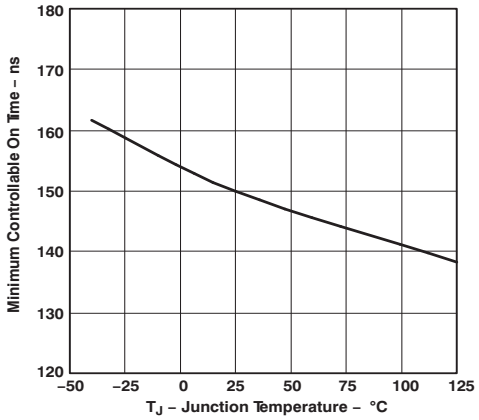


Figure 7. Minimum Controllable On Time vs. Junction Temperature

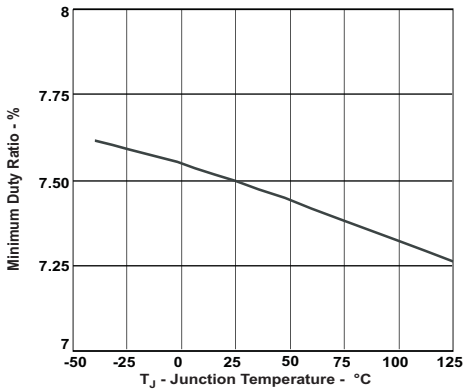


Figure 8. Minimum Controllable Duty Ratio vs. Junction Temperature

7 Detailed Description

7.1 Overview

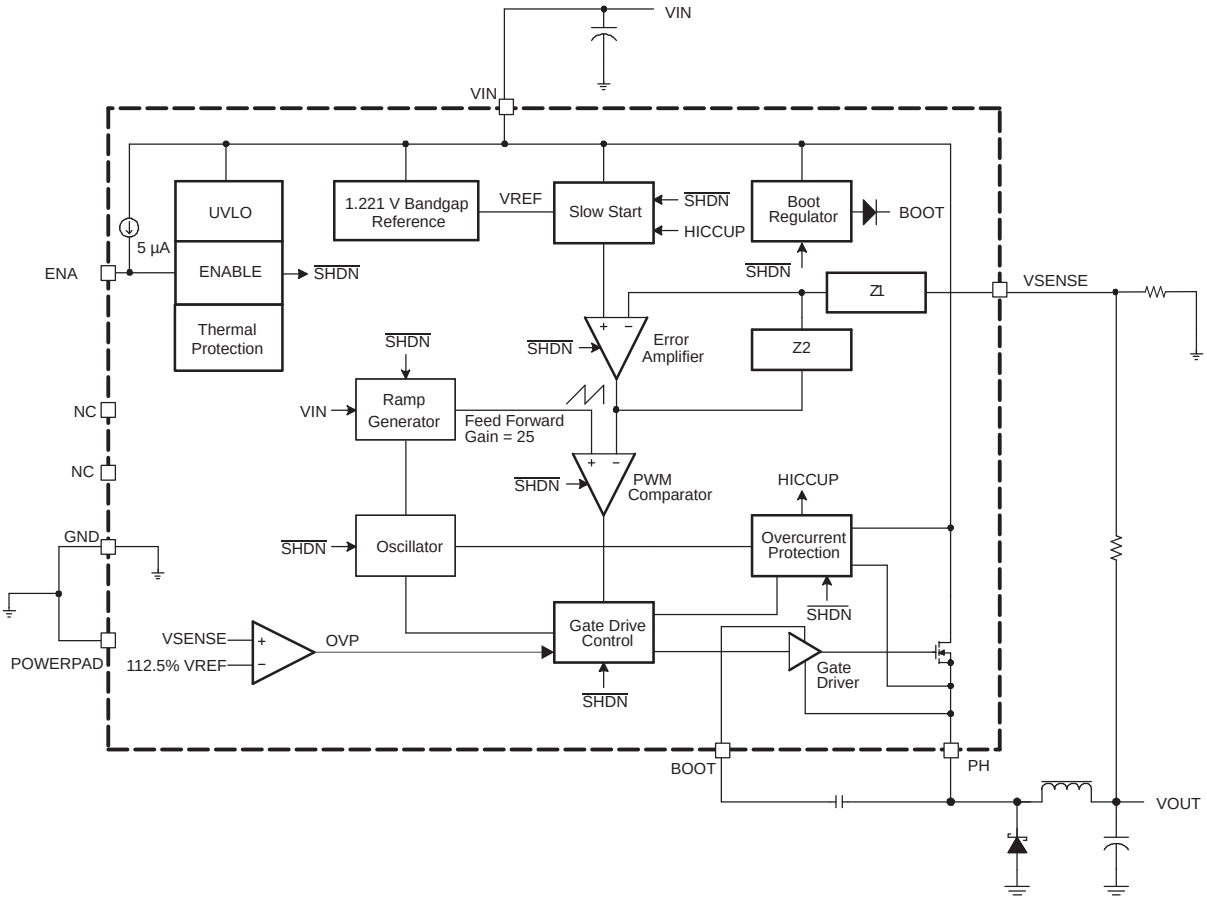
The TPS543x is a 3-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The TPS5431 is intended to operate from power rails up to 23 V and the TPS5430 up to 36 V. These devices implement constant-frequency voltage-mode control with voltage feed forward for improved line regulation and line transient response. Internal compensation reduces design complexity and external component count.

The integrated 110-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 3-A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to PH pins. The TPS543x reduces the external component count by integrating the bootstrap recharge diode.

The TPS543x has a default input start-up voltage of 5.3 V typical. The ENA pin can be used to disable the TPS543x reducing the supply current to 18 µA. An internal pullup current source enables operation when the ENA pin is floating. The TPS543x includes an internal slow-start circuit that slows the output rise time during start up to reduce in rush current and output voltage overshoot. The minimum output voltage is the internal 1.221-V feedback reference. Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 112.5% of the desired output voltage.

Internal cycle-by-cycle overcurrent protection limits the peak current in the integrated high-side MOSFET. For continuous overcurrent fault conditions the TPS543x will enter hiccup mode overcurrent limiting. Thermal protection protects the device from overheating.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500 kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

7.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

7.3.3 Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V will disable the regulator and activate the shutdown mode. The quiescent current of the TPS543x in shutdown mode is typically 18 µA.

The ENA pin has an internal pull-up current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow start time is 8 ms typically.

7.3.4 Undervoltage Lockout (UVLO)

The TPS543x incorporate an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

7.3.5 Boost Capacitor (BOOT)

Connect a 0.01 µF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

7.3.6 Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

The TPS543x implements internal compensation to simplify the regulator design. Since the TPS543x uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* in the applications section for more details.

7.3.7 Voltage Feed-Forward

The internal voltage feed-forward provides a constant dc power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain, i.e.

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk}-\text{pk}}} \quad (1)$$

The typical feed forward gain of TPS543x is 25.

Feature Description (continued)

7.3.8 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

7.3.9 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, i.e. hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

7.3.10 Overvoltage Protection

The TPS543x has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% x VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

7.3.11 Thermal Shutdown

The TPS543x protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

7.4 Device Functional Modes

7.4.1 Operation near Minimum Input Voltage

The TPS543x is recommended to operate with input voltages above 5.5 V. The typical VIN UVLO threshold is 5.3 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage the device will not switch. If EN is floating or externally pulled up to greater up than 1.3 V, when $V_{(VIN)}$ passes the UVLO threshold the TPS543x will become active. Switching is enabled and the slow-start sequence is initiated. The TPS543x starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

7.4.2 Operation with ENA control

The enable start threshold voltage is 1.3 V max. With ENA held below the 0.5 V minimum stop threshold voltage the TPS543x is disabled and switching is inhibited even if VIN is above its UVLO threshold. The quiescent current is reduced in this state. If the ENA voltage is increased above the max start threshold while $V_{(VIN)}$ is above the UVLO threshold, the device becomes active. Switching is enabled and the slow-start sequence is initiated. The TPS543x starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS543x is a 3-A, step down regulator with an integrated high side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. Example applications are: High Density Point-of-Load Regulators for Set-top Box, DVD, LCD and Plasma Displays, High Power LED Supply, Car Audio, Battery Chargers, and other 12-V and 24-V Distributed Power Systems. Use the following design procedure to select component values for the TPS543x. This procedure illustrates the design of a high frequency switching regulator. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

8.2 Typical Applications

8.2.1 12-V Input to 5.0-V Output

Figure 9 shows the schematic for a typical TPS5430 application. The TPS5430 can provide up to 3 A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD™ underneath the device must be soldered down to the printed-circuit board.

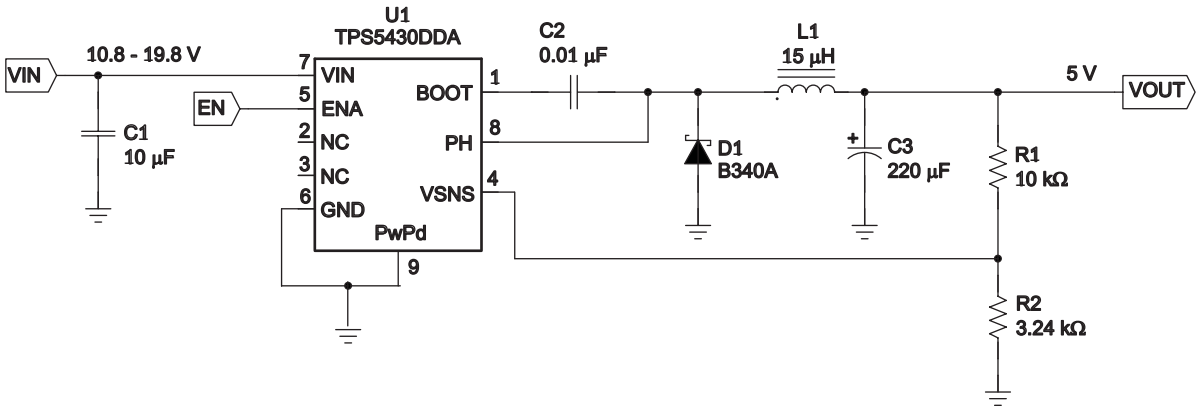


Figure 9. Application Circuit, 12 V Input to 5.0 V Output

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters:

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	10.8 V to 19.8 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

8.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS5430. This section presents a simplified discussion of the design process.

8.2.1.2.1 Switching Frequency

The switching frequency for the TPS5430 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.1.2.2 Input Capacitors

The TPS5430 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The recommended value for the decoupling capacitor, C1, is 10 µF. A high quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by Equation 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{IN} is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 3 :

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this case the input ripple voltage would be 156 mV and the RMS ripple current would be 1.5 A. The maximum voltage across the input capacitors would be V_{IN} max plus delta $V_{IN}/2$. The chosen input decoupling capacitor is rated for 25 V and the ripple current capacity is greater than 3 A, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5430 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.1.2.3 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Since the TPS5430 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.1.2.3.1 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 4:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5430, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point and relatively low load currents can be sourced before discontinuous operation.

For this design example use K_{IND} = 0.2 and the minimum inductor value is calculated to be 12.5 µH. The next highest standard value is 15 µH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 5:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (5)$$

and the peak inductor current can be determined with Equation 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (6)$$

For this design, the RMS inductor current is 3.003 A, and the peak inductor current is 3.31 A. The chosen inductor is a Sumida CDRH104R-150 15 µH. It has a saturation current rating of 3.4 A and a RMS current rating of 3.6 A, easily meeting these requirements. A lesser rated inductor could be used, however this device was chosen because of its low profile component height. In general, inductor values for use with the TPS5430 are in the range of 10 µH to 100 µH.

8.2.1.2.3.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed loop crossover frequency will be between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^{2}}{85\ V_{OUT}} \tag{7}$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \tag{8}$$

For a desired crossover of 18 kHz and a 15 µH inductor, the calculated value for the output capacitor is 220 µF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \tag{9}$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}\ (MAX) = \frac{ESR_{MAX}\ x\ V_{OUT}\ x\ \left(V_{IN(MAX)}\ -\ V_{OUT}\right)}{N_C\ x\ V_{IN(MAX)}\ x\ L_{OUT}\ x\ F_{SW}} \tag{10}$$

Where:

- ΔV_{PP} is the desired peak-to-peak output ripple.
- N_C is the number of parallel output capacitors.
- F_{SW} is the switching frequency.

For this design example, a single 220 µF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB220M, rated at 10 V with a maximum ESR of 40 mΩ and a ripple current rating of 3 A. An additional small 0.1 µF ceramic bypass capacitor may also used, but is not included in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \tag{11}$$

Where:

- N_C is the number of output capacitors in parallel.
- F_{SW} is the switching frequency.

Other capacitor types can be used with the TPS5430, depending on the needs of the application.

8.2.1.2.4 Output Voltage Set-Point

The output voltage of the TPS5430 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using Equation 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \tag{12}$$

For any TPS5430 design, start with an R1 value of 10 kΩ. R2 is then 3.24 kΩ.

8.2.1.2.5 BOOT Capacitor

The BOOT capacitor should be 0.01 µF.

8.2.1.2.6 Catch Diode

The TPS5430 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is $V_{IN(MAX)}$ + 0.5 V. Peak current must be greater than $I_{OUT(MAX)}$ plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

8.2.1.2.7 Advanced Information

8.2.1.2.7.1 Output Voltage Limitations

Due to the internal design of the TPS543x, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D \tag{13}$$

Where

V_{INMIN} = minimum input voltage
I_{OMAX} = maximum load current
V_D = catch diode forward voltage.
R_L= output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D \tag{14}$$

Where

V_{INMAX} = maximum input voltage
I_{OMIN} = minimum load current
V_D = catch diode forward voltage.
R_L= output inductor series resistance.

This equation assumes nominal on resistance for the high side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

8.2.1.2.7.2 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS543x. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS543x. Equation 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \quad (15)$$

Where

fp0 = 2165 Hz, fz1 = 2170 Hz, fz2 = 2590 Hz

fp1 = 24 kHz, fp2 = 54 kHz, fp3 = 440 kHz

fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

8.2.1.2.7.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: Pcon = I_{OUT}^{2} x Rds(on) x V_{OUT}/V_{IN}

Switching Loss: Psw = V_{IN} x I_{OUT} x 0.01

Quiescent Current Loss: Pq = V_{IN} x 0.01

Total Loss: Ptot = Pcon + Psw + Pq

Given T_A => Estimated Junction Temperature: $T_J = T_A$ + Rth x Ptot

Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX}$ – Rth x Ptot

8.2.1.3 Application Curves

The performance graphs (Figure 10 through Figure 16) are applicable to the circuit in Figure 9. T_a= 25 °C. unless otherwise specified.

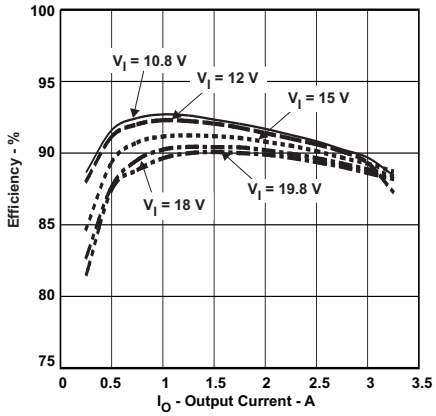


Figure 10. Efficiency vs. Output Current

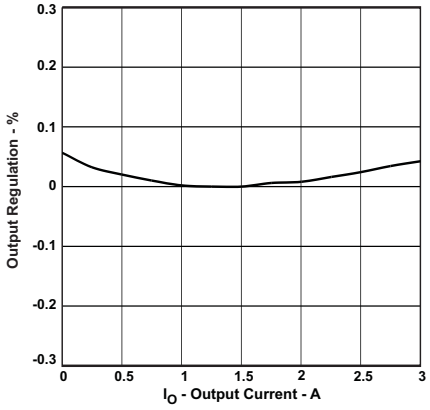


Figure 11. Output Regulation % vs. Output Current

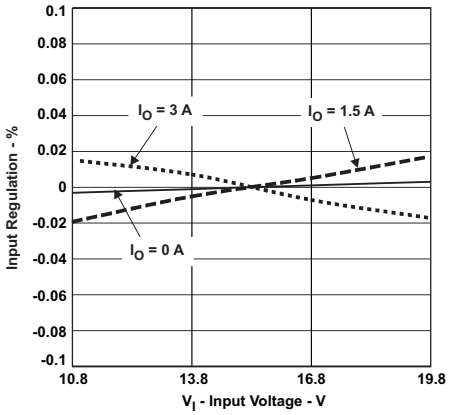


Figure 12. Input Regulation % vs. Input Voltage

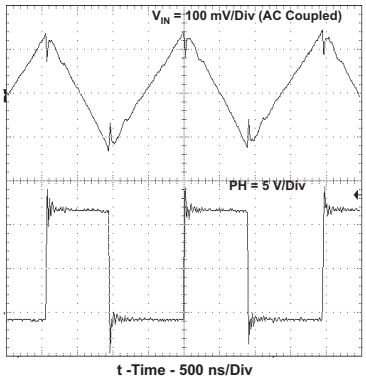


Figure 13. Input Voltage Ripple and PH Node, I_O = 3 A.

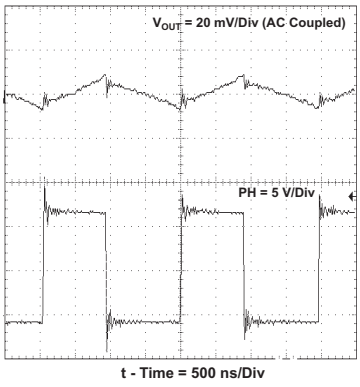


Figure 14. Output Voltage Ripple and PH Node, I_O = 3 A

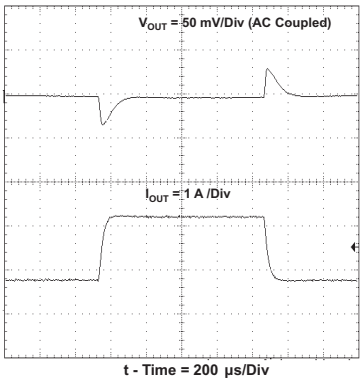


Figure 15. Transient Response, I_O Step 0.75 to 2.25 A.

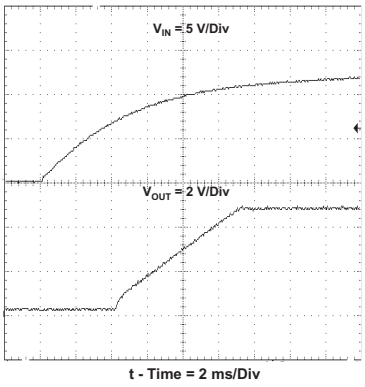


Figure 16. Startup Waveform, V_{IN} and V_{OUT}.

8.2.2 Wide Input Voltage Ranges with TPS5430

Figure 17 shows an application circuit using the wide input voltage range of the TPS5430.

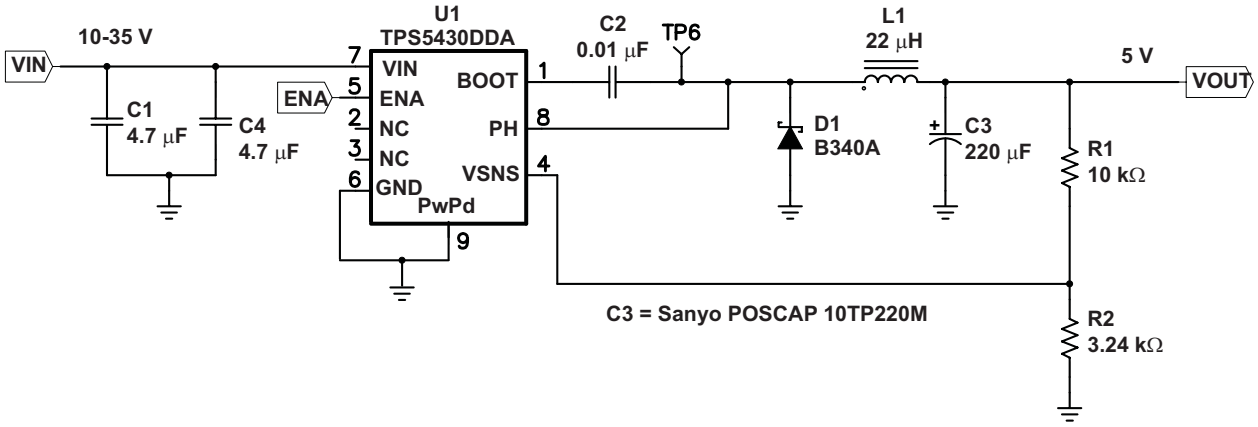


Figure 17. 10 V– 35 V Input to 5 V Output Application Circuit

8.2.2.1 Design Requirements

For this design example, use the following as the input parameters. This circuit is also designed with a larger value output inductor and a lower closed loop crossover frequency.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 35 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	500 kHz

8.2.2.2 Detailed Design Procedure

The design procedure is similar to what is given for the design example in Detailed Design Procedure.

8.2.2.3 Wide Input Voltage Ranges with TPS5431

Figure 18 shows an application circuit using the wide input voltage range of the TPS5431.

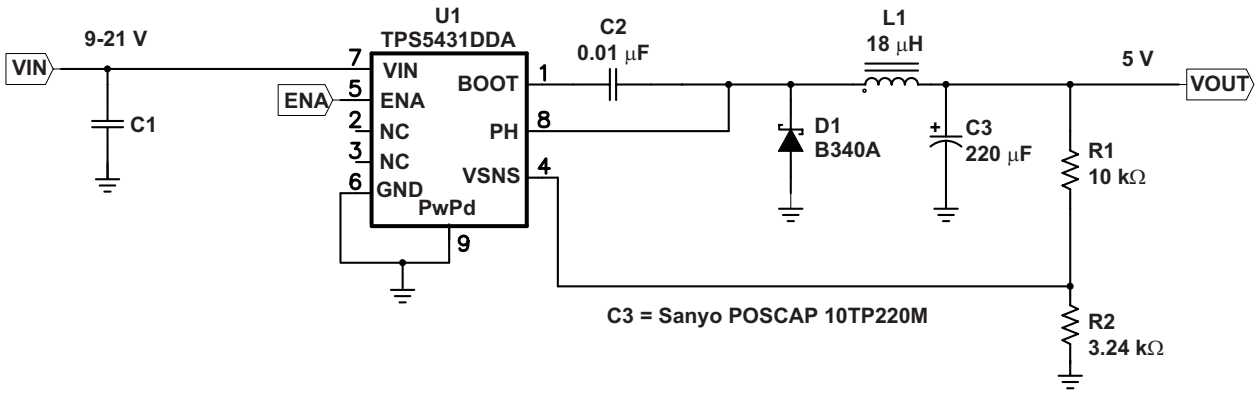


Figure 18. 9 V – 21 V Input to 5 V Output Application Circuit

8.2.2.3.1 Design Requirements

For this design example, use the following as the input parameters. This circuit is also designed with a larger value output inductor and a lower closed loop crossover frequency.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	9 V to 21 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	500 kHz

8.2.2.3.2 Detailed Design Procedure

The design procedure is similar to what is given for the design example in Detailed Design Procedure.

8.2.3 Circuit Using Ceramic Output Filter Capacitors

Figure 19 shows an application circuit using all ceramic capacitors for the input and output filters.

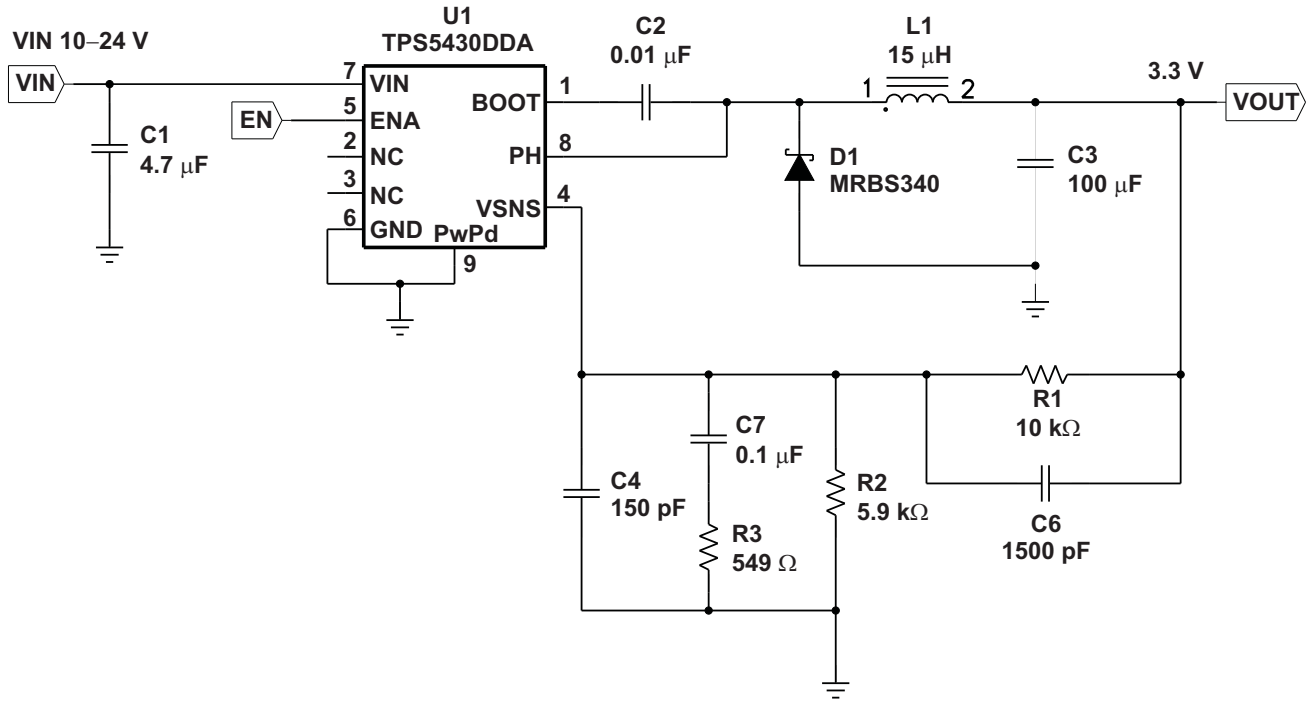


Figure 19. Ceramic Output Filter Capacitors Circuit

8.2.3.1 Design Requirements

For this design example, use the following as the input parameters. This circuit is also designed with a ceramic output filter capacitor.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 24 V
Output voltage	3.3 V
Input ripple voltage	300 mV
Output current rating	3 A
Operating frequency	500 kHz

8.2.3.2 Detailed Design Procedure

The design procedure is similar to what is given for the design example in Detailed Design Procedure, except for the selection of the output filter capacitor values and the design of the additional compensation components required to stabilize the circuit.

8.2.3.2.1 Output Filter Component Selection

Using Equation 11, the minimum inductor value is 12 µH. A value of 15 µH is chosen for this design.

When using ceramic output filer capacitors, the recommended LC resonant frequency should be no more than 7 kHz. Since the output inductor is already selected at 15 µH, this limits the minimum output capacitor value to:

$$C_O\,(MIN) \geq \frac{1}{(2\pi \times 7000)^2 \times L_O} \tag{16}$$

The minimum capacitor value is calculated to be 34 µF. For this circuit a larger value of capacitor yields better transient response. A single 100 µF output capacitor is used for C3. It is important to note that the actual capacitance of ceramic capacitors decreases with applied voltage. In this example, the output voltage is set to 3.3 V, minimizing this effect.

8.2.3.2.2 External Compensation Network

When using ceramic output capacitors, additional circuitry is required to stabilize the closed loop system. For this circuit, the external components are R3, C4, C6, and C7. To determine the value of these components, first calculate the LC resonant frequency of the output filter:

$$F_{LC} = \frac{1}{2\pi \sqrt{L_O \times C_O\,(EFF)}} \tag{17}$$

For this example the effective resonant frequency is calculated as 4109 Hz

The network composed of R1, R2, R3, C5, C6, and C7 has two poles and two zeros that are used to tailor the overall response of the feedback network to accommodate the use of the ceramic output capacitors. The pole and zero locations are given by the following equations:

$$Fp1 = 500000 \times \frac{V_O}{F_{LC}} \tag{18}$$

$$Fz1 = 0.7 \times F_{LC} \tag{19}$$

$$Fz2 = 2.5 \times F_{LC} \tag{20}$$

The final pole is located at a frequency too high to be of concern. The second zero, fz2 as defined by Equation 20 uses 2.5 for the frequency multiplier. In some cases this may need to be slightly higher or lower. Values in the range of 2.3 to 2.7 work well. The values for R1 and R2 are fixed by the 3.3 V output voltage as calculated using Equation 12. For this design R1 = 10 kΩ and R2 = 5.90 kΩ. With Fp1 = 401 Hz, Fz1 = 2876 Hz and Fz2 = 10.3 kHz, the values of R3, C6 and C7 are determined using Equation 21, Equation 22, and Equation 23:

$$C7 = \frac{1}{2\pi \times Fp1 \times (R1 \parallel R2)} \tag{21}$$

$$R3 = \frac{1}{2\pi \times Fz1 \times C7} \tag{22}$$

$$C6 = \frac{1}{2\pi \times Fz2 \times R1} \tag{23}$$

For this design, using the closest standard values, C7 is 0.1 µF, R3 is 549 Ω, and C6 is 1500 pF. C4 is added to improve load regulation performance. It is effectively in parallel with C6 in the location of the second pole frequency, so it should be small in relationship to C6. C4 should be less the 1/10 the value of C6. For this example, 150 pF works well.

For additional information on external compensation of the TPS5430, TPS5431 or other wide voltage range devices, see SLVA237 *Using TPS5410/20/30/31 With Aluminum/Ceramic Output Capacitors*

9 Power Supply Recommendations

The TPS5430 is designed to operate from an input voltage supply range between 5.5 V and 36 V. The TPS5431 is designed to operate from an input voltage supply range between 5.5 V and 23 V. This input supply should remain within the input voltage supply range. If the input supply is located more than a few inches from the TPS543x converter bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS543x ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7 µF ceramic with a X5R or X7R dielectric.

There should be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown below.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in Figure 20, use a via connection to a different layer to route to the ENA pin.

10.2 Layout Example

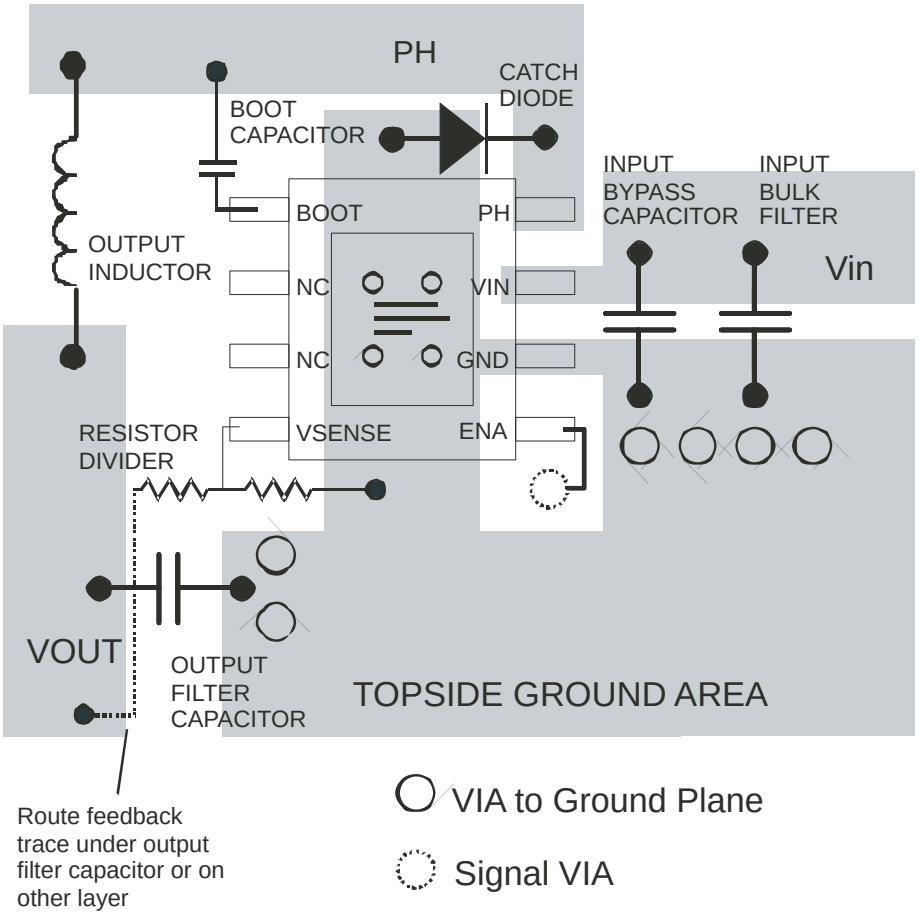
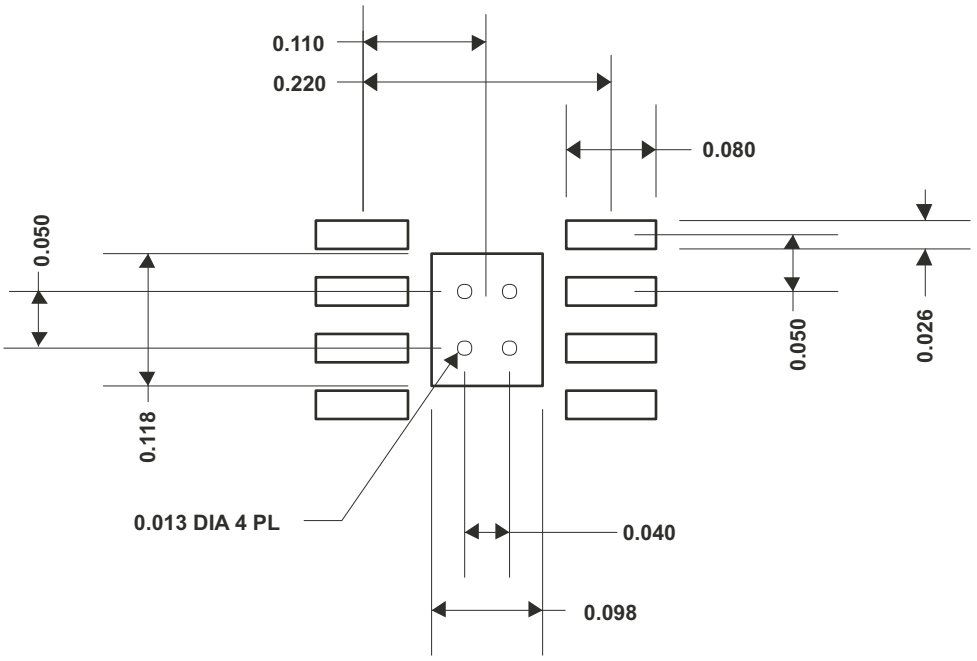


Figure 20. Design Layout

Layout Example (continued)



All dimensions in inches

Figure 21. Recommended Land Pattern

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	REFERENCE DESIGN
TPS5430	Click here	Click here	Click here	Click here	Click here	
TPS5431	Click here	Click here	Click here	Click here	Click here	

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

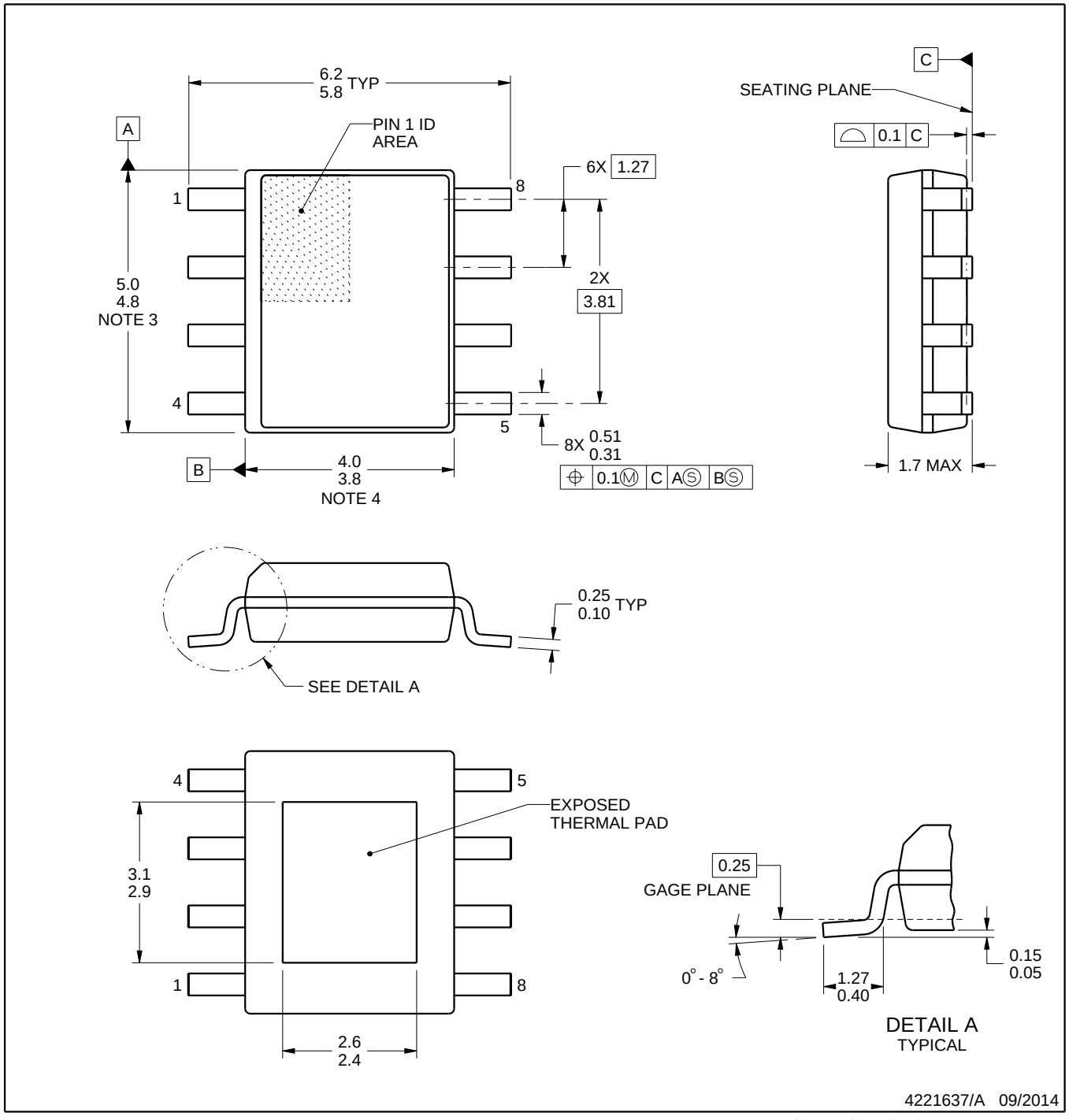
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DDA0008J

PowerPAD™ - 1.7 mm max height

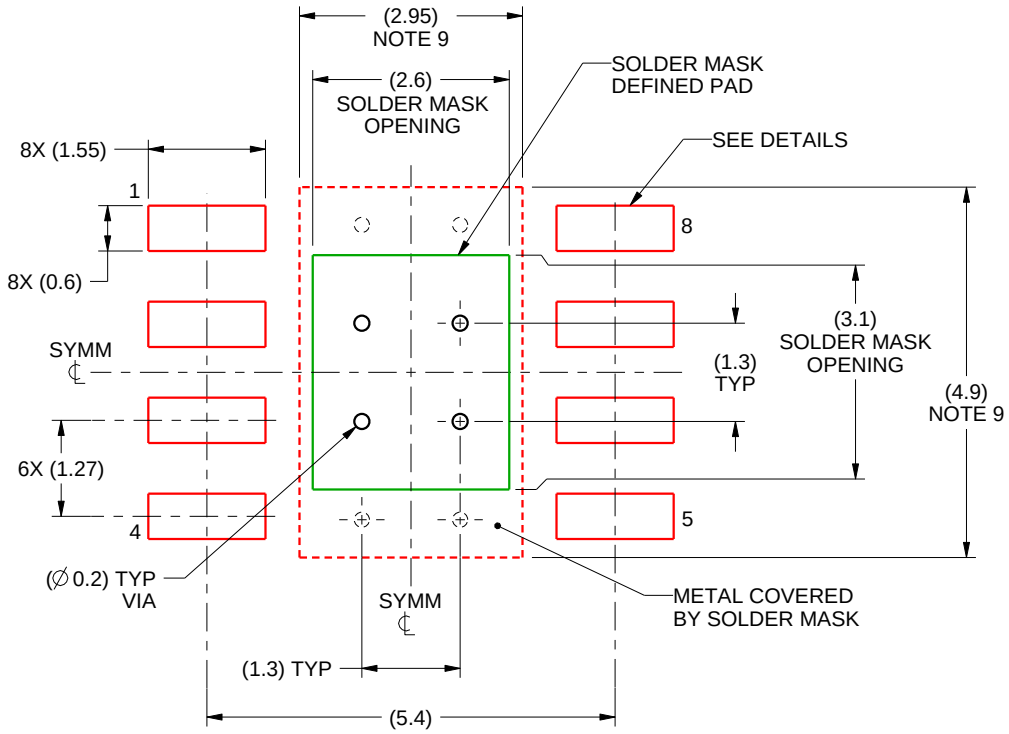
PLASTIC SMALL OUTLINE



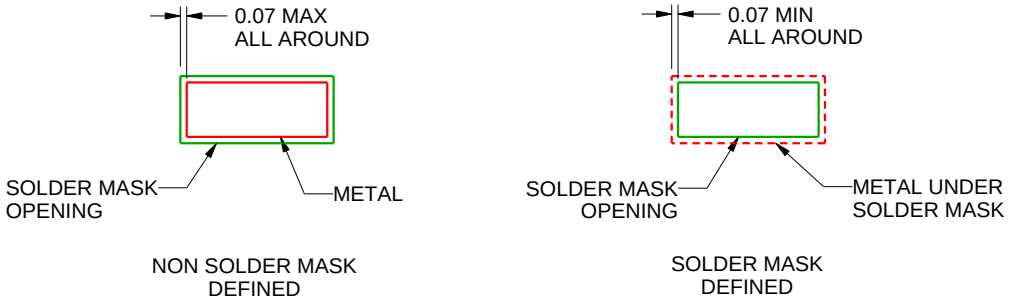
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

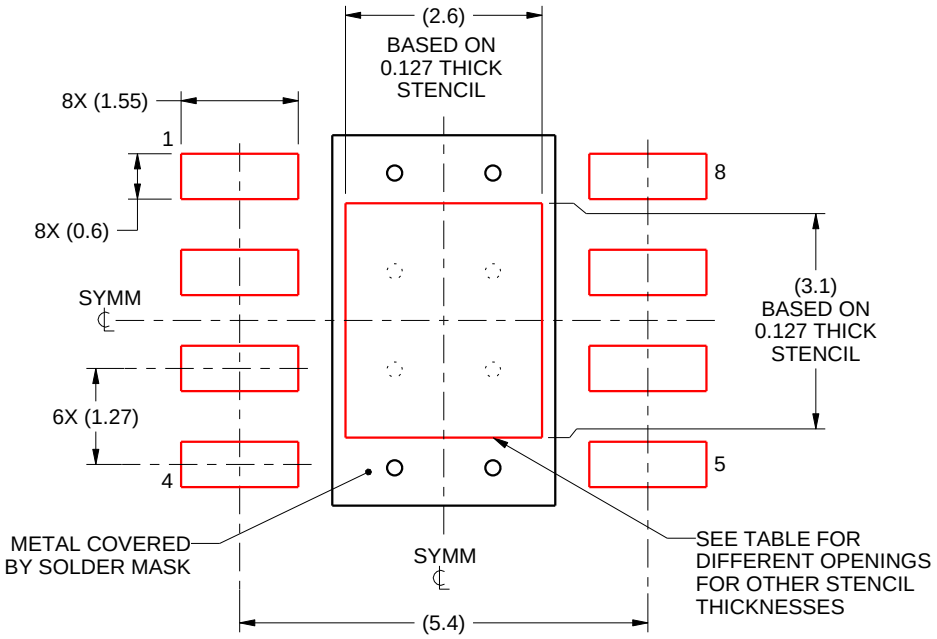


SOLDER MASK DETAILS

4221637/A 09/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.93 X 3.49
0.127	2.6 X 3.1 (SHOWN)
0.152	2.38 X 2.83
0.178	2.20 X 2.62

4221637/A 09/2014

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5430DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5430DDAG4	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5430DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5430DDARG4	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5431DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples
TPS5431DDAG4	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples
TPS5431DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples
TPS5431DDARG4	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

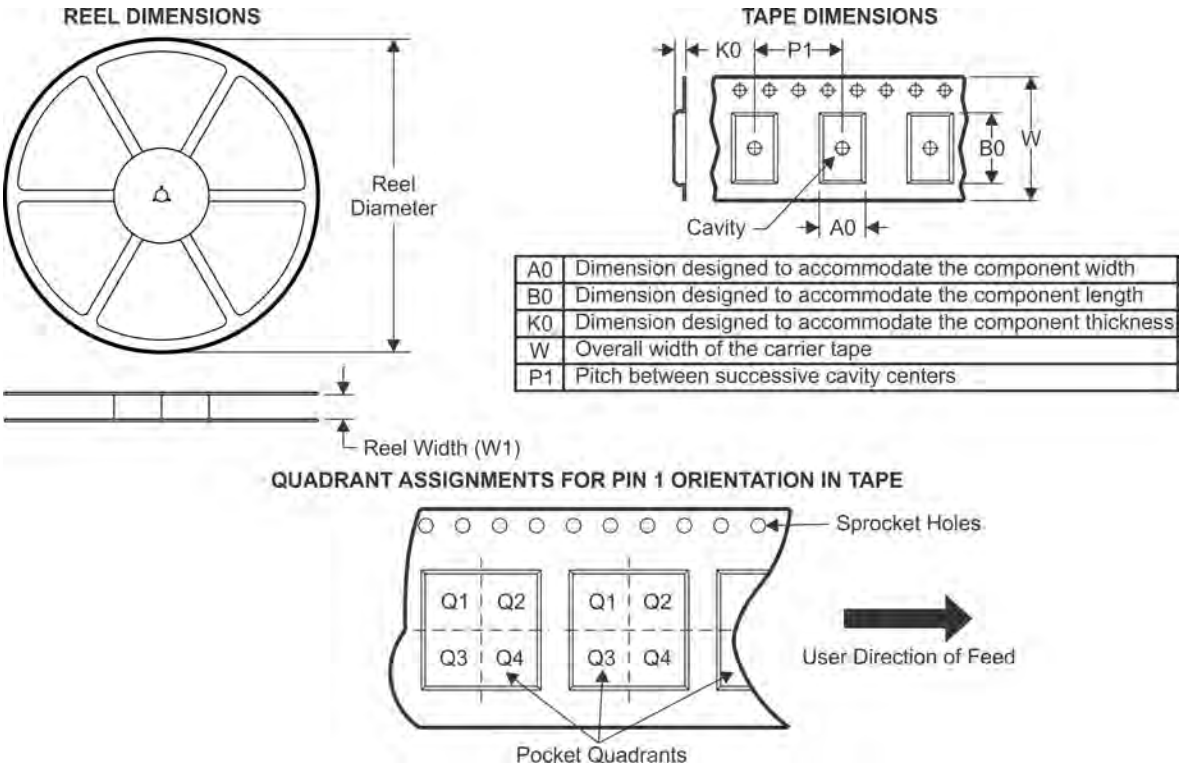
OTHER QUALIFIED VERSIONS OF TPS5430 :

- Automotive: TPS5430-Q1
- Enhanced Product: TPS5430-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

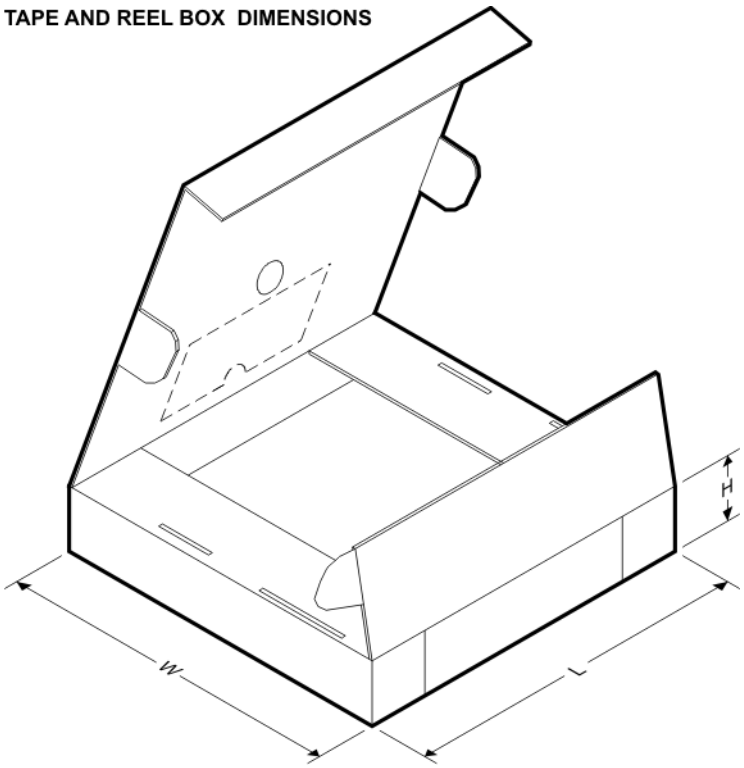


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5430DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS5431DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5430DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
TPS5431DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0

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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

CEL

GaAs INTEGRATED CIRCUIT

μPG2012TK

L-BAND SPDT SWITCH

DESCRIPTION

The μPG2012TK is a GaAs MMIC for L-band SPDT (Single Pole Double Throw) switch which were developed for mobile phone and another L-band application.

This device can operate frequency from 0.5 GHz to 2.5 GHz, having the low insertion loss and high isolation.

This device is housed in a 6-pin lead-less minimold package (1511). And this package is able to high-density surface mounting.

FEATURES

- Supply voltage : V_{DD} = 2.7 to 3.0 V (2.8 V TYP.)
- Switch control voltage : $V_{cont (H)}$ = 2.7 to 3.0 V (2.8 V TYP.)
  : $V_{cont (L)}$ = −0.2 to +0.2 V (0 V TYP.)
- Low insertion loss : L_{INS1} = 0.27 dB TYP. @ f = 0.5 to 1.0 GHz, V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V
  : L_{INS2} = 0.30 dB TYP. @ f = 2.0 GHz, V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V
  : L_{INS3} = 0.30 dB TYP. @ f = 2.5 GHz, V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V (Reference value)
- High isolation : ISL1 = 30 dB TYP. @ f = 0.5 to 2.0 GHz, V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V
  : ISL2 = 30 dB TYP. @ f = 2.5 GHz, V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V (Reference value)
- High-density surface mounting : 6-pin lead-less minimold package (1.5 × 1.1 × 0.55 mm)

APPLICATIONS

- L-band digital cellular or cordless telephone
- PCS, W-LAN, WLL and Bluetooth™ etc.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPG2012TK-E2	6-pin lead-less minimold (1511)	G3H	• Embossed tape 8 mm wide • Pin 1, 6 face the perforation side of the tape • Qty 5 kpcs/reel

Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: μPG2012TK-A

Caution: Observe precautions when handling because these devices are sensitive to electrostatic discharge

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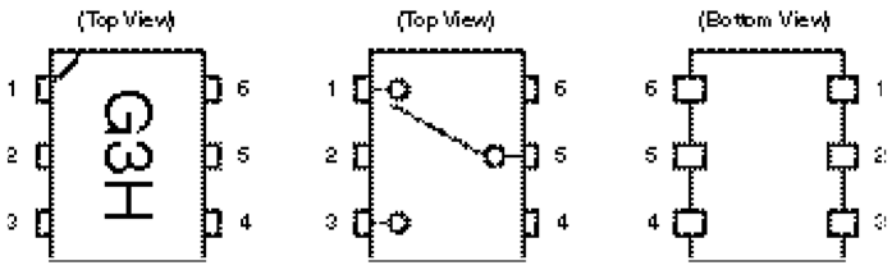
PIN CONNECTIONS AND INTERNAL BLOCK DIAGRAM



Pin No.	Pin Name
1	OUTPUT1
2	GND
3	OUTPUT2
4	V_{cont}
5	INPUT
6	V_{DD}

TRUTH TABLE

V_{cont}	INPUT–OUTPUT1	INPUT–OUTPUT2
Low	OFF	ON
High	ON	OFF

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	+6.0	V
Switch Control Voltage	V_{cont}	+6.0	V
Input Power	P_{in}	+26	dBm
Power Dissipation	P_D	150 Note	mW
Operating Ambient Temperature	T_A	–45 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Note Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB, T_A = +85°C

RECOMMENDED OPERATING RANGE (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}	2.7	2.8	3.0	V
Switch Control Voltage (H)	$V_{cont(H)}$	2.7	2.8	3.0	V
Switch Control Voltage (L)	$V_{cont(L)}$	–0.2	0	0.2	V

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V, DC cut capacitors = 56 pF, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Insertion Loss1	L_{INS1}	f = 0.5 to 1.0 GHz	–	0.27	0.50	dB
Insertion Loss2	L_{INS2}	f = 2.0 GHz	–	0.30	0.50	dB
Isolation1	ISL1	f = 0.5 to 2.0 GHz	24	30	–	dB
Input Return Loss	RL_{in}	f = 0.5 to 2.5 GHz	15	20	–	dB
Output Return Loss	RL_{out}	f = 0.5 to 2.5 GHz	15	20	–	dB
0.1 dB Gain Compression Input Power Note	$P_{in(0.1\ dB)}$	f = 2.0 GHz	+17.5	+20.5	–	dBm
Supply Current	I_{DD}		–	50	100	μA
Switching Control Current	I_{cont}		–	4	20	μA

Note $P_{in(0.1dB)}$ is measured the input power level when the insertion loss increases more 0.1 dB than that of linear range.

STANDARD CHARACTERISTICS FOR REFERENCE

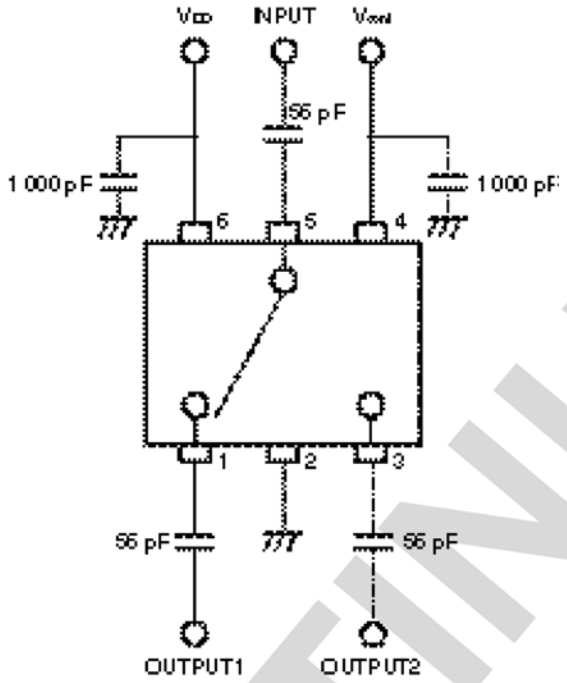
(T_A = +25°C, V_{DD} = 2.8 V,V_{cont} = 2.8 V/0 V, DC cut capacitors = 56 pF, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Insertion Loss3	L_{INS3}	f = 2.5 GHz	–	0.30	–	dB
Isolation2	ISL2	f = 2.5 GHz	–	30	–	dB
1 dB Gain Compression Input Power Note	$P_{in(1\ dB)}$	f = 2.0 GHz	–	+24.0	–	dBm
Switching Control Speed	tsw		–	300	–	ns

Note $P_{in(1dB)}$ is measured the input power level when the insertion loss increases more 1 dB than that of linear range.

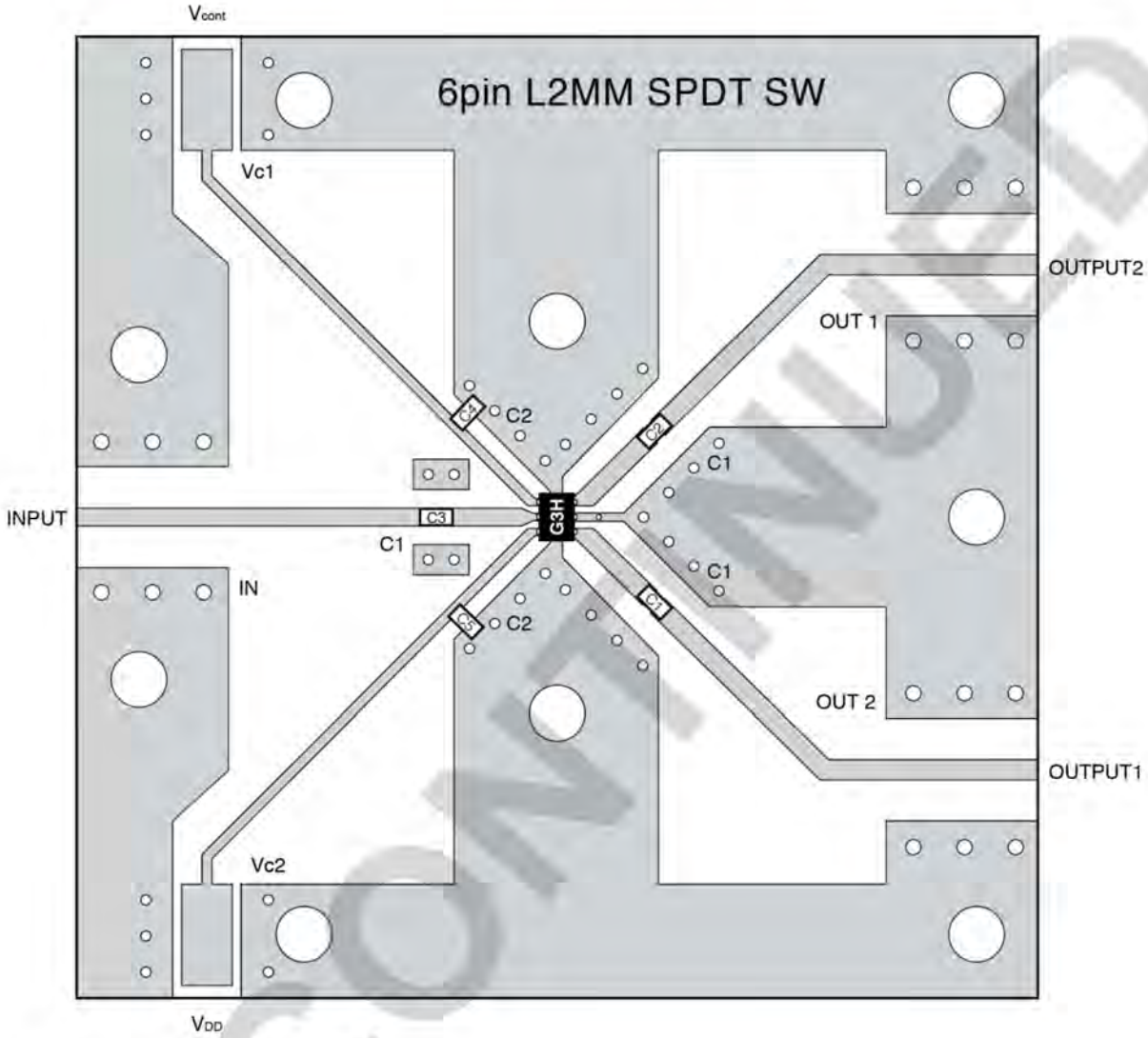
Caution This device is used it is necessary to use DC cut capacitors. The value of DC cut capacitors should be chosen to accommodate the frequency of operation, bandwidth, switching speed and the condition with actual board of your system. The range of recommended DC cut capacitor value is less than 100 pF.

EVALUATION CIRCUIT (V_{DD} = 2.8 V, V_{cont} = 2.8 V/0 V, DC cut capacitors = 56 pF)



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

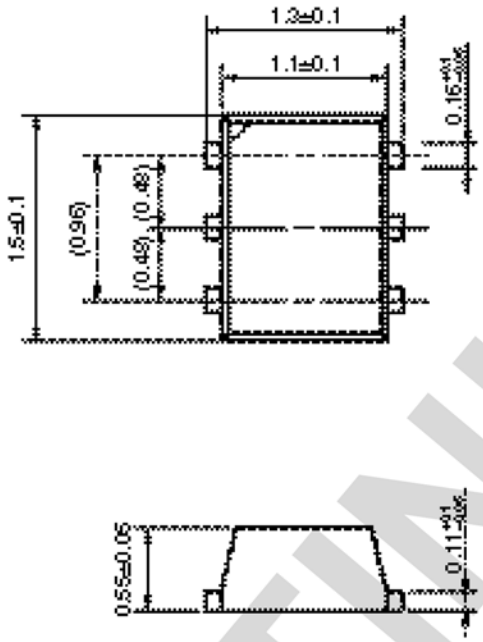


USING THE EVALUATION BOARD

Symbol	Values
C1, C2, C3	56 pF
C4, C5	1 000 pF

PACKAGE DIMENSIONS

6-PIN LEAD-LESS MINIMOLD (1511) (UNIT: mm)



Remark ( ): Reference value

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350

Caution Do not use different soldering methods together (except for partial heating).

SAFETY INFORMATION ON THIS PRODUCT

Caution GaAs Products	The product contains gallium arsenide, GaAs. GaAs vapor and powder are hazardous to human health if inhaled or ingested. • Do not destroy or burn the product. • Do not cut or cleave off any part of the product. • Do not crush or chemically dissolve the product. • Do not put the product in the mouth. Follow related laws and ordinances for disposal. The product should be excluded from general industrial waste or household garbage.