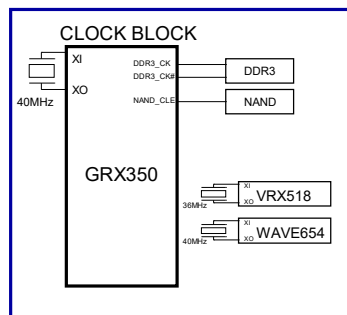
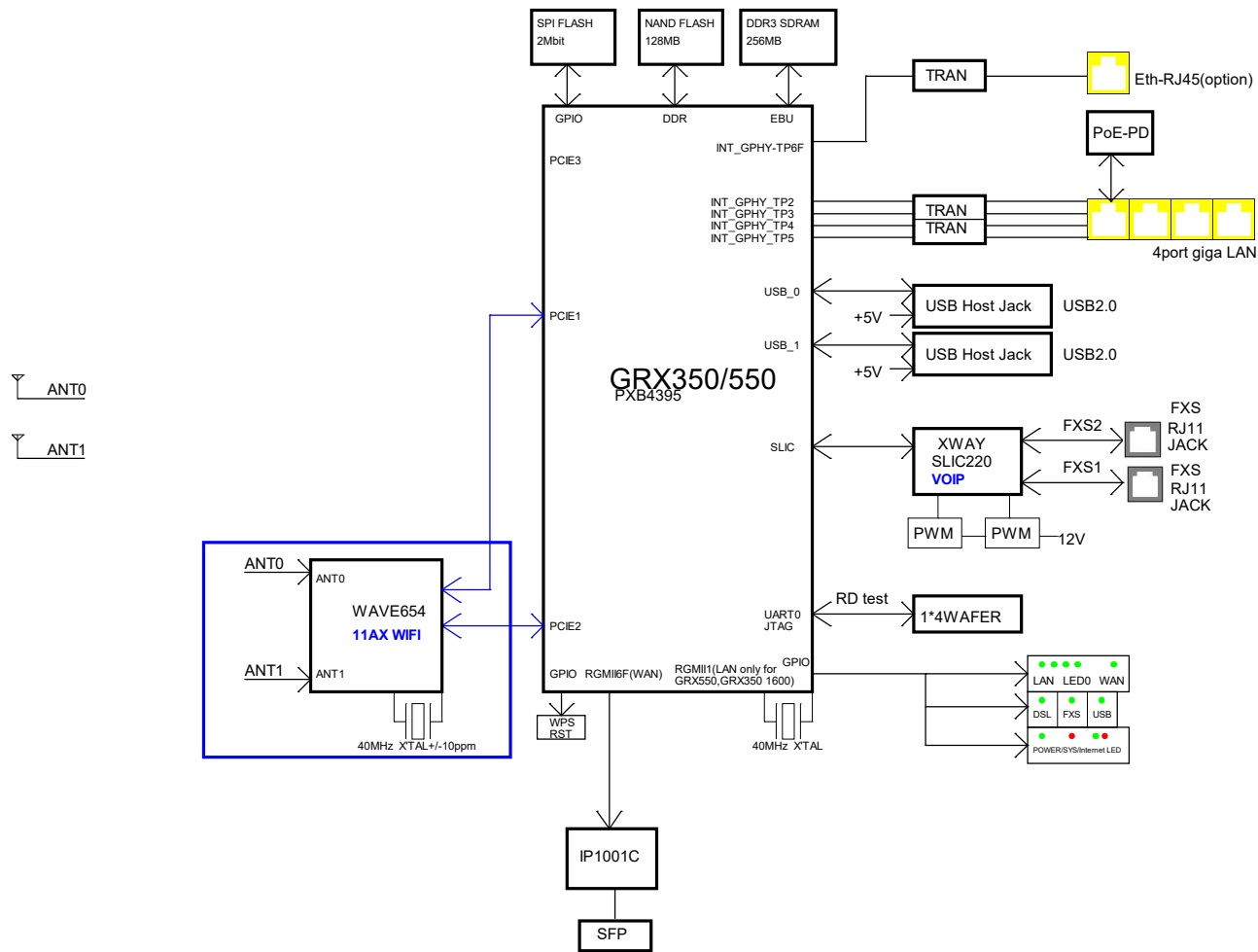
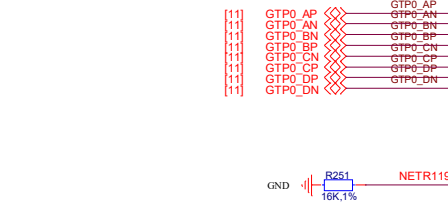




1. 100 ohm characteristic impedance control for TPI differential signal routing. Keep the reference plane of signal continuous.

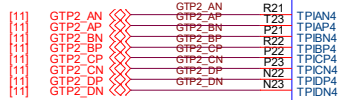
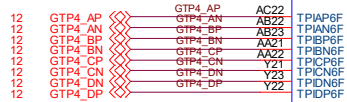
2. The TPI signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.



An external Rcal 16K ohm +/-1% resistor should be connect from the RCAL pin to ground. Place the Rcal resistor close to RCAL ball.

U5A

GPHY



RCAL

GRX350

HEATSINK CLIPS

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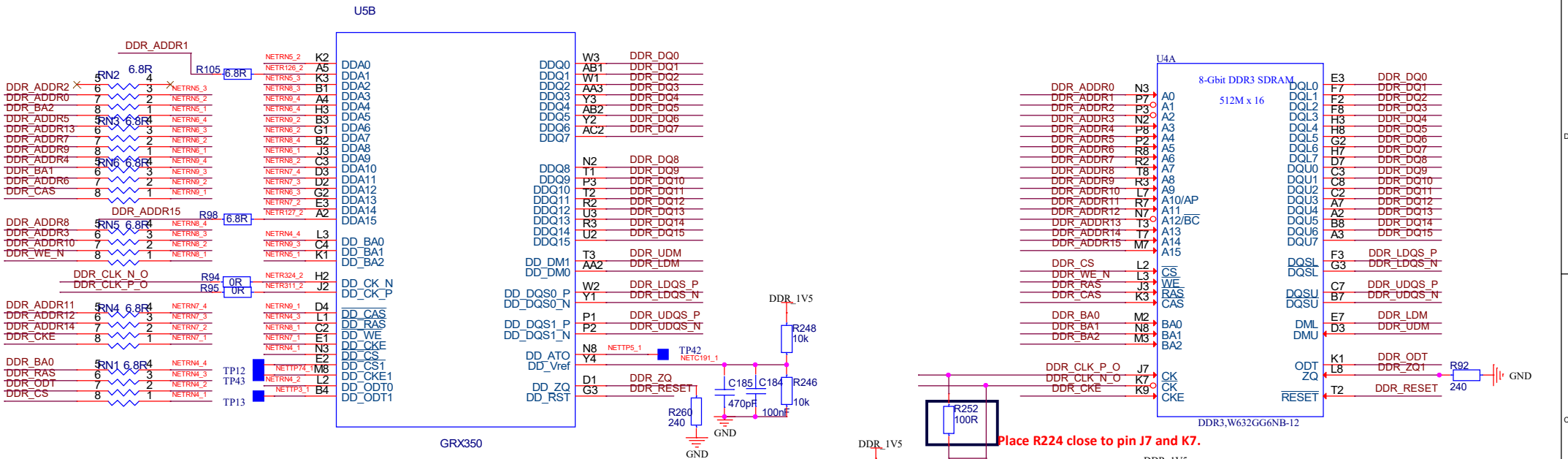
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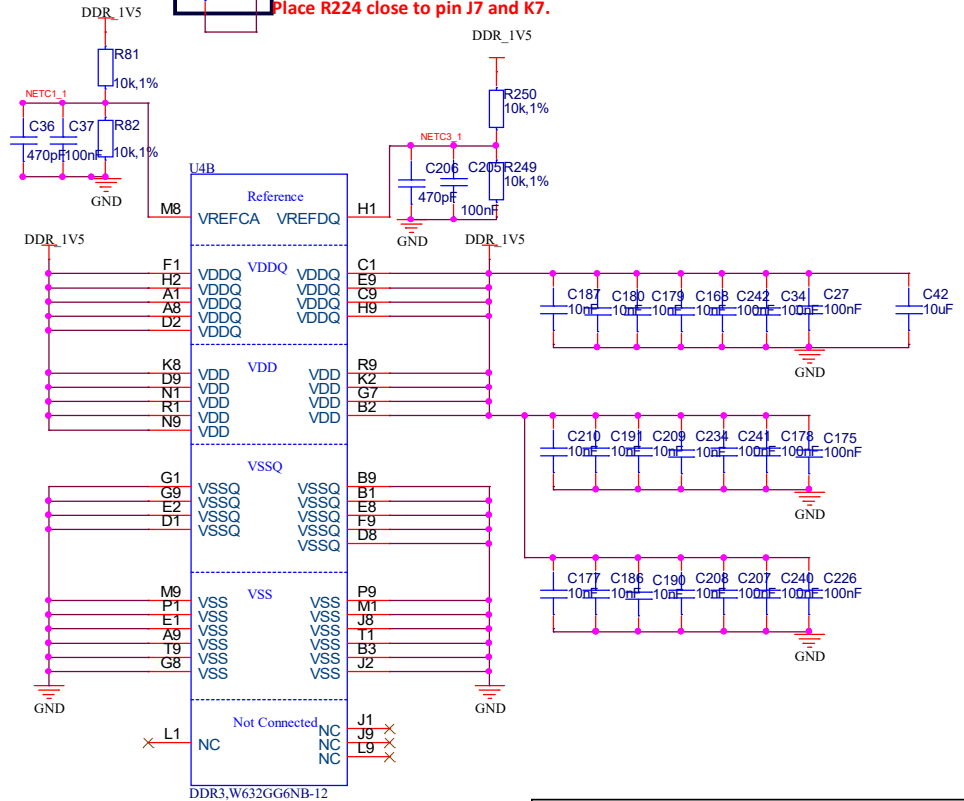
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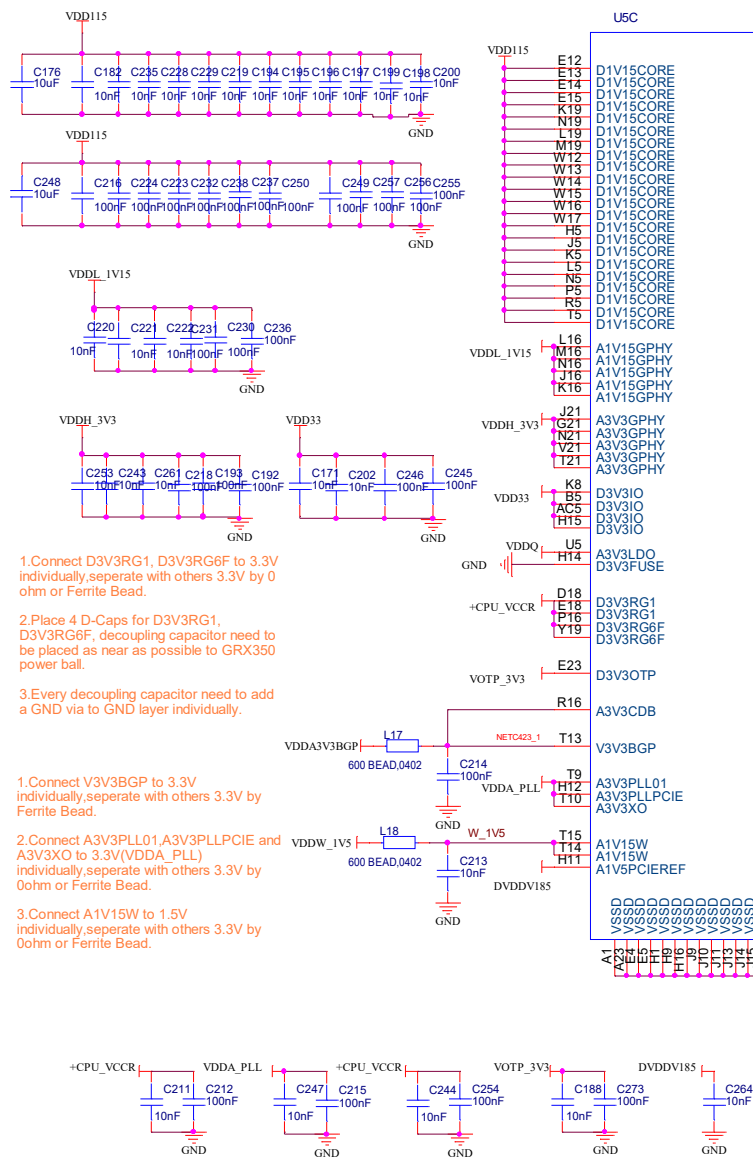


Qualified DDR3 List

Etron: EM6GC16EWXD-10H (64Mx16bit, single rank (CS0))
Micron: MT41K128M16JT-125:K (128Mx16bit, single rank (CS0))
Micron: MT41K256M16HA-125 IT:E (256Mx16bit, single rank (CS0))
Winbond: W634GG6LB-12 (256Mx16bit, single rank (CS0))
Etron: EM6GE16EWC-10H (256Mx16bit, single rank (CS0))
Nanya: NT5CB256M16DP-EK (256Mx16bit, single rank (CS0))
Micron: MT41KS12M16HA-125:A (512Mx16bit, single rank (CS0))

- Place 6.8ohm series termination resistors close to GRX350 for CA group.
- An external RZQ 240 ohm+/-1% resistor should be connect from the ZQ pin to ground on both GRX350 and DDR device.
- System DD_VREF and DDR device VREFCA and VREFDQ are separated, divided by 10K ohm +/-1% resistors.
- 55 ohm Single-End and 100 ohm Differential signals impedance control
- 5.5mils Single-End trace width, trace to trace clearance is 10mils
- Length Matching
Maximum trace length difference (skew) between DQS and DQS#: ± 4 mils (< 0.6 ps).
Maximum trace length difference (skew) DQ to DQS/ DQS# domain: ± 30 mils (< 10 ps).
Maximum trace length difference (skew) Addr/ Cmd to CK/ CK# domain: ± 70 mils (< 25 ps).
Maximum trace length difference (skew) DQS/ DQS# to CK/ CK# domain: ± 250 mils (< 90 ps).
- Crosstalk control (Note: H is distance from reference layer):
Keep edge-to-edge trace spacing within DQ/DM byte group $> 2H$
Keep edge-to-edge trace spacing within Cmd/Addr/Ctrl $> 2H$ (commonly known as CA)
Keep edge-to-edge trace separation for each group (DQ, DQS/ DQS#, CA, CK/ CK#) $> 3H$
- DDR CLK differential termination 100ohm place at the end on DDR device. as close to CLK pins as possible.
- Fly-By Topology & VTT Termination recommended for DDR3, if multiple devices are used.
- Carefully consider layout requirements of DDRn vendor!!!

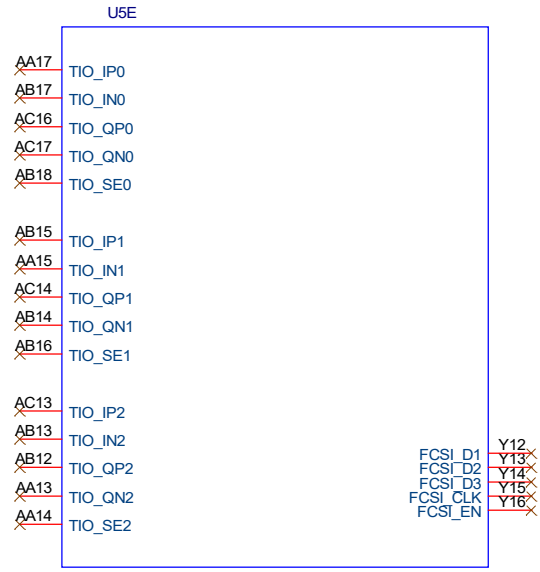




Power

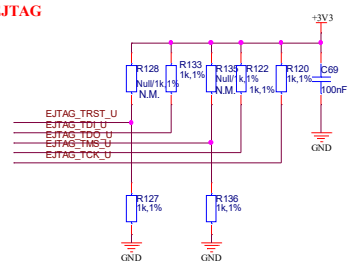
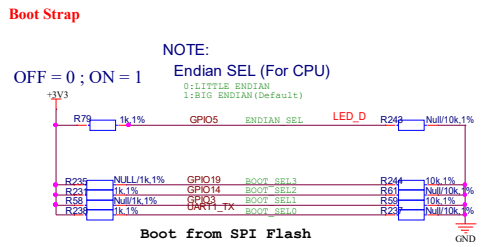
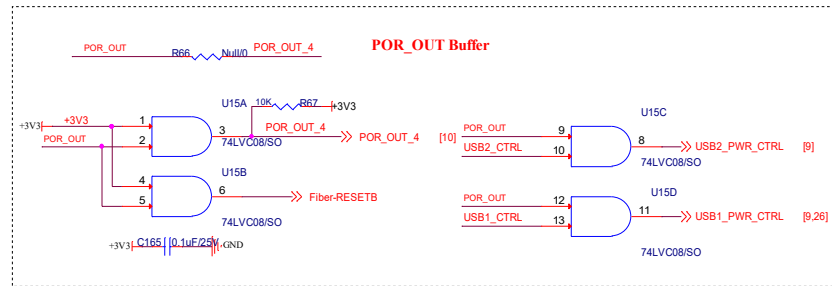
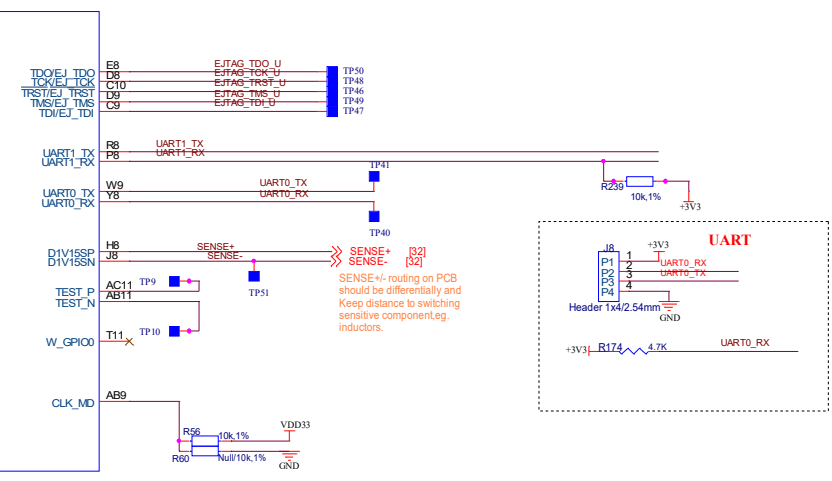
- 1.Connect A1V15USB0VP,A1V15USB1VP to 1.15V individually,separate with others 1.15V by 0 ohm or Bead.
- 2.Connect A1V15USB0VT,A1V15USB1VT to 1.15V individually,separate with others 1.15V by 0 ohm or Bead.
- 3.Connect A3V3USB,A3V3USBPVPH to 3.3V individually,separate with others 3.3V by 0 ohm or Bead.
- 4.Connect A1V15USB0,1 to 1.15V individually,separate with others 1.15V by 0 ohm or Bead.

- 1.Connect A3V3PCIE to 3.3V individually separate with others 3.3V by 0 ohm or Bead.
- 2.Connect A1V15PCIE1VT,A1V15PCIE2VT,A1V15PCIE3VT to 1.15V individually,separate with others 1.15V by 0 ohm or Bead.
- 3.Connect A1V15PCIE1VP,A1V15PCIE2VP,A1V15PCIE3VP to 1.15V individually,separate with others 1.15V by 0 ohm or Bead.



GRX350

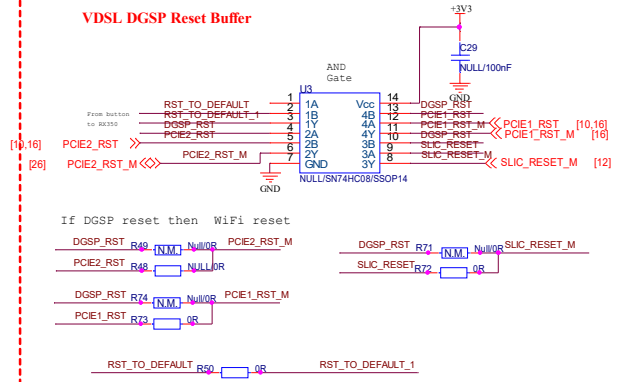
Trace capacitance for BBIO
interface must be below 10pF!
Recommend the maximum
length should be under 3 inch.

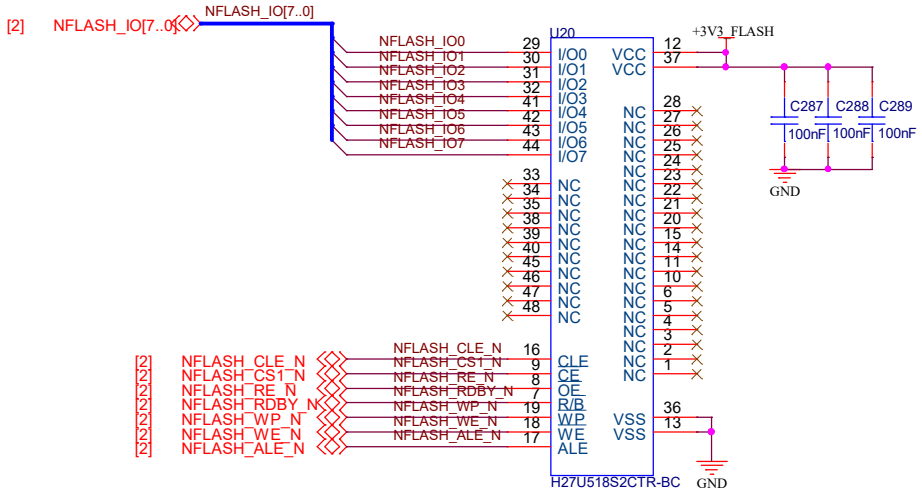


Strap Pin Setting Table

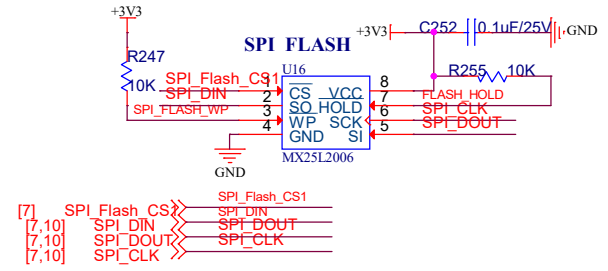
SP018 (BOOT_SEL1)	SP019 (BOOT_SEL1)	SP020 (BOOT_SEL1)	WAKE UP (WUP_SEL1)	Boot Source
0	0	1	0	UART w/ RESPIN
0	0	1	1	UART WAKE UP (w/ wake-up, SEC is WAKE device)
0	1	0	0	UART w/ RESPIN
0	1	0	1	UART FLASH or RESPONSE must be used for boot device
1	0	1	0	Legacy NAND (up to 25 years)
1	0	0	1	SP-NAND
1	1	0	0	Generation1-SP1 NAND
1	1	1	0	SP2, COMBINED NAND

All other options are reserved/not used.

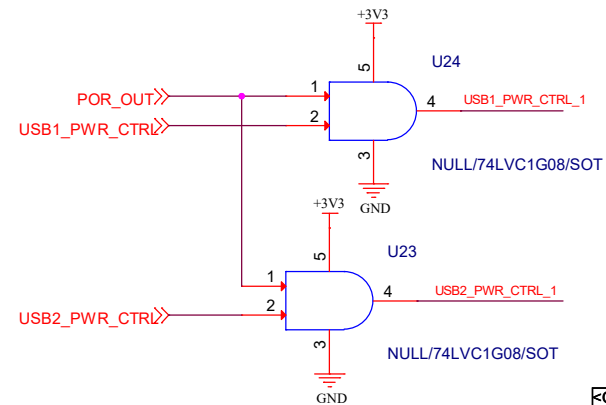
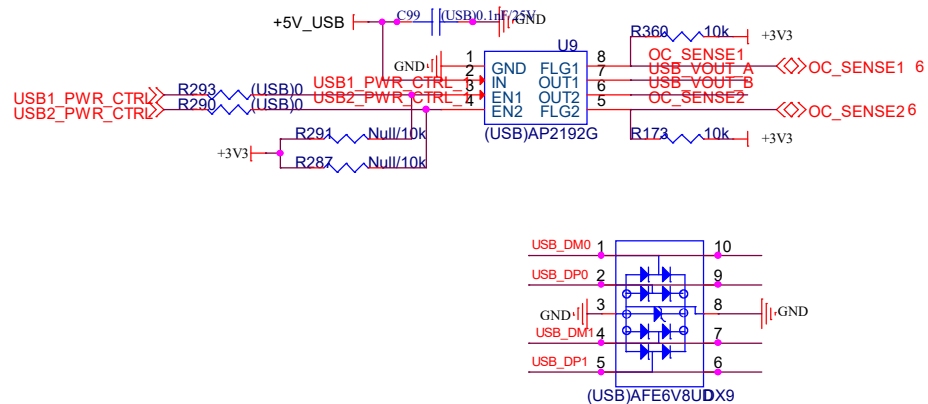
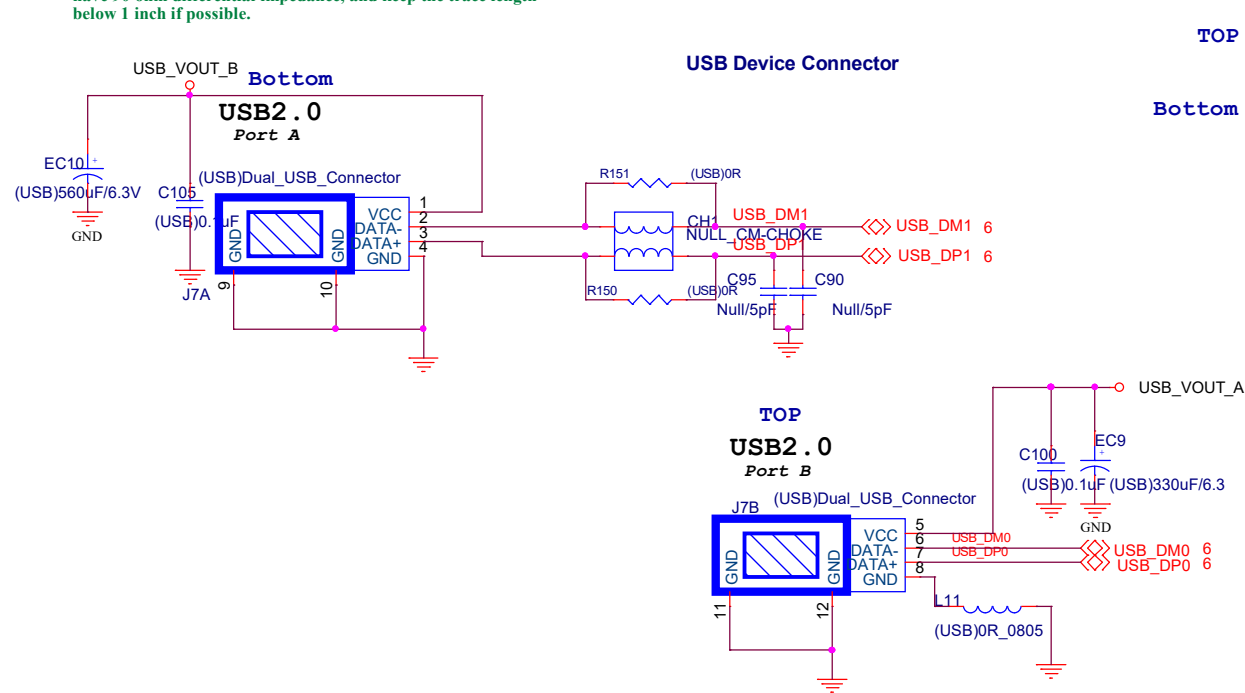




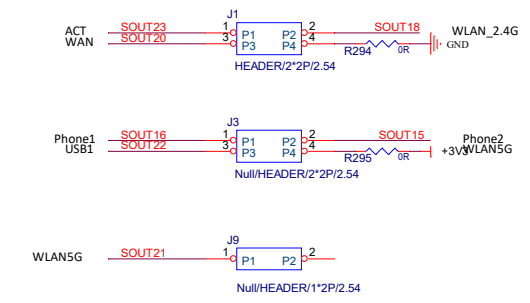
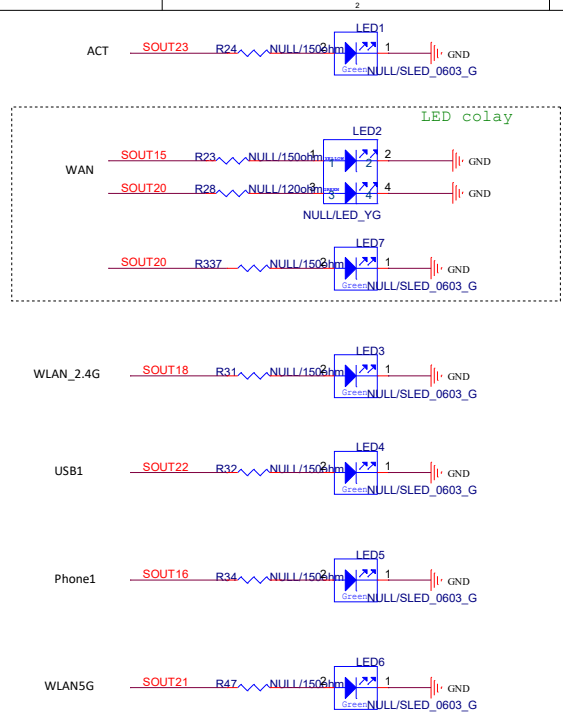
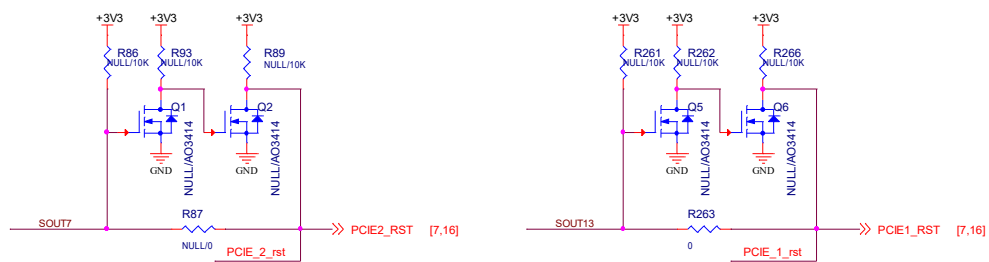
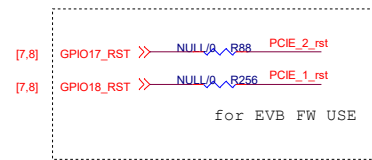
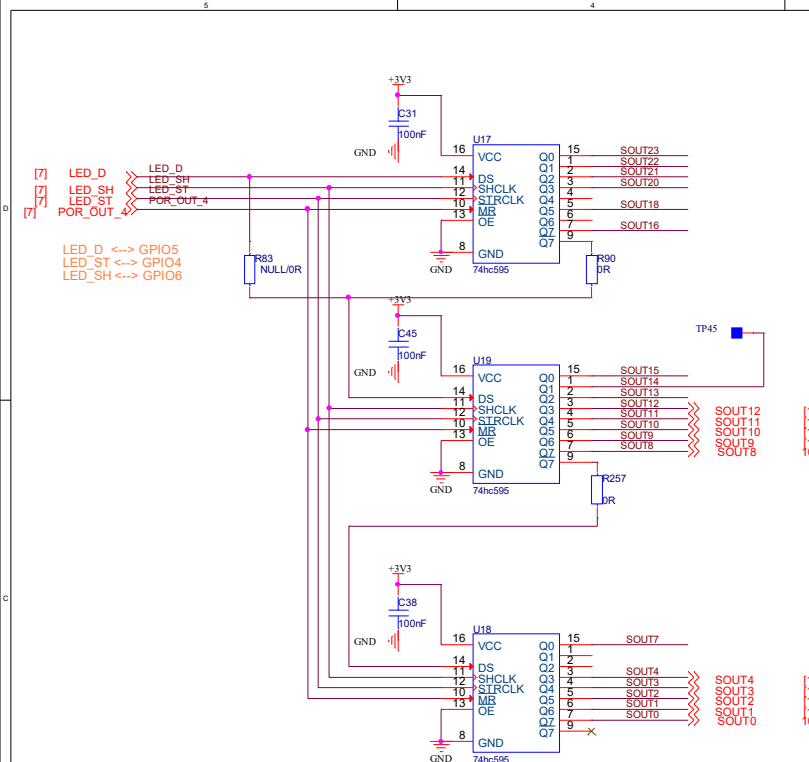
Qualified Nand Flash List	
Vendor	Model
Hynix	H27uag8, 8k
Hynix	H27u512, 512
Hynix	H27u4g8f2dtr, 2k
Hynix	H27u1g8f2btf, 2k
Samsung	K9F1208, 512
Samsung	K9flg08u0d, 2k
Samsung	K9g4g08u0b, 2k
Samsung	K9G8G08U0C, 8k
Spansion	S34ml01g100, 2k
Mircon	29f64g08cbaca, 8k
Mircon	29f32g08cbaca, 4k
Infineon	Hyf33ds51280, 512
Toshiba	Th58BVG3S0HTA00, 4k



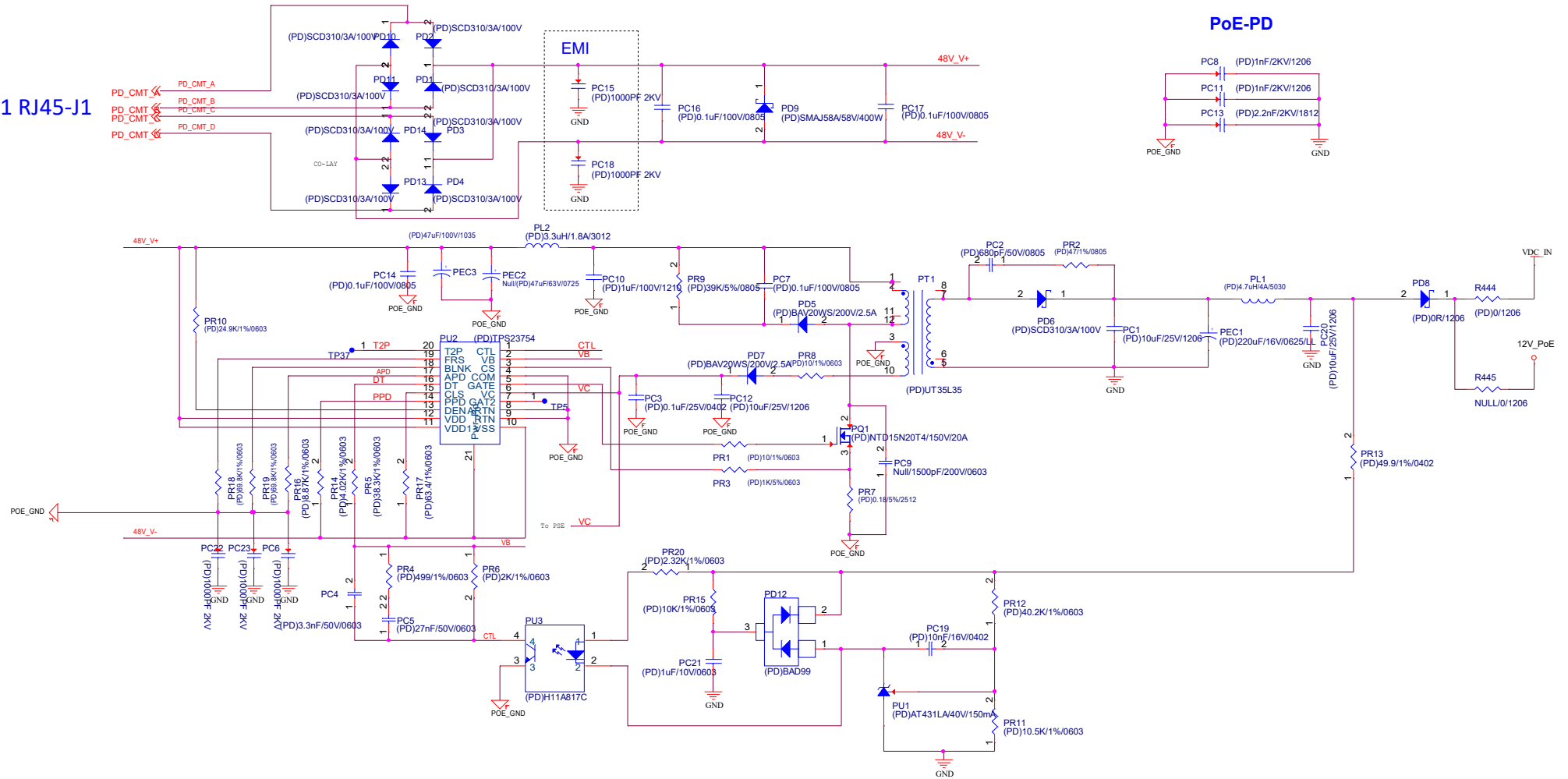
!!Note:
The PCB layout of the differential signal DP and DM should have 90 ohm differential impedance, and keep the trace length below 1 inch if possible.



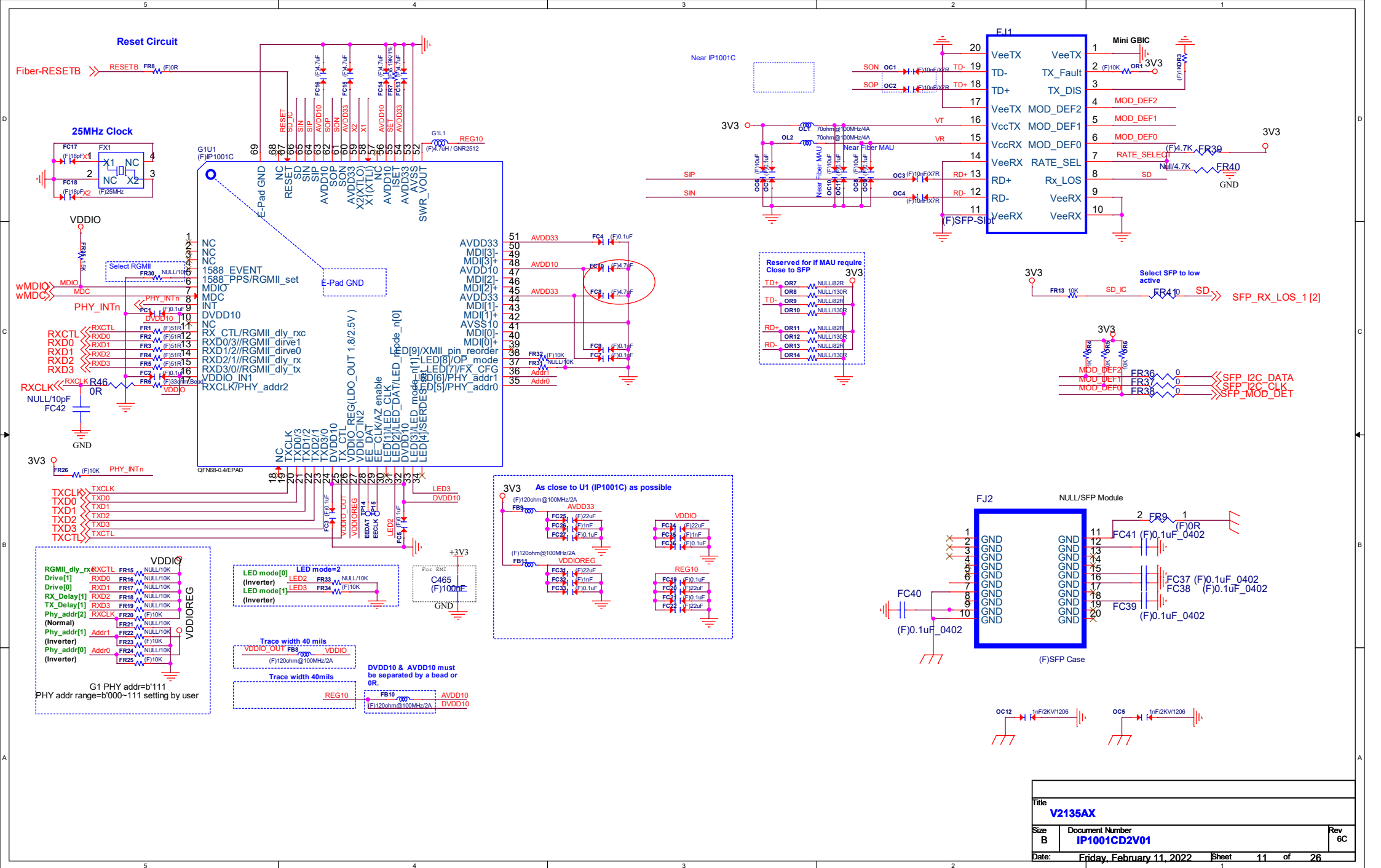
<OrgName>			
DrayTek			
Title			
USB_Port			
Size	Document Number	Rev	
B	V2135AX	6C	
Date:	Friday, February 11, 2022	Sheet	08 of 26



To LAN1 RJ45-J1



<OrgName> DrayTek	
Title POE PD	
Size	Document Number
Custom	V2135AX
Date	Friday, January 28, 2022
Sheet	11 of 26
Rev	BC



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				SY88004 : V _{out} =0.615+120K/(65K) $\times$ 1.036V Wav654 Range : 0.72V~1.05V
Table 32 JTAG Signals				
Ball No.	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	JTAG Reset
				Notes 1. Low active. 2. If the JTAG interface is not in use, this pin must be connected to V _{SS} .
	EJ_TRST	I	PU	EJTAG Reset
A35	TDI	I	PU	Test Data Input
	EJ_TDI	I		EJTAG Test Data Input
B33	TDO	O	PD	Test Data Output
				Note: pull down is needed for normal operation.
	EJ_TDO	O		EJTAG Test Data Output
B29	TMS	I	-	Test Mode Select
	EJ_TMS	I		EJTAG Mode Select

--

UART CONN

PCIE FINGER

Figure 10 shows four recommended PCB layout diagrams for the ADXL345, each representing a different signal path (TX_LB_0, RX_LB_0, TX_LB_2, RX_LB_2) connected to a 2G_TX or 2G_RX pin. Each diagram includes a series resistor (XR48, XR49, XR58, XR53) and two shunt capacitors (XC52, XC46, XC53, XC47, XC66, XC65, XC64, XC57) connected to ground. The components are specified as 10pF/25V/0201/2%.

The figure contains two circuit diagrams, CH1 and CH3, representing the input and output matching networks for the ACX 5G BPF (XU65) and ACX 5G BPF (XU66).

CH1: ACX 5G BPF (XU65) Input Matching Network

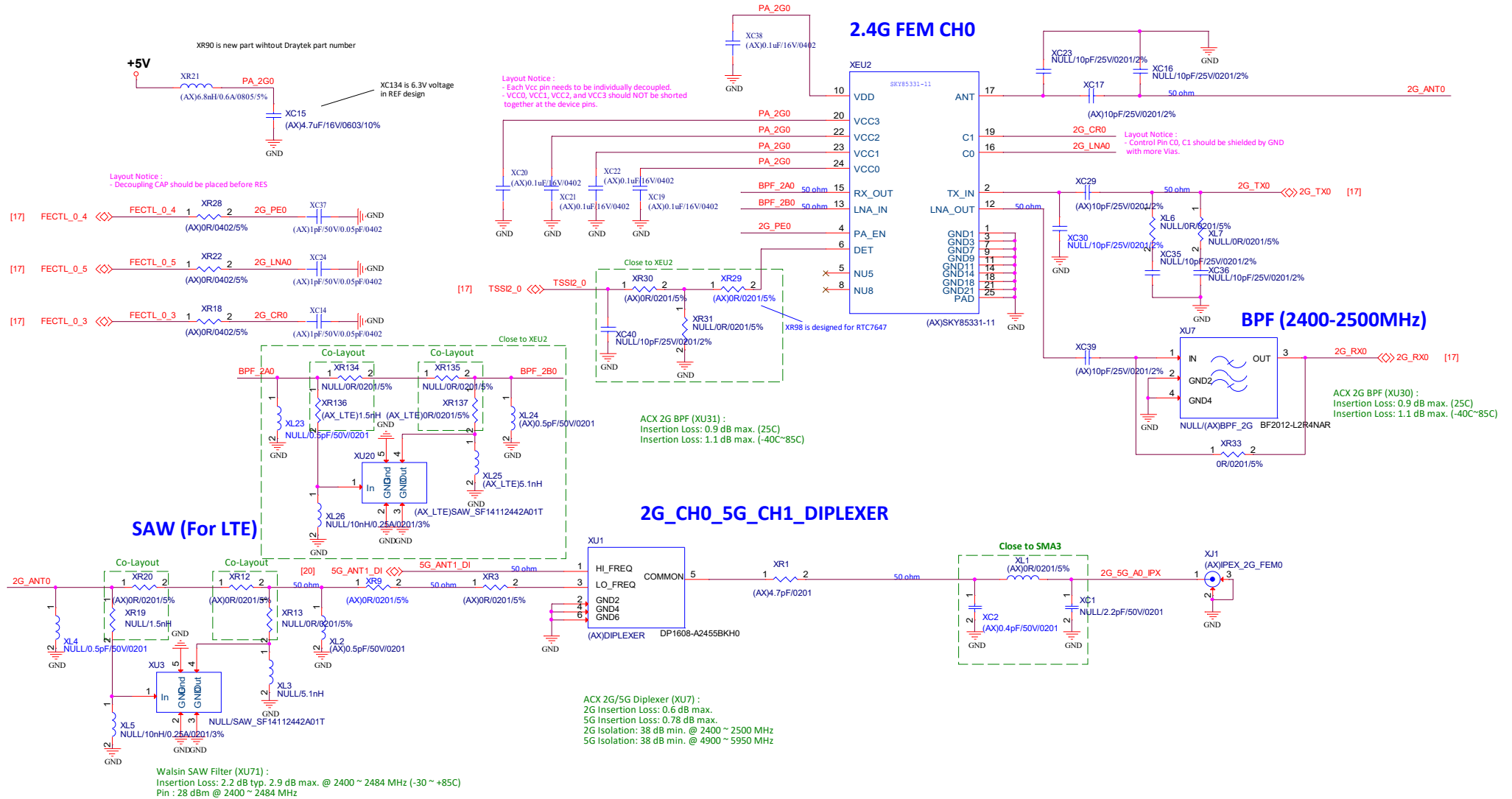
- Input:** TX_HB_1 (1) connected to a series resistor XR47 (AXJ0R0201/5%) and a series resistor XR41 (NULL0R0201/5%).
- Matching Network:** A series resistor XR46 (AXJ0R0201/5%) followed by a shunt capacitor XC58 (NULL10pF/25V/0201/2%).
- Output:** 5G_TX1 (2) connected to a series resistor XR43 (AXJ0R0201/5%) and a series resistor XR41 (NULL0R0201/5%).
- Component Values:** XR47, XR41, XR46, XR43 are 0.201 ohm resistors. XC58 is a 10 pF capacitor.
- Grounding:** The shunt capacitor XC58 is connected to GND.
- Performance:** ACX 5G BPF (XU65); Insertion Loss: 0.7 dB max.

CH3: ACX 5G BPF (XU66) Input Matching Network

- Input:** TX_HB_3 (1) connected to a series resistor XR64 (NULL0R0201/5%) and a series resistor XR83 (AXJ0R0201/5%).
- Matching Network:** A series resistor XR62 (NULL0R0201/5%) followed by a shunt capacitor XC69 (NULL10pF/25V/0201/2%).
- Output:** 5G_TX3 (2) connected to a series resistor XR61 (AXJ0R0201/5%) and a series resistor XR62 (NULL0R0201/5%).
- Component Values:** XR64, XR62, XR83, XR61 are 0.201 ohm resistors. XC69 is a 10 pF capacitor.
- Grounding:** The shunt capacitor XC69 is connected to GND.
- Performance:** ACX 5G BPF (XU66); Insertion Loss: 0.7 dB max.

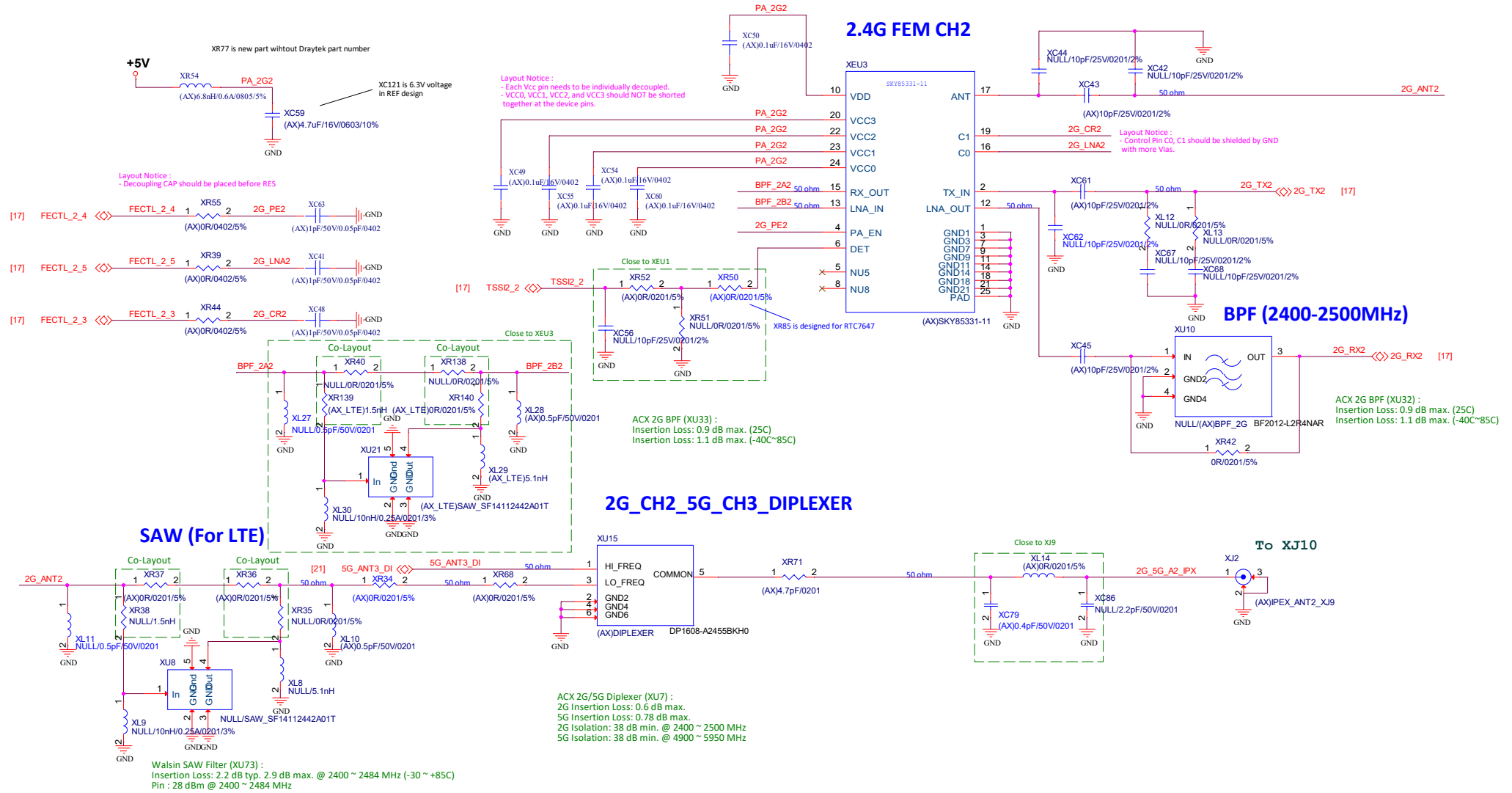
The schematic diagram illustrates the power plane connections for 5V and VDD1V5. It shows a network of capacitors (XR110, XR4, XR132, XR117) connected to a 5V supply and various power planes (5V_AX, VDD1V5_AX, VDD3V3_AX, VDD1V_AX). The capacitors are labeled with their values: (AX)0R1206/5%.

SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V



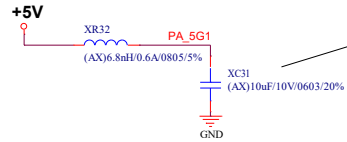
SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V

2.4G FEM CH2

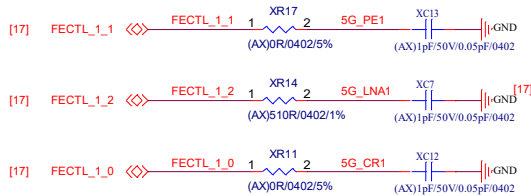


<OrgName>		DrayTek	
File		RF_2.4G_FEM_CH2	
Size	Document Number	Rev	
Custom	V2135AX	6C	
Date:	Friday, January 28, 2022	Sheet	19 of 26

XR103 is new part without Drytek part number

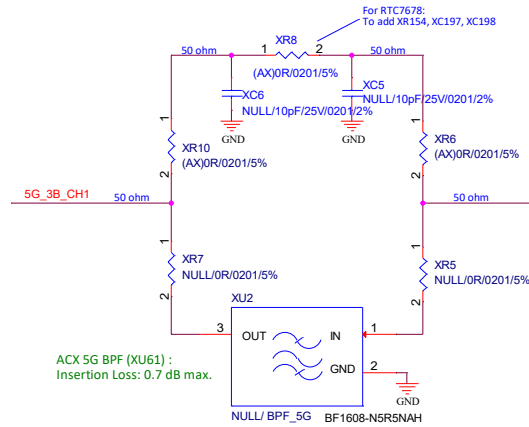


Layout Notice :
- Decoupling CAP should be placed before RES



ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)

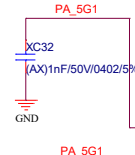


ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)

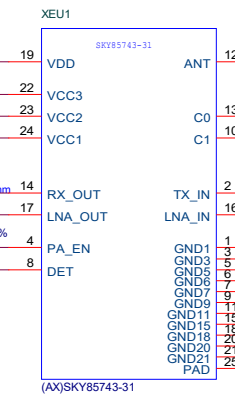
Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.



5G FEM CH1

SKY85743-31:
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9

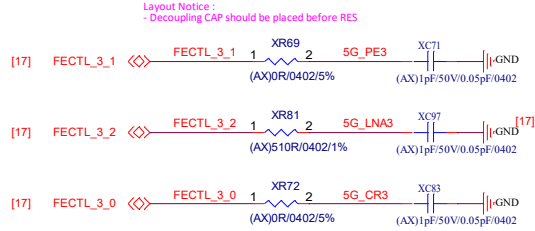
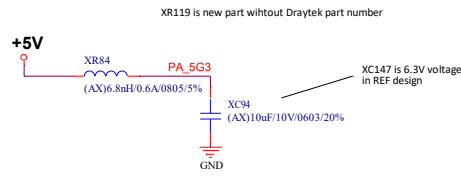


BPF (5150-5950MHz)

XU11 preserved to test and debug only

5G_ANT1

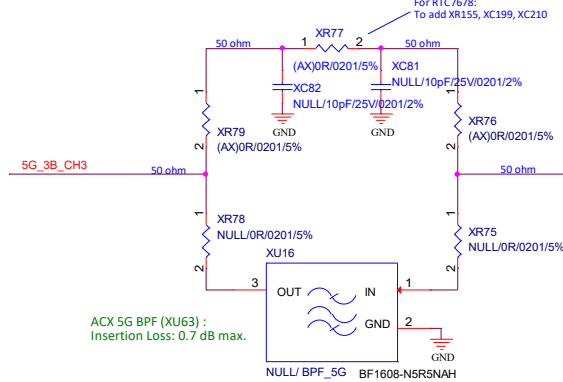
<OrgName> DrayTek		
File RF_5G_FEM_CH1		
Size	Document Number	Rev
Custom	V2135AX	6C
Date: Friday, January 28, 2022 Sheet 20 of 26		



5G_RX3 <>> 5G_RX3

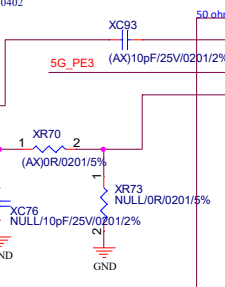
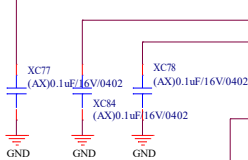
ACX 5G BPF (XU63) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)



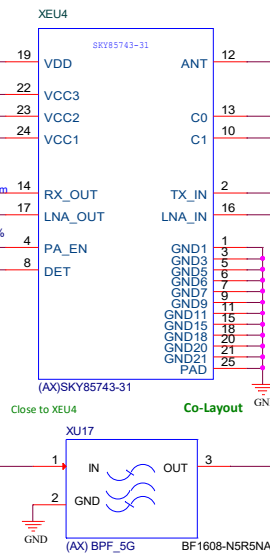
BPF (5150-5950MHz)

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

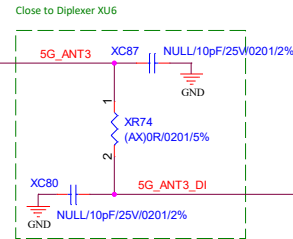
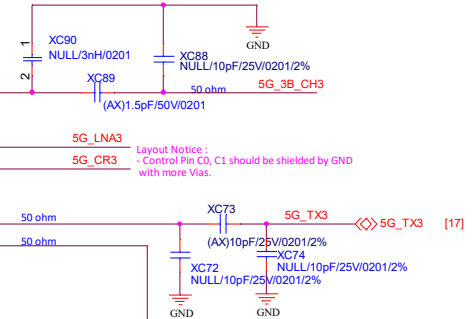


SKY85743-31:
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9

5G FEM CH3



BPF (5150-5950MHz)

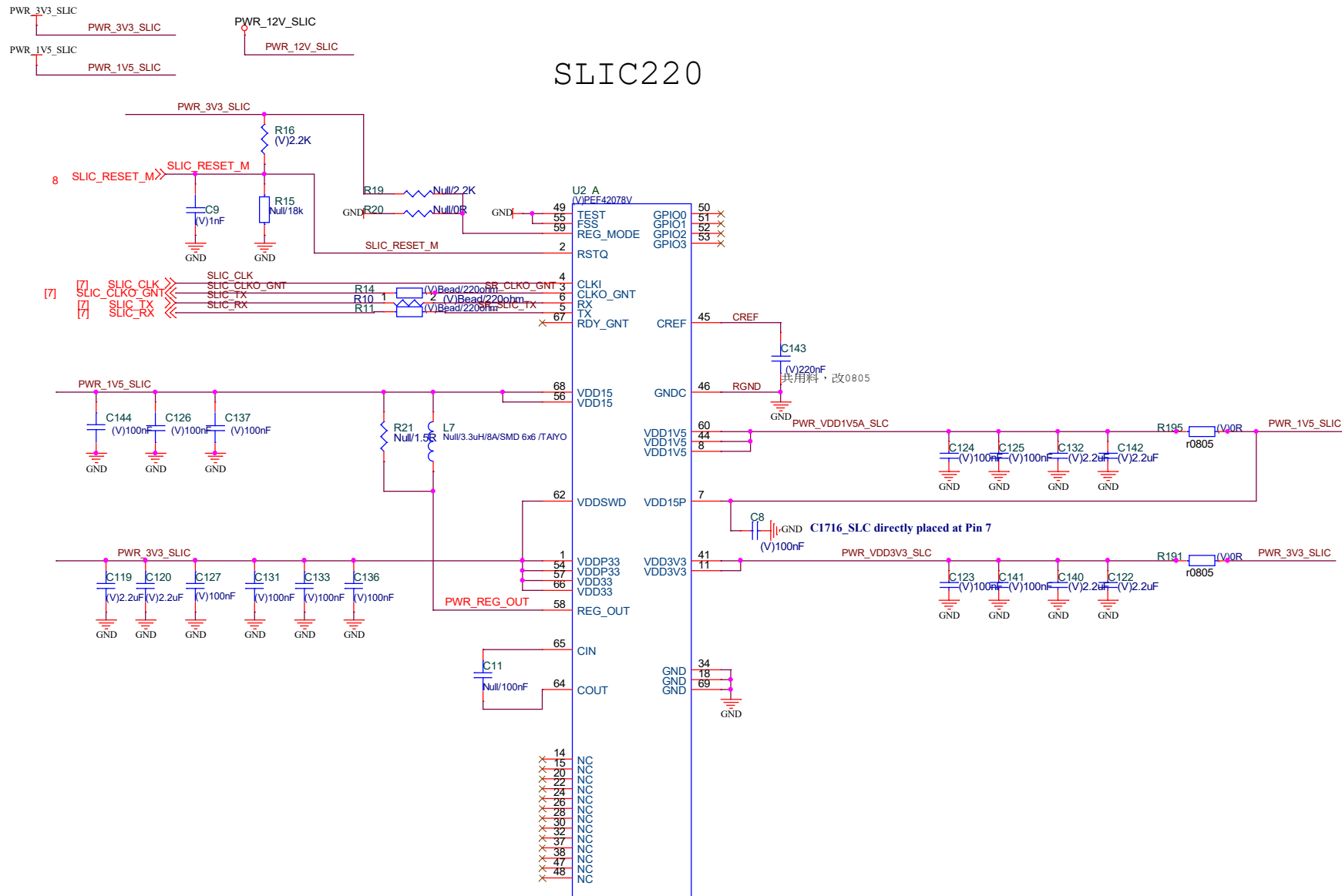


5G_ANT3

XU12 preserved to test and debug only

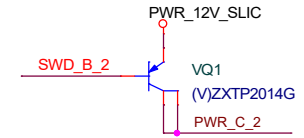
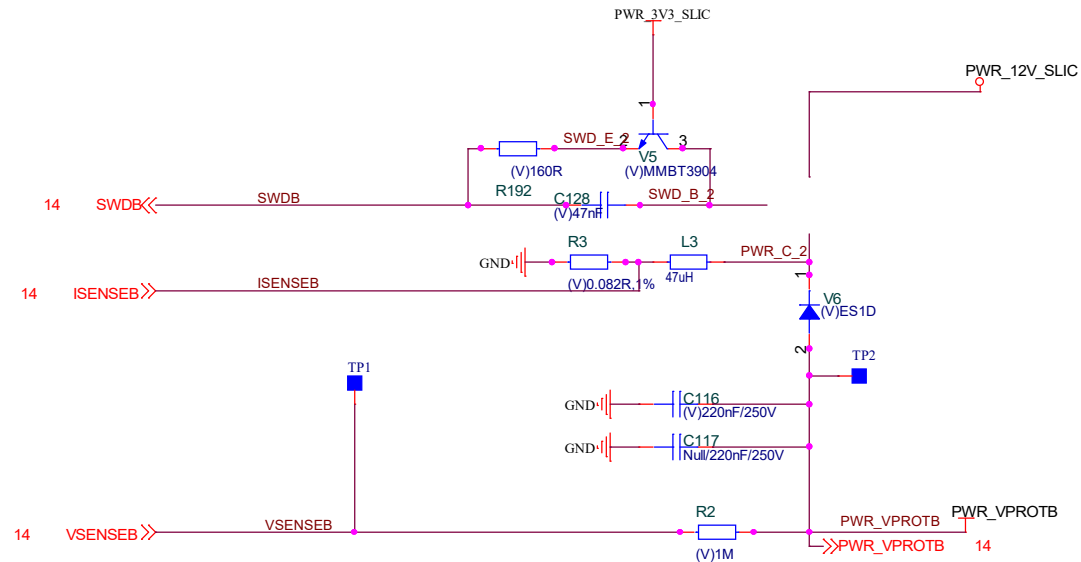
<OrgName> DrayTek		
File RF_5G_FEM_CH3		
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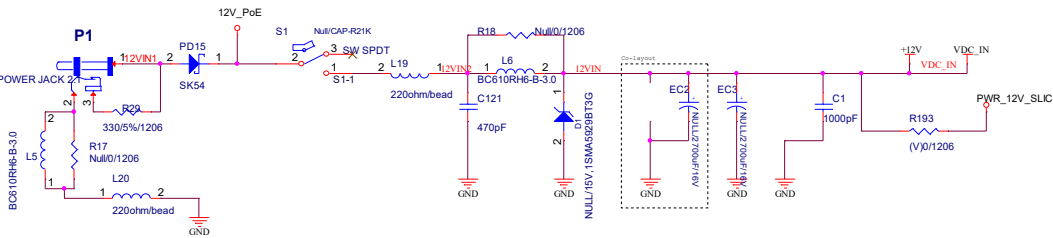
DCDC Type
Dedicated DCDC = T0.2
Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the relating part and the DSL must be maintain.

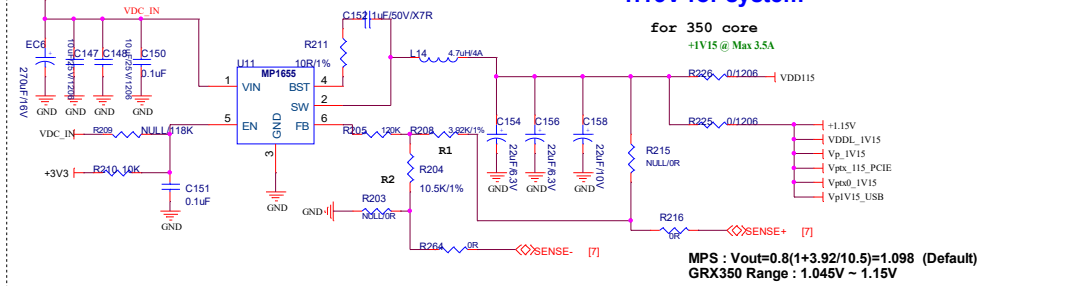


Component	Dedicated DCDC	Combined DCDC
R77	0.082R	0.068R
L9	47uH/1.8A	33uH/2.1A
C204	mount	X
C1806	X	mount

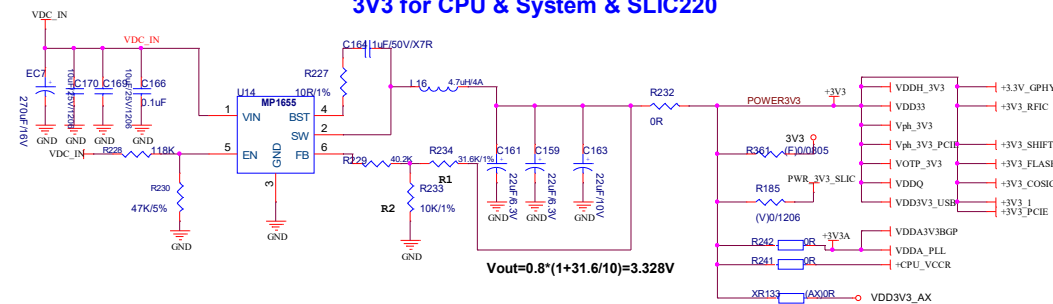
12V DC Power Input



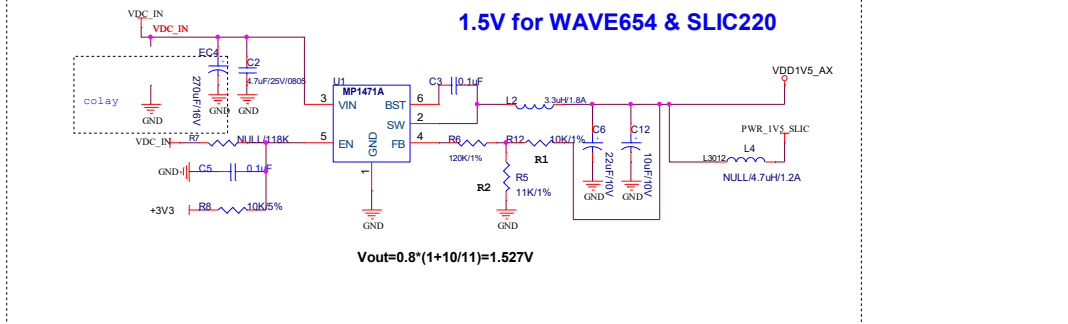
1.15V for system



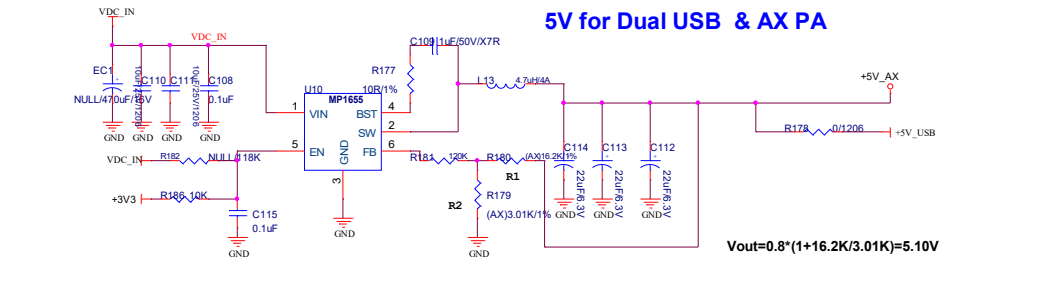
3V3 for CPU & System & SLIC220



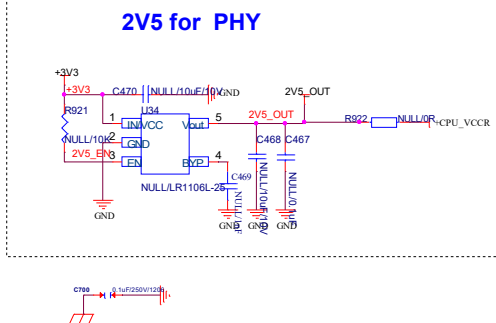
1.5V for WAVE654 & SLIC220



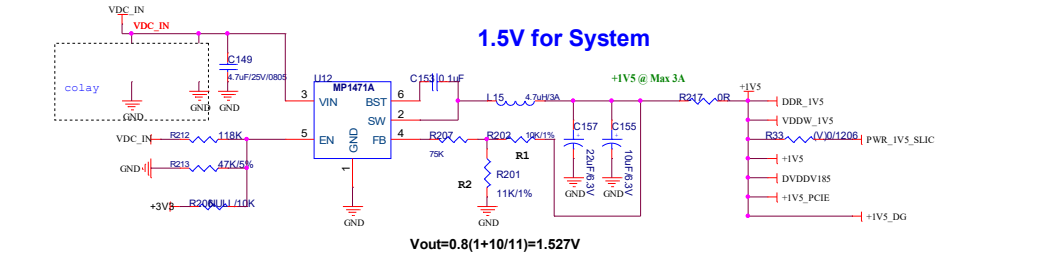
5V for Dual USB & AX PA



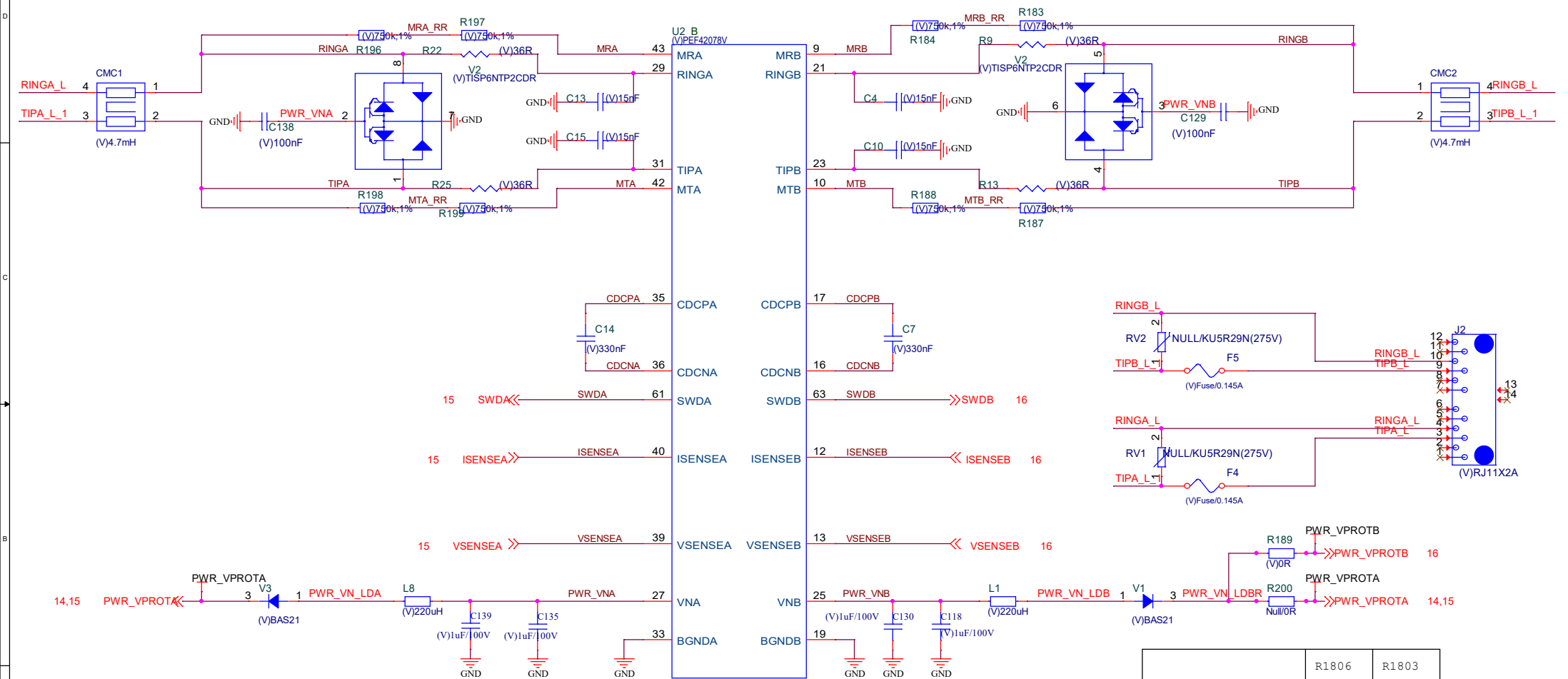
2V5 for PHY



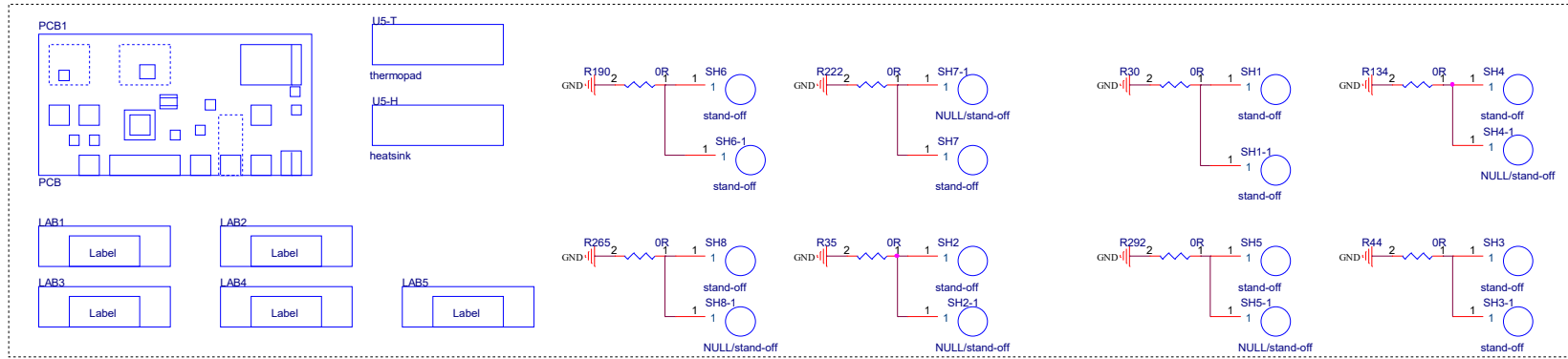
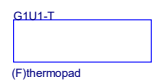
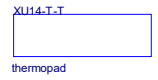
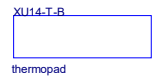
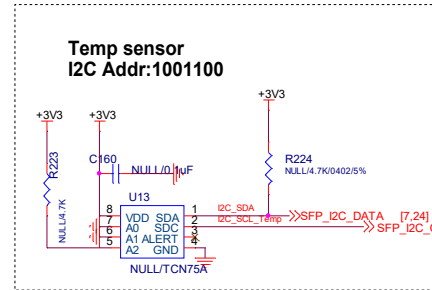
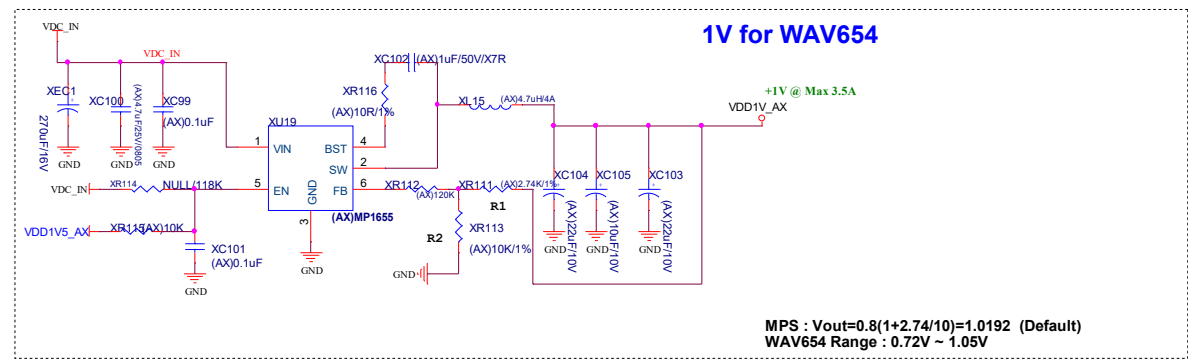
1.5V for System



SLIC220

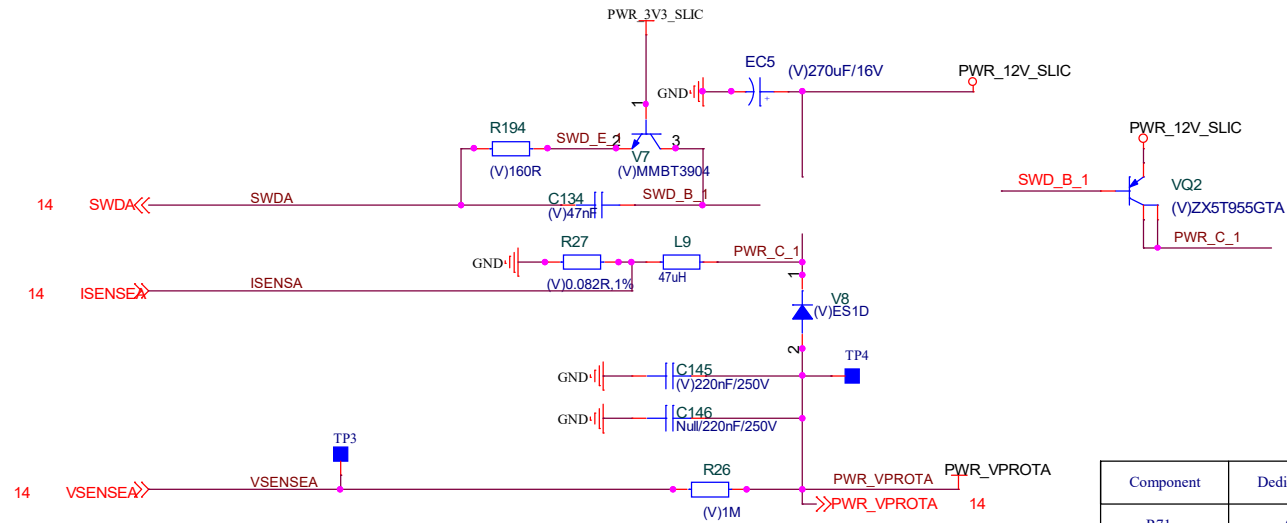


	R1806	R1803
Dedicated DCDC mode	Mounted	X
Combined DCDC mode	X	Mounted



<OrgName>		DrayTek	
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Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the radiating part and the DSL must be maintain.



Component	Dedicated DCDC	Combined DCDC
R71	0.082R	0.068R
L7	47uH/1.8A	33uH/2.1A
C196	mount	X
C1805	X	mount

REVISION HISTORY

Version	Date	List of Modification	Page
V6A	2021-02-02	1. Remove VRX518 circuit 2. Add EWAN circuit 3. Add IP1001 circuit	Ian
	2020-12-10	2.4GHz FEM (152-5331900-00G,SKY85331-11) : 1. Add XU31, XU33 2. Remove XC12, XC13, XC10, XC11 3. Null XR101, XR88, XU30, XU32 4. Place XR137, XR136 5. Remove XR146, XR149, XR142, XR145 5GHz FEM (152-5743900-00G,SKY85743-31) : 1. Add XU51, XU53 for co-layout with XU52, XU54 2. Remove XR117, XR113, XC16, XC17 3. Remove XR118, XR129, XC181, XC182 4. Place XR11, XR12 6. Null XU61, XR10, XR135 7. Place XR139, XR140 8. Null XU63, XR138, XR141	mChen
V6B	2021-06-16	1. Add U20, XR135, XR135, XR136, XR137, XL23, XL24, XL25, XL26 2. Add U21, XR40, XR138, XR139, XR140, XL27, XL28, XL29, XL30 3. PEC3 change footprint EC/1050 4. Add PD15, R444, R445 5. Add J9 6. XC15, XC59 change C0805 7. Add SH4-1	Ian
V6C	2022-01-04	1. Modify EC7 ,EC6 to 270uF. 2. Add U34 curcuit	Ian

BOM Difference

	V2765ax	V2765Vax							
(VD)	V	V							
(V)	NULL	V							
(5)	V	V							
(PD)	NULL	NULL							
(AX)	V	V							
(NPD)	V	V							
(AX_LTE)	NULL	NULL							

<OrgName>			DrayTek
Title			BOM Difference
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