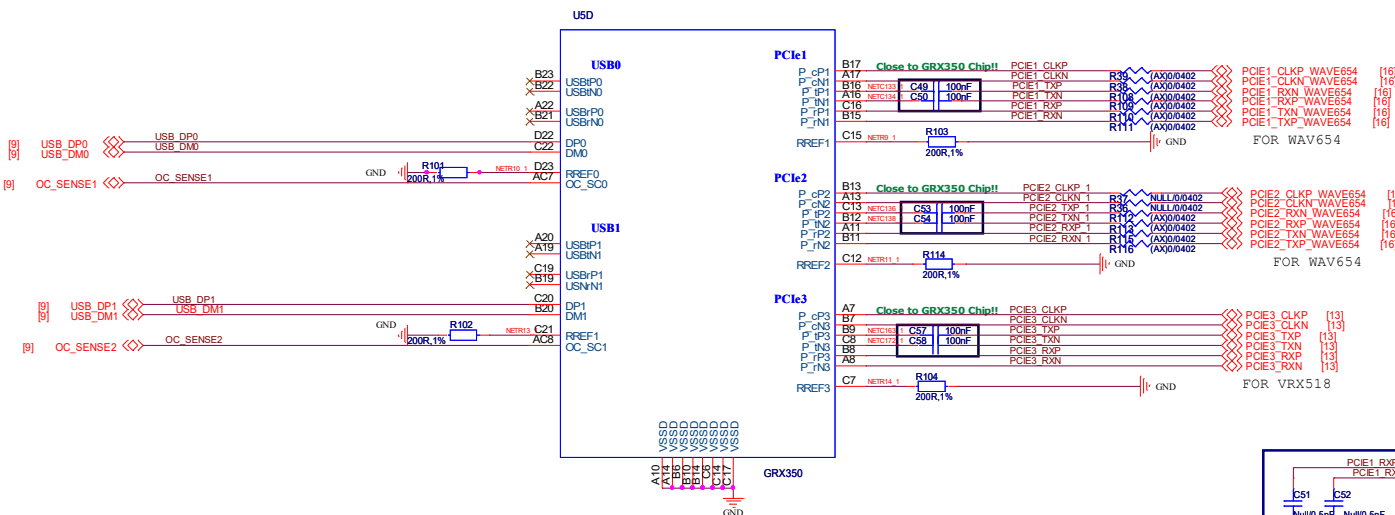
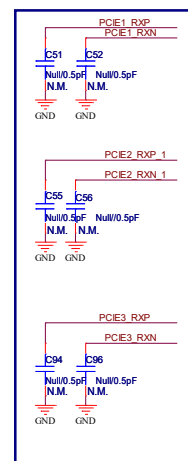


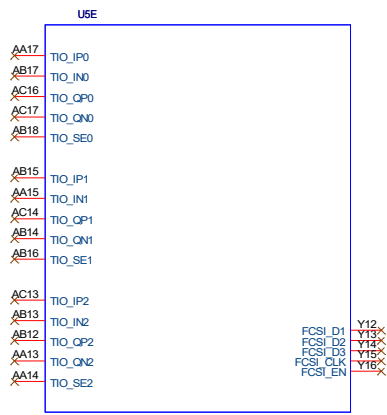
Size Custom		Document Number V2765AX_V1		Rev 6B
Date:		Friday, December 17, 2021		Sheet 2 of 34



1. An external Rref 200 ohm $\pm$ 1% resistor should be connect from the USB RREF0, RREF1 pins to ground. Place the Rref resistor close to RREF balls.
2. Place 2 AC coupling capacitors on USB TX pairs , <0.5inch length to GRX350 is recommended.
3. 90 ohm characteristic impedance control for USB differential signal routing. Keep the reference plane of signal continuous.
4. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.
5. Populate sufficient GND vias nearby each PCIe differential pairs to tighten adjacent GND plane with GND layer.
1. An external Rref 200 ohm $\pm$ 1% resistor should be connect from the 3 PCIe RREF pins to ground. Place the Rref resistors close to RREF balls.
2. Place 2 AC coupling capacitors on PCIe TX pairs , <0.5inch length to GRX350 is recommended.
3. 100 ohm characteristic impedance control for differential signal routing. Keep the reference plane of signal continuous.
4. In case with ≥ 2 PCIe differential pairs routing on PCB, a footprint of shielding case to enclose all these differential pairs is highly recommended for the compliance of EN300-328 V1.8.1 standard.
5. 0.5pF capacitors to ground on PCIe RX pairs, place them close to GRX350.
6. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.
7. Populate sufficient GND vias nearby each PCIe differential pairs to tighten adjacent GND plane with GND layer.

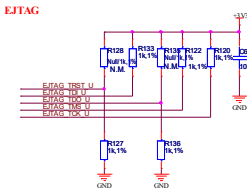
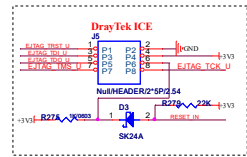
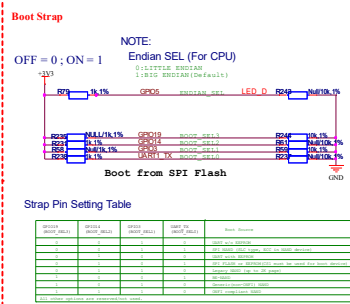
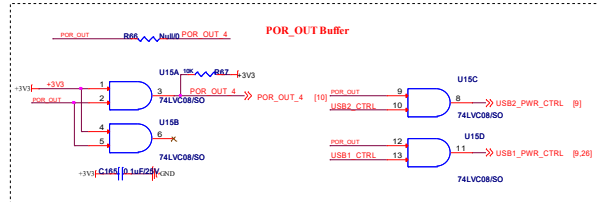
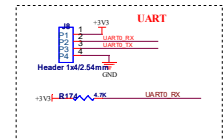


DrayTek			
File: GRX350_PCIE_USB			
Size: V2765AX_V1	Document Number		Rev: 6B
Date: Friday, December 17, 2021	Sheet: 5	of 34	

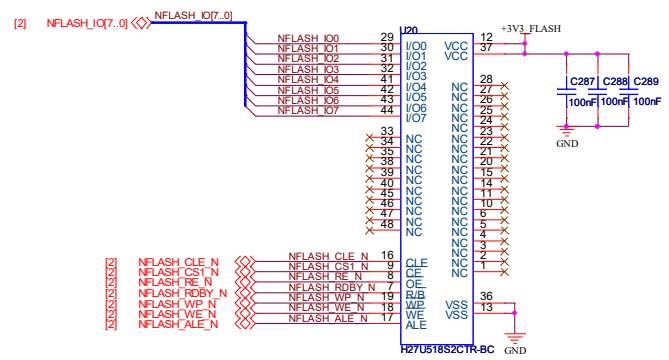


Trace capacitance for BBIO
interface must be below 10pF!
Recommend the maximum
length should be under 3 inch.

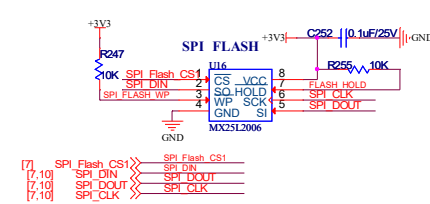
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Title		GRX350_BBIO	
Size	Document Number	Rev	
Custom	V2765AX V1	6B	
Date	Friday, December 17, 2021	Sheet	6 of 34



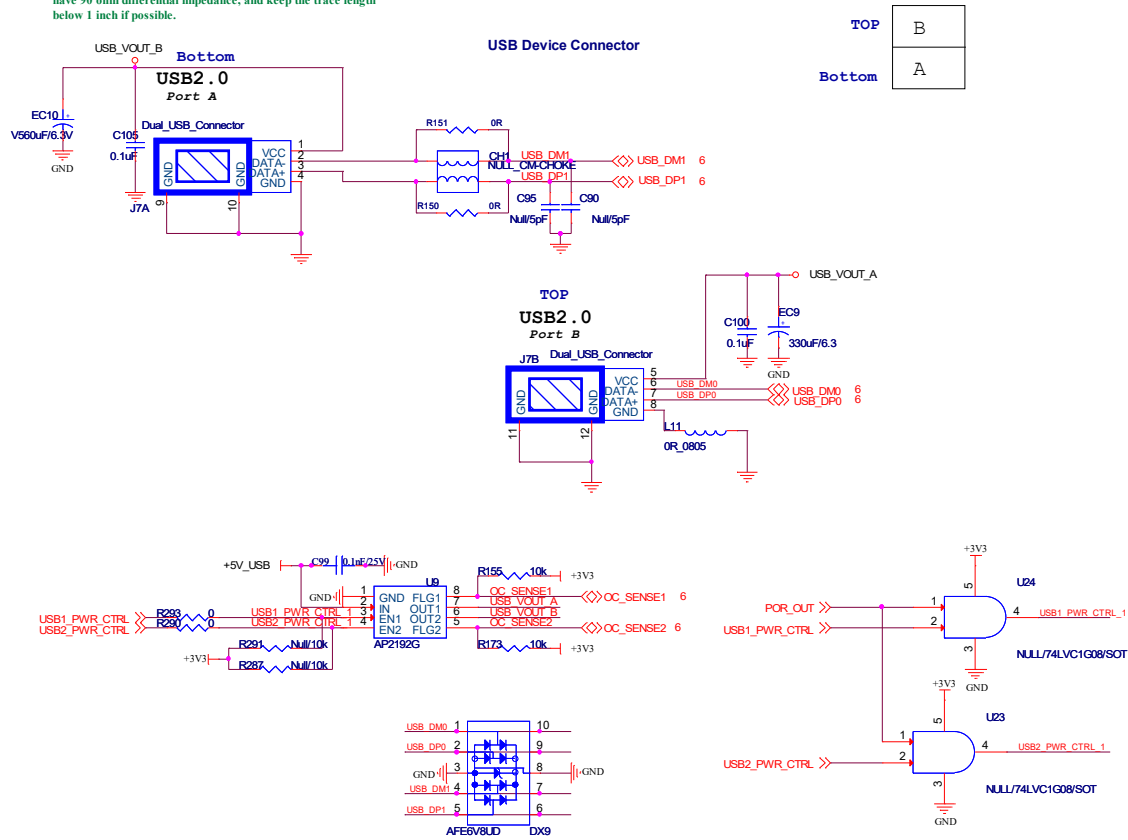
OPTION (OPTION_NAME)	OPTION4 (OPTION_NAME)	OPTION5 (OPTION_NAME)	OPTION6 (OPTION_NAME)	Book Review
0	0	0	0	OPTION name ERROR
0	0	0	1	OPTION4 name ERROR: NOT in OPTION device
0	1	0	0	OPTION name ERROR
0	1	0	1	OPTION4 or OPTION5 must be used for book device
0	1	1	0	Invalid OPTION: not in 30 pages
1	0	0	0	OPTION name ERROR
1	0	0	1	Invalid OPTION: NOT in 30 pages
1	1	0	0	OPTION name ERROR
1	1	0	1	OPTION name ERROR



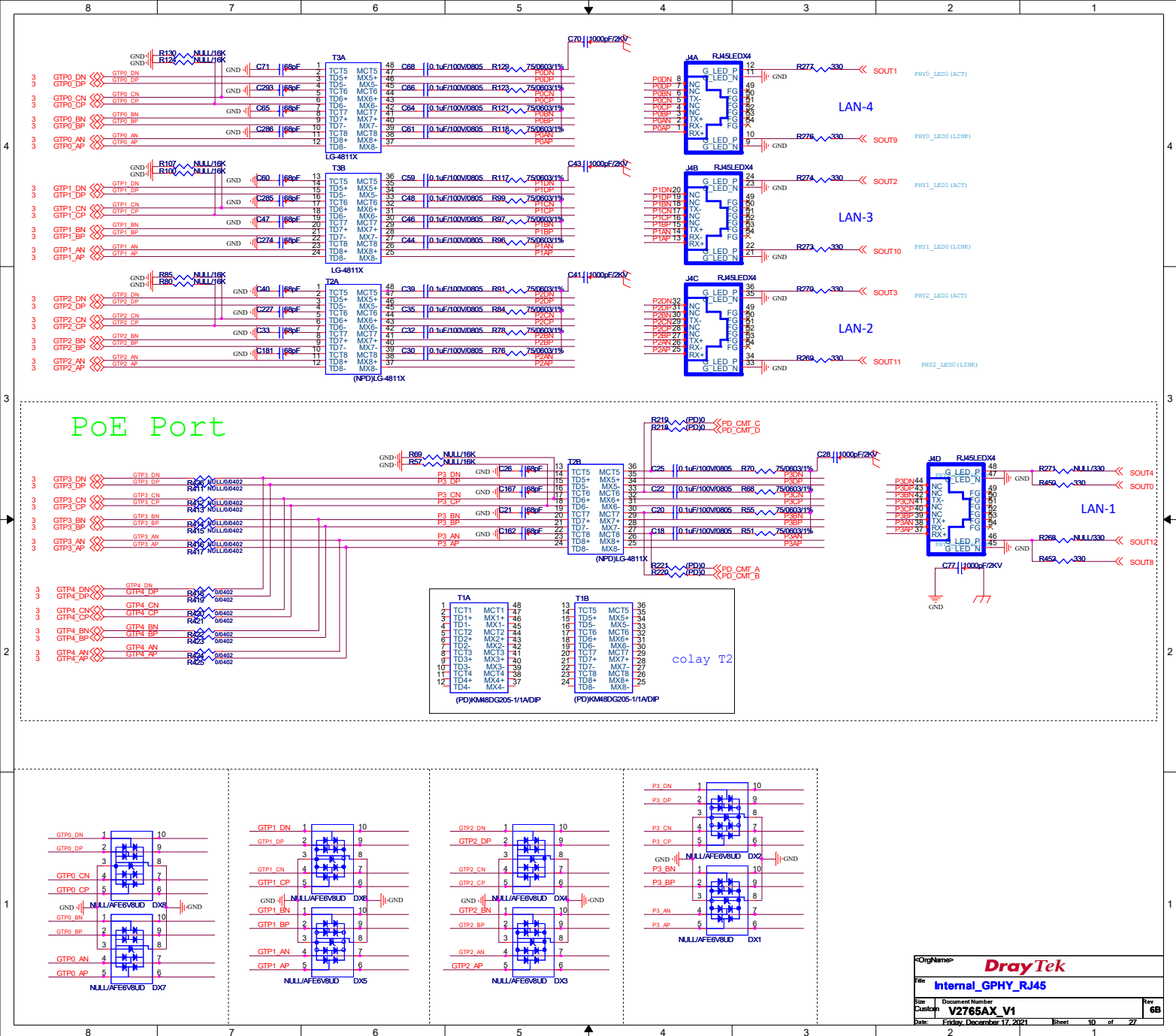
Qualified Nand Flash List	
Vendor	Model
Hynix	H27mg8, 8k
Hynix	H27u512, 512
Hynix	H27u4g82dtr, 2k
Hynix	H27u1g82btf, 2k
Samsung	K9F1208, 512
Samsung	K9M1g08u0d, 2k
Samsung	K9g4g08u0b, 2k
Samsung	K9G8G08U0C, 8k
Spansion	S34m01g100, 2k
Micron	29F64g08chaba, 8k
Micron	29F2g08chaba, 4k
Infineon	HyG3ds51280, 512
Toshiba	Th58BVG3S0HTA00, 4k



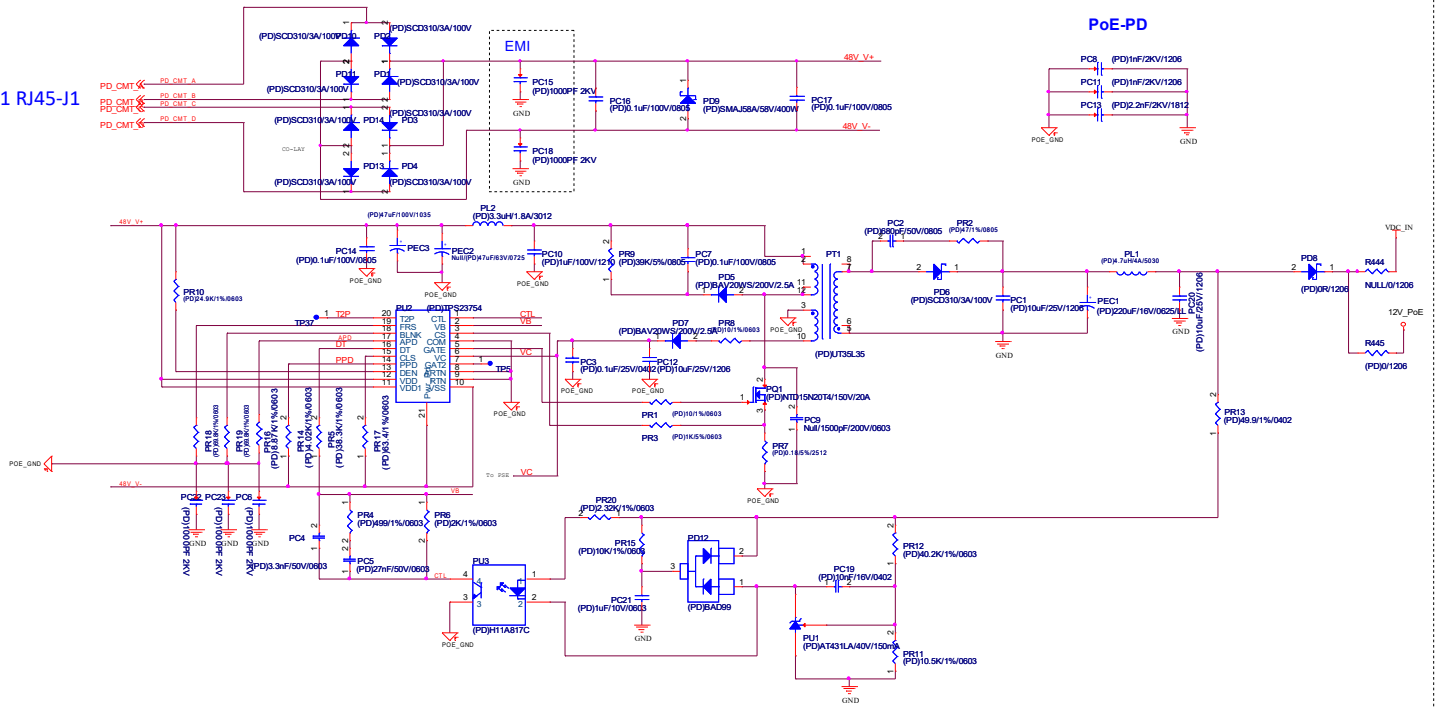
!!!Note:
The PCB layout of the differential signal DP and DM should have 90 ohm differential impedance, and keep the trace length below 1 inch if possible.



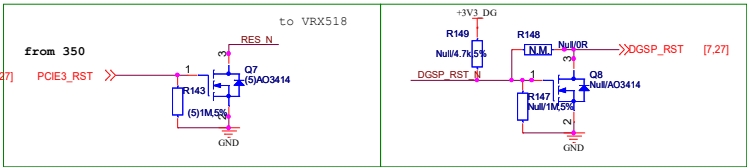
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Title		USB_Port	
Rev	Document Number	V2765AX_V1	
B		Rev	
Date: Friday, December 17, 2021		Sheet 08 of 27	

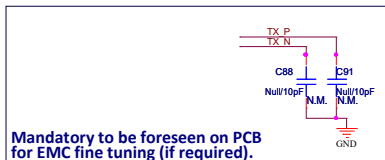
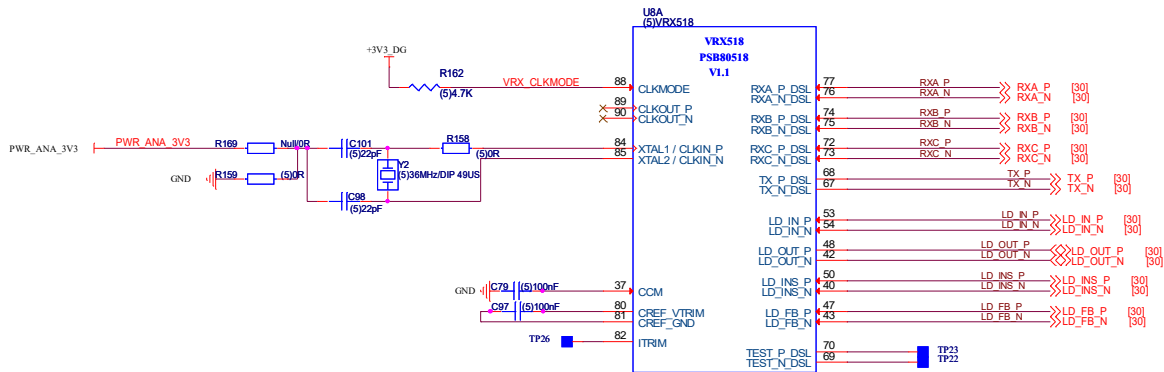


To LAN1 RJ45-J1



~OrgName~		DrayTek	
Title		POE PD	
Size	Document Number	V2765AX_V1	
C		Rev	
Date		Wednesday, December 22, 2022 18:01	
		11 of 27	

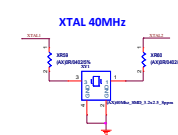
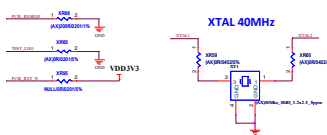
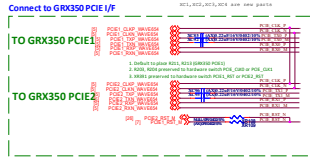
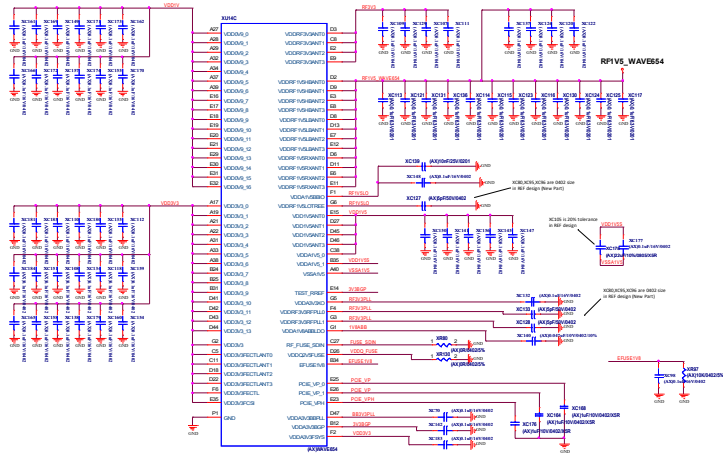
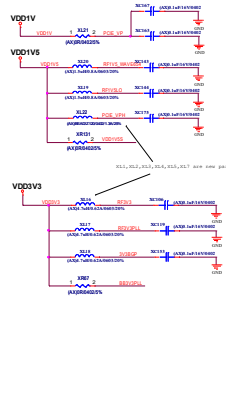




Place protection (SMBD7000 is only valid for xRX300, for xRX200-family we need DSL70) close to transformer and connect it by 1mm track width.

OrgName>		DrayTek	
Title		1st_VRX518 AFE	
Size	Document Number	Rev	
Custom	V2765AX V1	6B	
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WAVE654 PCIE / GPIO / SPI



Reserved for GP8654 Reference Design

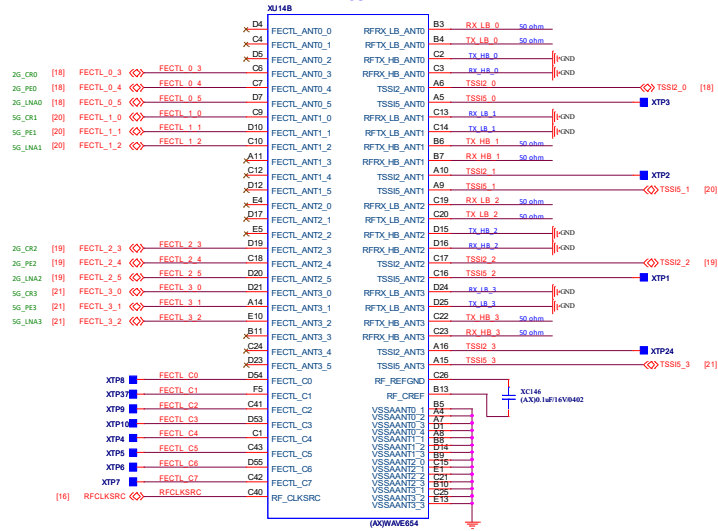
Table 32	JTAG Signals			
Ball No.	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	JTAG Reset
				Notes
				1. Low active
				2. If the JTAG interface is not in use, this pin must be connected to V _{DD}
E1	TRST	I	PU	JTAG Reset
A35	TDI	I	PU	Test Data Input
E1	TDI	I	PU	Test Data Input
TDO	TDO	O	PD	Test Data Output
				Note: pull down is needed for normal operation
E1	TDO	O	PD	Test Data Output
TMS	TMS	I		Test Mode Select
E1	TMS	I		Test Mode Select

Reserved for GP8654 Reference Design

Reserved for GP8654 Reference Design

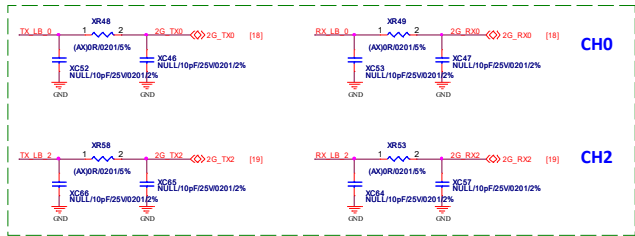
UART CONN

WAVE654 RF

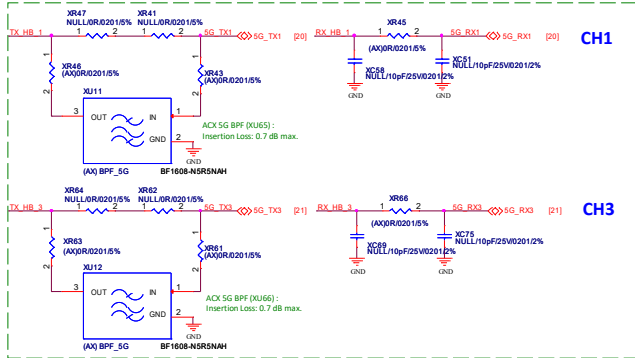


PCIE FINGER

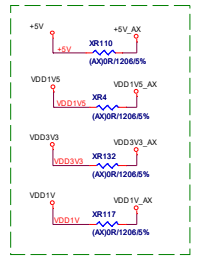
2.4G Front-End



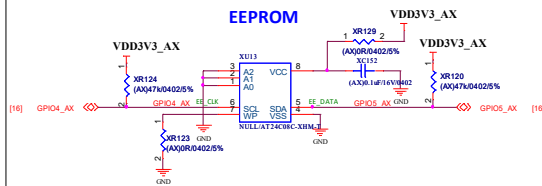
5G Front-End



Connect to main board DCDC

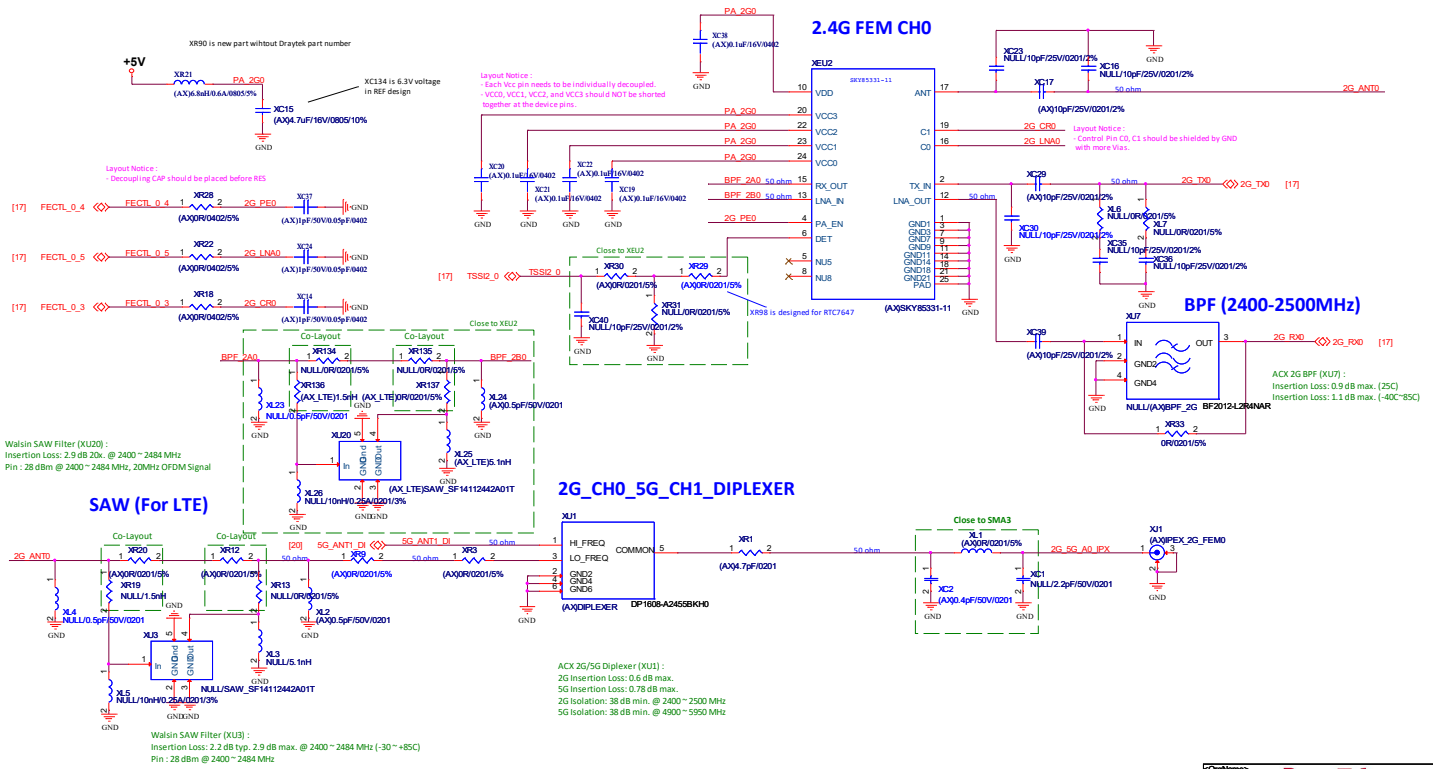


SY98004 - Vout=0.60+120K/165K=1.036V
WAVE654 Range : 0.72V ~ 1.05V



OrgName	DrayTek
Doc No	WAVE654_RF
Doc Ver	V2765AX_V1
Doc Date	2024-12-17
Doc Author	WAVE654

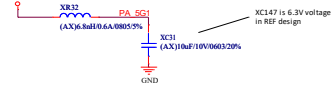
SKY85331-11:
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V



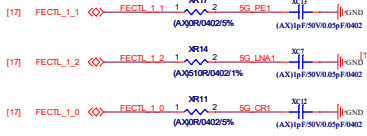
<OrgName>		DrayTek	
Title			
RF_24G_FEM_CHO			
Size	Document Number		Rev
Custom	V2765AX V1		6B
Date:	Friday, December 17, 2021		
	Rising 18 of 34		

SKY85743-31
Output power: +21 dBm, -43 dB DEVm, MCS11
Output power: +22 dBm, -40 dB DEVm, MCS11
Output power: +24 dBm, -35 dB DEVm, MCS9

XR103 is new part without Draytek part number



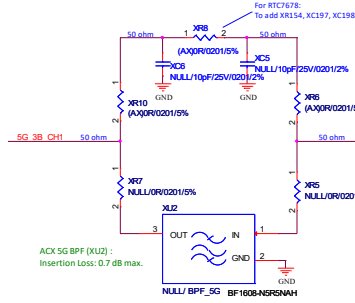
Layout Notice:
- Decoupling CAP should be placed before RES



SG_RX1

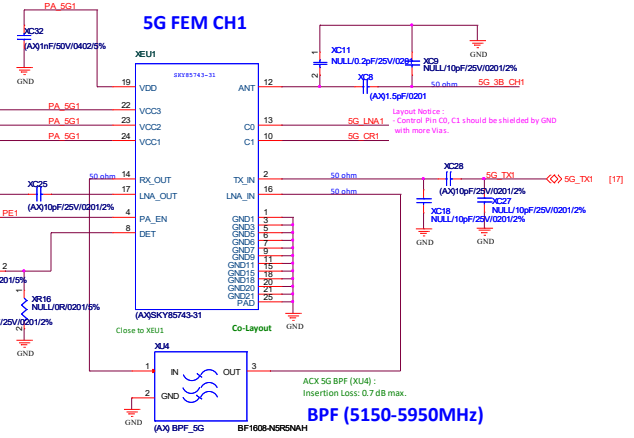
ACX 5G BPF (XU5):
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)



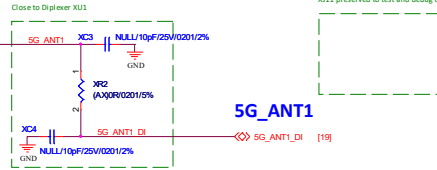
BPF (5150-5950MHz)

5G FEM CH1



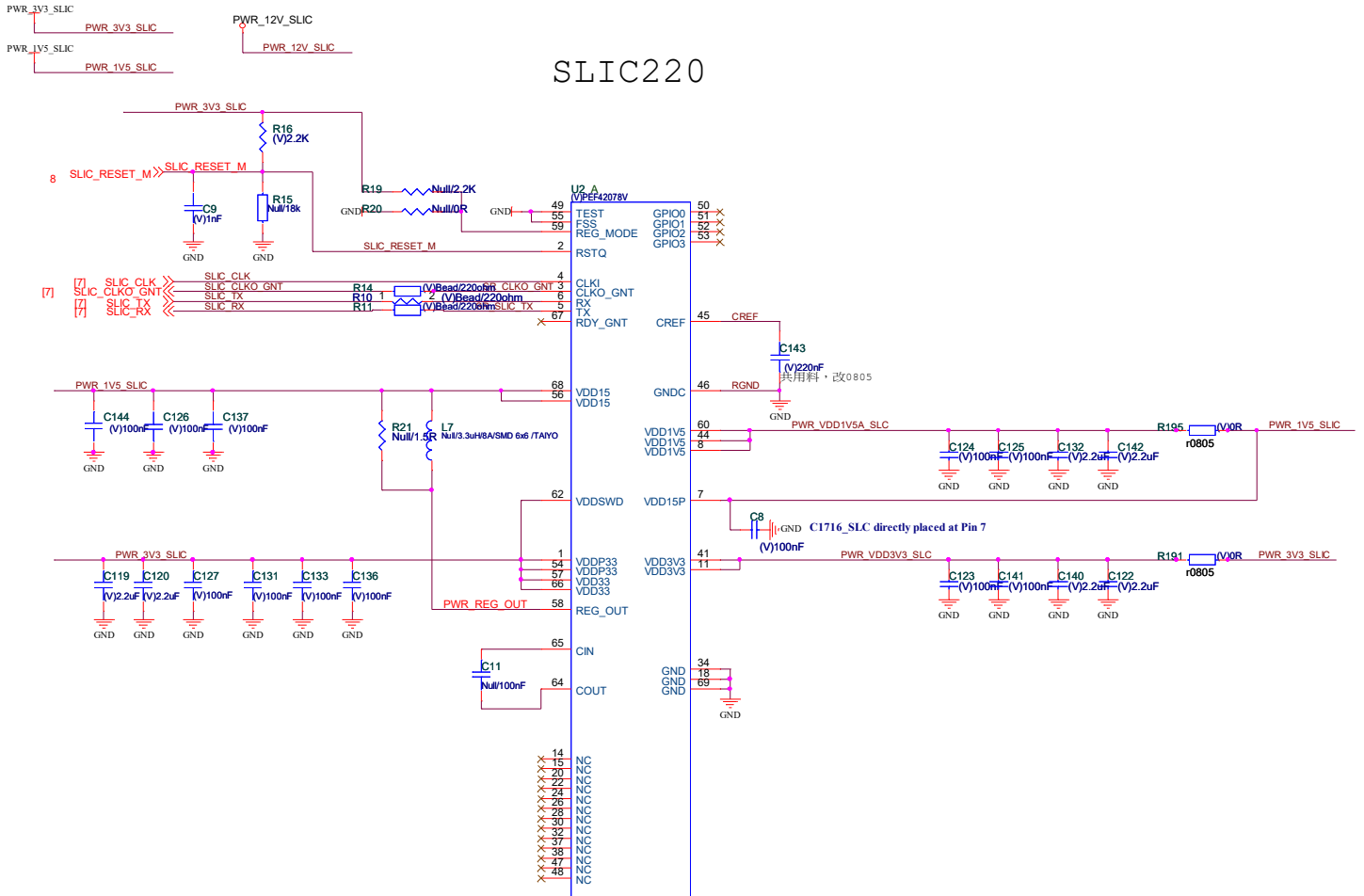
BPF (5150-5950MHz)

5G_ANT1



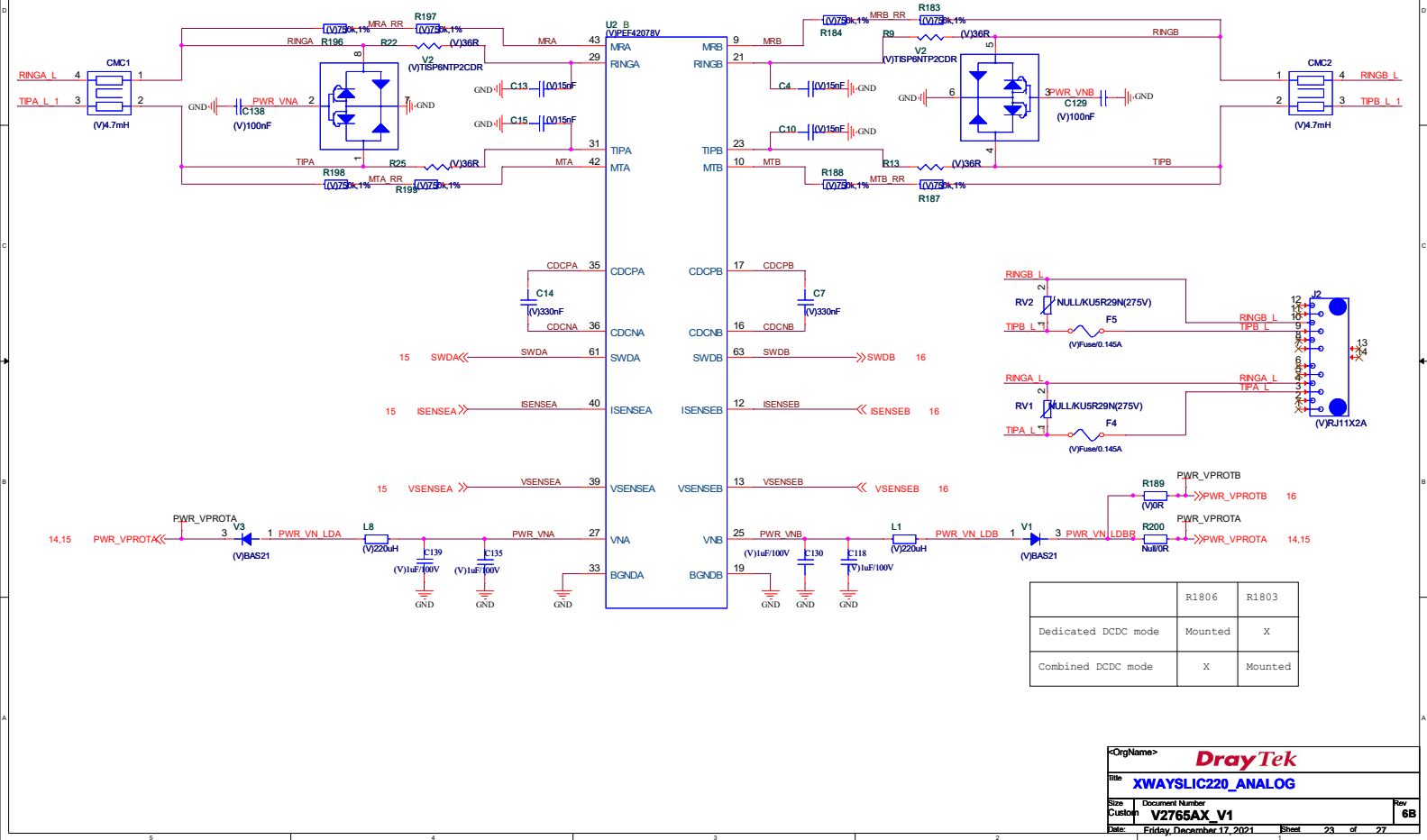
DrayTek	
RF_5G_FEM_CH1	
Size	6B
Custom	V2765AX V1
Date: Friday, December 17, 2023	

SLIC220

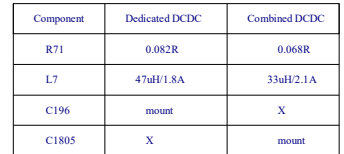


<OrgName>		DrayTek	
File		XWAYSLIC220_DIGITAL	
Size	Document Number	Rev	
Custom	V2765AX_V1	6B	
Date:	Friday, December 17, 2021	Sheet	22 of 27

SLIC220

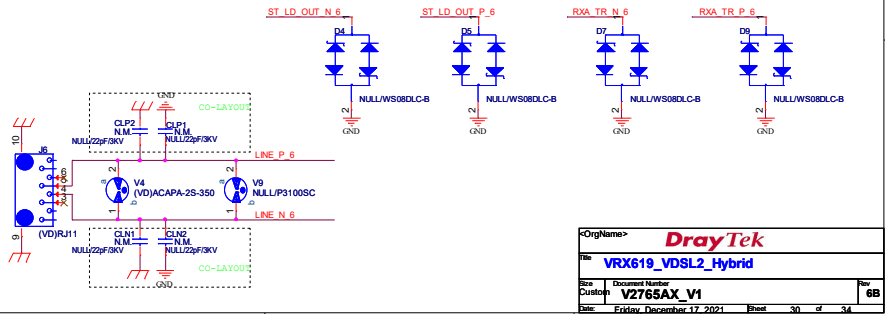
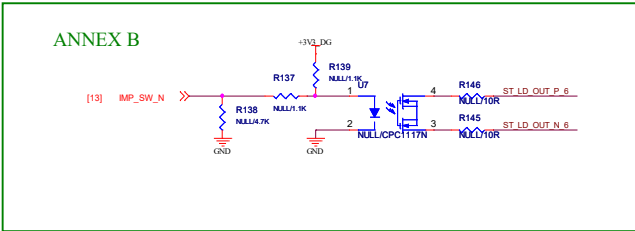
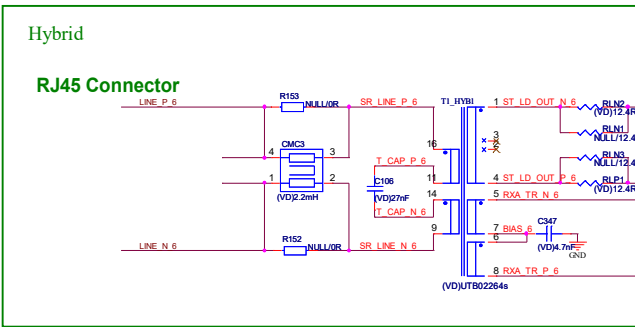
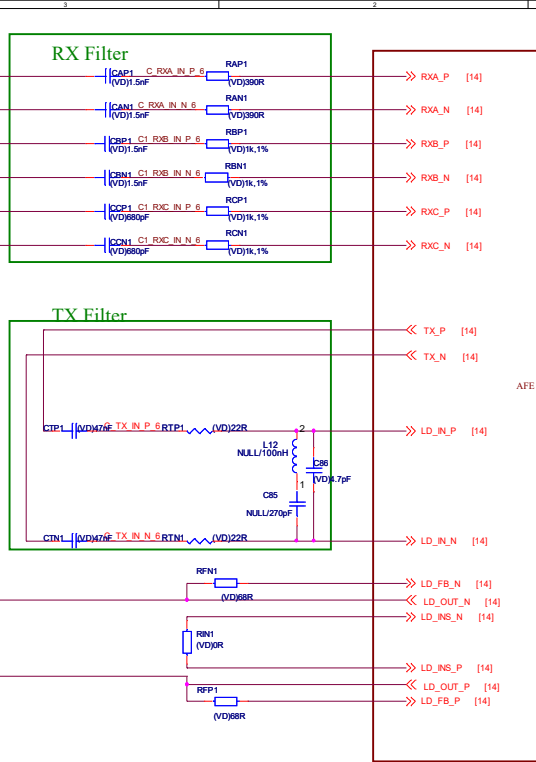
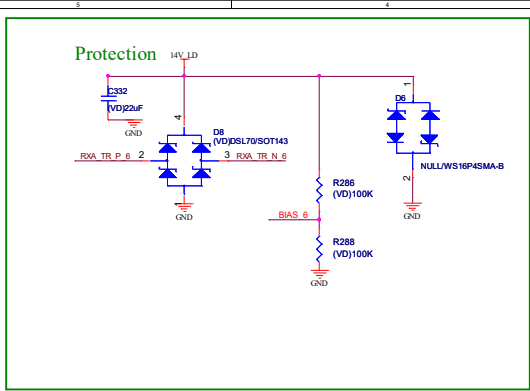


Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the relating part and the DSL must be maintain.



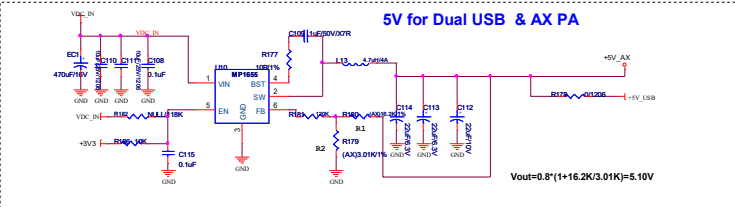
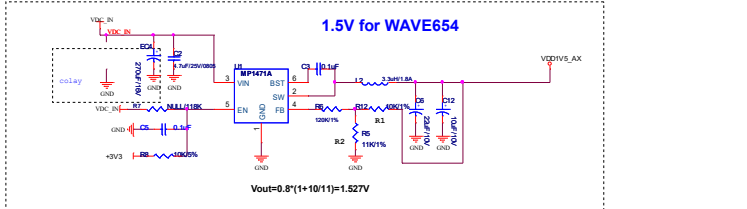
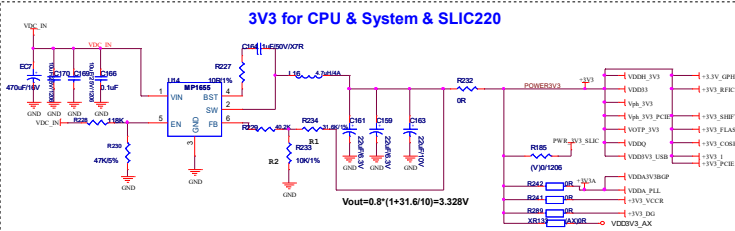
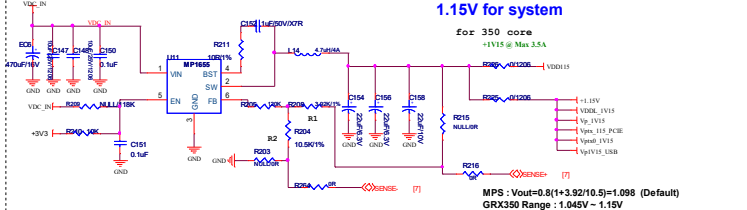
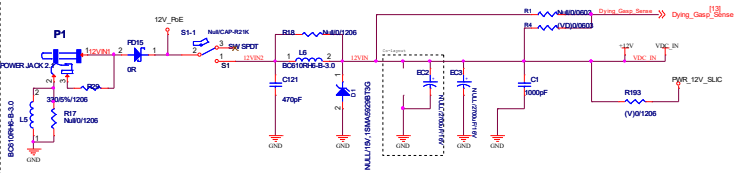
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Title U1_PNP_DCDC_T02_V11	
Size Custom	Document Number V2765AX_V1
Date: Friday, December 17, 2021	Sheet 24 of 27
Rev 6B	

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the radiating part and the DSL must be maintain.

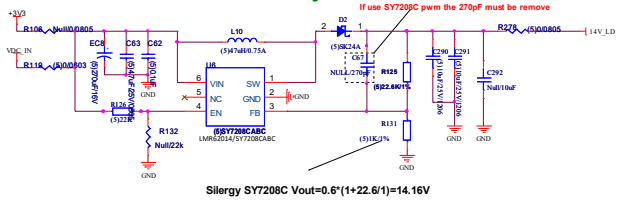


DrayTek	
File	VRX619_VDSL2_Hybrid
Size	Document Number
Custom	V2765AX_V1
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12V DC Power Input

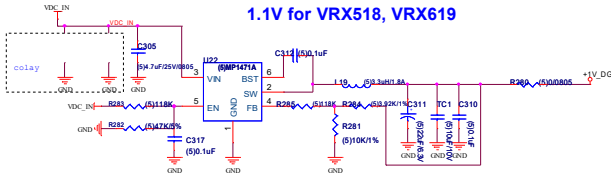


DC to DC Boost 12V to 14V circuitry

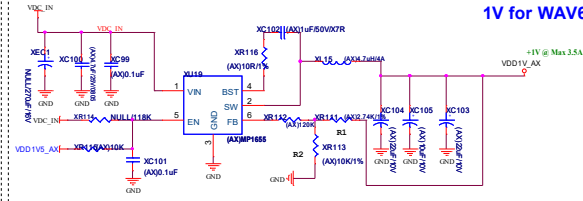


Silergy SY7208C $V_{out}=0.6 \cdot (1+22.6/1)=14.16V$

1.1V for VRX518, VRX619

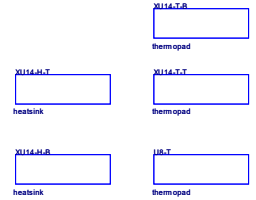
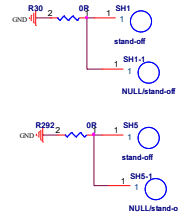
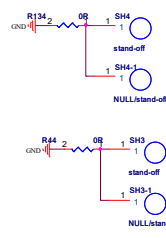
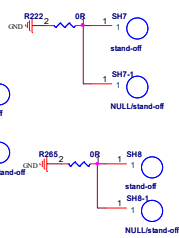
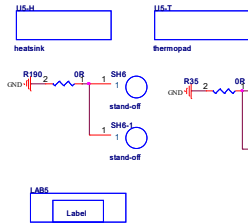
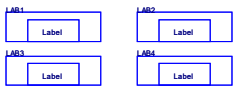
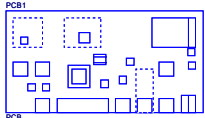
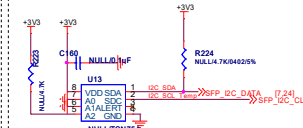

$$V_{out} = 0.8 \cdot (1 + 3.92K/10K) = 1.113V$$

1V for WAV654



MPS : $V_{out}=0.8(1+2.74/10)=1.0192$ (Default)
WAV654 Range : 0.72V ~ 1.05V

Temp sensor
I2C Addr:1001100



REVISION HISTORY

Version	Date	List of Modification	Page
V0A	2020-12-01		Ian
	2020-12-10	2.4GHz FEM (152-5331900-00G,SKY85331-11) : 1. Add XU31, XU33 2. Remove XC12, XC13, XC10, XC11 3. Null XR101, XR88, XU30, XU32 4. Place XR137, XR136 5. Remove XR146, XR149, XR142, XR145 5GHz FEM (152-5743900-00G,SKY85743-31) : 1. Add XU51, XU53 for co-layout with XU52, XU54 2. Remove XR117, XR115, XC16, XC17 3. Remove XR118, XR129, XC181, XC182 4. Place XR11, XR12 6. Null XU61, XR10, XR135 7. Place XR139, XR140 8. Null XU63, XR138, XR141	mChen
V6B	2021-11-26	1. C332,C302 change to C1206 2. colay INT_GPHY-TP6F circuit 3. NULL XC90; XC89 change 1.5PF; XR1,XR71 change 4.7pF 4. add J9, FD15, R445, R444 5. XC15,XC59 change to C0805 6. J6 change to 8 pin RJ45	Ian

<OrgName>

DrayTek

Title

History

Size

Document Number

Rev

Custom

V2765AX_V1

6B

Date:

Friday, December 17, 2021

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BOM Difference

	V2765ax	V2765Vax							
(VD)	V	V							
(V)	NULL	V							
(5)	V	V							
(PD)	NULL	NULL							
(AX)	V	V							
(NPD)	V	V							
(AX_LTE)	NULL	NULL							