

1. 100 ohm characteristic impedance control for TPI differential signal routing. Keep the reference plane of signal continuous.

2. The TPI signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.

An external Rcal 16K ohm +/-1% resistor should be connect from the RCAL pin to ground. Place the Rcal resistor close to RCAL ball.

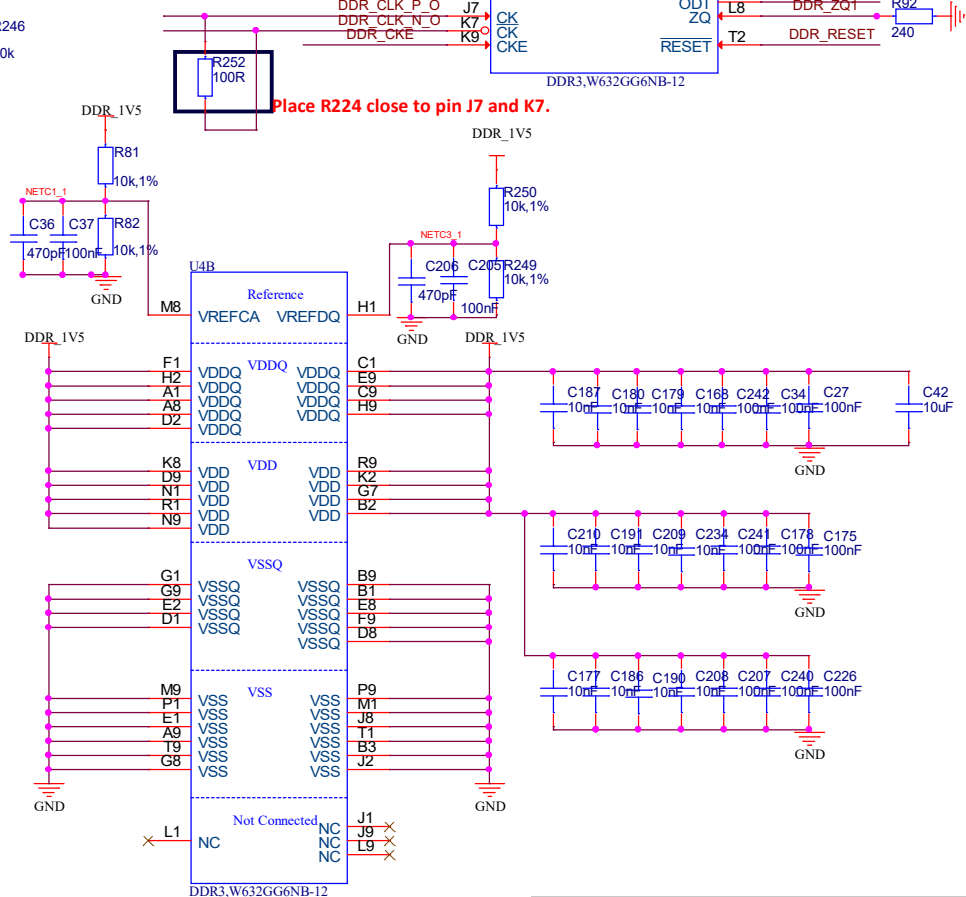
1. Defines FL_CS1 (GPIO23) as only CS for a Parallel NAND Flash.
2. FL_RDBY and FL_WP pull high by 10K ohm resistor.
3. Add bypass capacitors for the power supply pins of NAND Flash and place them closer to power supply pins.
4. Leave all NAND Flash signals away from high-speed digital signals, analog signals, and power traces.

1. Add 24.9 ohm serial resistor on RGMII TX signals (TXCLK, TXCTL, TXD0TXD3) near GRX350

2. 50 ohm impedance for RGMII signal routing. Keep the reference plane of RGMII signal continuous.

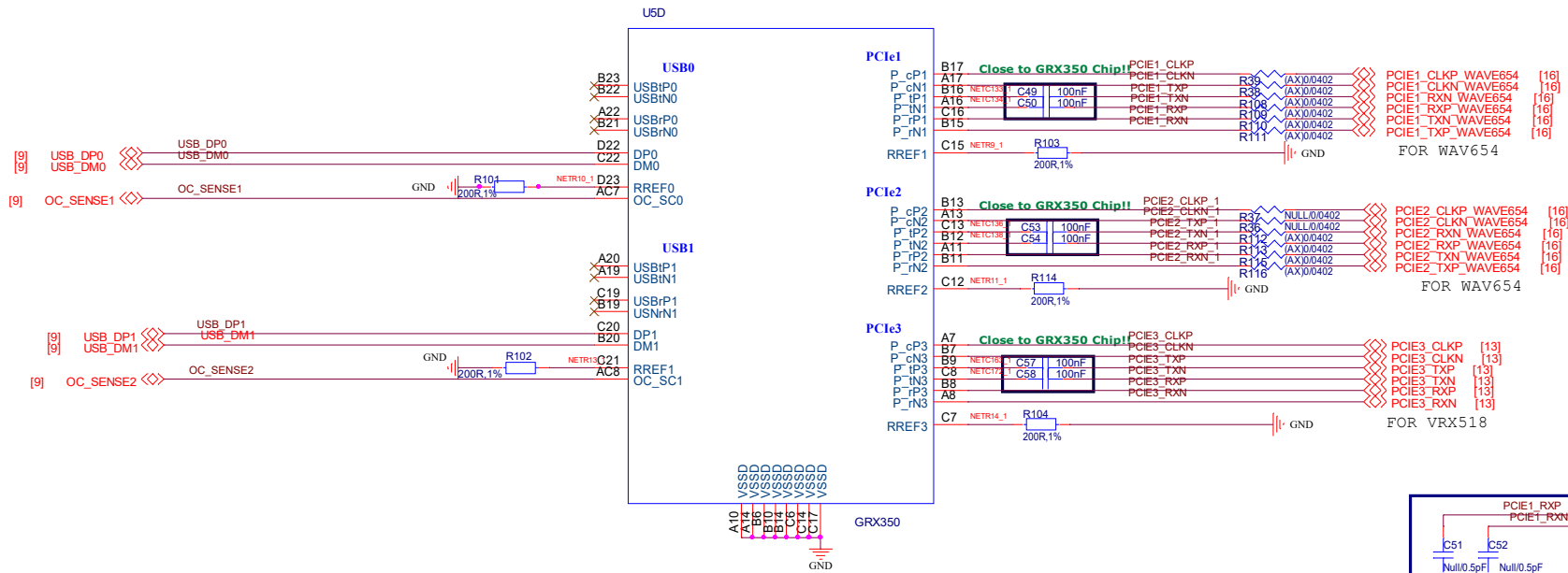
3. The RGMII RX/TX signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.

"1" for VRX518 detect
"0" for VRX618 detect



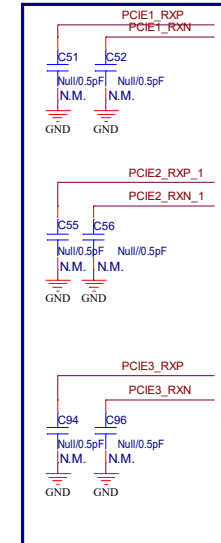
Etron: EM6GC16EWD-10H (64Mx16bit, single rank (CS0))
 Micron: MT41K128M16JT-125:K (128Mx16bit, single rank (CS0))
 Micron: MT41K256M16HA-125 IT:E (256Mx16bit, single rank (CS0))
 Winbond: W634GG6LB-12 (256Mx16bit, single rank (CS0))
 Etron: EM6GE16EWC-10H (256Mx16bit, single rank (CS0))
 Nanya: TS5CB256M16DP-EK (256Mx16bit, single rank (CS0))
 Micron: MT41K512M16HA-125:A (512Mx16bit, single rank (CS0))

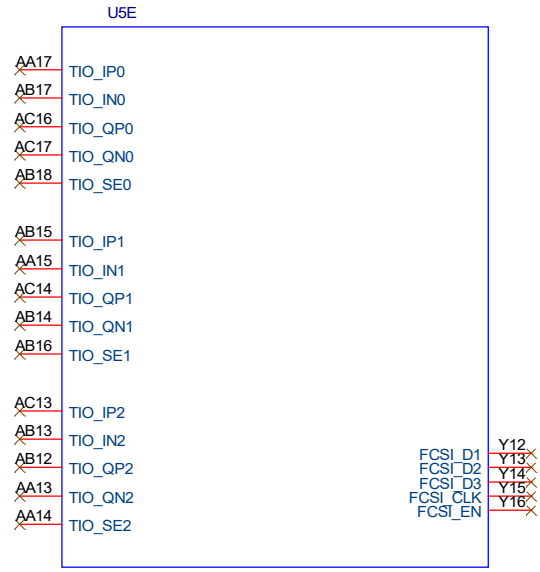
- | | |
|---|--|
| <div> <div><OrigName></div> <div>DrayTek</div> </div> | |
| <div> <div>Title</div> <div>GRX350_DDR3_x16</div> </div> | |
| <div> <div>Size Custom</div> <div>Document Number</div> </div> | <div> <div>V2766AX</div> <div>Rev</div> </div> |
| <div> <div>Date:</div> <div>Thursday, July 21, 2022</div> </div> | <div> <div>Sheet</div> <div>3</div> <div>of</div> <div>34</div> </div> |



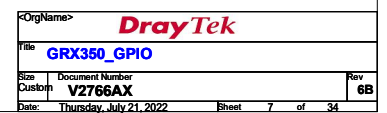
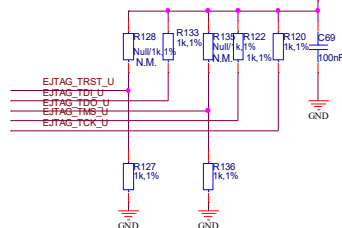
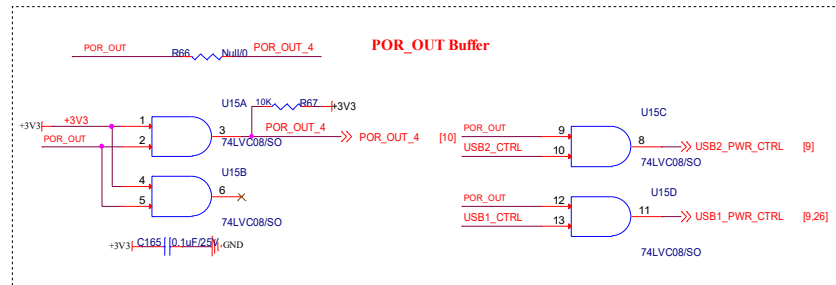
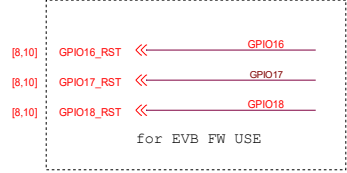
1. An external Rref 200 ohm $\pm$ 1% resistor should be connect from the USB RREF0, RREF1 pins to ground. Place the Rref resistor close to RREF balls.
2. Place 2 AC coupling capacitors on USB TX pairs , <0.5inch length to GRX350 is recommended.
3. 90 ohm characteristic impedance control for USB differential signal routing. Keep the reference plane of signal continuous.
4. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.
5. Populate sufficient GND vias nearby each PCIe differential pairs to tighten adjacent GND plane with GND layer.

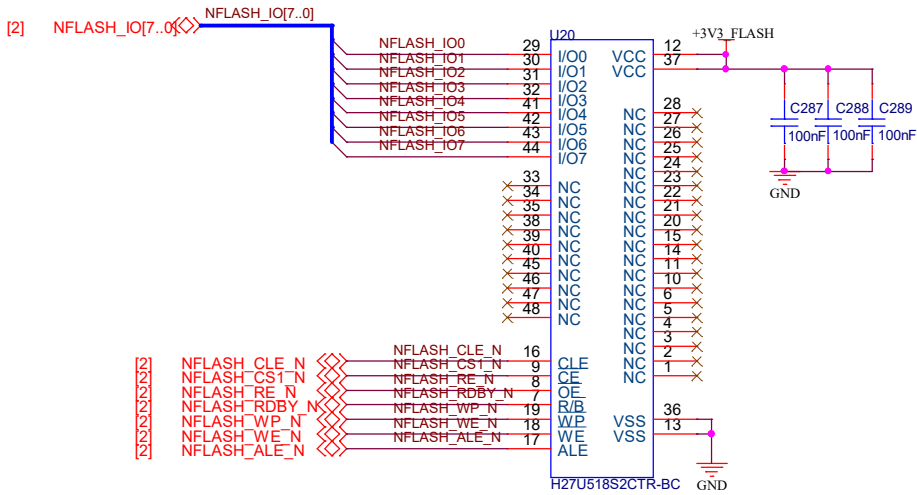
1. An external Rref 200 ohm $\pm$ 1% resistor should be connect from the 3 PCIe RREF pins to ground. Place the Rref resistors close to RREF balls.
2. Place 2 AC coupling capacitors on PCIe TX pairs , <0.5inch length to GRX350 is recommended.
3. 100 ohm characteristic impedance control for differential signal routing. Keep the reference plane of signal continuous.
4. In case with ≥ 2 PCIe differential pairs routing on PCB, a footprint of shielding case to enclose all these differential pairs is highly recommended for the compliance of EN300-328 V1.8.1 standard.
5. 0.5pF capacitors to ground on PCIe RX pairs, place them close to GRX350.
6. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.
7. Populate sufficient GND vias nearby each PCIe differential pairs to tighten adjacent GND plane with GND layer.



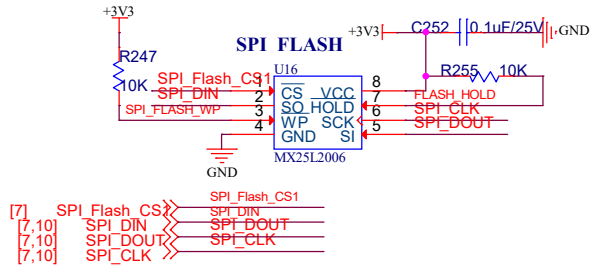


Trace capacitance for BBIO
interface must be below 10pF!
Recommend the maximum
length should be under 3 inch.



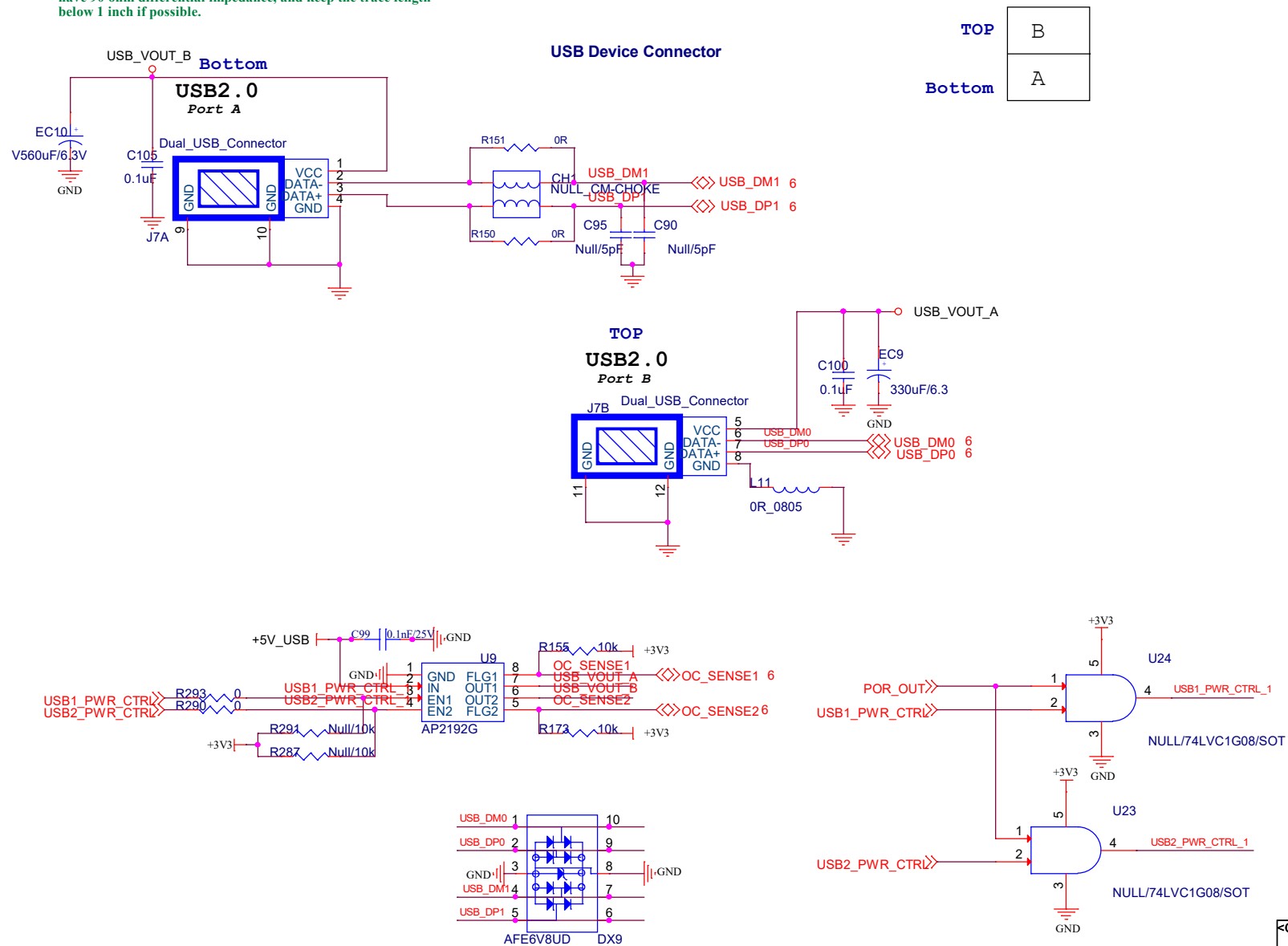


Qualified Nand Flash List	
Vendor	Model
Hynix	H27uag8, 8k
Hynix	H27u512, 512
Hynix	H27u4g8f2dtr, 2k
Hynix	H27u1g8f2btf, 2k
Samsung	K9F1208, 512
Samsung	K9f1g08u0d, 2k
Samsung	K9g4g08u0b, 2k
Samsung	K9G8G08U0C, 8k
Spansion	S34ml01g100, 2k
Mircon	29f64g08cbaca, 8k
Mircon	29f32g08cbaca, 4k
Infineon	Hyf33ds51280, 512
Toshiba	Th58BVG3S0HTA00, 4k

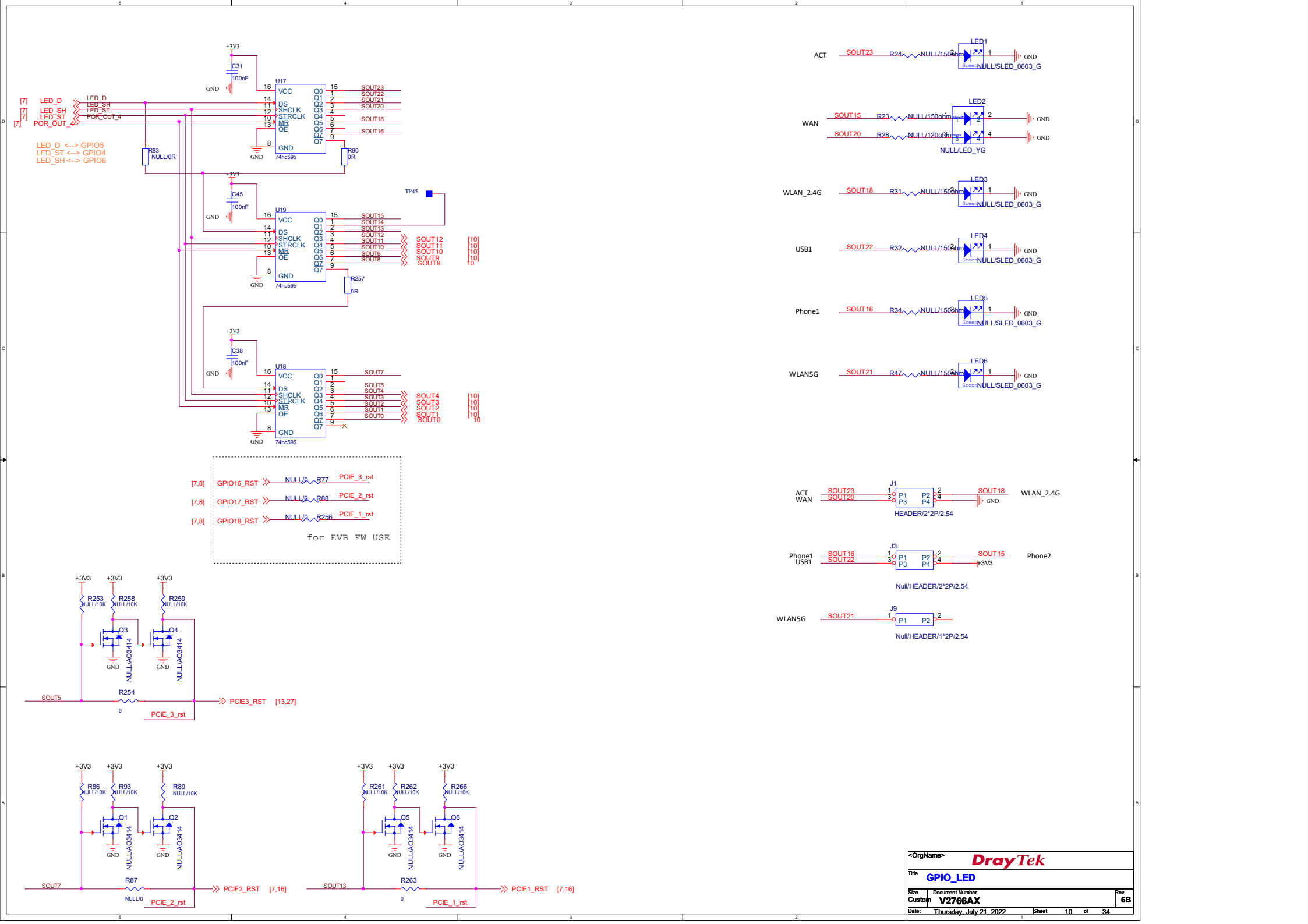


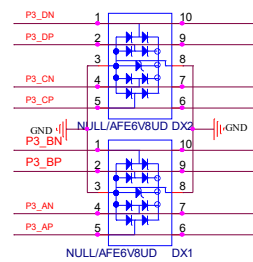
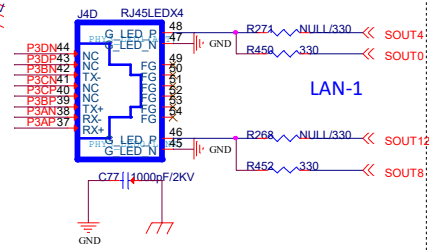
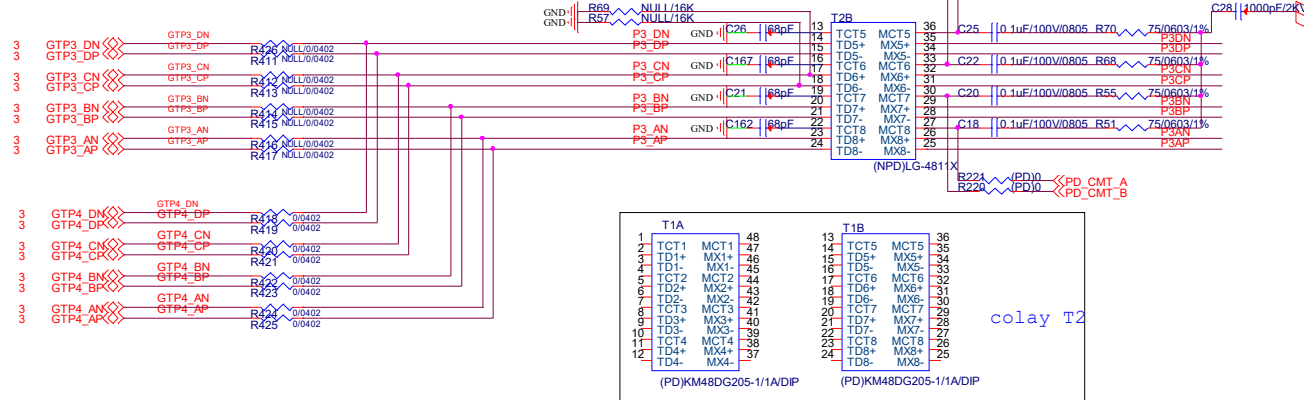
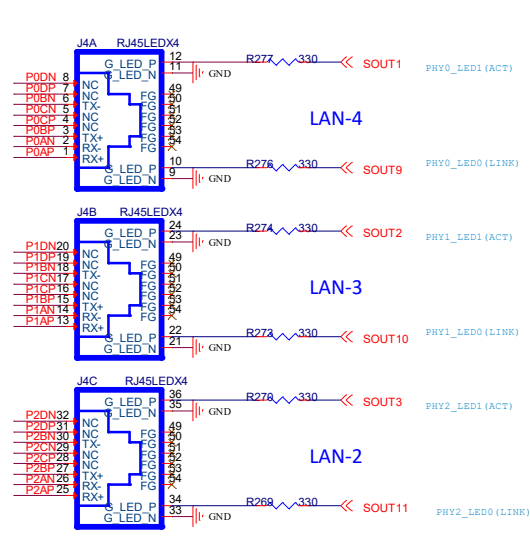
<OrgName>		DrayTek	
Title		NAND_FLASH	
Size	Document Number	Rev	
B	V2766AX	6B	
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!!Note:
The PCB layout of the differential signal DP and DM should have 90 ohm differential impedance, and keep the trace length below 1 inch if possible.

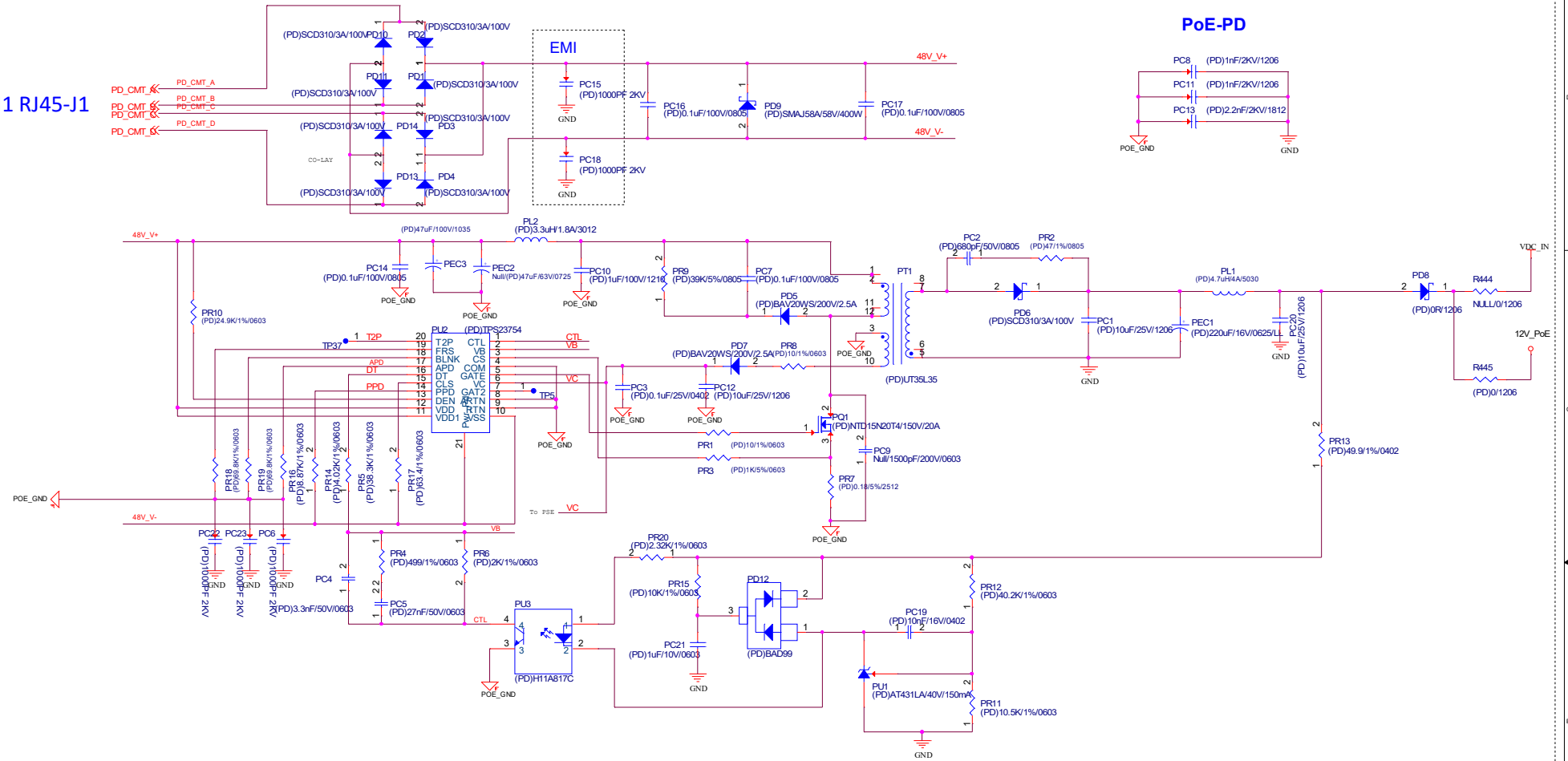


<OrgName> DrayTek	
Title USB_Port	
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To LAN1 RJ45-J1



[illegible]

SY88004 - Vout=0.61±120K/165K±1.036V WAV654 Range : 0.72V~ 1.05V				
Table 32 JTAG Signals				
Ball No.	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	JTAG Reset
				Notes 1. Low active; 2. If the JTAG interface is not in use, this pin must be connected to V _{ss}
	EJ_TRST	I	PU	EJTAG Reset
A35	TDI	I	PU	Test Data Input
	EJ_TDI	I		EJTAG Test Data Input
B33	TDO	O	PD	Test Data Output
				<i>Note: pull down is needed for normal operation.</i>
	EJ_TDO	O		EJTAG Test Data Output
B29	TMS	I	–	Test Mode Select
	EJ_TMS	I		EJTAG Mode Select

Ball No	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	JTAG Reset Notes 1. Low active. 2. If the JTAG interface is not in use, this pin must be connected to V_{SS} .
	EJ_TRST	I	PU	EJTAG Reset
A35	TDI	I	PU	Test Data Input
	EJ_TDI	I	PU	EJTAG Test Data Input
B33	TDO	O	PD	Test Data Output Note: pull down is needed for normal operation.
	EJ_TDO	O	PD	EJTAG Test Data Output
B29	TMS	I	–	Test Mode Select
	EJ_TMS	I	–	EJTAG Mode Select

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UART CONN

PCIE FINGER

Four circuit diagrams for channel 19 (CH19) are shown, arranged in a 2x2 grid. Each diagram represents a different signal path (TX or RX) for a specific channel. The top row shows the TX path for channel 19 (TX_TB_0) and the RX path for channel 19 (RX_LB_0). The bottom row shows the TX path for channel 19 (TX_LB_2) and the RX path for channel 19 (RX_LB_2). Each diagram includes a 10pF capacitor to ground and a 25V/0.021/12% capacitor in parallel with the main signal line. The components are labeled with their respective part numbers and values.

CH1

TX_HB_1 1 2 1 2 5G_TX1 5G_TX1 [20] RX_HB_1 1 2 5G_RX1 5G_RX1 [20]

XUR47 NULL0R/0201/5% XUR41 NULL0R/0201/5% XUR46 (AX)0R/0201/5% XUR43 (AX)0R/0201/5%

XU11 ACX 5G BPF (XU65) : Insertion Loss: 0.7 dB max.

(AX) BPF_5G BF1608-N5R5NAH

CH3

TX_HB_3 1 2 1 2 5G_TX3 5G_TX3 [21] RX_HB_3 1 2 5G_RX3 5G_RX3 [21]

XUR64 NULL0R/0201/5% XUR62 NULL0R/0201/5% XUR63 (AX)0R/0201/5% XUR61 (AX)0R/0201/5%

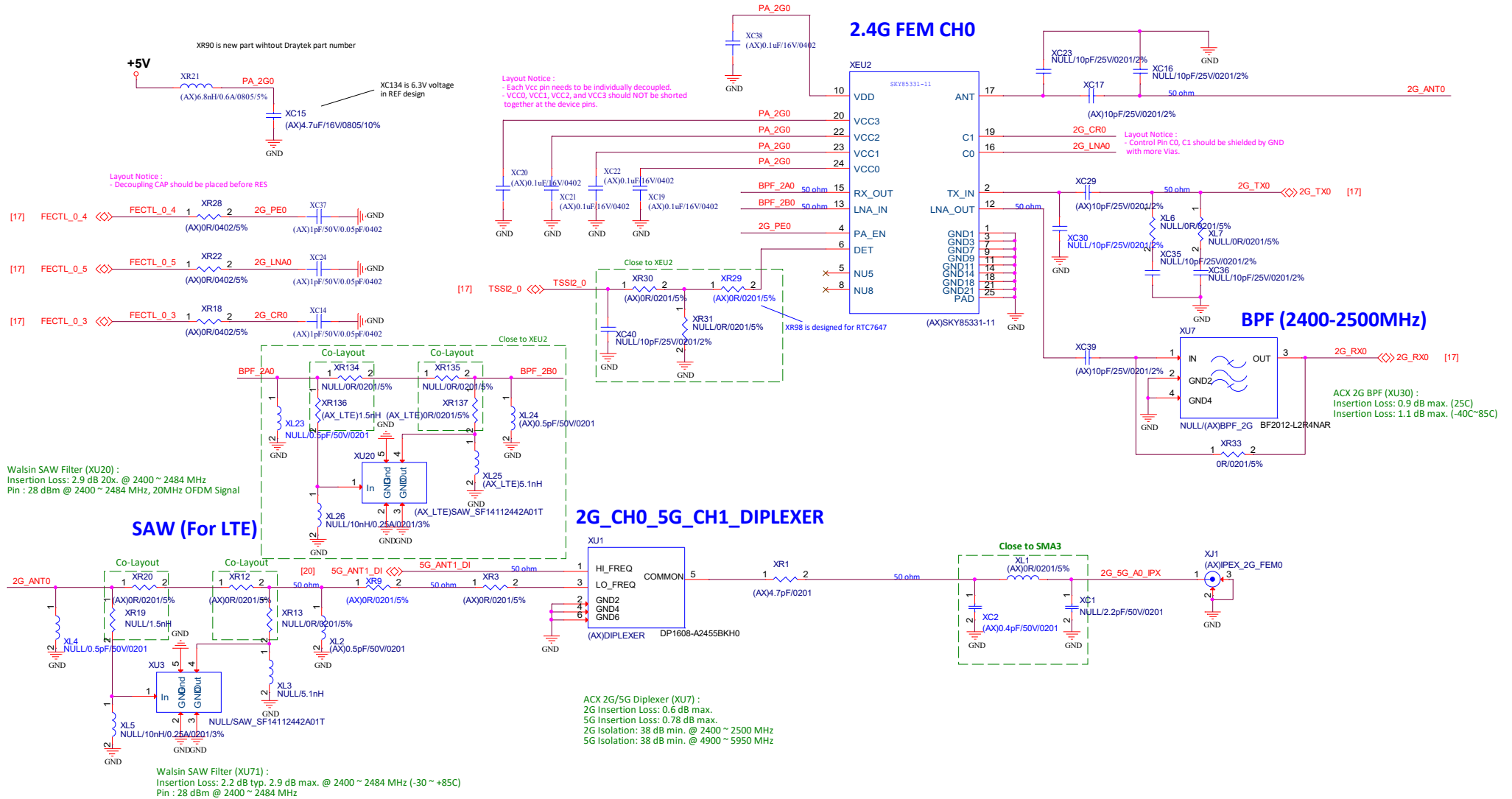
XU12 ACX 5G BPF (XU66) : Insertion Loss: 0.7 dB max.

(AX) BPF_5G BF1608-N5R5NAH

The schematic diagram illustrates a resistor network with four resistors: XR110, XR4, XR132, and XR117. The input voltages are +5V and VDD1V5, and the output voltages are +5V_AX and VDD1V5_AX. The resistors are connected in a bridge-like configuration, with the output voltages being a fraction of the input voltages. The resistors are labeled with their values and tolerance: (X)J0R1206/5%.

[illegible]

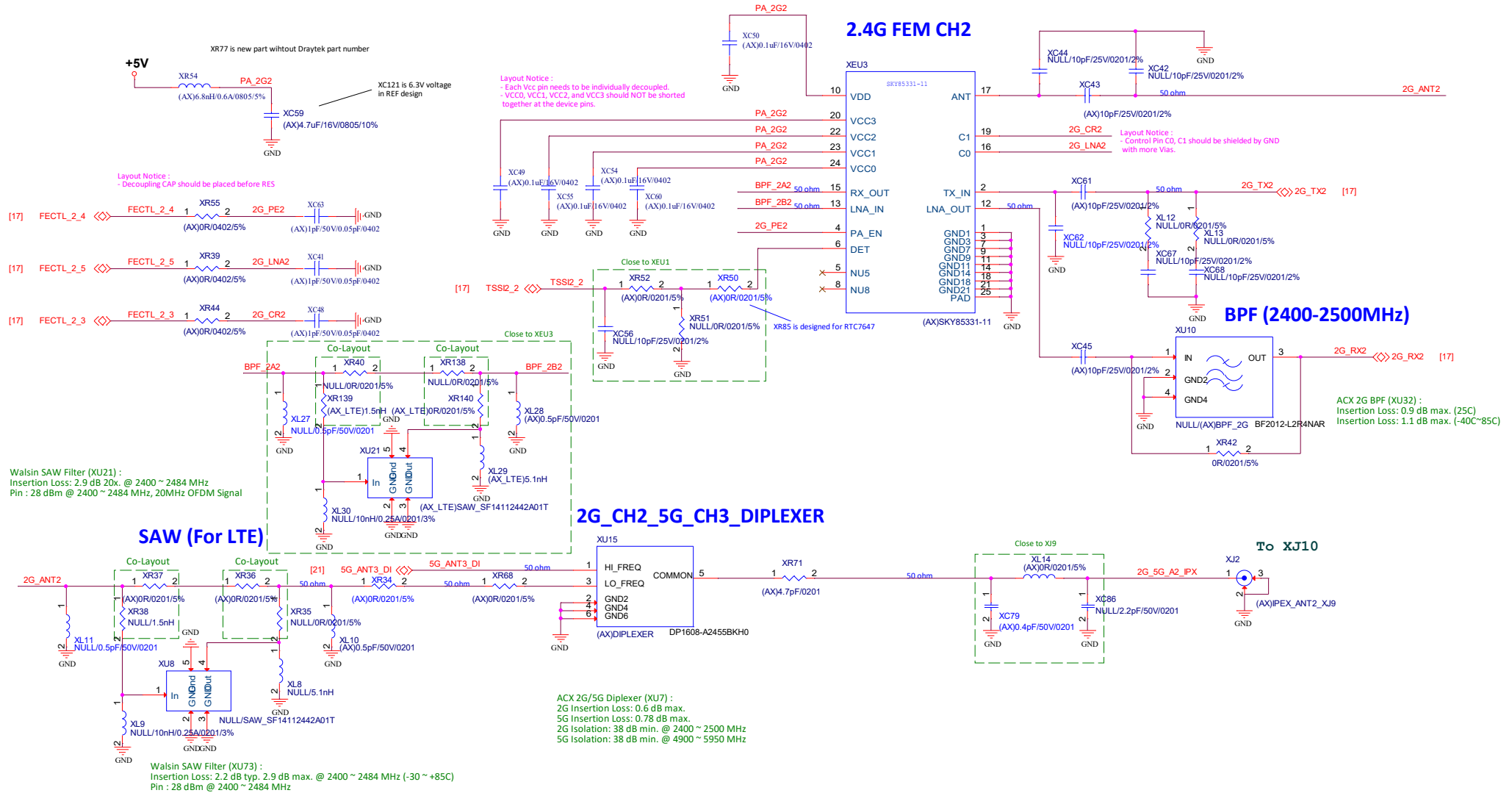
SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V



<OrgName>		DrayTek	
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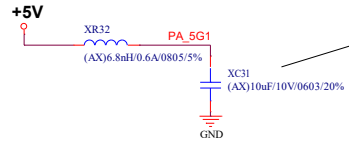
SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V

2.4G FEM CH2

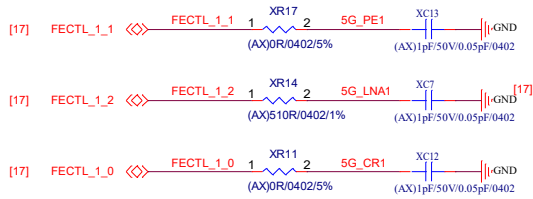


<OrgName>		DrayTek	
Title		RF_2.4G_FEM_CH2	
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XR103 is new part without Drytek part number

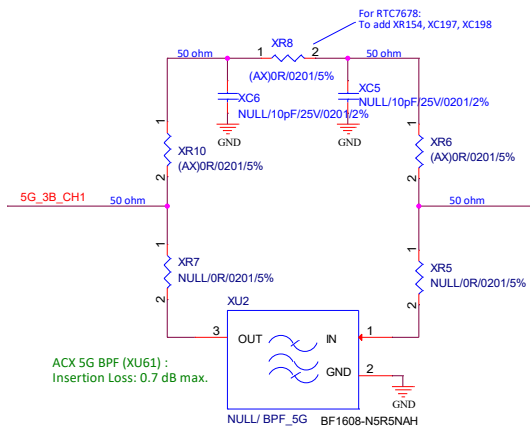


Layout Notice :
- Decoupling CAP should be placed before RES



ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)

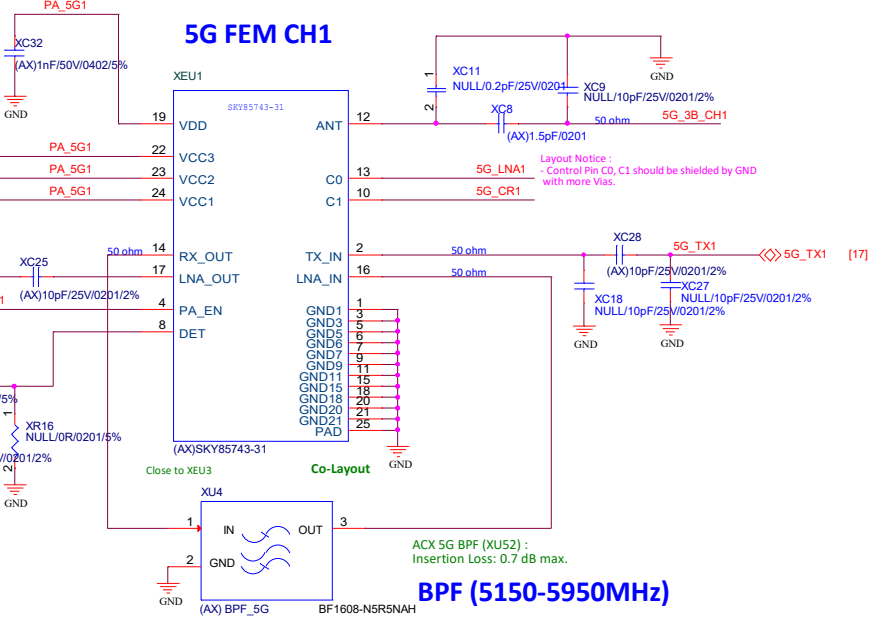


ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)

SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9

5G FEM CH1



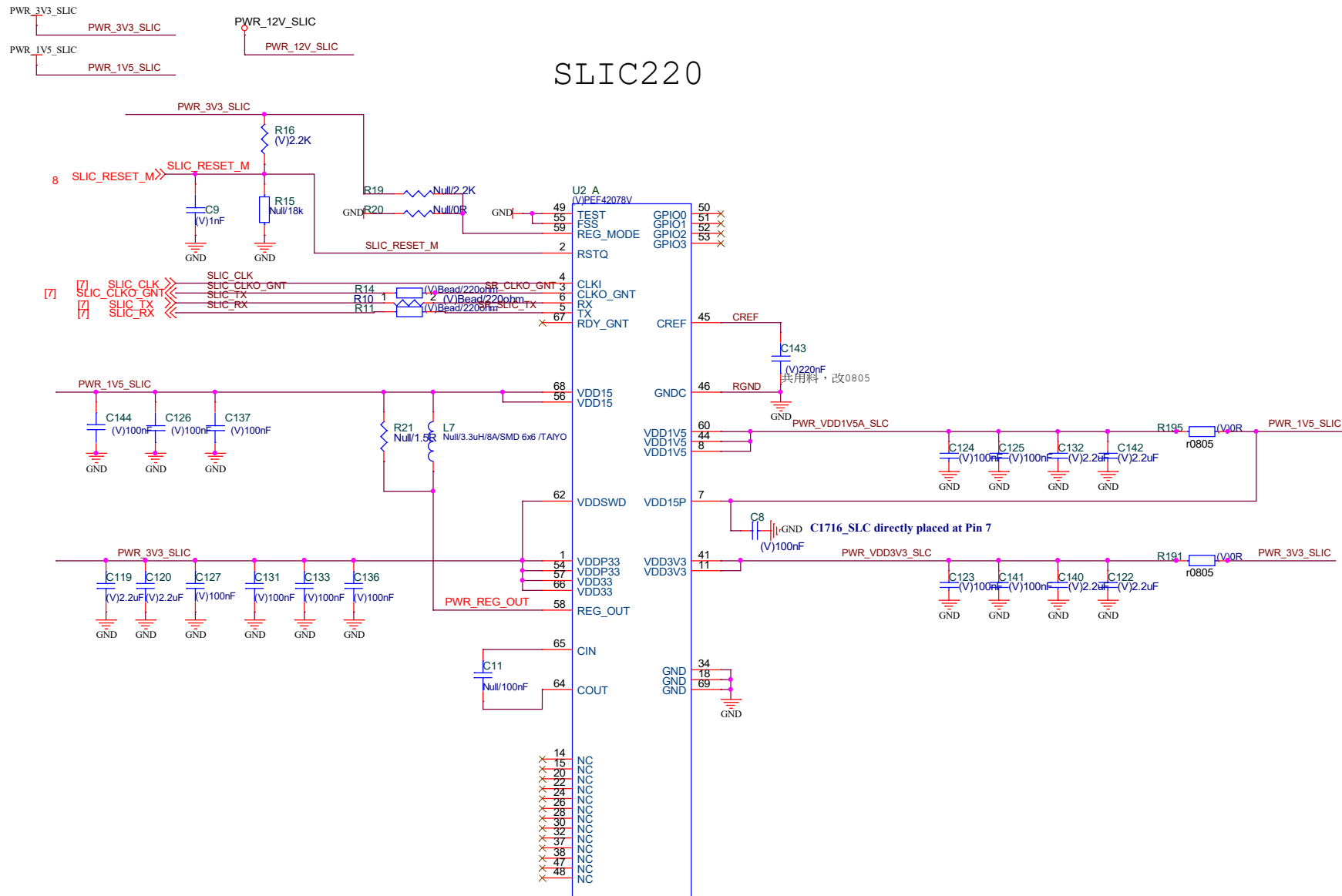
BPF (5150-5950MHz)

XU11 preserved to test and debug only

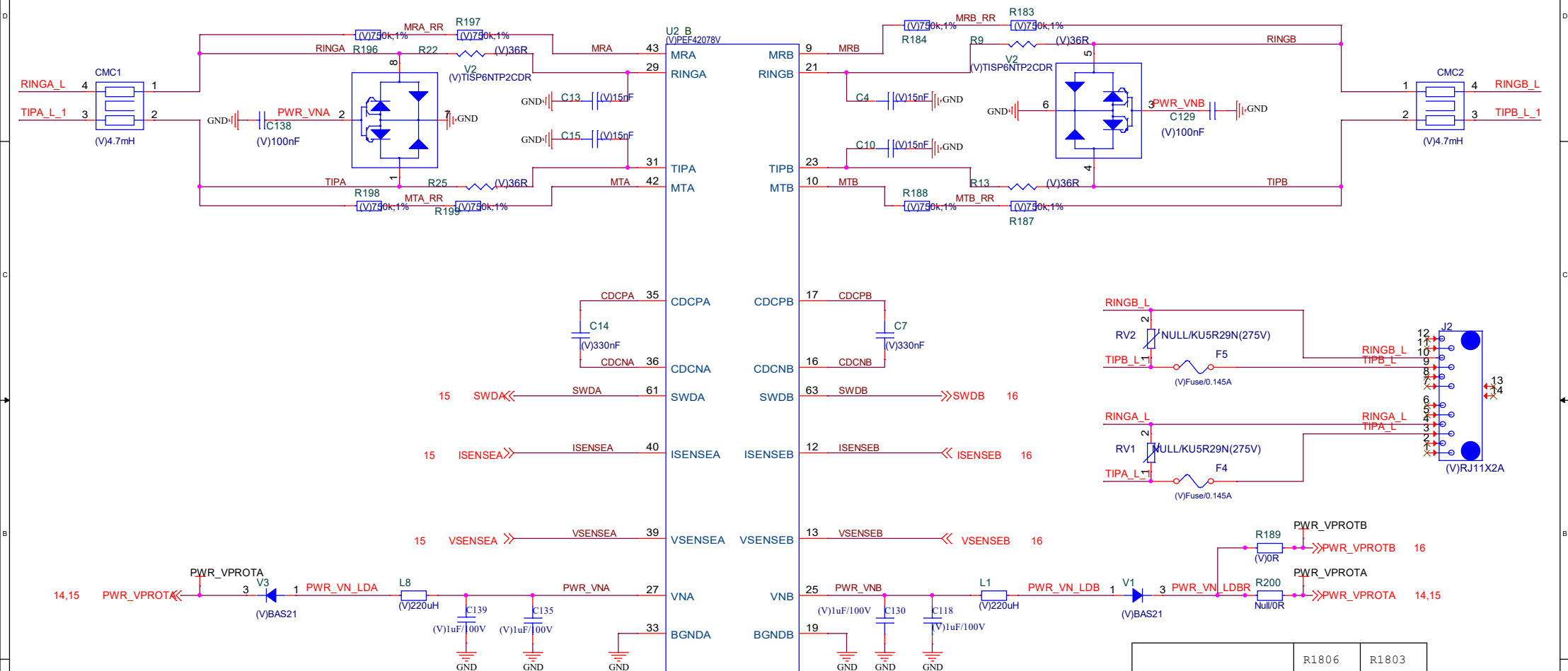
5G_ANT1

<OrgName> DrayTek		
File RF_5G_FEM_CH1		
Size Custom	Document Number V2766AX	Rev 6B
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SLIC220

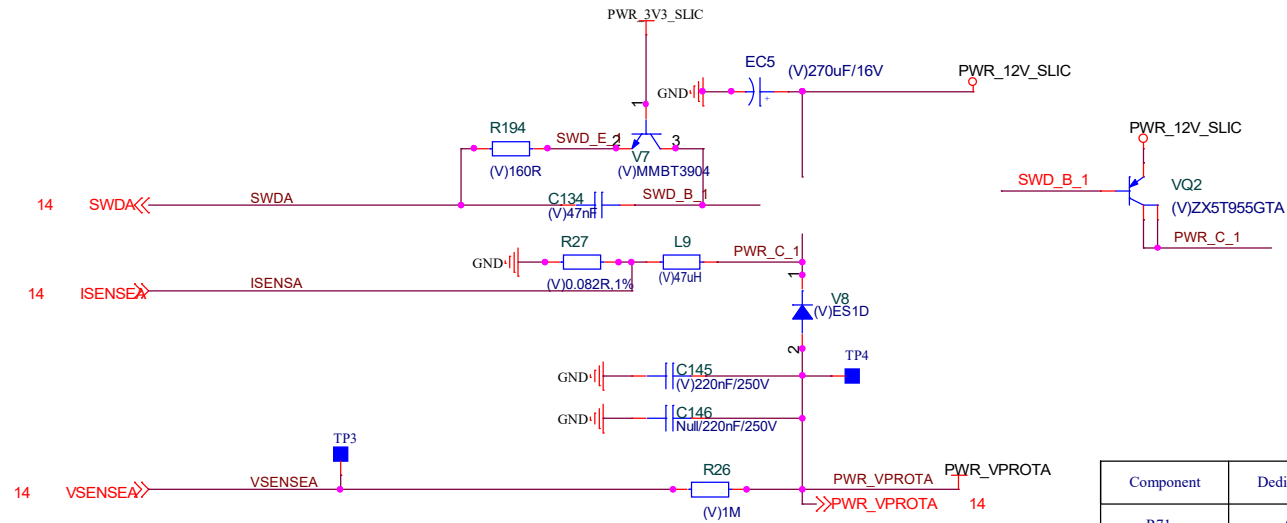


SLIC220



	R1806	R1803
Dedicated DCDC mode	Mounted	X
Combined DCDC mode	X	Mounted

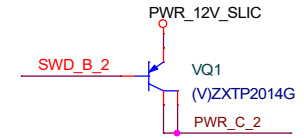
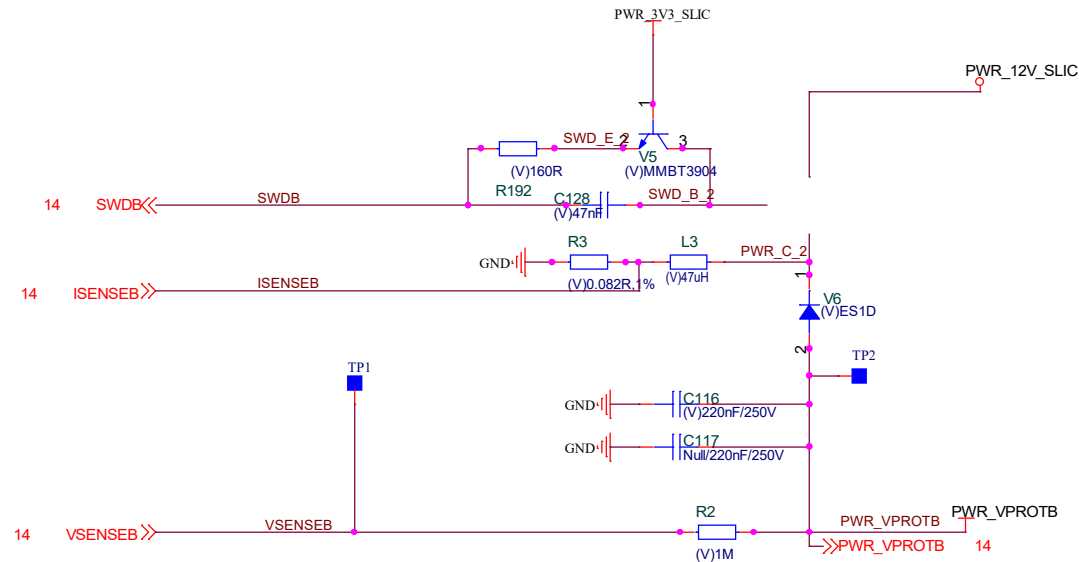
Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the radiating part and the DSL must be maintain.



Component	Dedicated DCDC	Combined DCDC
R71	0.082R	0.068R
L7	47uH/1.8A	33uH/2.1A
C196	mount	X
C1805	X	mount

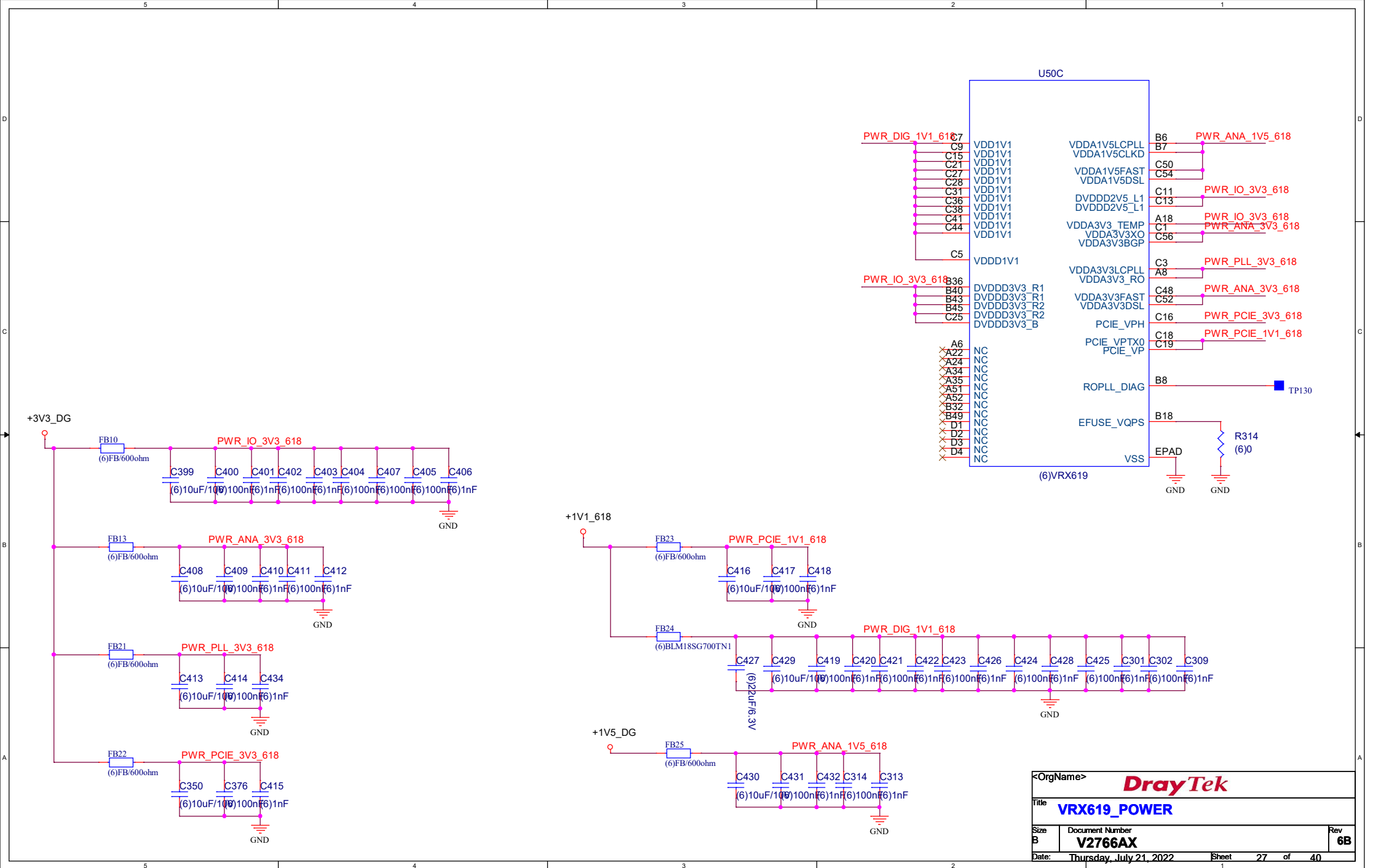
DCDC Type
Dedicated DCDC = T0.2
Combined DCDC = T1.1

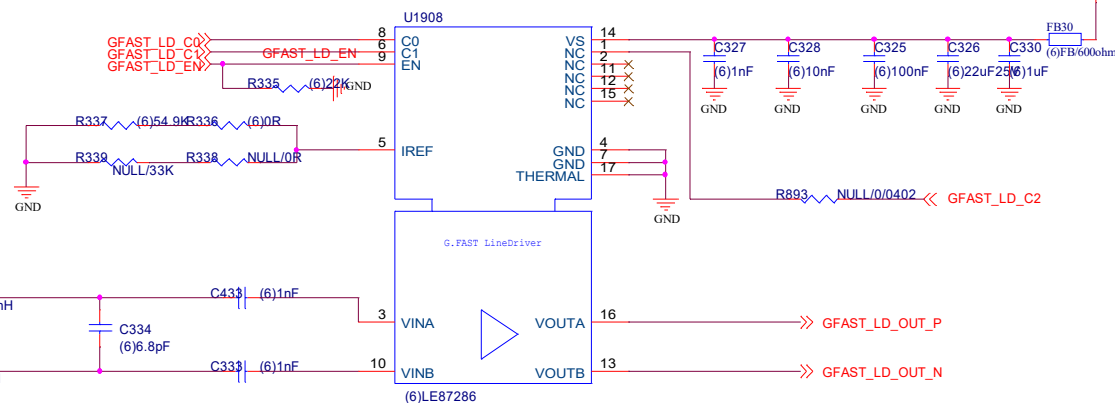
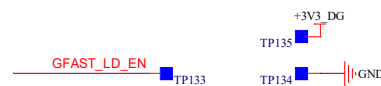
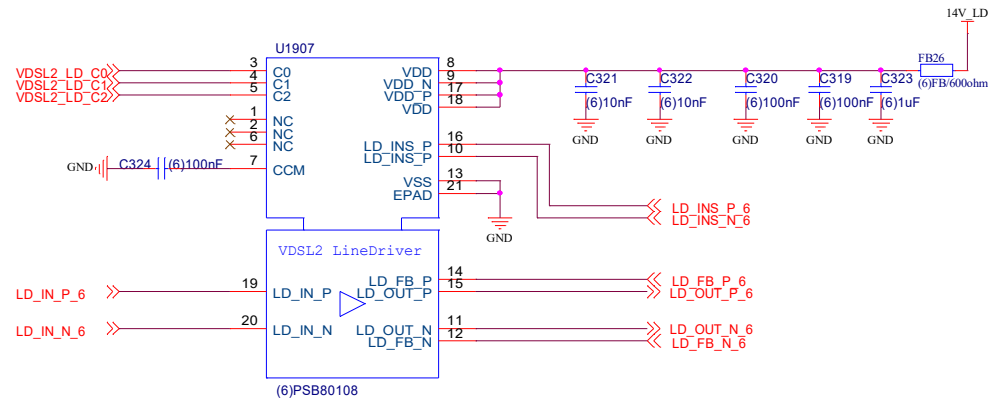
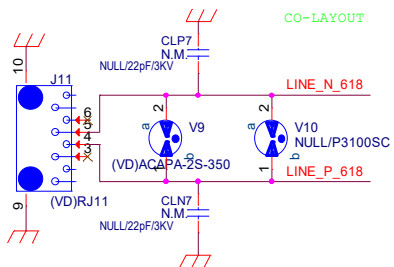
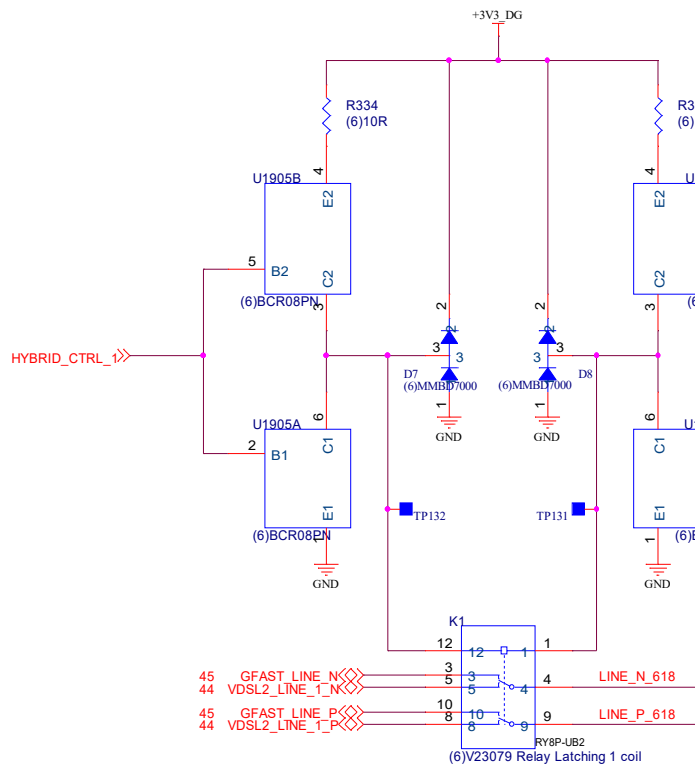
Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the relating part and the DSL must be maintain.



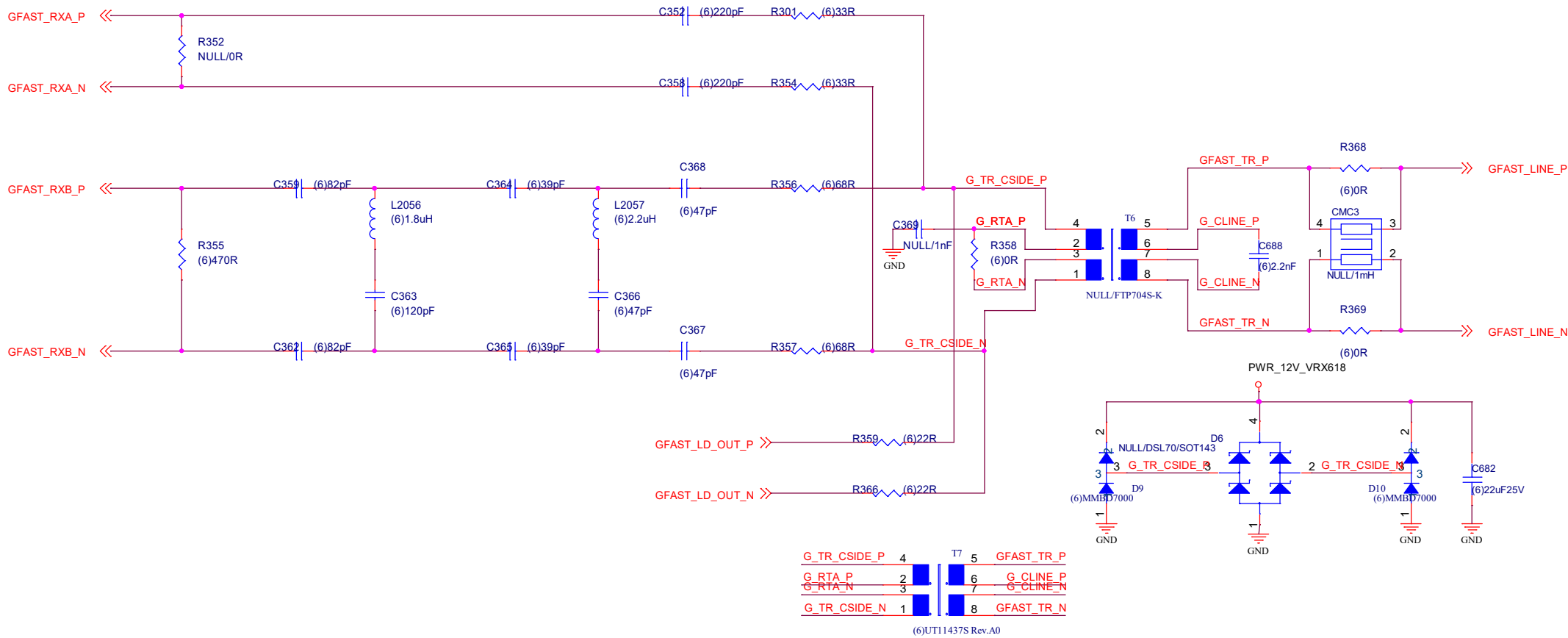
Component	Dedicated DCDC	Combined DCDC
R77	0.082R	0.068R
L9	47uH/1.8A	33uH/2.1A
C204	mount	X
C1806	X	mount







<OrgName>		DrayTek	
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<OrgName>		DrayTek	
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REVISION HISTORY

Version	Date	List of Modification	Page
V0A	2020-12-01		Ian
	2020-12-10	2.4GHz FEM (152-5331900-00G,SKY85331-11) : 1. Add XU31, XU33 2. Remove XC12, XC13, XC10, XC11 3. Null XR101, XR88, XU30, XU32 4. Place XR137, XR136 5. Remove XR146, XR149, XR142, XR145 5GHz FEM (152-5743900-00G,SKY85743-31) : 1. Add XU51, XU53 for co-layout with XU52, XU54 2. Remove XR117, XR113, XC16, XC17 3. Remove XR118, XR129, XC181, XC182 4. Place XR11, XR12 6. Null XU61, XR10, XR135 7. Place XR139, XR140 8. Null XU63, XR138, XR141	mChen
V6B	2021-5-28	1. Change VRX619 circuit 2. Add J9 3. colay internal PHY 4	Ian
V6C	2022-02-24	1.C326,C682,C685 colay C1206	Ian
V6D	2022-07-18	1.Add C766, C767, C691, C768, C769, C692, C770, C771, C693	Ian

BOM Difference

	V2765ax	V2765Vax							
(VD)	V	V							
(V)	NULL	V							
(5)	V	V							
(PD)	NULL	NULL							
(AX)	V	V							
(NPD)	V	V							
(AX_LTE)	NULL	NULL							

<OrgName>			DrayTek
Title			BOM Difference
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