AIROC™ Bluetooth® LE module

General description

The CYW20829B0-P4xxI100 is a fully integrated Bluetooth® LE wireless module. The CYW20829B0-P4xxI100 includes an onboard crystal oscillator, passive components, flash memory, and the CYW20829 silicon device. Refer to the **CYW20829** datasheet for additional details on the capabilities of the silicon device used in this module.

The CYW20829B0-P4xxI100 supports high-performance analog-to-digital conversion audio input, I^2S/PCM, CAN, LIN for automotive use cases and other standard communication and timing peripherals. The CYW20829B0-P4xxI100 includes a royalty-free Bluetooth® stack compatible with Bluetooth® 5.4 core spec in a 14.5 × 19 × 1.95 mm package.

The CYW20829B0-P4xxI100 includes 1 MB of onboard serial flash memory and is designed for standalone operation. The CYW20829B0-P4xxI100 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYW20829B0-P4xxI100 is fully qualified by Bluetooth® SIG and is targeted at applications requiring cost-optimized Bluetooth® wireless connectivity.

The CYW20829B0-P4xxI100 is offered in two certified versions CYW20829B0-P4TAI100, and CYW20829B0-P4EPI100. The CYW20829B0-P4TAI100 includes an integrated trace antenna. The CYW20829B0-P4EPI100 supports an external antenna through a RF solder pad output.

Module description

- Module size: 14.5 × 19 × 1.95 mm
- Bluetooth® 5.4 core spec qualified module
  - QDID: TBD
  - Declaration ID: TBD
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 1-MB on-module serial flash memory
- Up to 26 GPIOs
- Temperature range: –30°C to +85°C
- 96-MHz Arm® Cortex®-M33 CPU with single-cycle multiply and memory protection unit (MPU)
- Maximum TX output power
  - Programmable TX power: up to 11 dBm
    - Bluetooth® LE connection range of up to 500 meters at 10 dBm[1]
- RX sensitivity:
  - LE-1 Mbps: –98 dBm
  - LE-2 Mbps: –95 dBm
  - Coded PHY 500 kbps (LE-LR): –101 dBm
  - Coded PHY 125 kbps (LE-LR): –106 dBm

Note

1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +10.0 dBm. Actual range will vary based on end product design, environment, receive sensitivity, and transmit output power of the central device.

Power consumption

- Bluetooth® LE current consumption
  - RX current: 5.6 mA @ LE 1 Mbps
  - TX current: 5.2 mA @ 0 dBm
  - Deep Sleep mode current with 64 KB SRAM retention: 4.5 µA
  - HIDOFF (Deep Sleep): 0.5 µA

Functional capabilities

- Flexible clocking options
  - 8-MHz internal main oscillator (IMO) with ±2% accuracy
  - Ultra-low-power 32-kHz internal low-speed oscillator (ILO)
  - Two oscillators: High-frequency (24-MHz) for radio PLL and low-frequency (32-kHz watch crystal) for LPO
  - 48-MHz low power IHO (internal oscillator)
  - Frequency-locked loop (FLL) for multiplying IMO frequency
  - Integer and fractional peripheral clock dividers
- Quad SPI (QSPI)/serial memory interface (SMIF)
  - eXecute-In-Place (XIP) from external quad SPI flash
  - On-the-fly encryption and decryption
  - Support for DDR
  - Supports single, dual, and quad interfaces with throughput up to 384-Mbps
- Serial Communication
  - Three run-time configurable Serial Communication Blocks (SCBs)
    - First SCB: Configurable as SPI or I^2C
    - Second SCB: Configurable as SPI or UART
    - Third SCB: Configurable as I^2C or UART
- Audio subsystem
  - Two pulse density modulation (PDM) channels and one I2 S channel with time division multiplexed (TDM) mode
- Timing and pulse-width modulation
  - Seven 16-bit and two 32-bit Timer/Counter Pulse-Width Modulator (TCPWM) blocks, for MCU. Multiple PWMs needed for color LEDs.
  - PWM supports center-aligned, edge, and pseudo-random modes
- ADC and MIC
  - Sigma-delta switched cap ADC for audio and DC measurements
- Up to 32 programmable GPIOs
  - One I/O port (8 I/Os) enables Boolean operations on GPIO pins; available during system Deep Sleep
  - Programmable drive modes, strengths, and slew rates
  - Two overvoltage-tolerant (OVT) pins
  - Up to six, used for SMIF

- Security built into platform architecture
  - ROM-based root of trust via uninterruptible “Secure Boot”
  - Step-wise authentication of execution images
  - Secure execution of code in execute-only mode for protected routines
  - All debug and test ingress paths can be disabled
  - Up to four protection contexts (One available for customer code)
  - Secure debug support via authenticated debug token
  - Encrypted image support for external SMIF memory
- Cryptography hardware
  - Hardware Acceleration for symmetric cryptographic methods and hash functions
  - True Random Number Generation (TRNG) function

Benefits

CYW20829B0-P4xxI100 provides all necessary components required to operate Bluetooth® LE communication standards.

- Proven ready-to-use hardware design
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation and over-the-air updates
- Bluetooth® SIG listed with QDID and declaration ID
- Fully certified module eliminates the time needed for design, development, and certification processes
- ModusToolbox™ provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a Bluetooth® application

More information

Infineon provides a wealth of data at **www.infineon.com** to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: **AIROC™ Bluetooth® LE & Bluetooth® portfolio**, **Module portfolio**
- **CYW20829 Bluetooth® silicon datasheet**
- Development kits:
  - **CYW920829B0M2P4TAI100-EVK**, CYW20829B0-P4TAI100 evaluation board
  - **CYW920829B0M2P4EPI100-EVK**, CYW20829B0-P4EPI100 evaluation board
- Test and debug tools:
  - **CYSmart**, Bluetooth® LE test and debug tool (Windows)
  - **CYSmart Mobile**, Bluetooth® LE test and debug tool (Android/iOS Mobile App)
- Knowledge base article
  - **KBA97095** - EZ-Bluetooth® LE module placement
  - **KBA213976** - FAQ for Bluetooth® LE and regulatory certifications with EZ-BLE modules
  - **KBA210802** - Queries on Bluetooth® LE qualification and declaration processes
  - **KBA218122** - 3D Model Files for EZ-BLE/EZ-BT modules

Development environments

ModusToolbox™ software is a modern, extensible development environment supporting a wide range of Infineon microcontroller devices. It provides a flexible set of tools and a diverse, high-quality collection of application-focused software. These include configuration tools, low-level drivers, libraries, and operating system support, most of which are compatible with Linux®, macOS®, and Windows®-hosted environments. ModusToolbox™ software does not include proprietary tools or custom build environments. This means you choose your compiler, your IDE, your RTOS, and your ecosystem without compromising usability or access to our industry leading CAPSENSE™, AIROC™, Bluetooth®, Wi-Fi, security, and low-power features.

Technical support

- **Infineon community:** Whether you are a customer, partner, or a developer interested in the latest innovations, the developer community offers you a place to learn, share, and engage with both Infineon experts and other embedded engineers around the world.
- Visit our **support** page and contact a **local sales representatives**. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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1 Overview

1.1 Functional block diagram

Figure 1 illustrates the CYW20829B0-P4xxI100 functional block diagram.

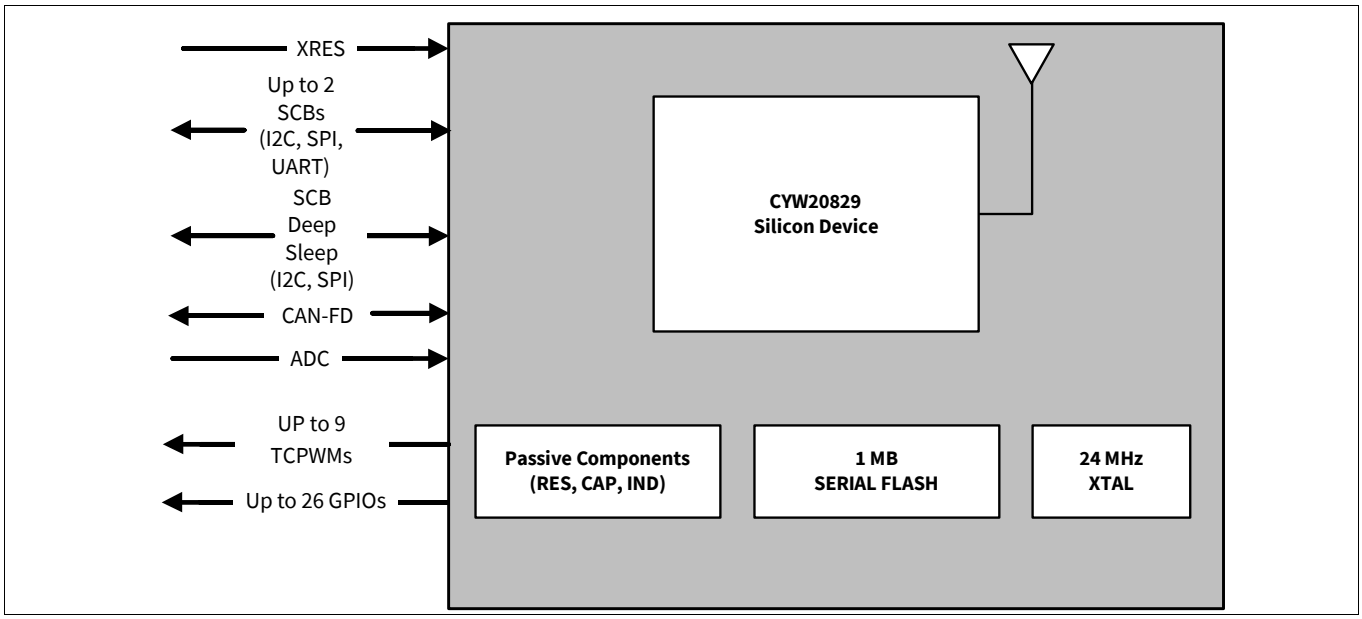


Figure 1 Functional block diagram (GPIOs)

1.2 Module description

The CYW20829B0-P4xxI100 module is a complete module designed to be soldered to the application's main board.

1.2.1 Module dimensions and drawing

Infineon reserves the right to select components from various vendors to achieve the Bluetooth® module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in **Figure 2**. All dimensions are in millimeters (mm).

Table 1 Module design dimensions

Dimension item		Specification
Module dimensions	Length (X)	14.5 ± 0.15 mm
	Width (Y)	19 ± 0.15 mm
Antenna connection location dimensions	Length (X)	14.5 mm
	Width (Y)	4.62 mm
PCB thickness	Height (H)	0.50 ± 0.05 mm
Shield height	Height (H)	1.45-mm typical
Maximum component height	Height (H)	1.45-mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.95-mm typical

See **Figure 2** for the mechanical reference drawing for CYW20829B0-P4xxI100.

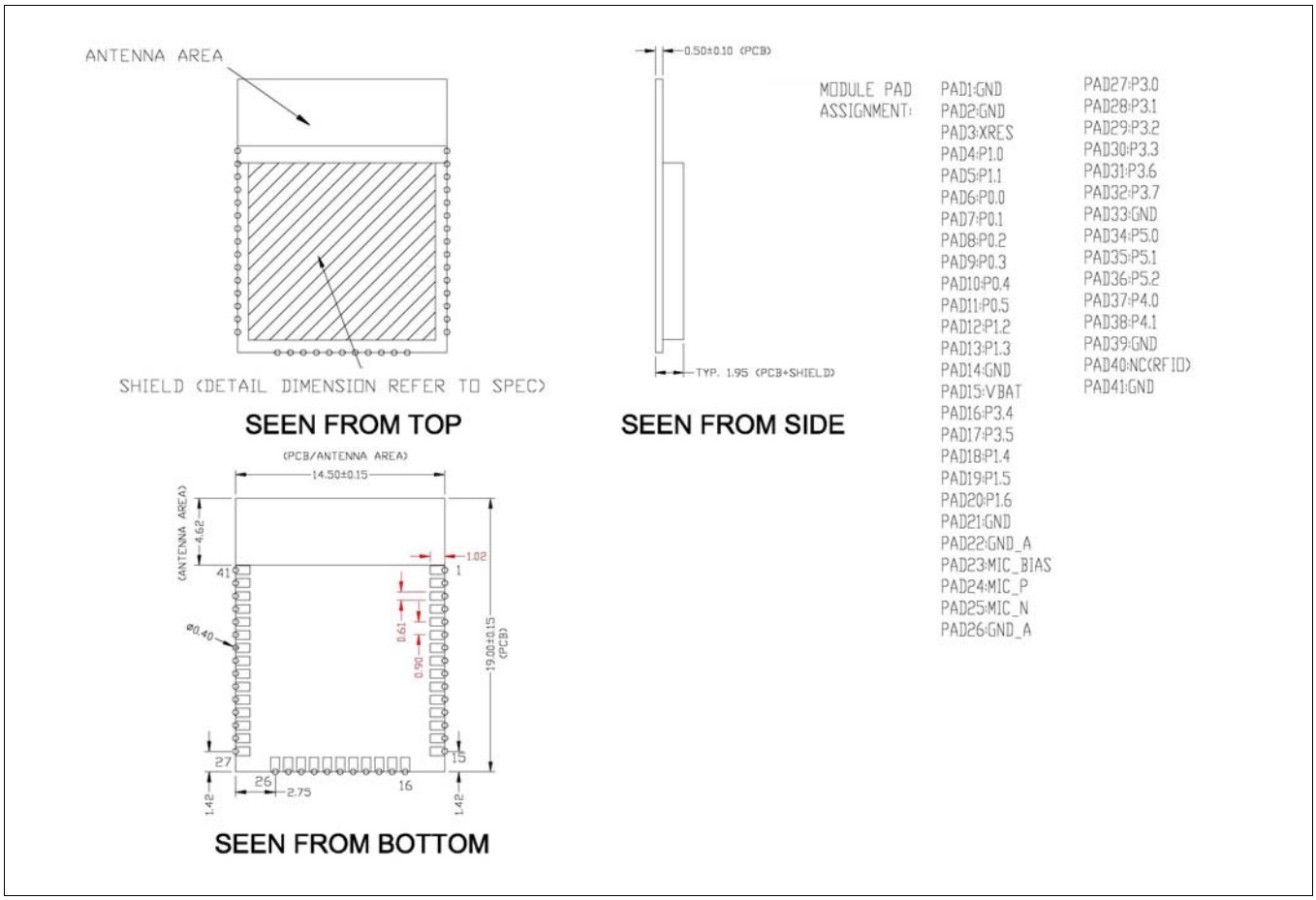


Figure 2 Module mechanical drawing

Notes

2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see **"Recommended host PCB layout"** on page 11.
3. The CYW20829B0-P4TAI100, CYW20829B0-P4EPI100 includes castellated pad connections, denoted as the circular openings at the pad location above.

2 Pad connection interface

As shown in the bottom view of **Figure 2**, the CYW20829B0-P4xxI100 connects to the host board via solder pads on the backside of the module. **Table 2** and **Figure 3** detail the solder pad length, width, and pitch dimensions of the CYW20829B0-P4xxI100 module.

Table 2 Connection description

Part number	Name	Connections	Connection type	Pad length dimension	Pad width dimension	Pad pitch
CYW20829B0-P4TAI100	SP	41	Solder pads	1.02 mm	0.61 mm	0.90 mm
CYW20829B0-P4EPI100	SP	41	Solder pads	1.02 mm	0.61 mm	0.90 mm

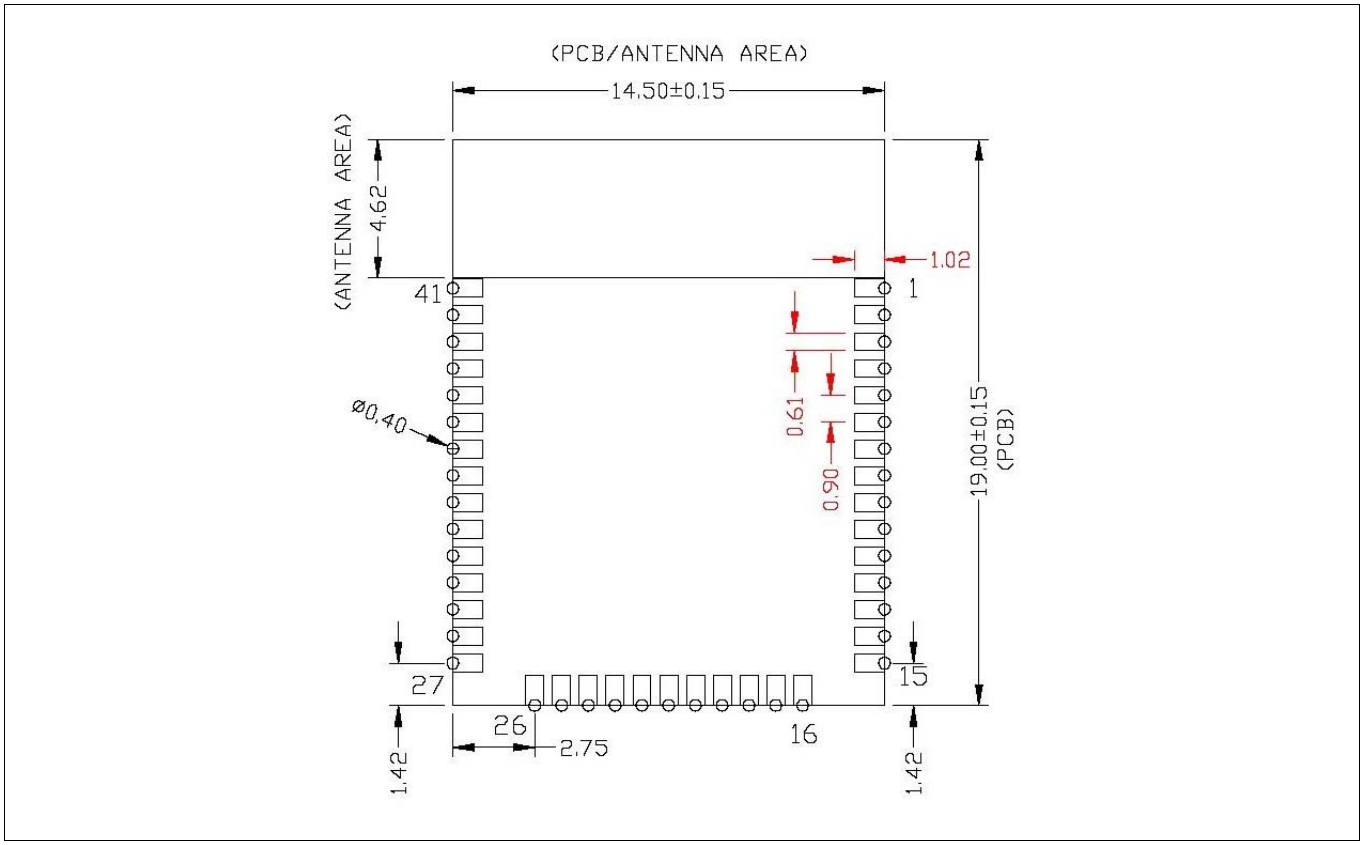


Figure 3 Solder pad dimensions (seen from bottom)

To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the module (see **Figure 2**) must not contain ground or signal traces. This keepout area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Bluetooth® module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keepout area stated in item 2. Refer to **AN96841** for module placement best practices.

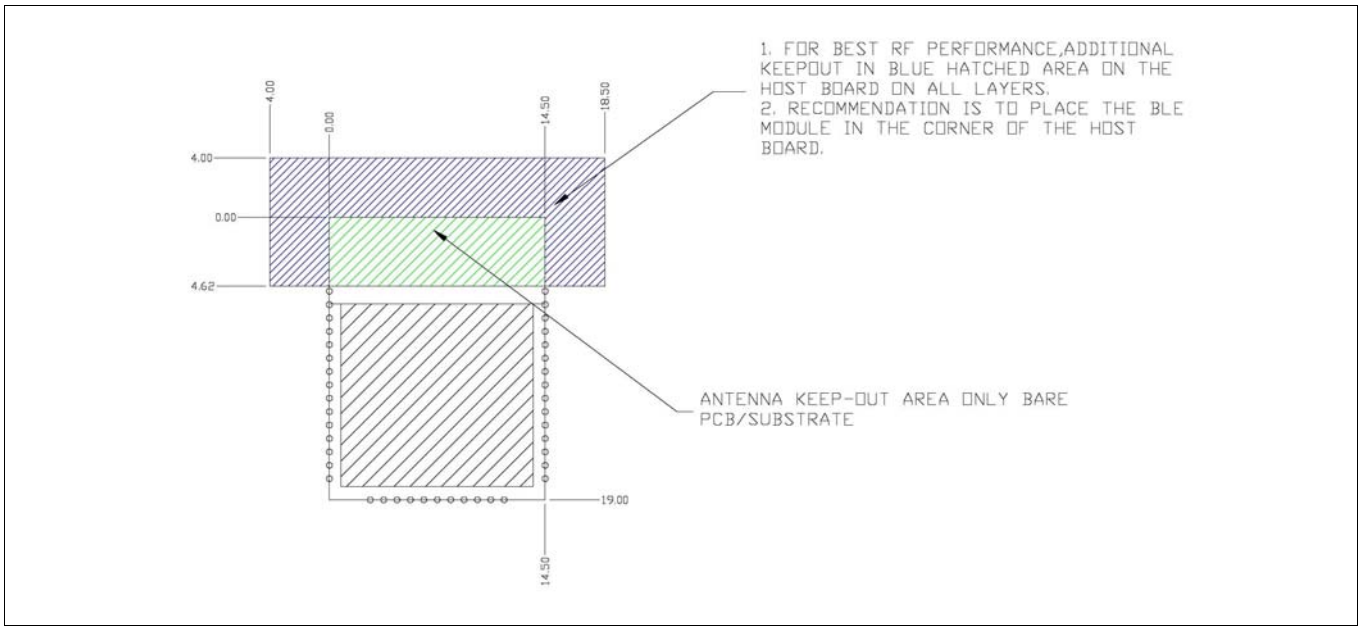


Figure 4 Recommended host PCB keepout area around the CYW20829B0-P4xxI100 antenna

3 Recommended host PCB layout

Figure 5 provides details that can be used for the recommended host PCB layout pattern for the CYW20829B0-P4xxI100. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.64 mm from center of the pad on either side) shown in **Figure 4** is the minimum recommended host pad length. The host PCB layout pattern can be completed using either **Figure 5**. It is not necessary to use all figures to complete the host PCB layout pattern.

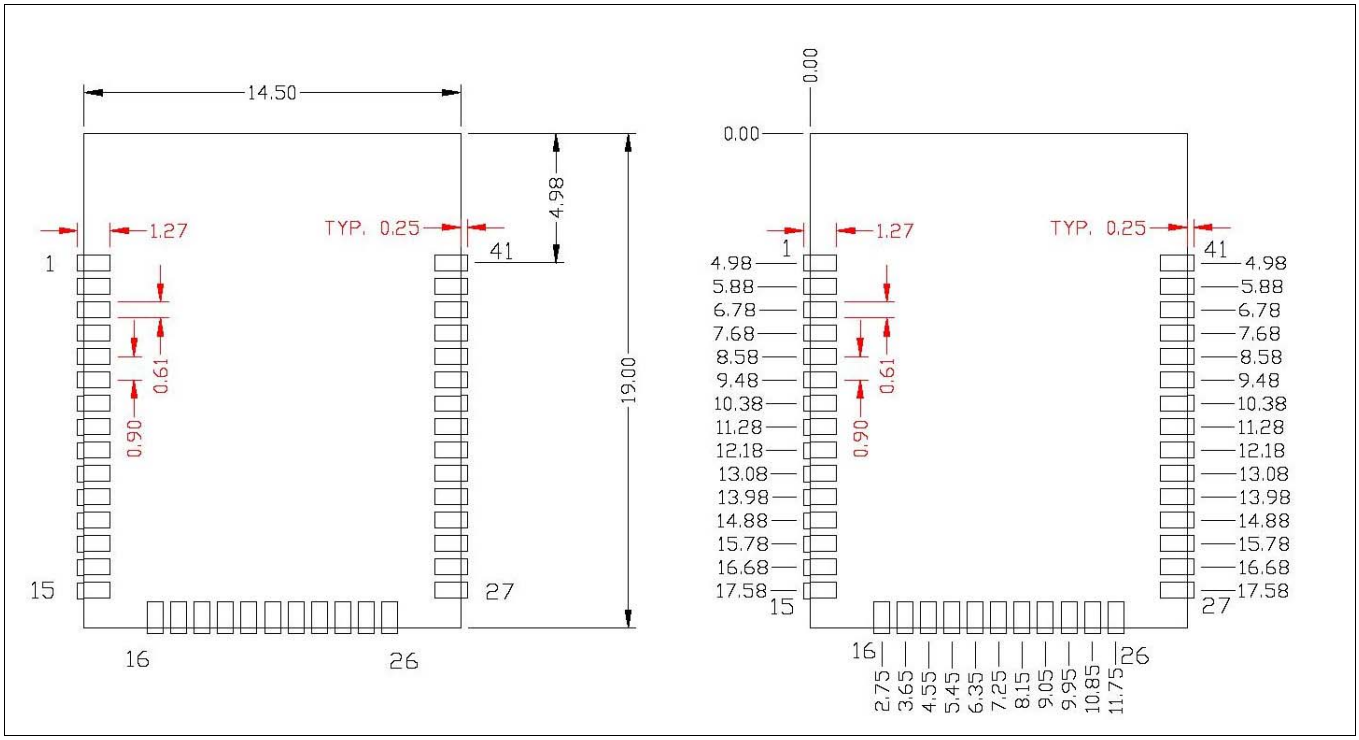


Figure 5 CYW20829B0-P4xxI100 host layout (dimensioned)

4 Module connections

Table 3 details the solder pad connection definitions and available functions for the pad connections for the CYW20829B0-P4xxI100 module. Table 3 lists the solder pads on the CYW20829B0-P4xxI100 module, the silicon device pin, and denotes what functions are available for each solder pad.

Table 3 Pin assignments

Module pad name	Pin number	Silicon pin name	Pin number	I/O	Power domain	Description
Microphone		**Microphone**				
MIC_P	24	MIC_P	54	I	VDDA	Microphone positive input
MIC_N	25	MIC_N	55			Microphone negative input
MIC_BIAS	23	MIC_BIAS	53	O		Microphone bias supply
GND_A	22, 26					Analog ground for microphone
Power supply						
VBAT	15	2.75 V~3.6 V				
Ground pins						
GND	1, 2, 14, 21, 33, 39, 41					
Radio I/O						
RFIO	40			I/O		External antenna port (only for CYW20829B0-P4EPI100)

Table 4 GPIO pin descriptions

Module pad name	Pad number	Silicon pin name	Silicon pin number	Direction Default	POR state	Power domain	Description
P0.0	6	P0.0	32	I/O	Floating	VDDO	General input and output port. See **Table 13** for alternate functions.
P0.1	7	P0.1	33	I/O	Floating	VDDO	
P0.2	8	P0.2	34	I/O	Floating	VDDO	
P0.3	9	P0.3	35	I/O	Floating	VDDO	
P0.4	10	P0.4	36	I/O	Floating	VDDO	
P0.5	11	P0.5	37	I/O	Floating	VDDO	
P1.0	4	P1.0	38	I/O	Floating	VDDO	
P1.1	5	P1.1	39	I/O	Floating	VDDO	
P1.2	12	P1.2	40	I/O	Floating	VDDO	
P1.3	13	P1.3	41	I/O	Floating	VDDO	
P1.4	18	P1.4	43	I/O	Floating	VDDO	
P1.5	19	P1.5	44	I/O	Floating	VDDO	
P1.6	20	P1.6	45	I/O	Floating	VDDO	
P3.0	27	P3.0	1	I/O	Floating	VDDO	
P3.1	28	P3.1	2	I/O	Floating	VDDO	
P3.2	29	P3.2	3	I/O	Floating	VDDO	
P3.3	30	P3.3	4	I/O	Floating	VDDO	
P3.4	16	P3.4	5	I/O	Floating	VDDO	
P3.5	17	P3.5	6	I/O	Floating	VDDO	
P3.6	31	P3.6	8	I/O	Floating	VDDO	
P3.7	32	P3.7	9	I/O	Floating	VDDO	
P4.0	37	P4.0	13	I/O	Floating	VDDO	
P4.1	38	P4.1	14	I/O	Floating	VDDO	
P5.0/ WCO_OUT	34	P5.0/ WCO_OUT	10	I/O	Floating	VDDO	
WCO_OUT		WCO_OUT					
P5.1/ WCO_IN	35	P5.1/ WCO_IN	11	I/O	Floating	VDDO	
P5.2	36	P5.2	12		Floating	VDDO	
XRES	3	XRES	23	I	Floating	VDDO	

Notes

4. The CYW20829B0-P4xxI100 contains a single SPI (SPI1) peripheral supporting both master or slave configurations. SPI2 is used for on-module serial memory interface.
5. In Master mode, any available GPIO can be configured as SPI1_CS. This function is not explicitly shown in **Table 23**.

5 Connections and optional external components

5.1 Power connections (VBAT)

The CYW20829B0-P4xxI100 contains one power supply connection, VBAT, which accepts a supply input range of 2.75 V to 3.6 V for CYW20829B0-P4xxI100. **Table 15** provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in **Table 15**.

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection and the recommended ferrite bead value is 330 Ω, 100 MHz.

5.1.1 Considerations and optional components for Brown Out (BO) conditions

Power supply design must be completed to ensure that the CYW20829B0-P4xxI100 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the following range:

$$V_{IL} \leq VDDIN \leq V_{IH}$$

Refer to **Table 16** for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (that is, battery installation, high-value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Refer to **Figure 6** for the recommended circuit design when using an external voltage detection IC.

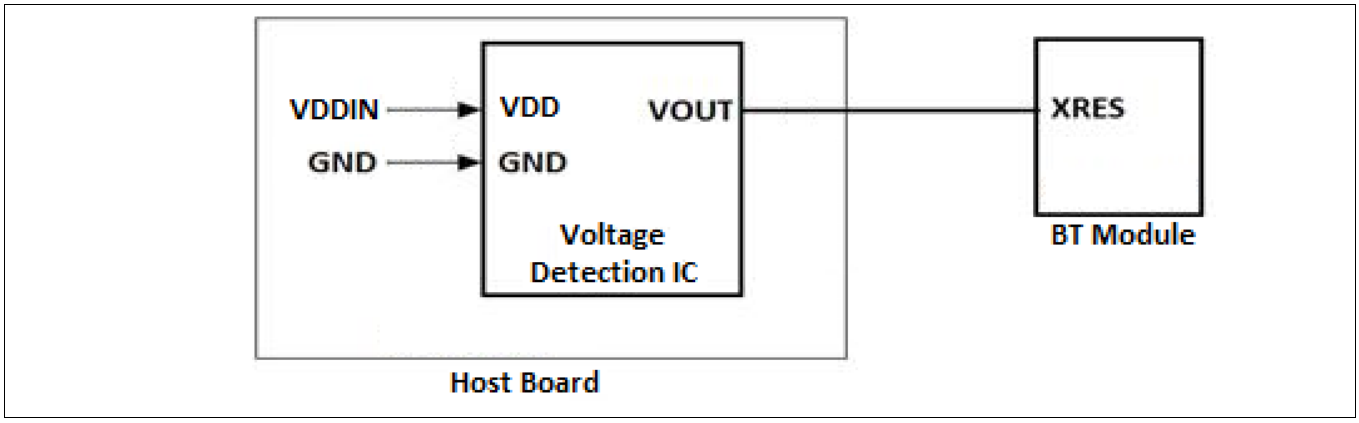


Figure 6 Reference circuit block diagram for external voltage detection IC

In the event that the module does encounter a Brown Out condition, and is operating erratically or is not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

5.2 External reset (XRES)

The CYW20829B0-P4xxI100 has an integrated power-on reset circuit, which completely resets all circuits to a known power-on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYW20829B0-P4xxI100 module (solder pad 3). The CYW20829B0-P4xxI100 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYW20829B0-P4xxI100 is required to be held low 50 ms after the VBAT power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of the CYW20829B0-P4xxI100 module and pull XRES low until VBAT is stable. XRES is recommended to be released 50 ms after VBAT is stable.
- If the XRES connection of the CYW20829B0-P4xxI100 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYW20829B0-P4xxI100 to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VBAT power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VBAT stability.
- The XRES release timing may be controlled by an external voltage detection IC. XRES should be released 50 ms after VBAT is stable.

Connections and optional external components

Figure 7 illustrates the CYW20829B0-P4xxI100 schematic.

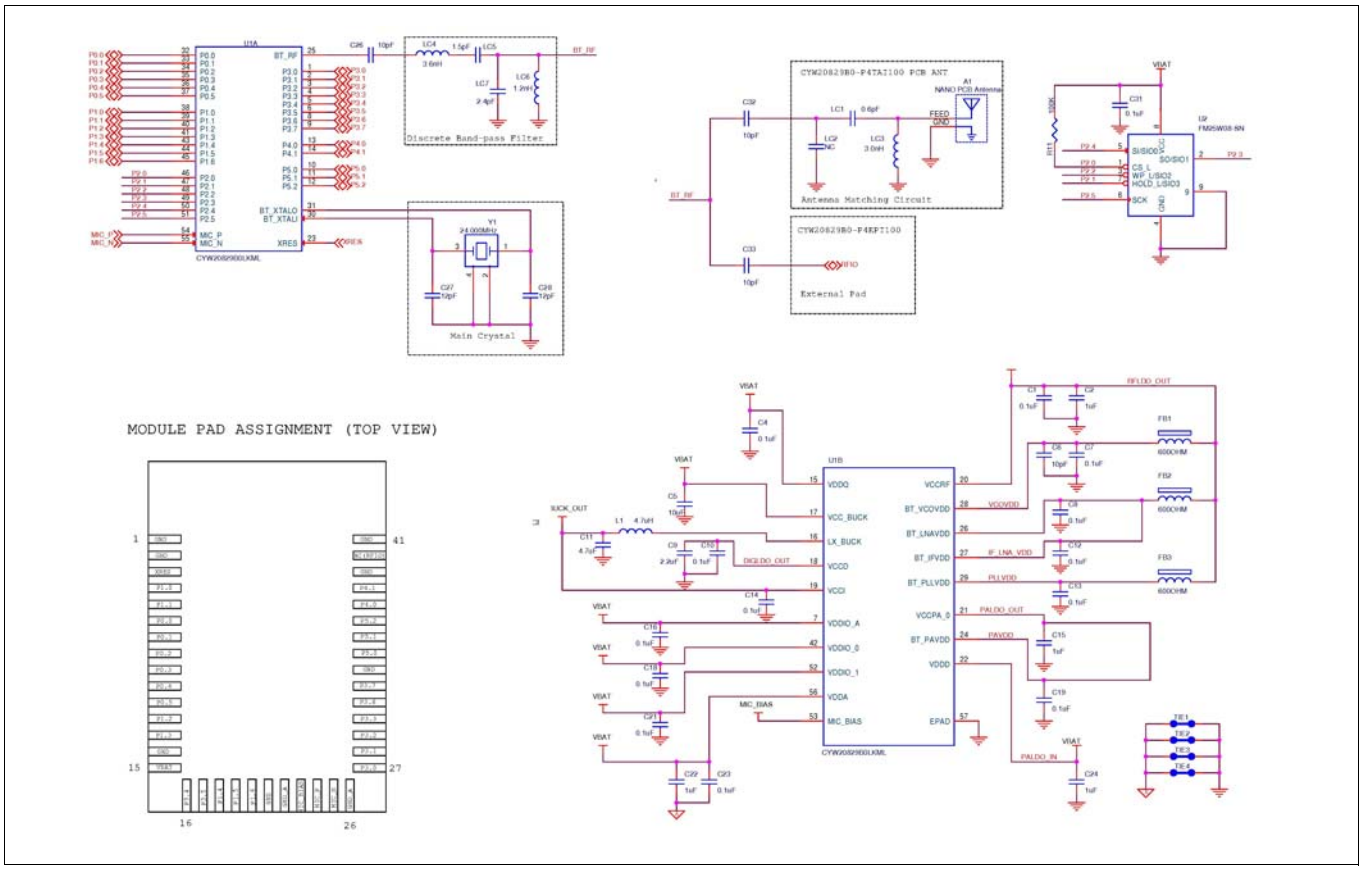


Figure 7 CYW20829B0-P4xxI100 schematic diagram

5.3 Critical components list

Table 5 details the critical components used in the CYW20829B0-P4xxI100 module.

Table 5 Critical component list

Component	Reference designator	Description
Silicon	U1	56-pin QFN Bluetooth® LE silicon device - CYW20829
Silicon	U2	8-pin TDF8N, 1 MB Serial Flash
Crystal	Y1	24 MHz, 8 pF

5.4 Antenna design

Table 6 details trace antenna used in the CYW20829B0-P4TAI100 module. For more information, see Table 6.

Table 6 Trace antenna specifications

Item	Description
Frequency range	2400 MHz–2500 MHz
Peak gain	–0.5-dBi typical
Return loss	10-dB minimum

Table below details the qualified dipole antenna used in the CYW20829B0-P4EPI100 module. Any antenna of equivalent or less gain can be used without additional application and testing for FCC regulations. For more information, see Table below.

Table Dipole antenna specifications

Item	Description
Manufacture	Pulse
Part number	W1010
Frequency range	2400 MHz–2500 MHz
Peak gain	2.0-dBi typical

6 Functional description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in **Figure 1**. For more detailed information, refer to the following documentation:

- Board Support Package (BSP) documentation

  BSPs are available on **GitHub**. They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example **here**. This **search link** finds all currently available BSPs on the Infineon **GitHub** site.

- Hardware Abstraction Layer (HAL) API reference manual

  The Infineon HAL provides a high-level interface to configure and use hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The **HAL API Reference** provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.

6.1 CPU and memory subsystem

AIROC™ CYW20829 has multiple bus masters, as **Figure 1** shows. They are: CPU, datawire, QSPI, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm® AMBA high-performance bus (AHB) arbitration. An interprocessor communication block (IPC) provides communication between the CPU and the Bluetooth® LE sub-system.

6.1.1 CPU

The Cortex®-M33 has single-cycle multiply and a memory protection unit (MPU). It can run at up to 96 MHz in LP mode and 48 MHz in ULP mode. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

Cortex®-M33 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the **Armv8-M architecture reference manual**).

The main MCU also implements device-level security, safety, and protection features. Cortex®-M33 provides a secure, interruptible boot function. This guarantees that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

The CPU has the following power draw, at V_{DDD} = 3.0 V and using the internal buck regulator.

Table 7 Active current slope at V_{DDD} = 3.0 V using the internal buck regulator

System power mode		
CPU	ULP	LP
	22 µA/MHz	40 µA/MHz

The CPU can be selectively placed in Sleep and Deep Sleep power modes as defined by Arm®. The CPU also implements a Deep Sleep RAM (DS-RAM) mode in which almost all the circuits except RAM are powered OFF. Data in RAM is retained to maintain state. Upon exit, the CPU goes through a reset but can use the data in RAM to skip software initialization.

The CPU also has nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

CYW20829 has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in the CPU.

CPU debug and trace features are as follows:

- Six hardware breakpoints and four watchpoints, serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.

6.1.2 Interrupts

The CPU has interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn.

Each interrupt supports eight configurable priority levels. One system interrupt can be mapped to the CPU non-maskable interrupts (NMI). Multiple interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC.

6.1.3 Datawire

Datawire is a light weight DMA controller with 16 channels, which support CPU-independent accesses to memory and peripherals. The descriptors for the channels are in SRAM and the number of descriptors is limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination.

6.1.4 Cryptography accelerator (Cryptolite)

A combination of HW and SW is able to support several cryptographic functions. Specifically it supports the following functions:

- Encryption/decryption
  - AES-128 hardware accelerator with following supported modes:
    - Electronic Code Book (ECB)
    - Cipher Block Chaining (CBC)
    - Cipher Feedback (CFB)
    - Output Feedback (OFB)
    - Counter (CTR)
- Hashing
  - Secure Hash Algorithm (SHA-256) hardware accelerator
- Message Authentication Functions (MAC)
  - Hashed Message Authentication Code (HMAC) acceleration using SHA-256 hardware
- True Random Number Generator (TRNG)
- Vector unit hardware accelerator
  - Digital Signature Verification using RSA
  - Digital Signature Verification using ECDSA

6.1.5 Protection units

CYW20829 has multiple types of protection to control erroneous or unauthorized access to memory and peripheral registers.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secure/non-secure, and protection context.

Protection units are configured at “Secure Boot” to control access privileges and rights for bus masters and peripherals. Up to eight protection contexts (“Secure Boot” is in protection context 0) allow access privileges for memory and system resources to be set by the “Secure Boot” process per protection context by bus master and code privilege level. Multiple protection contexts are available.

6.1.6 AES-128

AES-128 component to accelerate block cipher functionality. This functionality supports forward encryption of a single 128 bit block with a 128 bit key. SHA-256 component to accelerate hash functionality. This component supports message schedule calculation for a 512-bit message chunk and processing of a 512-bit message chunk.

6.1.7 Vector unit (VU)

VU component to accelerate asymmetric key cryptography (for example, RSA and ECC). This component supports large integer multiplication, addition, and so on. TRNG component based on a set of ring oscillators. The TRNG includes a HW health monitor.

6.1.8 Controller area network flexible data-rate (CAN FD)

CYW20829 supports the CAN FD controller that supports one CAN FD channel. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware. All functions concerning the handling of messages are implemented by the RX and TX handlers. The RX handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The TX handler is responsible for the transfer of transmit messages from the message RAM to the CAN core, and provides transmit-message status.

6.1.9 Local interconnect network (LIN)

CYW20829 contains a LIN channel. Each channel supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN channel connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each block also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

6.1.10 Real time clock (RTC)

- Year/Month/Date, Day-of-week, Hour:Minute:Second fields
- 12- and 24-hour formats
- Automatic leap-year correction

6.1.11 Memory

CYW20829 contains the SRAM, ROM, and eFuse memory blocks.

- SRAM: CYW20829 has 256-KB of SRAM. Power control and retention granularity is 64-KB blocks allowing the user to control the amount of memory retained in Deep Sleep. Memory is not retained in Hibernate mode.
- ROM: The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code (ROM Boot) for several system functions. The ROM contains, primarily device initialization and security. ROM code is executed, in protection context 0.
- eFuse: A one-time programmable (OTP) eFuse array consists of 1024 bits, which are reserved for system use such as Die ID, Device ID, initial trim settings, device life cycle, and security settings. Some of the bits are available for storing security key information and hash values and can be programmed by the user for device security.

  Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of ‘0’ to ‘1’. To program an eFuse, VDDIO1 must be at 2.5 V ± 5%.

  Because blowing an eFuse is an irreversible process, programming is recommended only in mass production under controlled factory conditions by Infineon provided provisioning tools.

6.1.12 Boot code

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Device trim setting (calibration)
- Setting the device protection units
- Setting device access restrictions for secure life cycle states
- Configures the Debug Access Port
- In secure life cycle supports secure debug via authenticated debug token
- Configures the SMIF for external flash access
- In secure life cycle validates first user code in external flash by checking its digital signature. Supports OTF decryption of encrypted images in external flash
- Copies the application bootstrap from the external flash to SRAM and jumps to the ROM. It cannot be changed and acts as the Root of Trust in a secure system.

It should also be noted that the ROM code sets the system clock to 48 MHz IHO source.

6.1.13 Memory map

The 32-bit (4 GB) address space is divided into the regions shown in **Table 9**. Note that code can be executed from the Code, and Internal RAM or External flash.

Table 8 Address map

Address range	Name	Use
0x0000 0000 to 0x1FFF FFFF	Code	Program code region. It includes the exception vector table, which starts at address 0.
0x2000 0000 to 0x3FFF FFFF	SRAM	Data region
0x4000 0000 to 0x5FFF FFFF	Peripheral	All peripheral registers. Code cannot be executed from this region. Bit-band in this region is not supported.
0x6000 0000 to 0x8FFF FFFF	External NVM	SMIF/Quad SPI, (see the **"QSPI interface serial memory interface (SMIF)"** on page 30 section). Code can be executed from this region.
0xA000 0000 to 0xDFFF FFFF	External Device	Not used
0xE000 0000 to 0xE00F FFFF	Private Peripheral Bus	Provides access to peripheral registers within the CPU core.
0xE010 0A000 to 0xFFFF FFFF	Device	Device-specific system registers

The device memory map is shown in **Table 9**.

Table 9 Internal memory address map

Address range	Memory type	Size
0x0000 0000 to 0x0001 0000	ROM	64 KB
0x2000 0000 to 0x 2004 0000	SRAM	Up to 256 KB

7 System resources

7.1 Power system

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The V_{DDD} supply (1.7 V to 3.6 V) powers an on-chip buck regulator which offers a selectable (1.0 V or 1.16 V) core operating voltage (VCCD). The selection lets users choose between two system power modes:

- System Low Power (LP) operates VCCD at 1.1 V and offers high performance, with no restrictions on device configuration.
- System Ultra Low Power (ULP) operates VCCD at 1.0 V for exceptional low power, but imposes limitations on clock speeds.

The Bluetooth® radio requires 1.1 V for operation. Bluetooth® system may override user core voltage selection when the radio is turned on. System voltage will return to the user selected value automatically once Bluetooth® radio activity is completed. Refer to **"Power management unit"** on page 38 for more details.

7.1.1 Power modes

CYW20829 can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the relevant application note.

Power modes supported by CYW20829, in the order of decreasing power consumption, are:

- System Low Power (LP) - All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) - All peripherals and CPU power modes are available, but with limited speed
- CPU Active - CPU is executing code in system LP or ULP mode
- CPU Sleep - CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep - CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep - Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate - Device and I/O states are frozen and the device resets on wakeup
- Deep Sleep RAM - only RAM and IO states are retained. All system activity except for select low power peripherals ceases until system exits from this state. The CPU resets upon exit but can skip software initialization since RAM is retained.

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). System LP, ULP, Deep Sleep, Deep Sleep RAM and Hibernate modes are additional low-power modes supported by the CYW20829.

7.1.2 CYW20829 clock system

CYW20829 clock system consists of a combination of oscillators, external clock, and frequency-locked loop. Specifically, the following:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- Watch crystal oscillator (WCO)
- System 24-MHz crystal oscillator
- External clock input
- One frequency-locked loop (FLL)
- Internal high-speed oscillator (IHO)

Clocks may be buffered and brought out to a pin on a smart I/O port.

Table 10 shows the mapping of port and associated clock group mapped to peripherals.

Table 10 Mapping of clock groups to peripherals

PCLK group	Root clock (clk_hf)	Peripherals	Frequency		Description
			LP (1.1 V Typ)	ULP (1.0 V Typ)	
0	clk_hf0	CPU Trace	24 MHz	24 MHz	–
1	clk_hf1	SCB	96 MHz	48 MHz	Async peripherals: Strobe signals are driven through dividers; Interface clock is generated inside the peripheral with the main group clock.
		TCPWM			
		LIN			
		CANFD			
		SMARTIO			
2	clk_hf0	SMIF	96 MHz	48 MHz	Direct connection pass through from clk_hf. This clock is not used for interface clock, rather it is used for the MMIO clocks of SMIF, BTSS and CRYPTO. BTSS uses this clock for Master and Slave AHB/MMIO transactions, and SMIF also uses this clock for FAST/SLOW clocks.
		BTSS			
		CRYPTO			
3	clk_hf1	PDM	96 MHz	48 MHz	Uses PERI ACLK with default div by 2 option, required interface frequencies are obtained by further division inside the peripheral.
		TDM			
4	clk_hf2	BTSS	48 MHz	48 MHz	RPU clock for BTSS
5	clk_hf3	ADCMIC	24 MHz	24 MHz	Direct connection for ADCMIC, main source of clk_hf3 is clk_althf which is the BTSS ECO clock.
6	clk_hf1	SMIF	96 MHz	48 MHz	Direct connection for SMIF and SMARTIO peripherals. This clock is an interface clocks for these peripherals.

7.1.3 Internal main oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz and tolerance is ±2%.

7.1.4 Internal low-speed oscillator (ILO)

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

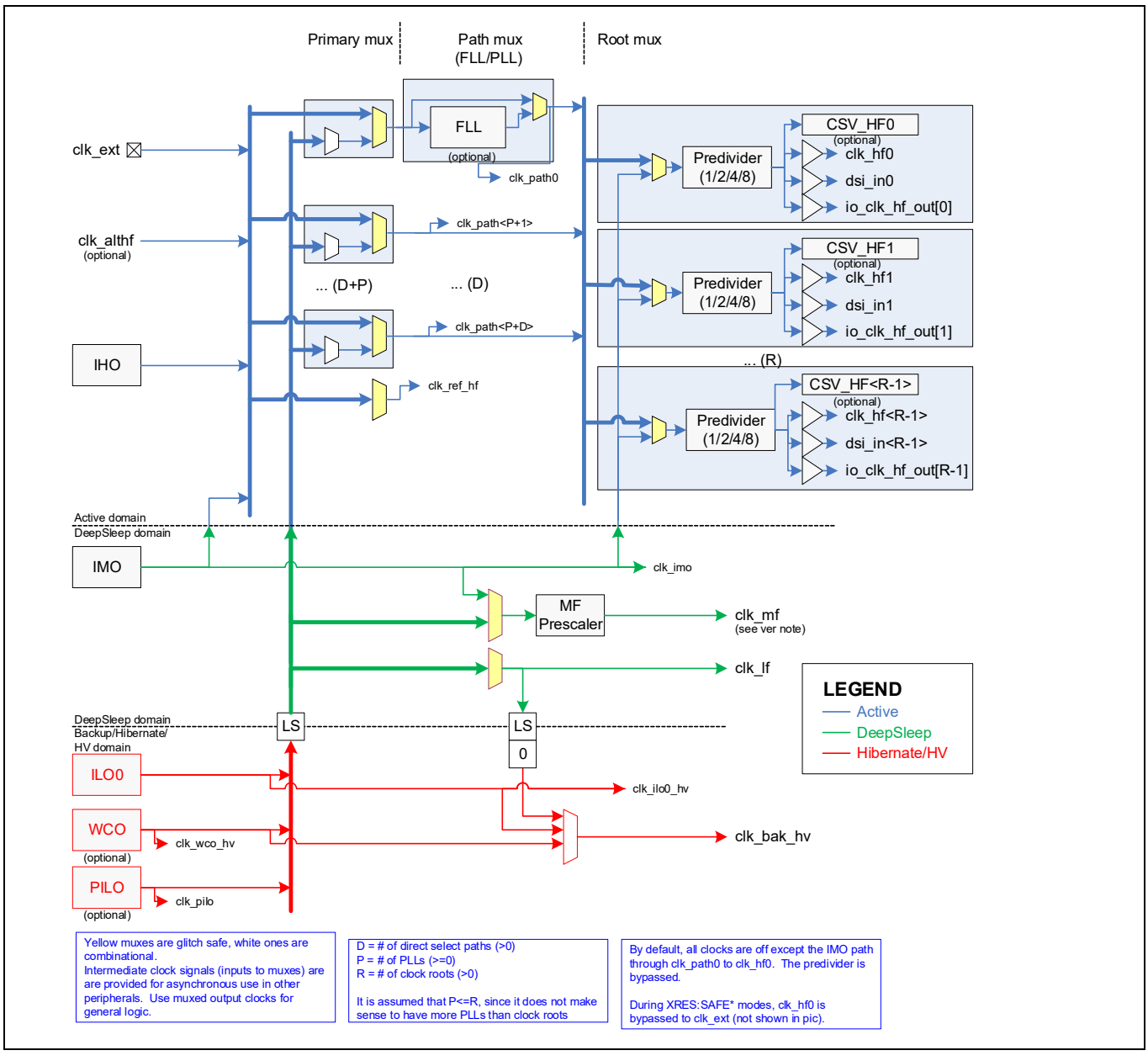


Figure 8 CYW20829 clocking diagram with corresponding oscillators

Note: Using PILO as the ILO clock source will result in longer boot time.

7.1.5 External crystal oscillators (ECO)

Figure 9 shows all of the external crystal oscillator circuits for CYW20829. The component values shown are typical; check the ECO specifications for the crystal values, and the crystal datasheet for the load capacitor values. The ECO and WCO require balanced external load capacitors. For more information, see the HW design guidelines. Note that its performance is affected by GPIO switching noise.

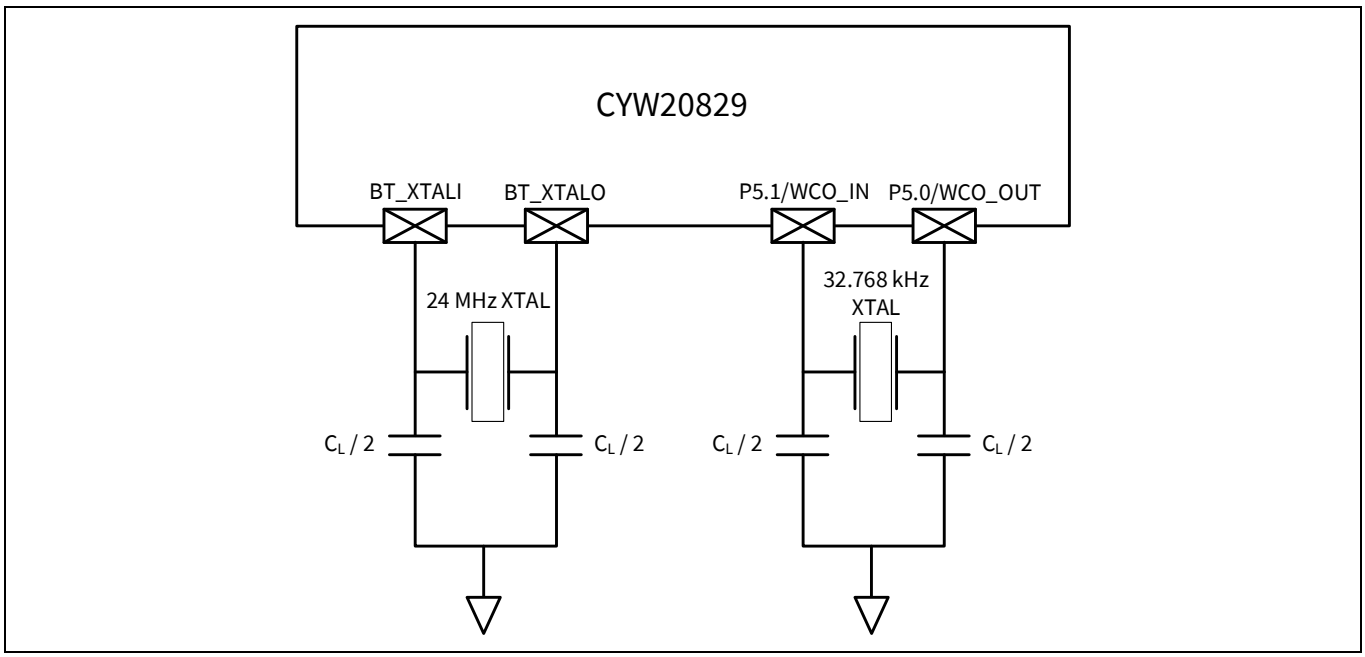


Figure 9 External oscillator

7.1.6 Watchdog timers (WDT, MCWDT)

CYW20829 has one WDT and two multi-counter WDTs (MCWDTs). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can do interrupt/wakeup generation in system LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can do periodic interrupt/wakeup generation in system LP/ULP and Deep Sleep power modes.

7.1.7 Clock dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are one or more:

- 8-bit clock dividers
- 16-bit integer clock dividers
- 16.5-bit fractional clock dividers
- 24.5-bit fractional clock divider

7.1.8 Trigger routing

CYW20829 contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers”, which connect a specific source to a destination. The user can enable or disable the route.

7.1.9 Reset

CYW20829 can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DDD} and generate a reset if V_{DDD} falls below the minimum required logic operating voltage.
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active LOW. It can be connected either to a pull-up resistor to V_{DDD}, or to an active drive circuit, as **Figure 10** shows. If a pull-up resistor is used, select its value to minimize current draw when the pin is pulled LOW; 10 kΩ is typical.

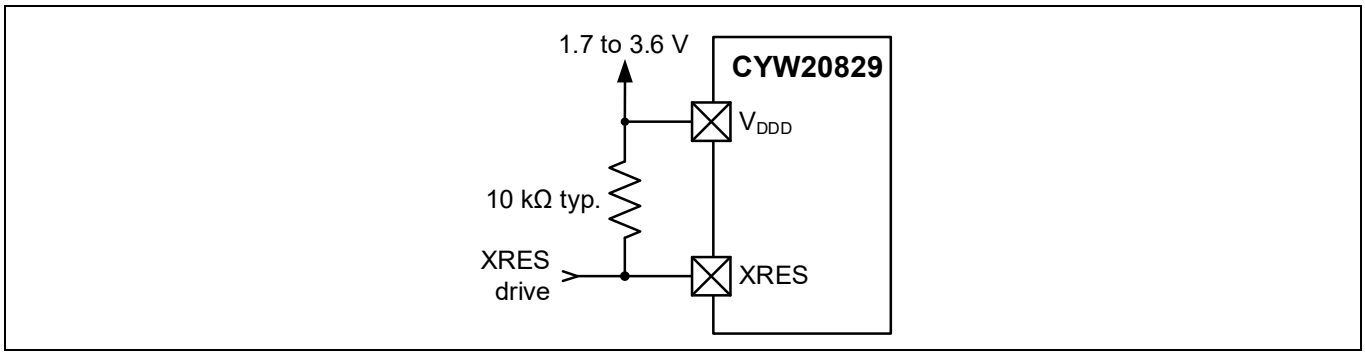


Figure 10 XRES connection diagram

- Watchdog Timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the system Hibernate low-power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

7.2 Bluetooth® LE radio and subsystem

CYW20829 incorporates a Bluetooth® 5.4 LE subsystem (BLESS) that contains the physical layer (PHY) and link layer (LL) engines with an embedded security engine. The Bluetooth® LE SS supports all Bluetooth® LE 5.4 features including LE 2 Mbps, LE Long Range, LE Advertising Extensions, LE Isochronous Channels, Periodic Advertising with Responses (PAwR), Encrypted Advertising Data, LE GATT Security Levels Characteristic and Advertising Coding Selection.

The physical layer consists of the digital PHY and the RF transceiver that transmits and receives Gaussian frequency shift keying (GFSK) packets at 1 or 2 Mbps over a 2.4 GHz ISM band, The device also supports Bluetooth® LE long range, both 500 and 125 kbps speeds.

The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50 Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it through the antenna.

7.3 Programmable analog-to-digital converter (ADC)

7.3.1 Sigma delta ADC

The ADC block is a single switched-cap Σ-Δ ADC core for audio and DC measurement. It operates at the 12-MHz clock rate and has 32 DC input channels, including eight GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC.

One of three internal references may be used for the ADC reference voltage: V_{DDA}, $V_{DDA/2}$, and an analog reference (AREF). AREF is nominally 1.2 V, trimmed to ±1%.

7.4 Programmable digital

- System Deep Sleep operation
- Asynchronous or synchronous (clocked) operation
- Can be synchronous or asynchronous

7.5 Fixed-function digital

7.5.1 Timer/counter/pulse-width modulator (TCPWM) block

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes
- Clock pre-scaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count - Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare - The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Two 32-bit TCPWMs
- Seven 16-bit TCPWMs

7.5.2 Serial communication blocks (SCB)

- This product line has three SCBs:
  - First SCB: Configurable as SPI or I^2C
  - Second SCB: Configurable as SPI or UART
  - Third SCB: Configurable as I^2C or UART
- One SCB (SCB #0) can operate in system Deep Sleep mode with an external clock; this SCB can be either SPI slave or I^2C slave.
- **I^2C mode:** The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI2C, which creates a mailbox address range and effectively reduces I^2C communication to reading from and writing to an array in the memory. The SCB supports a 256-byte FIFO for receive and transmit.
  The I^2C peripheral is compatible with I^2C standard-mode, Fast Mode, and Fast Mode Plus devices. The I^2C bus I/O is implemented with GPIO in open-drain modes.
- **UART mode:** This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO 7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.
- **SPI mode:** The SPI mode supports full SPI, Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and Microwire (half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with a 4-MHz clock.

7.5.3 QSPI interface serial memory interface (SMIF)

A serial memory interface is provided, running at up to 48 MHz. It supports single, dual and quad SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute-in-Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the CYW20829 internal address space, enabling code execution directly from the external memory. To improve performance, a 32 KB cache is included. XIP mode also supports AES-128 based on-the-fly encryption and decryption, enabling secure storage and access of code and data in the external memory.

7.6 GPIO

CYW20829 has up to 32 GPIOs, which implement:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled) on some IOs
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
  - Hold mode for latching previous state (used for retaining the I/O state in system Hibernate and deep sleep mode)
  - Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to eight pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 4 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than V_{DDD}. OVT pins are commonly used with I^2C, to allow powering the chip OFF while maintaining a physical connection to an operating I^2C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see **"Electrical characteristics"** on page 39.

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

In order to get the best performance, the following frequency and drive mode constraints may be applied. The DRIVE_SEL values (refer to **Table 11**) represent drive strengths.

Table 11 DRIVE_SEL values

Ports	Maximum frequency	Drive strength for V_{DDD} 2.7 V	Drive strength for V_{DDD} > 2.7 V
Ports 0, 1	8 MHz	DRIVE_SEL 2	DRIVE_SEL 3
Ports 2 to 5	16 MHz; 24 MHz for SPI	DRIVE_SEL 2	DRIVE_SEL 3

7.7 Special-function peripherals

7.7.1 Audio subsystem

This subsystem consists of the following hardware blocks:

- One inter-IC sound (I^2S) interface
- Two pulse-density modulation (PDM) to pulse-code modulation (PCM) decoder channels

The I^2S interface implements two independent hardware FIFO buffers - TX and RX, which can operate in master or slave mode. The following features are supported:

- Multiple data formats - I^2S, left-justified, Time Division Multiplexed (TDM) mode A, and TDM mode B
- Programmable channel/word lengths - 8/16/18/20/24/32 bits
- Internal/external clock operation. Up to 192 ksps
- Interrupt mask events - trigger, not empty, full, overflow, underflow, watchdog
- Configurable FIFO trigger level with datawire support

The I^2S interface is commonly used to connect with audio codecs, simple DACs, and digital microphones.

The PDM-to-PCM decoder implements a single hardware Rx FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length - 16/18/20/24 bits
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksps
- Programmable high-pass filter gain
- Interrupt mask events - not empty, overflow, trigger, underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM data line.

Each port pin has multiple alternate functions. These are defined in **Table 13**.

Table 13 Multiple alternate functions[6]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P0.0		tcpwm[0].line_compl[0]:3	tcpwm[0].line_compl[262]:0						pdm.pdm_clk[1]:0			tdm.tdm_tx_mck[0]:0	tdm.tdm_rx_mck[0]:0			keyscan.ks_col[2]			scb[0].spi_select1:0	
P0.1		tcpwm[0].line[1]:3	tcpwm[0].line[256]:1						pdm.pdm_data[1]:0			tdm.tdm_tx_sck[0]:0				keyscan.ks_col[3]			scb[0].spi_select2:0	
P0.2		tcpwm[0].line_compl[1]:3	tcpwm[0].line_compl[256]:1							peri.tr_io_input[4]:0		tdm.tdm_tx_fsync[0]:0				keyscan.ks_col[11]	scb[0].i2c_scl:0		scb[0].spi_mosi:0	
P0.3		tcpwm[0].line[0]:4	tcpwm[0].line[257]:1					scb[1].spi_select3:0				tdm.tdm_tx_sd[0]:0				keyscan.ks_col[12]	scb[0].i2c_sda:0		scb[0].spi_miso:0	
P0.4		tcpwm[0].line_compl[0]:4	tcpwm[0].line_compl[257]:1	srss.ext_clk:0	cpuss.trace_data[3]:1			scb[1].spi_select2:0		peri.tr_io_input[0]:0		tdm.tdm_rx_sck[0]:0				keyscan.ks_row[0]			scb[0].spi_clk:0	
P0.5		tcpwm[0].line[1]:4	tcpwm[0].line[258]:1		cpuss.trace_data[2]:1			scb[1].spi_select1:0		peri.tr_io_input[1]:0		tdm.tdm_rx_fsync[0]:0			smif.spihb_select1	keyscan.ks_row[1]			scb[0].spi_select0:0	
P1.0		tcpwm[0].line_compl[1]:4	tcpwm[0].line_compl[258]:1		cpuss.trace_data[1]:1	scb[1].uart_cts:0		scb[1].spi_select0:0			peri.tr_io_output[0]:0	tdm.tdm_rx_sd[0]:0				keyscan.ks_row[2]		cpuss.swj_swo_tdo		
P1.1		tcpwm[0].line[0]:5	tcpwm[0].line[259]:1		cpuss.trace_data[0]:1	scb[1].uart_rts:0		scb[1].spi_clk:0			peri.tr_io_output[1]:0					keyscan.ks_row[3]		cpuss.swj_swdoe_tdi		
P1.2		tcpwm[0].line_compl[0]:5	tcpwm[0].line_compl[259]:1		cpuss.trace_clock:1	scb[1].uart_rx:0	scb[2].i2c_scl:1	scb[1].spi_mosi:0		peri.tr_io_input[2]:0						keyscan.ks_row[4]		cpuss.swj_swdio_tms		
P1.3		tcpwm[0].line[1]:5	tcpwm[0].line[260]:1			scb[1].uart_tx:0	scb[2].i2c_sda:1	scb[1].spi_miso:0		peri.tr_io_input[3]:0						keyscan.ks_row[5]		cpuss.clk_swj_swclk_tclk		
P1.4		tcpwm[0].line_compl[1]:5	tcpwm[0].line_compl[260]:1								lin[0].lin_en[1]:0					keyscan.ks_col[4]				
P1.5		tcpwm[0].line[0]:6	tcpwm[0].line[261]:1								lin[0].lin_rx[1]:0					keyscan.ks_col[5]				
P1.6		tcpwm[0].line_compl[0]:6	tcpwm[0].line_compl[261]:1								lin[0].lin_tx[1]:0					keyscan.ks_col[6]	srss.cal_wave			
P2.0															smif.spihb_select0					
P2.1															smif.spihb_data3					
P2.2															smif.spihb_data2					
P2.3															smif.spihb_data1					

Note
6. The notation for a signal is of the form IPName[x].signal_name[u]:y.
IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize utilization of on-chip resources.

Table 13 Multiple alternate functions[6] *(continued)*

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P2.4															smif. spihb_ data0					
P2.5															smif. spihb_ clk					
P3.0	adcmic. gpio_ adc_in[0]	tcpwm[0]. line[0]:0	tcpwm[0]. line[256]:0		cpuss. trace_ data[3]:0	scb[2]. uart_cts:0		scb[1].spi_ select0:1						btss. uart_ cts:0		keyscan. ks_col[13]				
P3.1	adcmic. gpio_ adc_in[1]	tcpwm[0]. line_ compl[0]:0	tcpwm[0]. line_ ompl[256]:0		cpuss. trace_ data[2]:0	scb[2]. uart_rts:0		scb[1].spi_ clk:1			lin[0].lin_ en[0]:0			btss. uart_ rts:0		keyscan. ks_col[14]		cpuss.rst_ swj_trstn		
P3.2	adcmic. gpio_ adc_in[2]	tcpwm[0]. line[1]:0	tcpwm[0]. line[257]:0		cpuss. trace_ data[1]:0	scb[2]. uart_rx:0	scb[2].i2c_ scl:0	scb[1].spi_ mosi:1	pdm. pdm_ clk[0]:0	peri.tr_io_ input[6]:0	lin[0].lin_ rx[0]:0	canfd[0]. ttcan_rx[0]	adcmic. clk_pdm:0	btss. uart_ rxd:0		keyscan. ks_col[15]				
P3.3	adcmic. gpio_ adc_in[3]	tcpwm[0]. line_ compl[1]:0	tcpwm[0]. line_ ompl[257]:0		cpuss. trace_ data[0]:0	scb[2]. uart_tx:0	scb[2].i2c_ sda:0	scb[1].spi_ miso:1	pdm. pdm_ data[0]:0	peri.tr_io_ input[7]:0	lin[0].lin_ tx[0]:0	canfd[0]. ttcan_tx[0]	adcmic. pdm_ data:0	btss. uart_ txd:0		keyscan. ks_col[16]				
P3.4	adcmic. gpio_ adc_in[4]	tcpwm[0]. line[0]:1	tcpwm[0]. line[258]:0		cpuss. trace_ clock:0			scb[1].spi_ select3:1								keyscan. ks_col[7]				
P3.5	adcmic. gpio_ adc_in[5]	tcpwm[0]. line_ compl[0]:1	tcpwm[0]. line_ ompl[258]:0					scb[1].spi_ select2:1								keyscan. ks_col[8]				
P3.6	adcmic. gpio_ adc_in[6]	tcpwm[0]. line[1]:1	tcpwm[0]. line[259]:0					scb[1].spi_ select1:1								keyscan. ks_col[9]				
P3.7	adcmic. gpio_ adc_in[7]	tcpwm[0]. line_ compl[1]:1	tcpwm[0]. line_ ompl[259]:0													keyscan. ks_col[10]				
P4.0		tcpwm[0]. line_ compl[1]:2	tcpwm[0]. line_ ompl[261]:0													keyscan. ks_row[6]	scb[0]. i2c_scl:1		scb[0]. spi_ mosi:1	
P4.1		tcpwm[0]. line[0]:3	tcpwm[0]. line[262]:0													keyscan. ks_row[7]	scb[0]. i2c_sda:1		scb[0]. spi_ miso:1	
P5.0/ WCO_OUT		tcpwm[0]. line[0]:2	tcpwm[0]. line[260]:0	srss.ext_ clk:1		scb[2]. uart_cts:1		scb[1].spi_ select0:2	pdm. pdm_ clk[0]:1				adcmic. clk_pdm:1	btss. uart_ cts:1		keyscan. ks_col[17]				
P5.1/ WCO_IN		tcpwm[0]. line_compl [0]:2	tcpwm[0]. line_ ompl[260]:0						pdm. pdm_ data[0]:1				adcmic. pdm_ data:1			keyscan. ks_col[0]				
P5.2		tcpwm[0]. line[1]:2	tcpwm[0]. line[261]:0													keyscan. ks_col[1]				

Note
6. The notation for a signal is of the form IPName[x].signal_name[u]:y.
IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize utilization of on-chip resources.

9 Power management unit

The Power management unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

9.1 RF power management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

9.2 Host controller power management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in Deep Sleep (HIDOFF) mode.

9.3 BBC power management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth®-specified low-power connection mode. While in these low-power connection modes, the CYW20829B0-P4xxI100 runs on the low power oscillator and wakes up after a predefined time period.

The CYW20829B0-P4xxI100 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode

The CYW20829B0-P4xxI100 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF (Deep Sleep) mode, the CYW20829B0-P4xxI100 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

10 Electrical characteristics

Table 14 shows the maximum electrical ratings for voltages referenced to V_{DDIN} pad.

Table 14 Maximum electrical ratings

Rating	Symbol	Value	Unit
V_{DDIN}	–	3.795	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	
Operating ambient temperature range	T_{opr}	–30 to +85	°C
Storage temperature range	T_{stg}	–40 to +85	

Table 15 shows the power supply characteristics for the range T_J = 0°C to 125°C.

Table 15 Power supply

Parameter	Description	Min[7]	Typ	Max[7]	Unit
V_{DDIN}	Power supply input (CYW20829B0-P4xxI100)	2.75	–	3.6	V
V_{DDIN_RIPPLE}	Maximum power supply ripple for V_{DDIN} input voltage	–	–	100	mV

Table 16 shows the specifications for the digital voltage levels.

Table 16 Digital voltage levels

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.8	V
Input high voltage	V_{IH}	2.0	–	–	
Output low voltage	V_{OL}	–	–	0.4	
Output high voltage	V_{OH}	V_{DDIN} – 0.4	–	–	
Input capacitance (V_{DDMEM} domain)	C_{IN}	–	–	0.4	pF

Table 17 shows the current consumption measurements.

Note

7. Overall performance degrades beyond minimum and maximum supply voltages.The voltage range specified is determined by the minimum and maximum operating voltage of the SPI Serial Flash included on the module.

11 Chipset RF specifications

All specifications in **Table 18** are for industrial temperatures and are single-ended. Unused inputs are left open.

Table 18 Receiver RF specifications

Parameter	Conditions	Min	Typ[8]	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[9]	–	–	–98	–	–
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Interference performance					
TBD					
Out-of-band blocking performance (CW)[10]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000 MHz–2399 MHz	0.1% BER	–	–27	–	
2498 MHz–3000 MHz	0.1% BER	–	–27	–	
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	
Intermodulation performance[11]					
BT, Df = 4 MHz	–	–39.0	–	–	dBm
Spurious Emissions[12]					
30 MHz–1 GHz	–	–	–	–62	dBm
1 GHz–12.75 GHz	–	–	–	–47	
65 MHz–108 MHz	FM RX	–	–147	–	dBm/Hz
746 MHz–764 MHz	CDMA	–	–147	–	
851 MHz–894 MHz	CDMA	–	–147	–	
925 MHz–960 MHz	EDGE/GSM	–	–147	–	
1805 MHz–1880 MHz	EDGE/GSM	–	–147	–	
1930 MHz–1990 MHz	PCS	–	–147	–	
2110 MHz–2170 MHz	WCDMA	–	–147	–	

Notes

8. Typical operating conditions are 1.22-V operating voltage and 25°C ambient temperature.
9. The receiver sensitivity is measured at BER of 0.1% on the device interface.
10. Meets this specification using front-end band pass filter.
11. f0 = –64 dBm Bluetooth®-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth®-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n × 1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
12. Includes baseband radiated emissions.

Table 19 Transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class 1: GFSK TX power	–	–	10	–	dBm
Power control step	–	2	4	8	dB
Out-of-Band spurious emissions					
30 MHz to 1 GHz	–	–	–	–36.0[13]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[14]	
1.8 GHz to 1.9 GHz	–	–	–	–47.0	
5.15 GHz to 5.3 GHz	–	–	–	–47.0	

Table 20 Bluetooth® LE RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sense[15]	GFSK, 0.1% BER, 1 Mbps	–	–98	–	dBm
TX power	N/A	–	10	–	
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[16]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	

Notes

13.Maximum value is the value required for Bluetooth® qualification.
14.Meets this spec using a front-end band-pass filter.
15.Dirty TX is OFF.
16.At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

12 Timing and AC characteristics

In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

12.1 UART timing

Table 21 UART timing specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	1.50	Baud periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	0.67	
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	1.33	

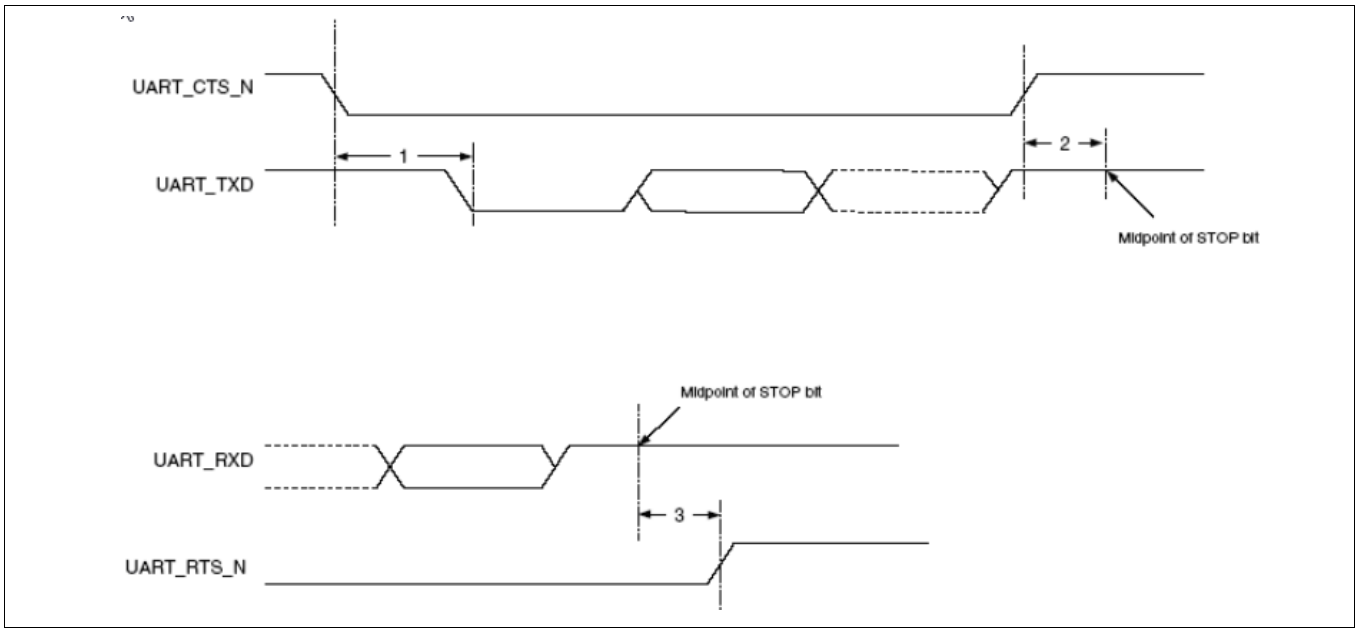


Figure 12 UART timing

12.2 SPI timing

The SPI interface supports clock speeds up to 12 MHz.

Table 22 and **Figure 13** show the timing requirements when operating in SPI Mode 0 and 2, and SPI Mode 1 and 3, respectively.

Table 22 SPI mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	
3	Time from master assert SPI_CSN to first clock edge	20	∞	
4	Setup time for MOSI data lines	8	½ SCK	
5	Hold time for MOSI data lines	8	½ SCK	
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	
8	Idle time between subsequent SPI transactions	1 SCK	∞	

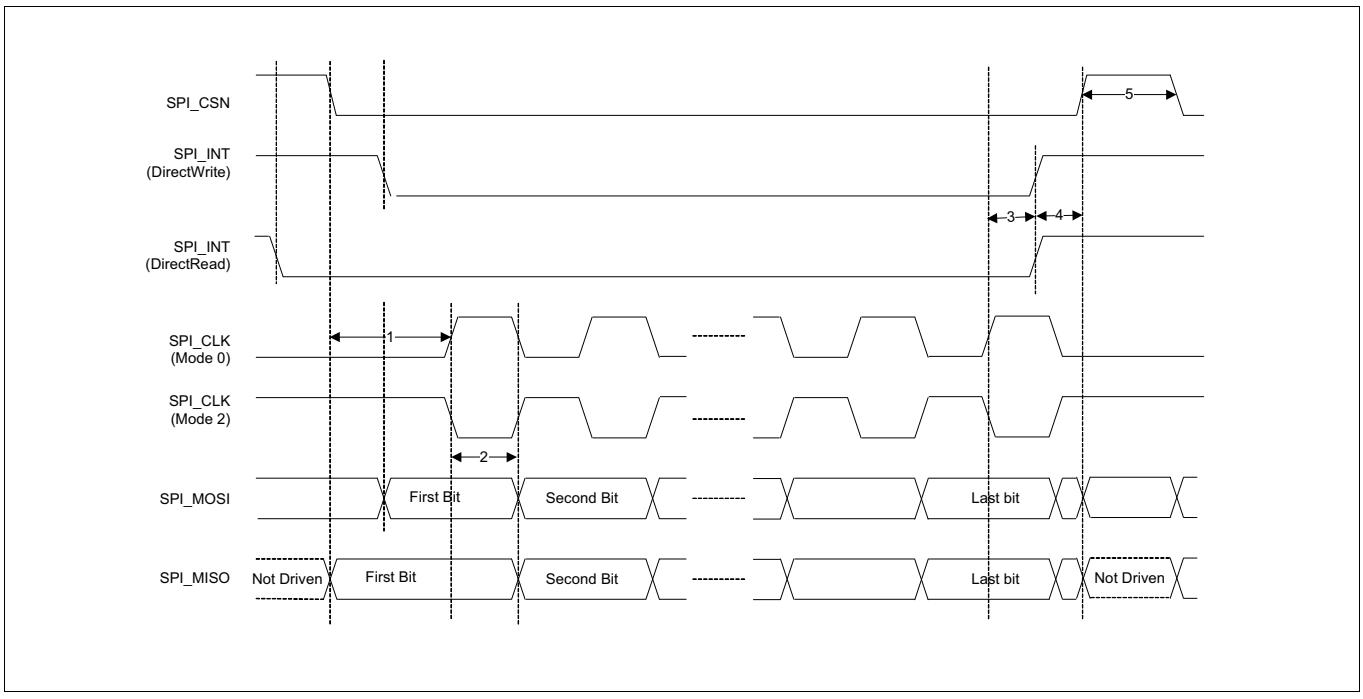


Figure 13 SPI timing – mode 0 and 2

Table 23 and **Figure 14** show the timing requirements when operating in SPI Mode 1 and 3.

Table 23 SPI mode 1 and 3

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	
5	Idle time between subsequent SPI transactions	1 SCK	–	

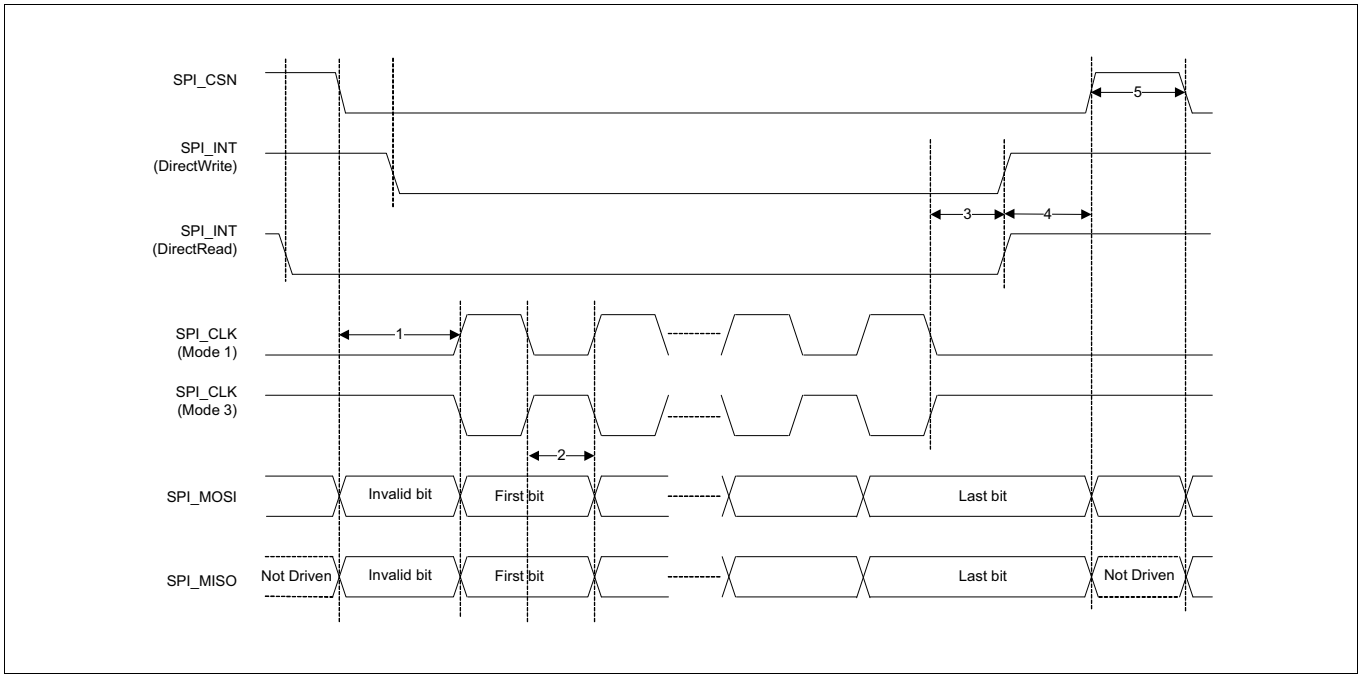


Figure 14 SPI timing – mode 1 and 3

12.3 I²C interface timing

Table 24 I²C interface timing specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	
4	Clock low time	650	–	
5	Clock high time	280	–	
6	Data input hold time[17]	0	–	
7	Data input setup time	100	–	
8	STOP condition setup time	280	–	
9	Output valid from clock	–	400	
10	Bus free time[18]	650	–	

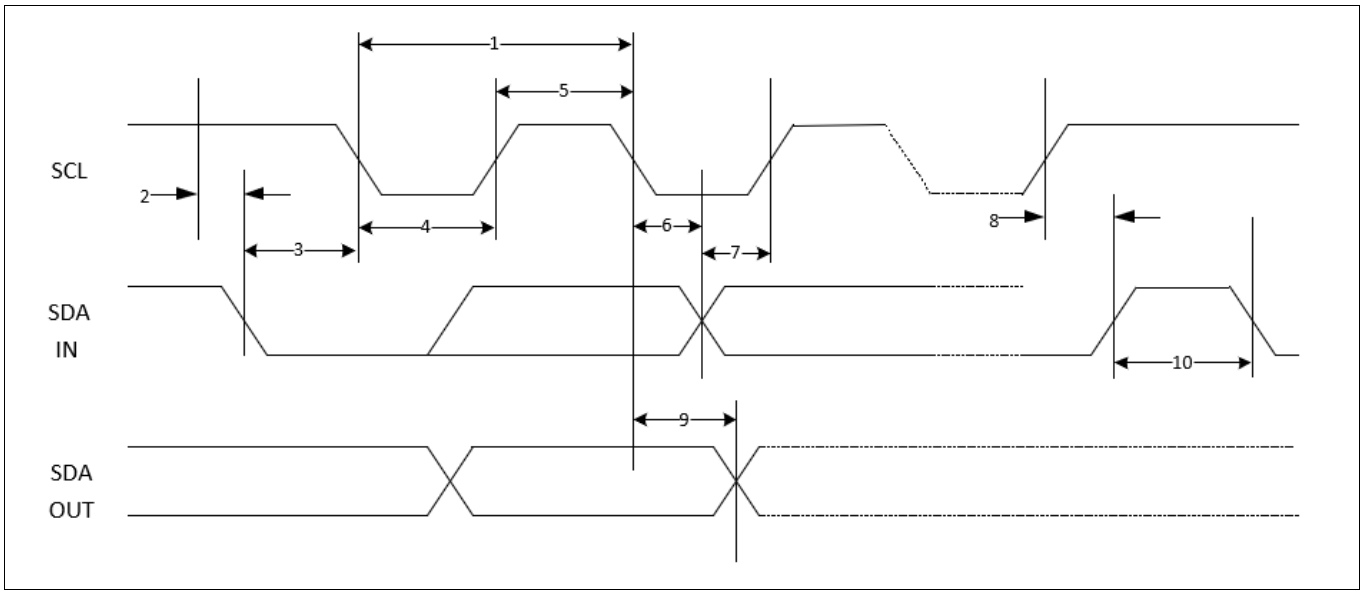


Figure 15 I²C Interface timing diagram

Notes

17. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
18. Time that the bus must be free before a new transaction can start.

Table 25 Timing for I²S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	19
Master mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	0.35 × T_{tr}	–	–	–	0.35 × T_{tr}	–	–	–	20
LOWt_{LC}	0.35 × T_{tr}	–	–	–	0.35 × T_{tr}	–	–	–	20
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	0.35 × T_{tr}	–	–	–	0.35 × T_{tr}	–	–	21
LOW t_{LC}	–	0.35 × T_{tr}	–	–	–	0.35 × T_{tr}	–	–	21
Rise time t_{RC}	–	–	0.15 × T_{tr}	–	–	–		–	22
Transmitter									
Delay t_{dtr}	–	–	–	0.8 × T	–	–	–	–	23
Hold time t_{htr}	0	–	–	–	–	–	–	–	22
Receiver									
Setup time t_{sr}	–	–	–	–	–	0.2 × T_r	–	–	24
Hold time t_{hr}	–	–	–	–	–	0	–	–	23

Note: The time periods specified in **Figure 16** and **Figure 17** are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Notes

19. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
20. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
21. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35 × T_r, any clock that meets the requirements can be used.
22. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than 0.15 × T_{tr}.
23. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
24. The data setup and hold time must not be less than the specified receiver setup and hold time.

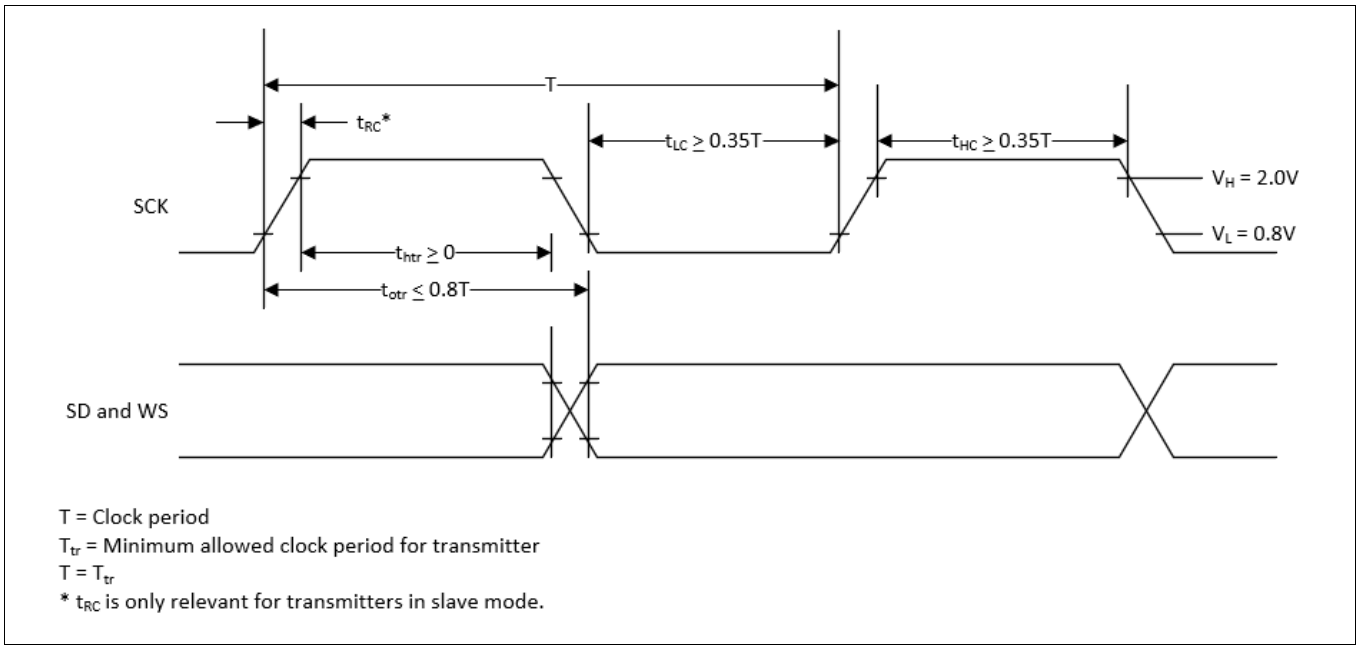


Figure 16 I²S transmitter timing

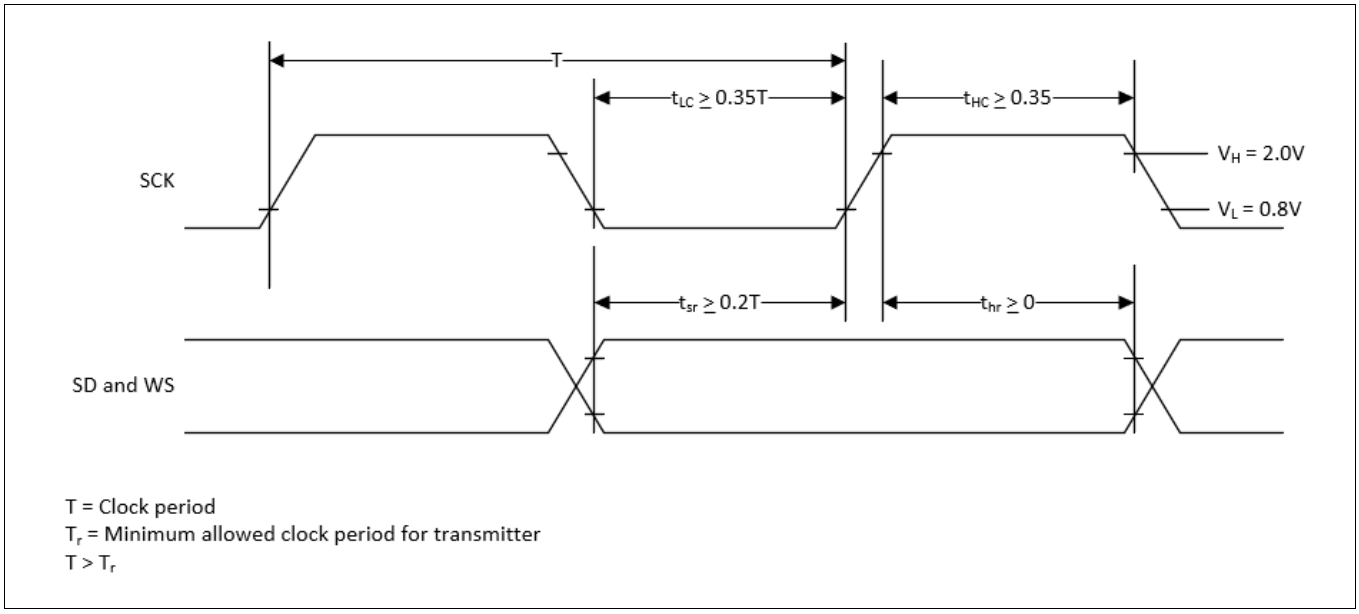


Figure 17 I²S receiver timing

13 Environmental specifications

13.1 Environmental compliance

This CYW20829B0-P4xxI100 Bluetooth® LE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Infineon module and components used to produce this module are RoHS and HF compliant.

13.2 RF certification

The CYW20829B0-P4xxI100 module will be certified under the following RF certification standards at production release.

- FCC: TBD
- CE
- IC: TBD
- MIC: TBD

13.3 Safety certification

The CYW20829B0-P4xxI100 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

13.4 Environmental conditions

Table 26 describes the operating and storage conditions for the Bluetooth® LE module.

Table 26 Environmental conditions for CYW20829B0-P4xxI100

Description	Minimum specification	Maximum specification
Operating temperature	–30°C	85°C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3°C/minute
Storage temperature	–40°C	85°C
Storage temperature and humidity	–	85°C at 85%
ESD: Module integrated into end system components[25]	–	15 kV Air 2.0 kV Contact

13.5 ESD and EMI protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note
25.This does not apply to the RF pins (ANT).

14 Regulatory information

14.1 FCC

FCC NOTICE:

The device CYW20829B0-P4xxI100 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Infineon may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

This module is only FCC authorized for the specific rule FCC 15.247 listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification, final host product requires Part 15 Subpart B compliance testing with the modular transmitter installed.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP829I10.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP829I10".

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in **Table 6**. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antenna in **Table 6**, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYW20829B0-P4xxI100 with the trace antenna is far below the FCC radio frequency exposure limits. Nevertheless, use CYW20829B0-P4xxI100 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 13 mm between the radiator and your body.

14.2 ISED

Innovation, Science and Economic Development Canada (ISED) Certification

CYW20829B0-P4xxI100 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development Canada (ISED),

License: IC: 7922A-829I10

Manufacturers of mobile, fixed, or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from **www.ic.gc.ca**.

This device has been designed to operate with the antennas listed in **Table 6**, having a maximum gain of –0.5 dBi. Antennas not included in this list or having a gain greater than –0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYW20829B0-P4xxI100 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYW20829B0-P4xxI100, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 16 mm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé. Cet équipement doit être installé et utilisé avec un minimum de 16 mm de distance entre la source de rayonnement et votre corps.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-829I10. In any case, the end product must be labeled in its exterior with “Contains IC: 7922A-829I10”

14.3 European declaration of conformity

Hereby, Infineon declares that the Bluetooth® module CYW20829B0-P4xxI100 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

All versions of the CYW20829B0-P4xxI100 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

14.4 MIC Japan

CYW20829B0-P4xxI100 is certified as a module with certification number TBD. End products that integrate CYW20829B0-P4xxI100 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

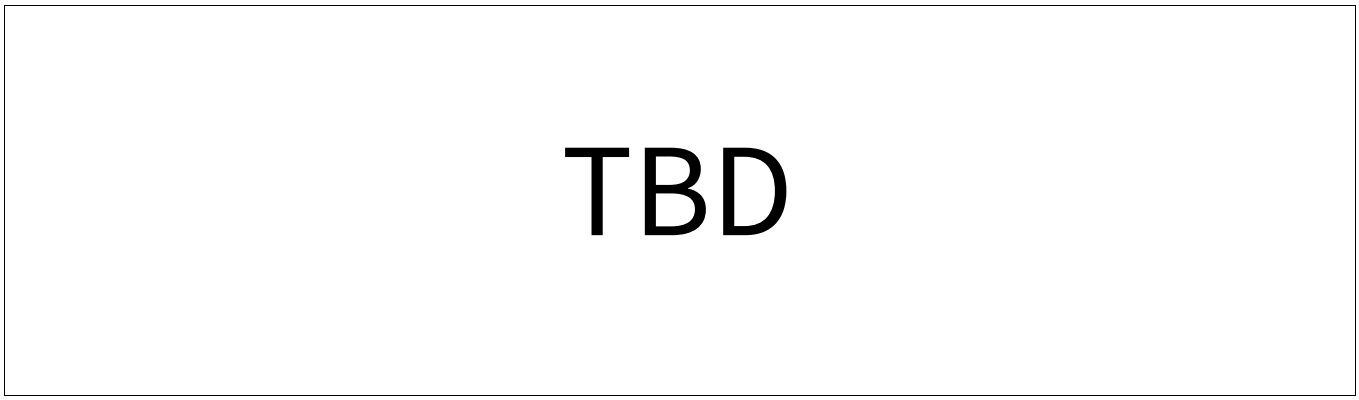


Figure 18 MIC label

15 Packaging

Table 27 Solder Reflow peak temperature

Module part number	Package	Maximum peak temperature	Maximum time at peak temperature	No. of cycles
CYW20829B0-P4TAI040	41-pad SMT	260°C	30 seconds	2
CYW20829B0-P4EPI040	41-pad SMT	260°C	30 seconds	2

Table 28 Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module part number	Package	MSL
CYW20829B0-P4TAI040	41-pad SMT	MSL 3
CYW20829B0-P4EPI040	41-pad SMT	MSL 3

The CYW20829B0-P4xxI100 is offered in tape and reel packaging. **Figure 19** details the tape dimensions used for the CYW20829B0-P4xxI100.

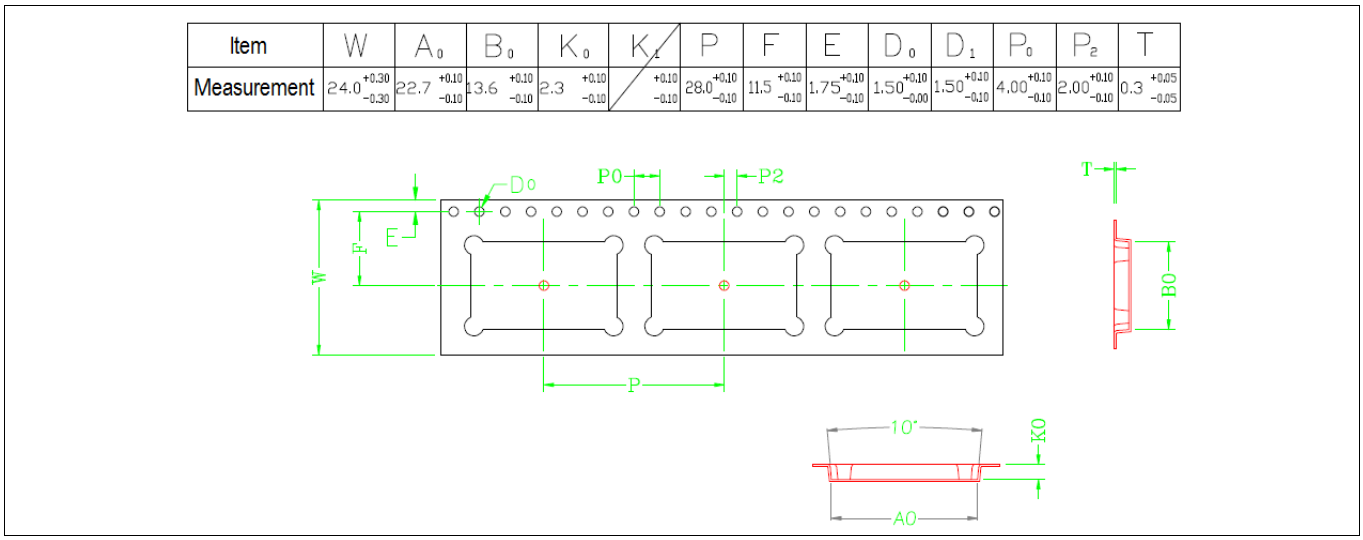


Figure 19 CYW20829B0-P4xxI100 tape dimensions

Figure 20 details the orientation of the CYW20829B0-P4xxI100 in the tape as well as the direction for unreeling.

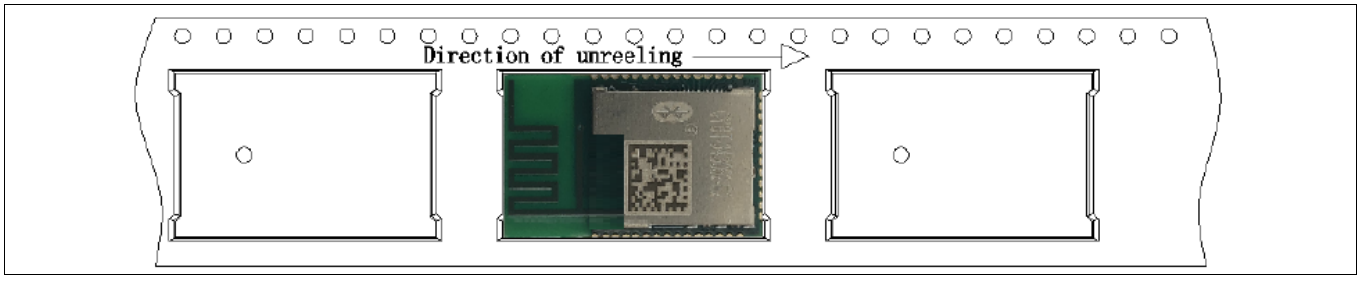
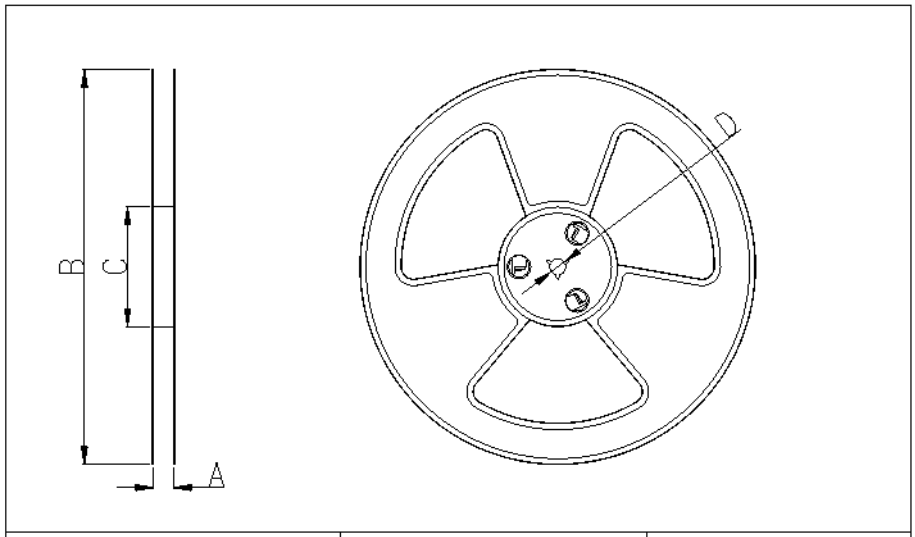


Figure 20 Component orientation in tape and unreeling direction

Figure 21 details reel dimensions used for the CYW20829B0-P4xxI100.



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.5	+0.5mm	−0.5mm
B	Reel Diameter	330.00	+1.5mm	−1.5mm
C	Outer Axis Diameter	100.00	+1.5mm	−1.5mm
D	Inner Axis Diameter	13.00	+0.5mm	−0.5mm

Figure 21 Reel dimensions

16 Ordering information

Table 29 lists the CYW20829B0-P4xxI100 part number and features. Table 30 lists the reel shipment quantities for the CYW20829B0-P4xxI100.

Table 29 Ordering information

Part number	CPU speed (MHz)	Flash size (KB)	RAM size (KB)	UART	I^2C (BSC)	PWM	Antenna	Package	Packaging
CYW20829B0-P4TAI040	96	1024	256	Yes	Yes	9	Trace	41-SMT	Tape and reel
CYW20829B0-P4EPI040	96	1024	256	Yes	Yes	9	Pad	41-SMT	Tape and reel

Table 30 Tape and reel package quantity and minimum order amount

Description	Minimum reel quantity	Maximum reel quantity	Comments
Reel quantity	500	500	Ships in 500 unit reel quantities.
Minimum order quantity (MOQ)	500	–	–
Order increment (OI)	500	–	–

The CYW20829B0-P4xxI100 is offered in tape and reel packaging. The CYW20829B0-P4xxI100 ships in a reel size of 500.

For additional information and a complete list of Infineon Wireless products, contact your local Infineon sales representative. To locate the nearest Infineon office, visit our website.

U.S. headquarters address	198 Champion Court, San Jose, CA 95134
U.S. headquarter contact info	(408) 943-2600
Website address	**https://www.infineon.com**

17 Acronyms

Table 31 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
ADV	advertising
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BLE	Bluetooth® Low Energy
Bluetooth® SIG	Bluetooth® Special Interest Group
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CE	European Conformity
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSA	Canadian Standards Association
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
ESD	electrostatic discharge
FCC	Federal Communications Commission
FET	field-effect transistor
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HCI	host controller interface
HVI	high-voltage interrupt, see also LVI, LVD
I/O	input/output, see also GPIO, DIO, SIO, USBIO
I2C, or IIC	Inter-Integrated Circuit, a communications protocol
IC	integrated circuit
IC	Industry Canada
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment

Table 31 Acronyms used in this document *(continued)*

Acronym	Description
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
KC	Korea Certification
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LNA	low noise amplifier
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MIC	Ministry of Internal Affairs and Communications (Japan)
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
Opamp	operational amplifier
PA	power amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset

Table 31 Acronyms used in this document *(continued)*

Acronym	Description
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QDID	qualification design ID
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
S/H	sample and hold
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I2C serial clock
SDA	I2C serial data
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
STN	super twisted nematic
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TN	twisted nematic
TRM	technical reference manual
TTL	transistor-transistor logic
TUV	Germany: Technischer Uberwachungs-Verein (Technical Inspection Association)
TX	transmit

Table 31 Acronyms used in this document *(continued)*

Acronym	Description
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

18 Document conventions

18.1 Units of measure

Table 32 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document version	Date of release	Description of changes
**	2023-12-20	Initial release.

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