CAMtasticDXP (TM):

Layers				Mid-Layer 2		

Impedance Requirements

Layer	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mil)	Trace Width (mil)	Trace Spacing (mil)	Trace Width (mil)	Trace Spacing (mil)
Mid-Layer2					

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.012mm	3.5	
3	Top Layer	Copper	0.035mm		
4	Dielectric1	FR4 0.2mm 35/35 copper	0.200mm	4.2	
5	Mid-Layer 1	Copper	0.035mm		
6	Dielectric2	FR4 0.22mm	0.220mm	4.2	
7	Mid-Layer 2	Copper	0.035mm		
8	Dielectric3	FR4 0.2mm 35/35 copper	0.200mm	4.2	
9	Signal Layer 1	Copper	0.035mm		
10	Dielectric 4	FR4 0.22mm	0.220mm	4.2	
11	Signal Layer 2	Copper			
12	Dielectric 5	FR4 0.2mm 00/35	0.200mm	4.2	
13	Bottom Layer	Copper	0.035mm		
14	Bottom Solder	Solder Resist	0.012mm	3.5	
15	Bottom Overlay				

Supplementary Note:
This board is formed creating a 4 layer board and then bonding bottom core and bot
the fabricated 4 layer board.
This process will create a 5 layer structure with 5 Cu layers and two drill hole pa
Once the 4 layer board is drilled , plating to 0.5 Oz Cu is required. The
bottom core and Cu are then bonded and drilled. Plated through holes should then
be plated to 0.5 Oz Cu (for the drill hole pairs between top and bottom layers). So
Silkscreen and chemical finishing should be
completed as final processing steps.

Note: board will go through (2) two 0.5 Oz plating processes.
Top & Bottom Layers: finished copper weight 35um +plating=60um

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg ☐ Metal Core ☐ Other ☐
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQU
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz ☐ 0.75oz ☐ 1oz ☐ Other ☐

5. FINISH - HASL (Lead) ☐ HASL ☐ Immersion Silver ☐ Immersion
Other ☐

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB (UC
- GREEN ☐ WHITE ☐ BLUE ☐ Other ☐

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM ☐ TOP ONLY ☐ BOTTOM ONLY ☐ NONE ☐
- WHITE ☐ BLACK ☐ Other ☐

8. IMPEDANCE CONTROL - NO ☐ YES ☐ SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DIM
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFE

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEP
IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION
TO DIMENSION GRAM

- CONFIDENTIAL -
THIS DRAWING CONTAINS PROPRIETARY INFORMATION
WHICH MAY NOT BE DISCLOSED TO OTHERS FOR ANY
PURPOSE WHATSOEVER OR USED FOR MANUFACTURING
PURPOSES WITHOUT PRIOR WRITTEN PERMISSION
FROM THE FUTURE ELECTRONICS CORPORATION.

Future Electronics — System
Future House
The Gloaty, Egham, SurreyUnited King
TW20 9AH

Designed by: Yves Francois	Drawn by: Yves Francois	Project #	Enersys RF Module
Checked by: David Woodcock	Approved by: David Woodcock	Title	6LA19470C
		Size: C	DWG NO: 6LA19470C
		Date:	19/04/2022