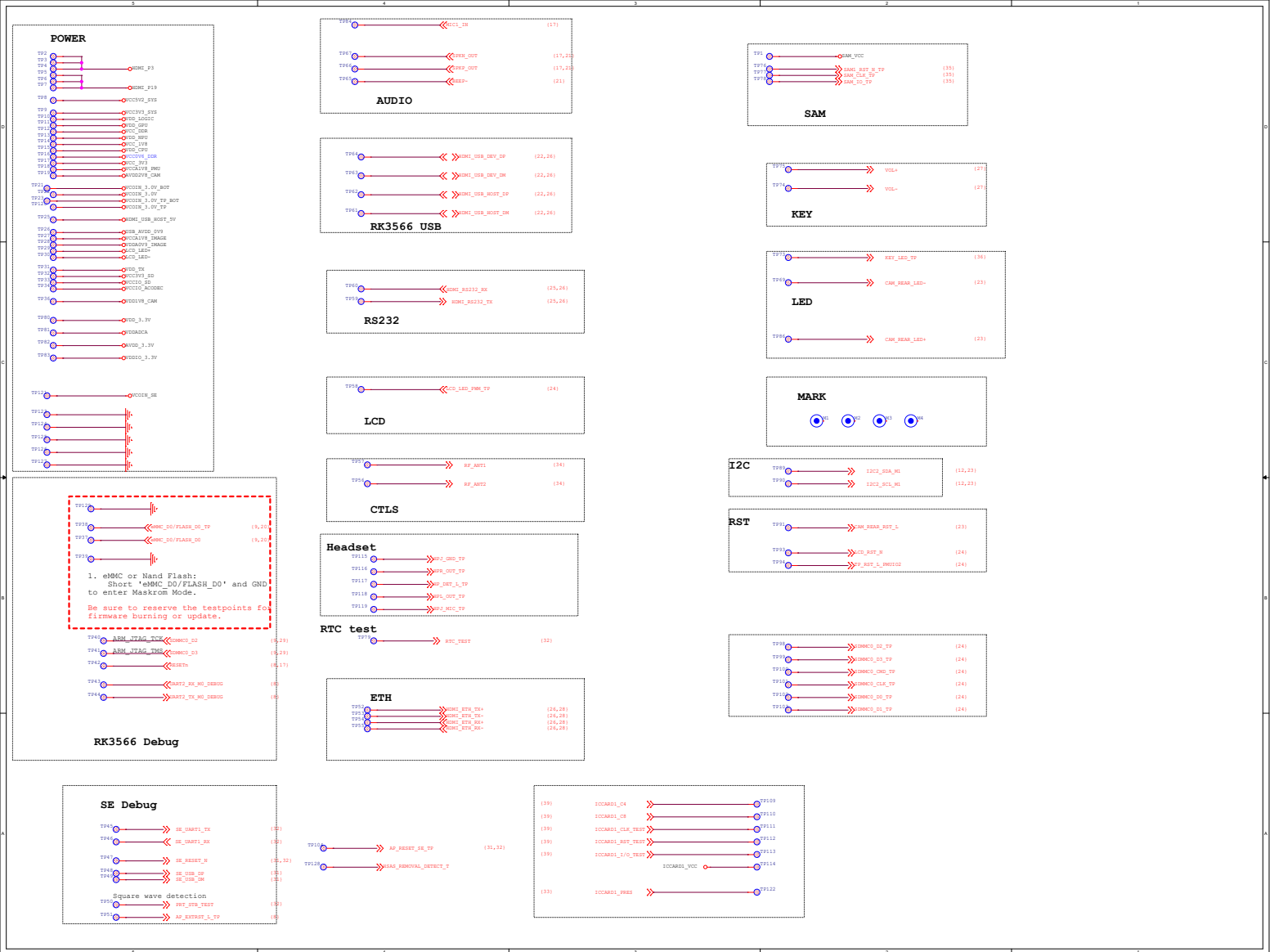
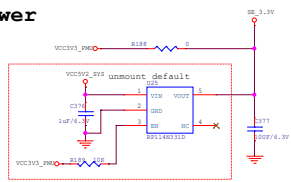
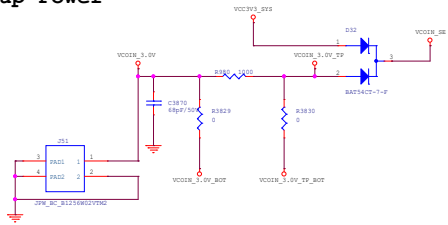




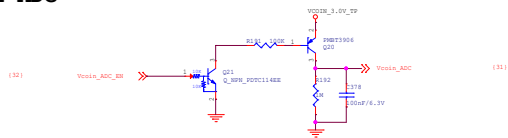
SE Power



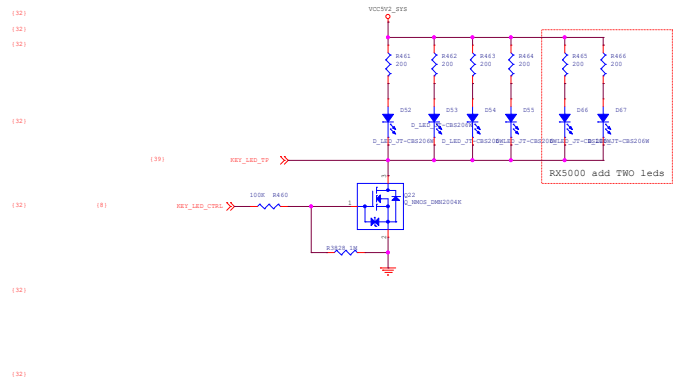
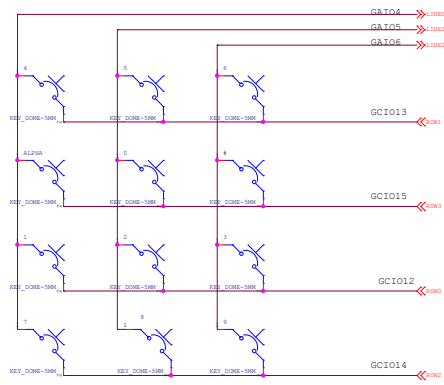
Backup Power



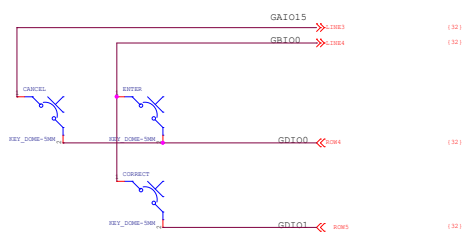
Vcoin ADC



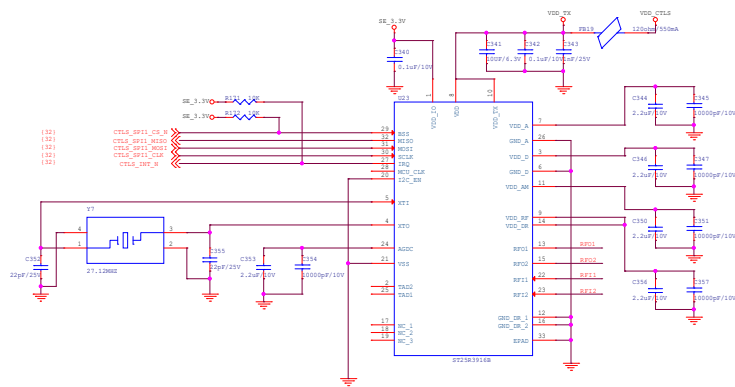
DIGITAL KEY



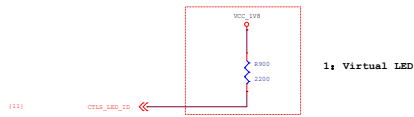
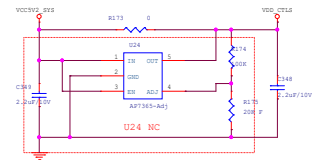
FUNC KEY



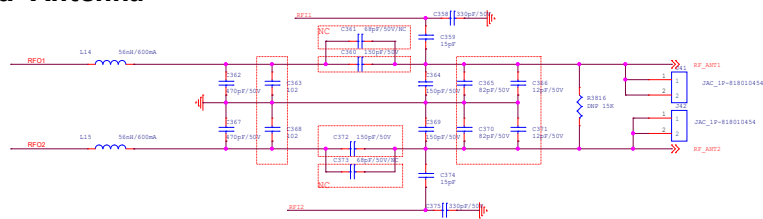
Contactless Card



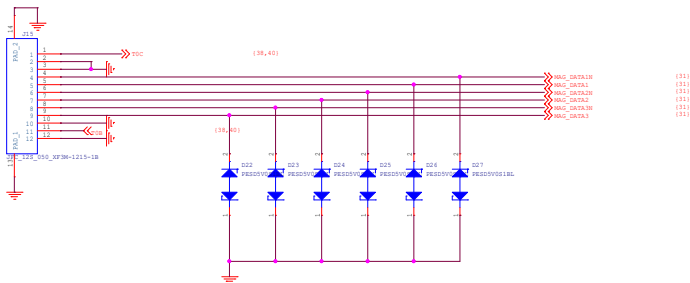
Contactless Card Power



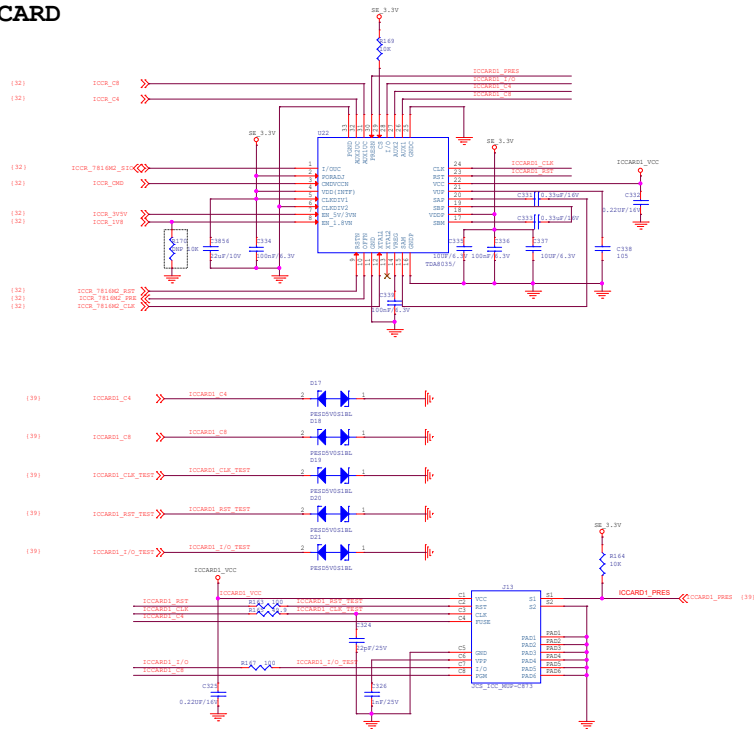
Contactless Card Antenna

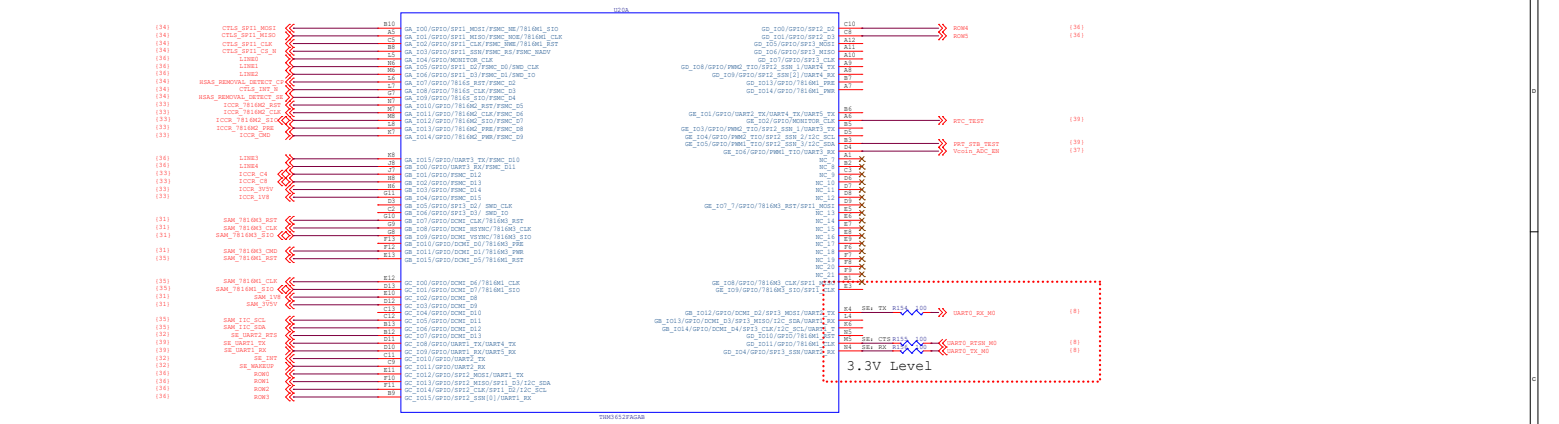


MAG

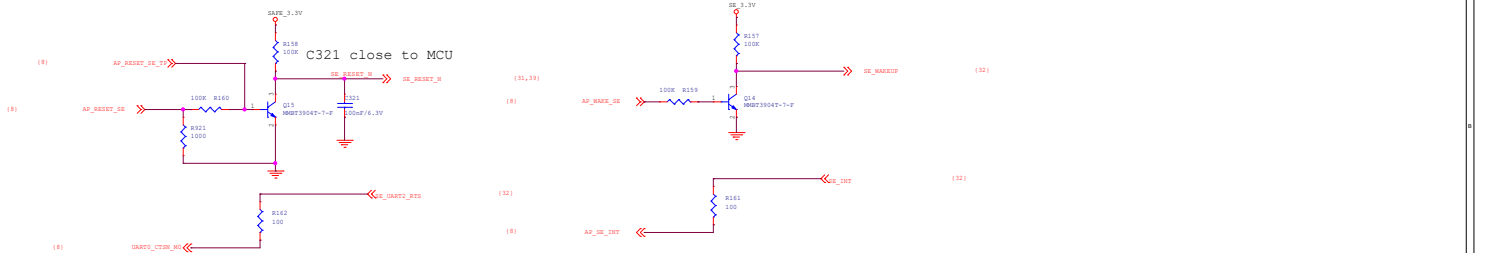


IC CARD

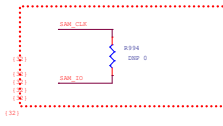
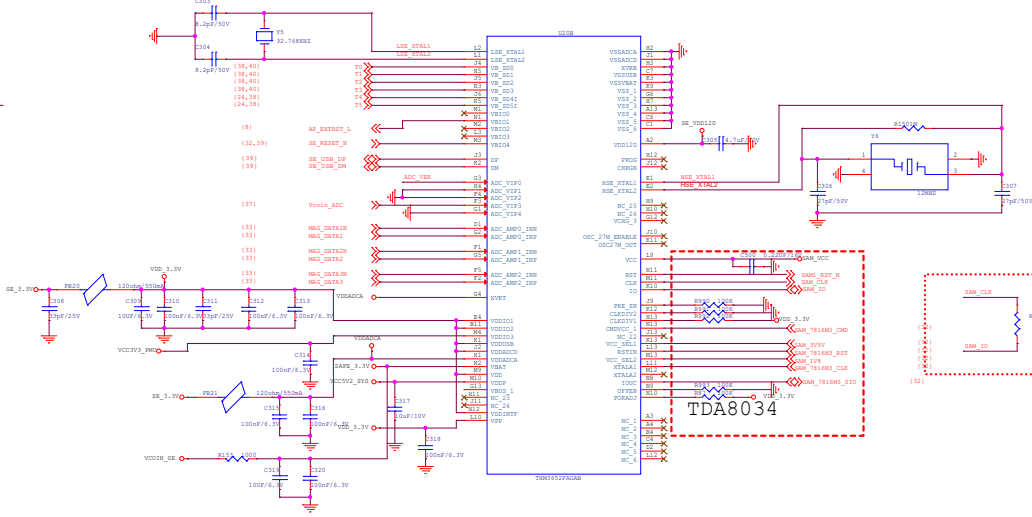
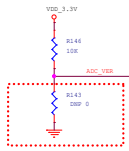




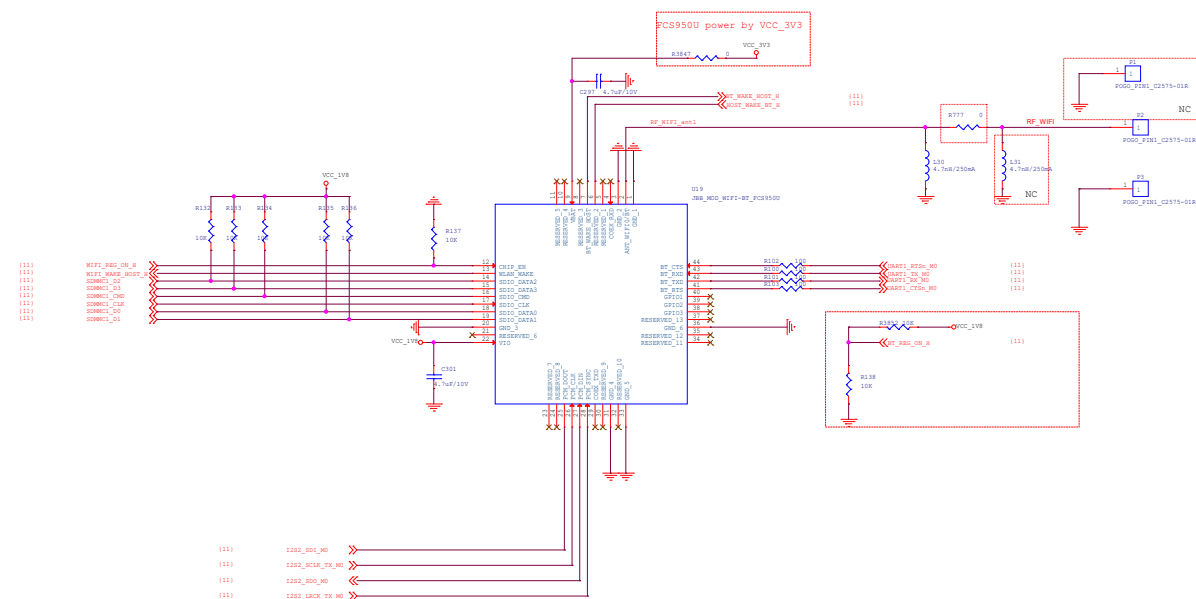
SE & AP Communication



SE MCU-1

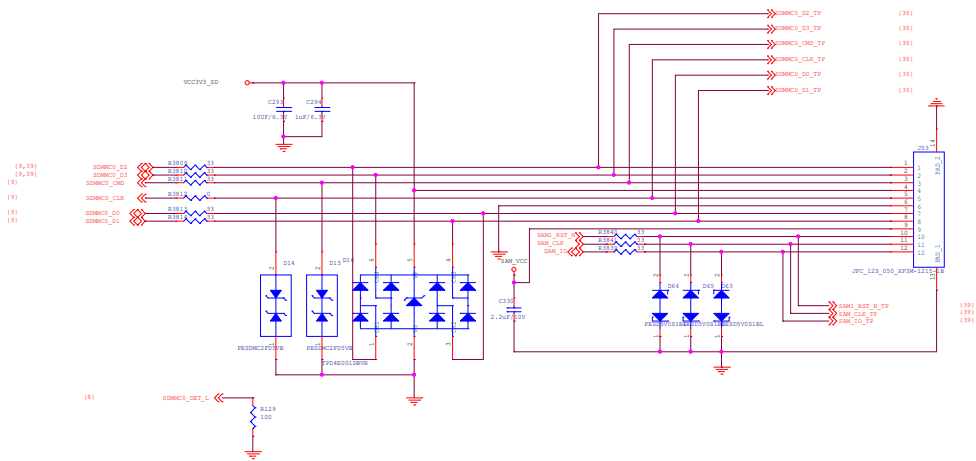


SDIO WIFI/BT Module



MicroSD Card

```
Note:
Take care of the type of MicroSD Card Jack,
The type here follow the logic below:
    DET is float @ card ejected; the internal pull up decided the IO pin status
    DET is connected to GND @ card inserted
If other type of Jack is used, need to shift the status of DET.
```



T0 sam-tf pcb

ADC KEY

The ADC KEY circuit diagram shows a differential input stage. The non-inverting input (VIN+) is connected to a voltage divider consisting of R109 (10k) and R108 (10k). The inverting input (VIN-) is connected to a voltage divider consisting of R104 (10k) and R105 (10k). The output of the op-amp is connected to R106 (10k) and the feedback pin. The circuit is powered by VCC+ and VCC-.

Key Name	ADC Value
VCC+/PWRCONV	9
VCC-	327

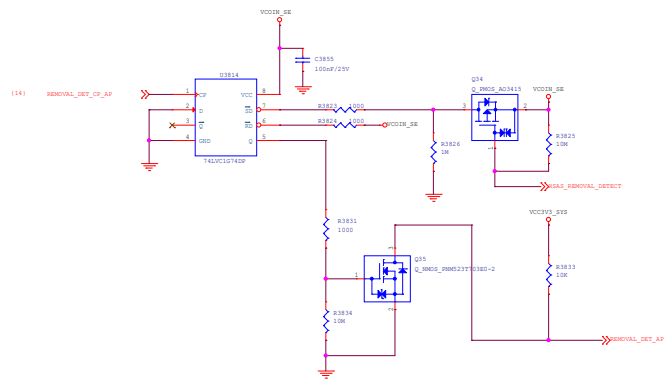
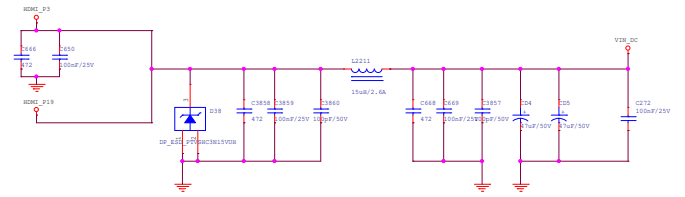
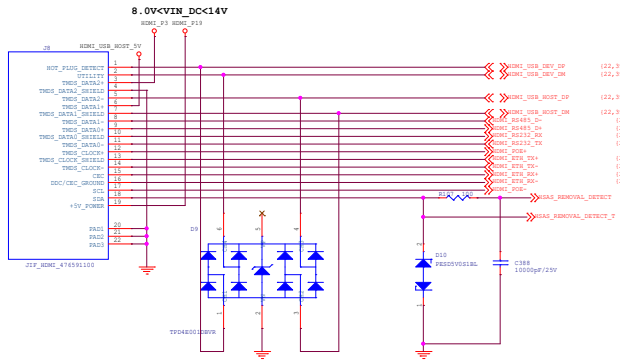
MFI

The MFI circuit diagram shows a differential input stage. The non-inverting input (VIN+) is connected to a voltage divider consisting of R109 (10k) and R108 (10k). The inverting input (VIN-) is connected to a voltage divider consisting of R104 (10k) and R105 (10k). The output of the op-amp is connected to R106 (10k) and the feedback pin. The circuit is powered by VCC+ and VCC-.

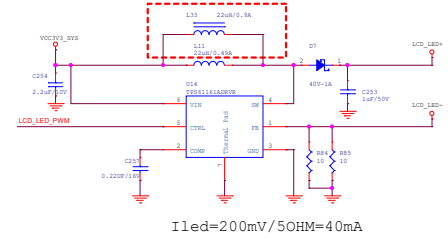
Proximity Sensor (option)

The Proximity Sensor (option) circuit diagram shows a differential input stage. The non-inverting input (VIN+) is connected to a voltage divider consisting of R109 (10k) and R108 (10k). The inverting input (VIN-) is connected to a voltage divider consisting of R104 (10k) and R105 (10k). The output of the op-amp is connected to R106 (10k) and the feedback pin. The circuit is powered by VCC+ and VCC-.

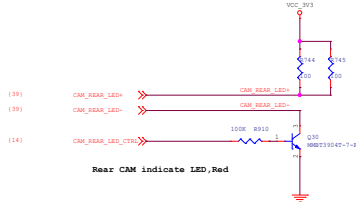
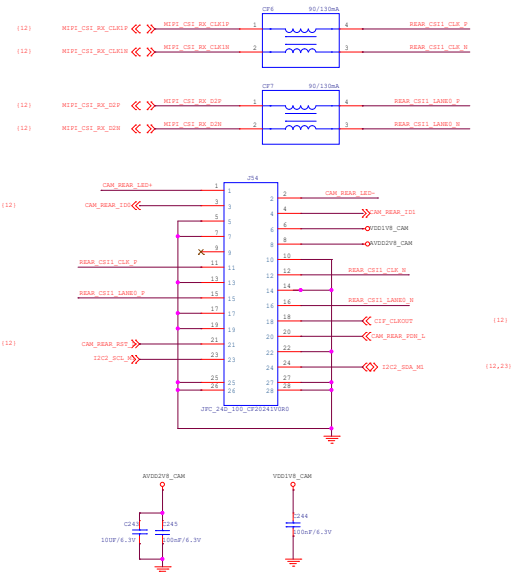
Cable Removal Detection



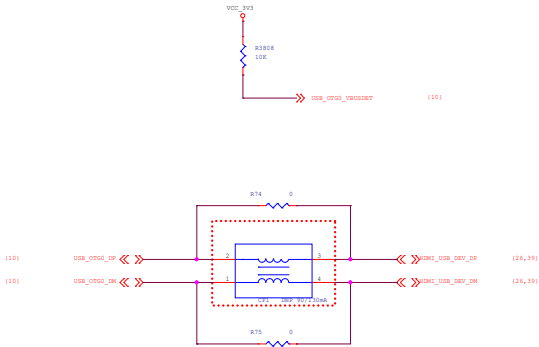
[illegible]



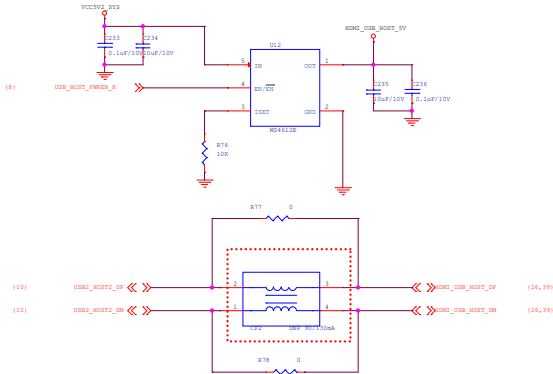
Rear Camera (option)



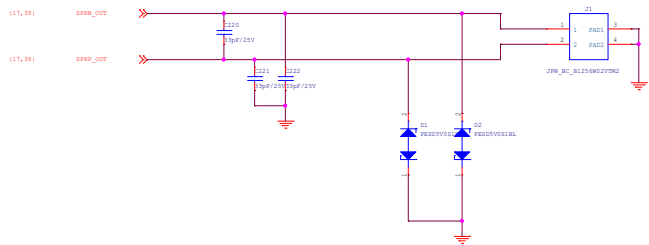
USB OTG0



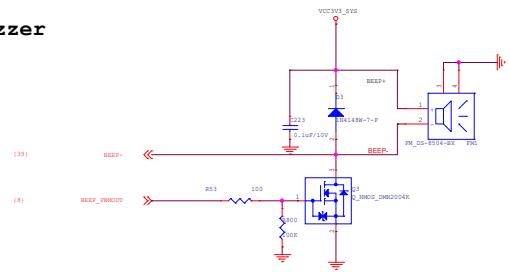
USB HOST2



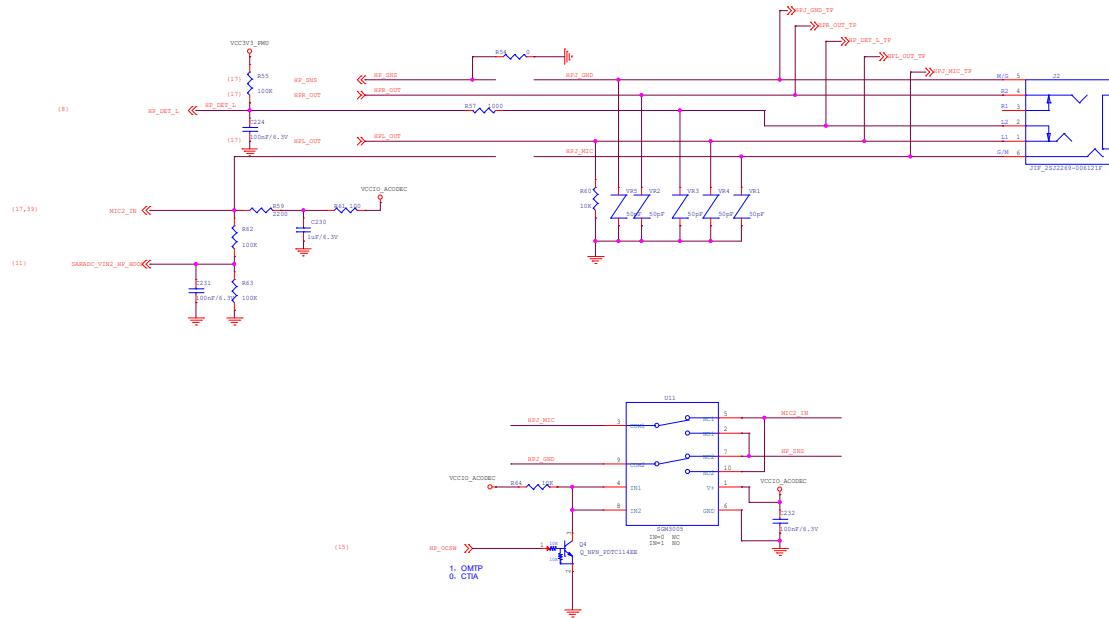
SPK



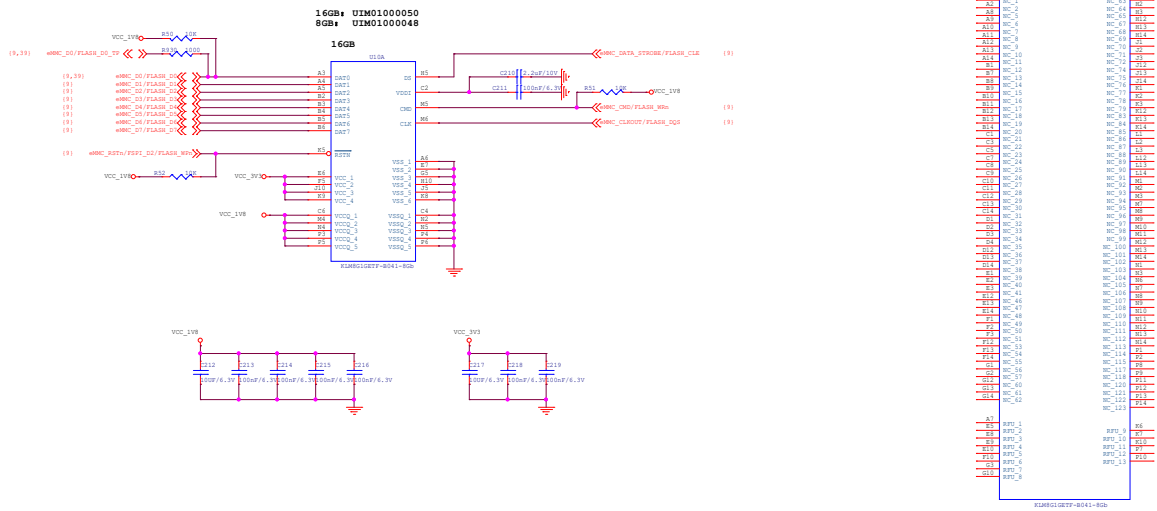
Buzzer



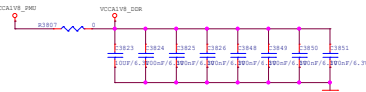
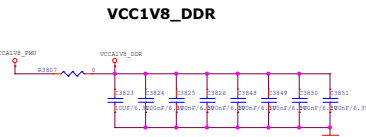
Headset



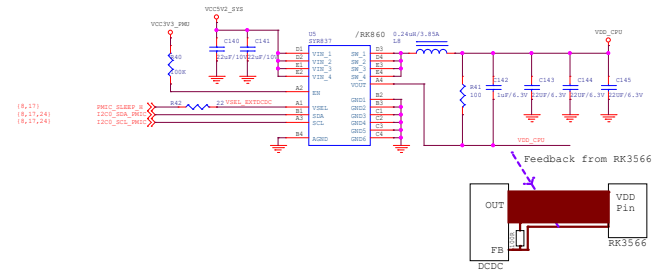
eMMC



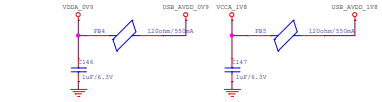
```
1GB: UIM04000032
2GB: UIM04000033
```



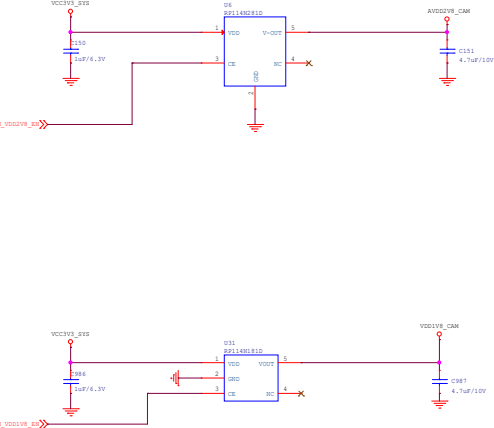
VDD_CPU_EXT



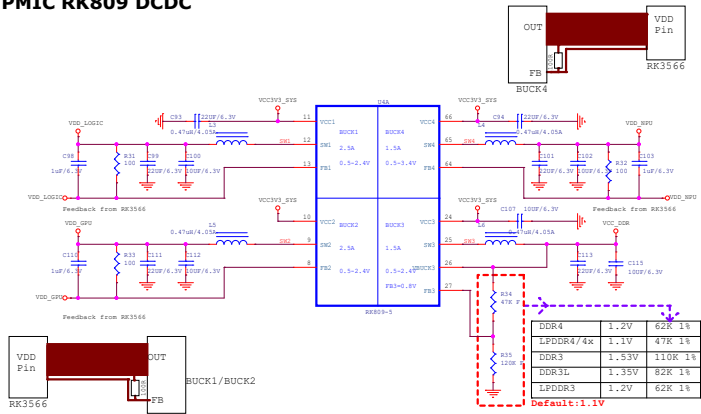
Power for USB



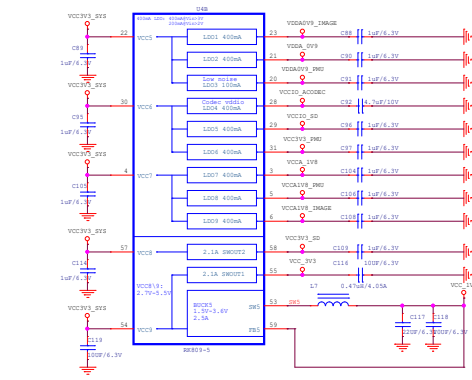
Power for Camera



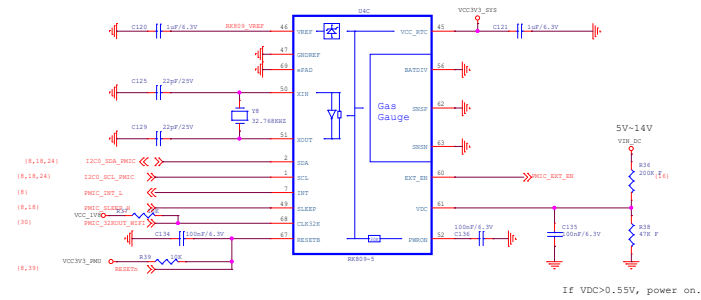
PMIC RK809 DCDC



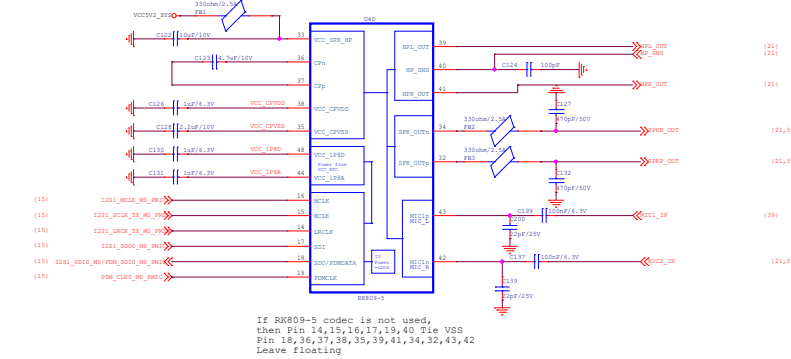
PMIC RK809 LDO



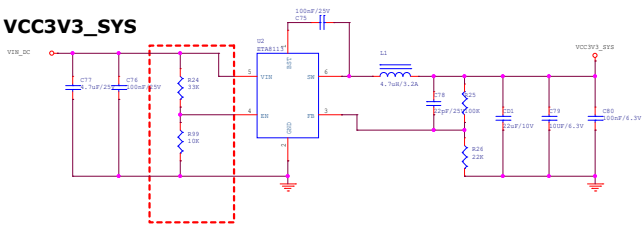
PMIC RK809 Management



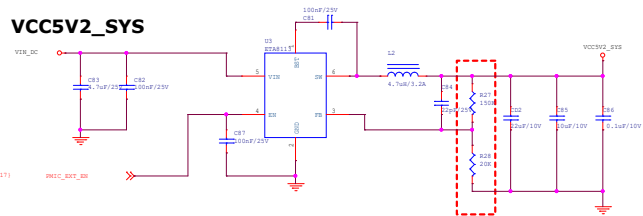
PMIC RK809 CODEC



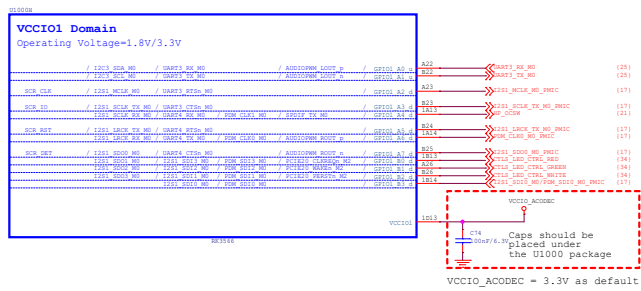
VCC3V3_SYS

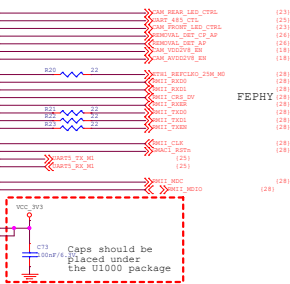


VCC5V2_SYS



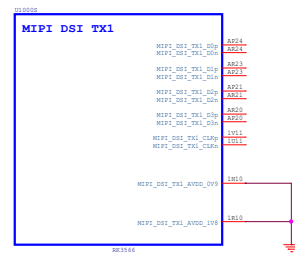
RK3566_H (VCCIO1 Domain)



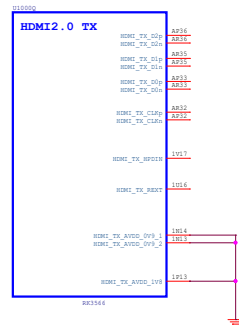
[illegible]

GMAC	Direction	GEPHY	GMAC	Direction	GEPHY
GMACx_TXD0	----->	PHYx_TXD0	GMACx_TXD0	----->	PHYx_TXD0
GMACx_TXD1	----->	PHYx_TXD1	GMACx_TXD1	----->	PHYx_TXD1
GMACx_TXD2	----->	PHYx_TXD2			
GMACx_TXD3	----->	PHYx_TXD3			
GMACx_TXEN	----->	PHYx_TXEN	GMACx_TXEN	----->	PHYx_TXEN
GMACx_TXCLK	----->	PHYx_TXCLK			
GMACx_RXD0	<-----	PHYx_RXD0	GMACx_RXD0	<-----	PHYx_RXD0
GMACx_RXD1	<-----	PHYx_RXD1	GMACx_RXD1	<-----	PHYx_RXD1
GMACx_RXD2	<-----	PHYx_RXD2			
GMACx_RXD3	<-----	PHYx_RXD3			
GMACx_RXDV	<-----	PHYx_RXDV	GMACx_RXDV	<-----	PHYx_CRS_DV
GMACx_RXCLK	<-----	PHYx_RXCLK			
GMACx_RXER	<-----		GMACx_RXER	<-----	PHYx_RXER
GMACx_MD0	<-----	PHYx_MD0	GMACx_MD0	<-----	PHYx_MD0
GMACx_MDIO	<-----	PHYx_MDIO	GMACx_MDIO	<-----	PHYx_MDIO
ETHX_TBSFCLK0_TSN	<-----	PHYx_XTALIN			
GMACx_MCLKINOUT	<-----	PHYx_CLKOUT125 (Option)	GMACx_MCLKINOUT	----->	PHYx_XTALIN/REFCLK
GPIO	<-----	PHYx_RSTn	GPIO	----->	PHYx_RSTn
GPIO	<-----	PHYx_INT/PMBE	GPIO	<-----	PHYx_INT/PMBE

	2
RK3566_S (MIPI_DSI_TX1)	



RK3566_Q (HDMI2.0 TX)



[illegible]

VCC_1V8

R1101 220k

R1102 220k

CC_INT

VCC_1V8

R11 220k

R13 220k

CC_INT

VCC_1V8

R200 220k

R200 220k

CC_INT

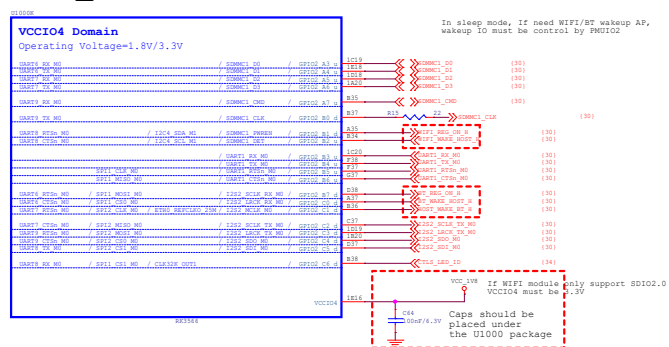
RX7000 only support DEVICE
CC_INT pull up, not CC_INT interrupt

```

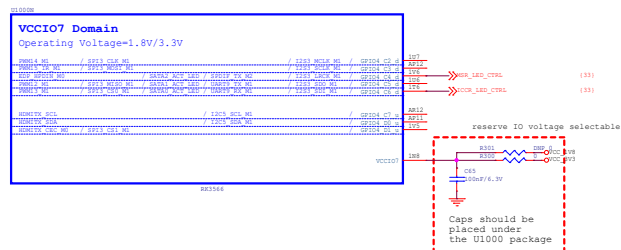
VCCIO0 Domain
Operating Voltage=1.8V/3.3V

CIP_W0 / BMC_W0000 / BMCW0_W0_M0 / 1250 MHz_M0 / VDD_W0000_W0_M0 / DT000_W0_M0
CIP_W1 / BMC_W0000 / BMCW0_W1_M1 / 1250 MHz_M1 / VDD_W0000_W1_M1 / DT000_W1_M1
CIP_W2 / BMC_W0000 / BMCW0_W2_M2 / 1250 MHz_M2 / VDD_W0000_W2_M2 / DT000_W2_M2
CIP_W3 / BMC_W0000 / BMCW0_W3_M3 / 1250 MHz_M3 / VDD_W0000_W3_M3 / DT000_W3_M3
CIP_W4 / BMC_W0000 / BMCW0_W4_M4 / 1250 MHz_M4 / VDD_W0000_W4_M4 / DT000_W4_M4
CIP_W5 / BMC_W0000 / BMCW0_W5_M5 / 1250 MHz_M5 / VDD_W0000_W5_M5 / DT000_W5_M5
CIP_W6 / BMC_W0000 / BMCW0_W6_M6 / 1250 MHz_M6 / VDD_W0000_W6_M6 / DT000_W6_M6
CIP_W7 / BMC_W0000 / BMCW0_W7_M7 / 1250 MHz_M7 / VDD_W0000_W7_M7 / DT000_W7_M7
CIP_W8 / BMC_W0000 / BMCW0_W8_M8 / 1250 MHz_M8 / VDD_W0000_W8_M8 / DT000_W8_M8
CIP_W9 / BMC_W0000 / BMCW0_W9_M9 / 1250 MHz_M9 / VDD_W0000_W9_M9 / DT000_W9_M9
CIP_W10 / BMC_W0000 / BMCW0_W10_M10 / 1250 MHz_M10 / VDD_W0000_W10_M10 / DT000_W10_M10
CIP_W11 / BMC_W0000 / BMCW0_W11_M11 / 1250 MHz_M11 / VDD_W0000_W11_M11 / DT000_W11_M11
CIP_W12 / BMC_W0000 / BMCW0_W12_M12 / 1250 MHz_M12 / VDD_W0000_W12_M12 / DT000_W12_M12
CIP_W13 / BMC_W0000 / BMCW0_W13_M13 / 1250 MHz_M13 / VDD_W0000_W13_M13 / DT000_W13_M13
CIP_W14 / BMC_W0000 / BMCW0_W14_M14 / 1250 MHz_M14 / VDD_W0000_W14_M14 / DT000_W14_M14
CIP_W15 / BMC_W0000 / BMCW0_W15_M15 / 1250 MHz_M15 / VDD_W0000_W15_M15 / DT000_W15_M15
CIP_W16 / BMC_W0000 / BMCW0_W16_M16 / 1250 MHz_M16 / VDD_W0000_W16_M16 / DT000_W16_M16
CIP_W17 / BMC_W0000 / BMCW0_W17_M17 / 1250 MHz_M17 / VDD_W0000_W17_M17 / DT000_W17_M17
CIP_W18 / BMC_W0000 / BMCW0_W18_M18 / 1250 MHz_M18 / VDD_W0000_W18_M18 / DT000_W18_M18
CIP_W19 / BMC_W0000 / BMCW0_W19_M19 / 1250 MHz_M19 / VDD_W0000_W19_M19 / DT000_W19_M19
CIP_W20 / BMC_W0000 / BMCW0_W20_M20 / 1250 MHz_M20 / VDD_W0000_W20_M20 / DT000_W20_M20
CIP_W21 / BMC_W0000 / BMCW0_W21_M21 / 1250 MHz_M21 / VDD_W0000_W21_M21 / DT000_W21_M21
CIP_W22 / BMC_W0000 / BMCW0_W22_M22 / 1250 MHz_M22 / VDD_W0000_W22_M22 / DT000_W22_M22
CIP_W23 / BMC_W0000 / BMCW0_W23_M23 / 1250 MHz_M23 / VDD_W0000_W23_M23 / DT000_W23_M23
CIP_W24 / BMC_W0000 / BMCW0_W24_M24 / 1250 MHz_M24 / VDD_W0000_W24_M24 / DT000_W24_M24
CIP_W25 / BMC_W0000 / BMCW0_W25_M25 / 1250 MHz_M25 / VDD_W0000_W25_M25 / DT000_W25_M25
CIP_W26 / BMC_W0000 / BMCW0_W26_M26 / 1250 MHz_M26 / VDD_W0000_W26_M26 / DT000_W26_M26
CIP_W27 / BMC_W0000 / BMCW0_W27_M27 / 1250 MHz_M27 / VDD_W0000_W27_M27 / DT000_W27_M27
CIP_W28 / BMC_W0000 / BMCW0_W28_M28 / 1250 MHz_M28 / VDD_W0000_W28_M28 / DT000_W28_M28
CIP_W29 / BMC_W0000 / BMCW0_W29_M29 / 1250 MHz_M29 / VDD_W0000_W29_M29 / DT000_W29_M29
CIP_W30 / BMC_W0000 / BMCW0_W30_M30 / 1250 MHz_M30 / VDD_W0000_W30_M30 / DT000_W30_M30
CIP_W31 / BMC_W0000 / BMCW0_W31_M31 / 1250 MHz_M31 / VDD_W0000_W31_M31 / DT000_W31_M31
CIP_W32 / BMC_W0000 / BMCW0_W32_M32 / 1250 MHz_M32 / VDD_W0000_W32_M32 / DT000_W32_M32
CIP_W33 / BMC_W0000 / BMCW0_W33_M33 / 1250 MHz_M33 / VDD_W0000_W33_M33 / DT000_W33_M33
CIP_W34 / BMC_W0000 / BMCW0_W34_M34 / 1250 MHz_M34 / VDD_W0000_W34_M34 / DT000_W34_M34
CIP_W35 / BMC_W0000 / BMCW0_W35_M35 / 1250 MHz_M35 / VDD_W0000_W35_M35 / DT000_W35_M35
CIP_W36 / BMC_W0000 / BMCW0_W36_M36 / 1250 MHz_M36 / VDD_W0000_W36_M36 / DT000_W36_M36
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CIP_W38 / BMC_W0000 / BMCW0_W38_M38 / 1250 MHz_M38 / VDD_W0000_W38_M38 / DT000_W38_M38
CIP_W39 / BMC_W0000 / BMCW0_W39_M39 / 1250 MHz_M39 / VDD_W0000_W39_M39 / DT000_W39_M39
CIP_W40 / BMC_W0000 / BMCW0_W40_M40 / 1250 MHz_M40 / VDD_W0000_W40_M40 / DT000_W40_M40
CIP_W41 / BMC_W0000 / BMCW0_W41_M41 / 1250 MHz_M41 / VDD_W0000_W41_M41 / DT000_W41_M41
CIP_W42 / BMC_W0000 / BMCW0_W42_M42 / 1250 MHz_M42 / VDD_W0000_W42_M42 / DT000_W42_M42
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CIP_W48 / BMC_W0000 / BMCW0_W48_M48 / 1250 MHz_M48 / VDD_W0000_W48_M48 / DT000_W48_M48
CIP_W49 / BMC_W0000 / BMCW0_W49_M49 / 1250 MHz_M49 / VDD_W0000_W49_M49 / DT000_W49_M49
CIP_W50 / BMC_W0000 / BMCW0_W50_M50 / 1250 MHz_M50 / VDD_W0000_W50_M50 / DT000_W50_M50
CIP_W51 / BMC_W0000 / BMCW0_W51_M51 / 1250 MHz_M51 / VDD_W0000_W51_M51 / DT000_W51_M51
CIP_W52 / BMC_W0000 / BMCW0_W52_M52 / 1250 MHz_M52 / VDD_W0000_W52_M52 / DT000_W52_M52
CIP_W53 / BMC_W0000 / BMCW0_W53_M53 / 1250 MHz_M53 / VDD_W0000_W53_M53 / DT000_W53_M53
CIP_W54 / BMC_W0000 / BMCW0_W54_M54 / 1250 MHz_M54 / VDD_W0000_W54_M54 / DT000_W54_M54
CIP_W55 / BMC_W0000 / BMCW0_W55_M55 / 1250 MHz_M55 / VDD_W0000_W55_M55 / DT000_W55_M55
CIP_W56 / BMC_W0000 / BMCW0_W56_M56 / 1250 MHz_M56 / VDD_W0000_W56_M56 / DT000_W56_M56
CIP_W57 / BMC_W0000 / BMCW0_W57_M57 / 1250 MHz_M57 / VDD_W0000_W57_M57 / DT000_W57_M57
CIP_W58 / BMC_W0000 / BMCW0_W58_M58 / 1250 MHz_M58 / VDD_W0000_W58_M58 / DT000_W58_M58
CIP_W59 / BMC_W0000 / BMCW0_W59_M59 / 1250 MHz_M59 / VDD_W0000_W59_M59 / DT000_W59_M59
CIP_W60 / BMC_W0000 / BMCW0_W60_M60 / 1250 MHz_M60 / VDD_W0000_W60_M60 / DT000_W60_M60
CIP_W61 / BMC_W0000 / BMCW0_W61_M61 / 1250 MHz_M61 / VDD_W0000_W61_M61 / DT000_W61_M61
CIP_W62 / BMC_W0000 / BMCW0_W62_M62 / 1250 MHz_M62 / VDD_W0000_W62_M62 / DT000_W62_M62
CIP_W63 / BMC_W0000 / BMCW0_W63_M63 / 1250 MHz_M63 / VDD_W0000_W63_M63 / DT000_W63_M63
CIP_W64 / BMC_W0000 / BMCW0_W64_M64 / 1250 MHz_M64 / VDD_W0000_W64_M64 / DT000_W64_M64
CIP_W65 / BMC_W0000 / BMCW0_W65_M65 / 1250 MHz_M65 / VDD_W0000_W65_M65 / DT000_W65_M65
CIP_W66 / BMC_W0000 / BMCW0_W66_M66 / 1250 MHz_M66 / VDD_W0000_W66_M66 / DT000_W66_M66
CIP_W67 / BMC_W0000 / BMCW0_W67_M67 / 1250 MHz_M67 / VDD_W0000_W67_M67 / DT000_W67_M67
CIP_W68 / BMC_W0000 / BMCW0_W68_M68 / 1250 MHz_M68 / VDD_W0000_W68_M68 / DT000_W68_M68
CIP_W69 / BMC_W0000 / BMCW0_W69_M69 / 1250 MHz_M69 / VDD_W0000_W69_M69 / DT000_W69_M69
CIP_W70 / BMC_W0000 / BMCW0_W70_M70 / 1250 MHz_M70 / VDD_W0000_W70_M70 / DT000_W70_M70
CIP_W71 / BMC_W0000 / BMCW0_W71_M71 / 1250 MHz_M71 / VDD_W
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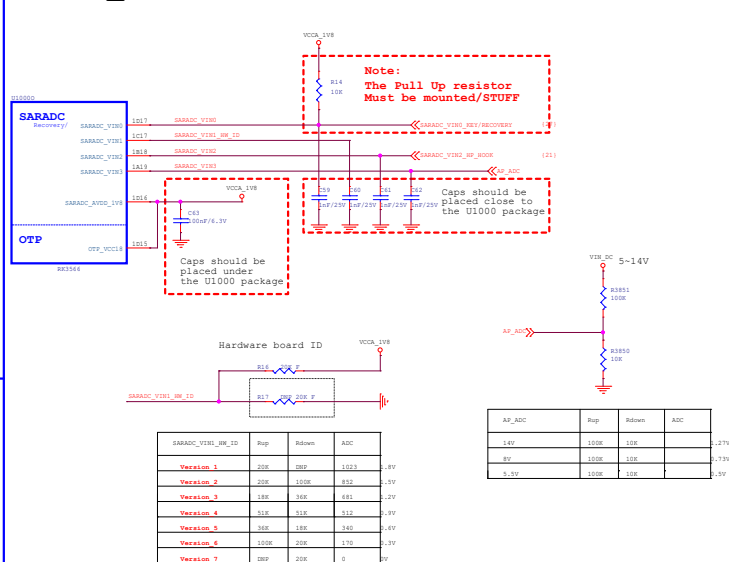
RK3566 K (VCCI04 Domain)



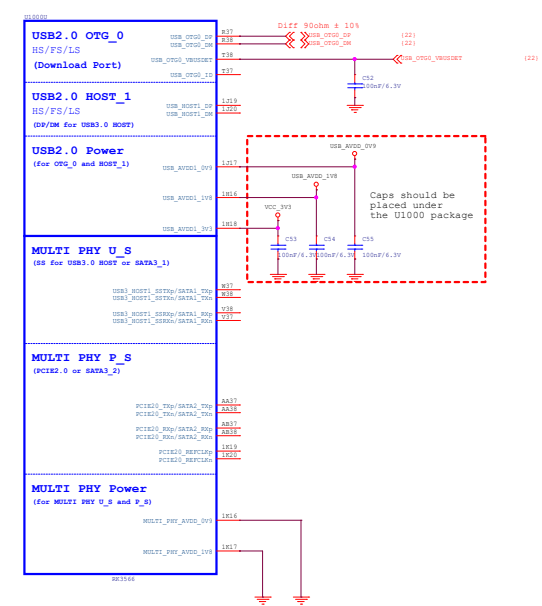
RK3566_N (VCCI07 Domain)



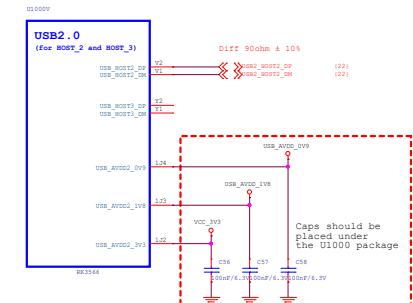
RK3566 O (SARADC/OTP)



RK3566_U (USB3.0/PCIe2.0x1/SATA)



RK3566_V (USB2.0 HOST)



Flash Power Manage



VCCIO3 Domain
Operating Voltage=1.8V/3.3V

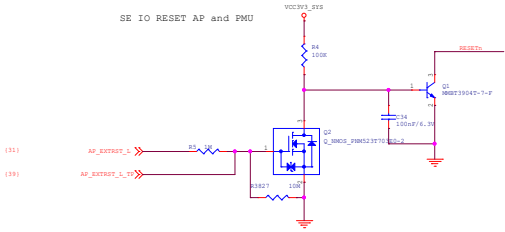
Pin	Signal	Pin	Signal
PWRM_NG1	SIGNALING_DQ	U10D0_NG1	SIGNALING_DQ
PWRM_NG2	SIGNALING_DQ	U10D0_NG2	SIGNALING_DQ
PWRM_NG3	SIGNALING_DQ	U10D0_NG3	SIGNALING_DQ
PWRM_NG4	SIGNALING_DQ	U10D0_NG4	SIGNALING_DQ
PWRM_NG5	SIGNALING_DQ	U10D0_NG5	SIGNALING_DQ
PWRM_NG6	SIGNALING_DQ	U10D0_NG6	SIGNALING_DQ

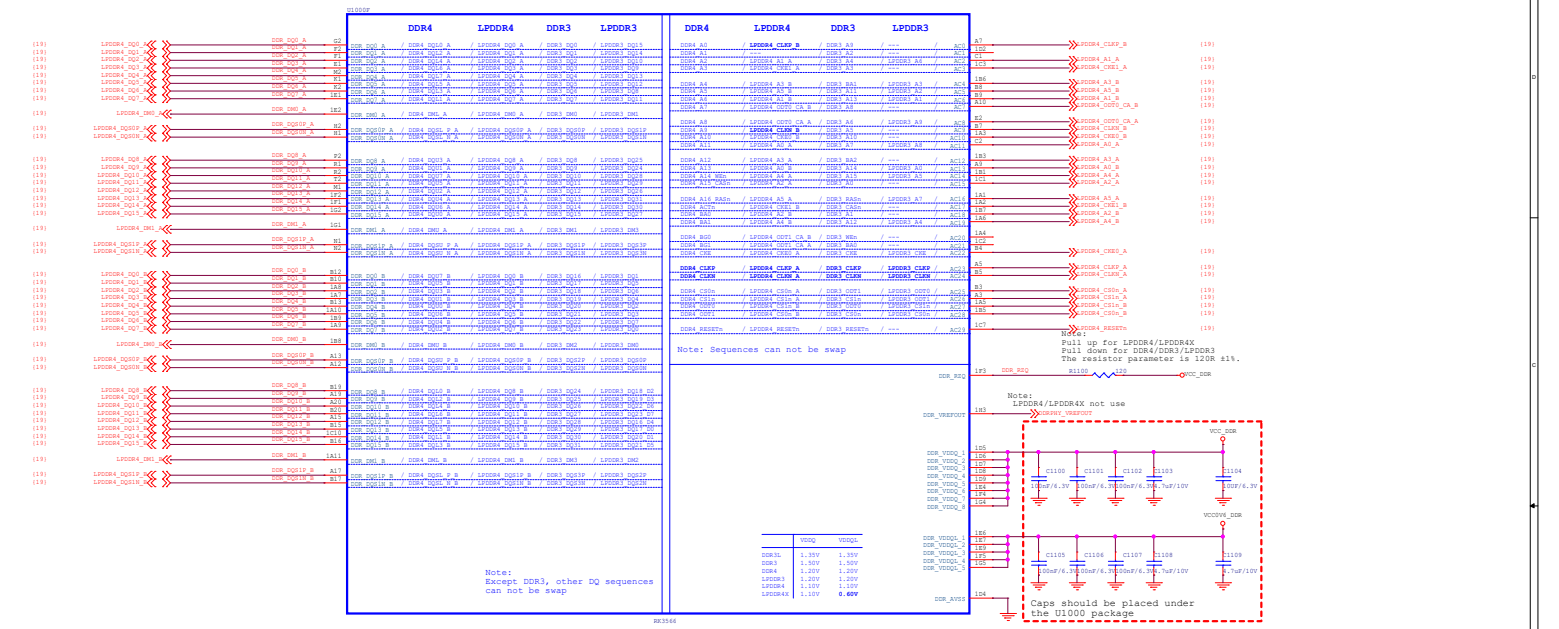
VCCIO3

0.1µF

VCCIO3_DQ

Caps should be placed under the U10D0 package





RK3566_ABCDE
(Power&GND)

