EM120R-GL&EM160R-GL

Hardware Design

LTE-A Module Series

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Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local office. For more information, please visit:
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About the Document

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1 Introduction

This document defines EM120R-GL&EM160R-GL and describes its air interfaces and hardware interfaces which are connected to customers' applications.

This document is applicable to the following modules:

- EM120R-GL
- EM160R-GL

This document can help customers quickly understand the interface specifications, electrical and mechanical details, as well as other related information of EM120R-GL&EM160R-GL. To facilitate its application in different fields, reference design is also provided for customers' reference. This document, coupled with application notes and user guides, can help customers use the module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EM120R-GL&EM160R-GL modules. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, use emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

EM120R-GL&EM160R-GL are LTE-A/UMTS/HSPA+ wireless communication modules with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks with standard PCI Express M.2 interface.

It supports embedded operating systems such as Windows, Linux and Android, and provides GNSS [1] and voice functionality [2] to meet customers' specific application demands.

The following table shows the frequency bands and GNSS types of EM120R-GL&EM160R-GL.

Table 1: Frequency Bands and GNSS Types of EM120R-GL&EM160R-GL

Mode	EM120R-GL&EM160R-GL
LTE-FDD (with Rx-diversity/MIMO [5])	B1 [4]/B2 [4]/B3 [4]/B4 [4]/B5/B7 [4]/ B8/B12/B13/B14/B17/B18/B19/B20/B25 [4]/B26/B28/ B29 [3]/B30 [4]/B32 [3] [4]/B66 [4]
LTE-TDD (with Rx-diversity/MIMO [5])	B38 [4]/B39 [4]/B40 [4]/B41 [4]/B42/B43/B46 [3]/B48
WCDMA (with Rx-diversity)	B1/B2/B3/B4/B5/B6/B8/B19
GNSS [1]	GPS; GLONASS; BeiDou/Compass; Galileo

NOTES

1. [1] GNSS function is optional.
2. [2] EM120R-GL&EM160R-GL contain **Telematics** version and **Data-only** version. **Telematics** version supports voice and data functions, while **Data-only** version only supports data function.
3. [3] LTE-FDD B29/B32 and LTE-TDD B46 support Rx only and are only for secondary component

carrier.
4. [4)] EM160R-GL supports up to 4 × 4 MIMO in DL direction.
5. [5)] MIMO antennas only apply for EM160R-GL.
6. For details about CA combinations, refer to ***document [1]***.

EM120R-GL&EM160R-GL can be applied in the following fields:

- Tablet PC and Laptop
- Remote Monitor System
- Vehicle System
- Wireless POS System
- Smart Metering System
- Wireless Router and Switch
- Other Wireless Terminal Devices

2.2. Key Features

The following table describes the detailed features of EM120R-GL&EM160R-GL.

Table 2: Key Features of EM120R-GL&EM160R-GL

Feature	Details
Function Interface	PCI Express M.2 Interface
Power Supply	Supply voltage: 3.135–4.4 V Typical supply voltage: 3.7 V
Transmitting Power	Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands Class 3 (24 dBm +1/-3 dB) for WCDMA
LTE Features	**EM160R-GL** Support up to LTE Cat 16 Support 1.4–100 MHz (5×CA) RF bandwidth Support 4 × 4 MIMO in DL direction Up to 1000 Mbps (DL)/150 Mbps (UL) **EM120R-GL** Support up to LTE Cat 12 Support 1.4–60 MHz (3×CA) RF bandwidth Support 2 × 2 MIMO in DL direction Up to 600 Mbps (DL)/150 Mbps (UL)

UMTS Features	Support 3GPP R9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max 42 Mbps (DL) ● HSUPA: Max 5.76 Mbps (UL) ● WCDMA: Max 384 Kbps (DL)/384 Kbps (UL)
Internet Protocol Features	● Support PPP/QMI/NTP*/TCP*/UDP*/FTP*/HTTP*/PING*/HTTPS*/SMTP*/MMS*/FTPS*/SMTPS*/SSL* protocols ● Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections
SMS	Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interfaces	Support (U)SIM card: 1.8/3.0 V Support Dual SIM Single Standby*
USB Interface	● Compliant with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0. ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentences output and voice over USB* ● Support USB serial drivers for: Windows: 7/8/8.1/10 Linux: 2.6/3.x/4.1–4.15 Android: 4.x/5.x/6.x/7.x/8.x/9.x
PCIe x1 Interface	Comply with *PCI Express Specification, Revision 2.1* and support 5 Gbps per lane Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentences output
Antenna connectors	**EM160R-GL** Provide Main, Rx-diversity/GNSS, MIMO1 and MIMO2 antenna connectors **EM120R-GL** Provide Main and Rx-diversity/GNSS antenna connectors
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen9 Lite of Qualcomm Protocol: NMEA-0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Physical Characteristics	Size: 42.0 ±0.15 mm × 30.0 ±0.15 mm × 2.3 ±0.1 mm Weight: approx. 6 g
Temperature Range	Operation temperature range: -25 °C to +75 °C [1)]

	Extended temperature range: -40 °C to +85 °C [2)] Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB 2.0 interface, PCIe interface and DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant. For those end devices with bad thermal dissipation condition, a thermal pad or other thermal conductive components may be required between the module and main PCB to achieve the full operating temperature range.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their values and exceed the specified tolerances. When the temperature returns to normal operating temperature level, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EM120R-GL&EM160R-GL.

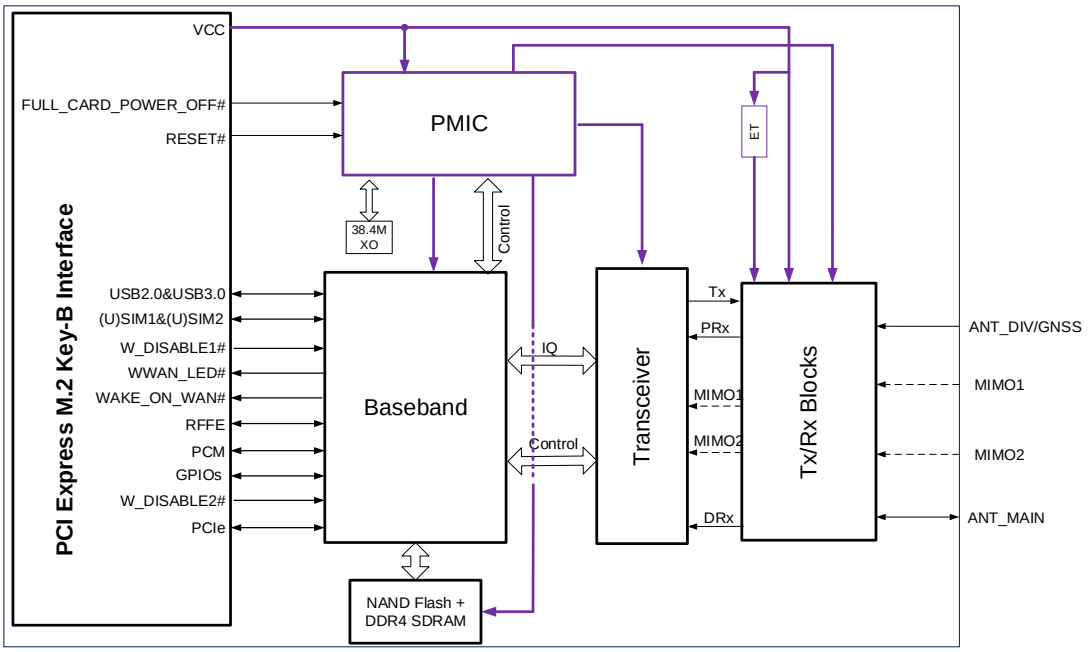


Figure 1: Functional Diagram

NOTE

MIMO1 and MIMO2 antennas are only applicable to the EM160R-GL module.

2.4. Evaluation Board

To help customers develop applications conveniently with EM120R-GL&EM160R-GL, Quectel supplies the evaluation board (M.2 EVB), USB to RS-232 converter cable, USB type-C cable, earphone, antenna and other peripherals to control or test the module. For more details, refer to ***document [2]***.

3 Application Interfaces

The physical connections and signal levels of EM120R-GL&EM160R-GL comply with PCI Express M.2 specifications. This chapter mainly describes the definition and application of the following interfaces/signals/pins of EM120R-GL&EM160R-GL:

- Power supply
- (U)SIM interfaces
- USB interface
- PCM interface*
- PCIe interface
- Control and indicator signals*
- Antenna tuner control interfaces*
- Configuration pins
- COEX UART Interface*

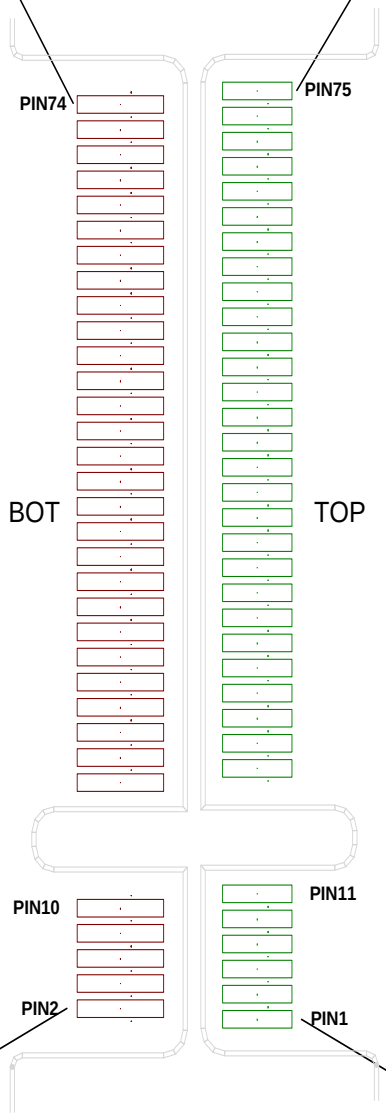
NOTE

"*" means under development.

3.1. Pin Assignment

The following figure shows the pin assignment of EM120R-GL&EM160R-GL. The top side contains EM120R-GL&EM160R-GL and antenna connectors.

No.	Pin Name
74	VCC
72	VCC
70	VCC
68	ANT_CONFIG
66	USIM1_DET
64	COEX_TXD
62	COEX_RXD
60	COEX3
58	RFFE_DATA
56	RFFE_CLK
54	PCIE_WAKE_N
52	PCIE_CLKREQ_N
50	PCIE_RST_N
48	USIM2_VDD
46	USIM2_RST
44	USIM2_CLK
42	USIM2_DATA
40	USIM2_DET
38	NC
36	USIM1_VDD
34	USIM1_DATA
32	USIM1_CLK
30	USIM1_RST
28	PCM_SYNC
26	W_DISABLE2#
24	PCM_DOUT/VDDIO
22	PCM_DIN
20	PCM_CLK
	Notch
	Notch
	Notch
	Notch
10	WWAN_LED#
8	W_DISABLE1#
6	FULL_CARD_POWER_OFF#
4	VCC
2	VCC



Pin Name	No.
CONFIG_2	75
GND	73
GND	71
CONFIG_1	69
RESET#	67
ANTCTL3	65
ANTCTL2	63
ANTCTL1	61
ANTCTL0	59
GND	57
PCIE_REFCLK_P	55
PCIE_REFCLK_M	53
GND	51
PCIE_RX_P	49
PCIE_RX_M	47
GND	45
PCIE_TX_P	43
PCIE_TX_M	41
GND	39
USB_SS_RX_P	37
USB_SS_RX_M	35
GND	33
USB_SS_TX_P	31
USB_SS_TX_M	29
GND	27
DPR	25
WAKE_ON_WAN#	23
CONFIG_0	21
Notch	
Notch	
Notch	
Notch	
GND	11
USB_DM	9
USB_DP	7
GND	5
GND	3
CONFIG_3	1

Figure 2: Pin Assignment

3.2. Pin Description

The following tables show the pin definition and description of EM120R-GL&EM160R-GL.

Table 2: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 3: Pin Description

Pin No.	M.2 Socket 2 WWAN Module Pinout	EM120R-GL&EM160R-GL Pin Name	I/O	Description	Comment
1	CONFIG_3	CONFIG_3		NC	
2	3.3V	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
3	GND	GND		Ground	
4	3.3V	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
5	GND	GND		Ground	
6	FULL_CARD_POWER_OFF#(I)(0/1.8V)	FULL_CARD_POWER_OFF#	DI	Turn on/off the module. When it is at low level, the module is powered	Pulled down internally.

				off. When it is at high level, the module is powered on.	
7	USB_D+	USB_DP	AI/AO	USB 2.0 differential data bus (+)	
8	W_DISABLE1#	W_DISABLE1#	DI	Airplane mode control. Active low.	1.8/3.3 V power domain
9	USB_D-	USB_DM	AI/AO	USB 2.0 differential data bus (-)	
10	GPIO_9	WWAN_LED#	OD	RF status indication. Active low.	
11	GND	GND		Ground	
12	Key	Notch		Notch	
13	Key	Notch		Notch	
14	Key	Notch		Notch	
15	Key	Notch		Notch	
16	Key	Notch		Notch	
17	Key	Notch		Notch	
18	Key	Notch		Notch	
19	Key	Notch		Notch	
20	GPIO_5 (AUDIO_0)	PCM_CLK	DI	PCM data bit clock. In master mode, it is an output signal. In slave mode, it is an input signal.	1.8 V power domain. If unused, keep it open.
21	CONFIG_0	CONFIG_0		EM120R-GL: Connected to GND internally; EM160R-GL: NC	
22	GPIO_6 (AUDIO_1)	PCM_DIN	PO	PCM data input	1.8 V power domain
23	GPIO_11 (WOWWAN#)	WAKE_ON_WAN#	OD	Wake up the host. Active low.	1.8/3.3 V power domain
24	GPIO_7 (AUDIO_2)	PCM_DOUT /VDDIO	DO/PO	PCM data output; Could be designed to be compatible with 1.8 V power supply.	1.8 V power domain

25	DPR	DPR	DI	Dynamic power reduction. Active low.	1.8 V power domain.
26	GPIO_10 (W_DISABLE2#)	W_DISABLE2#	DI	GNSS enable control. Active low.	1.8/3.3 V power domain
27	GND	GND		Ground	
28	GPIO_8 (AUDIO_3)	PCM_SYNC	IO	PCM data frame synchronization	1.8 V power domain
29	USB3.0-TX-	USB_SS_TX_M	AO	USB 3.0 transmit data (-)	
30	UIM-RESET	USIM1_RST	DO	(U)SIM1 card reset	1.8/3.0 V power domain
31	USB3.0-TX+	USB_SS_TX_P	AO	USB 3.0 transmit data (+)	
32	UIM-CLK	USIM1_CLK	DO	(U)SIM1 card clock	1.8/3.0 V power domain
33	GND	GND		Ground	
34	UIM-DATA	USIM1_DATA	IO	(U)SIM1 card data	Pulled up to USIM1_VDD internally.
35	USB3.0-RX-	USB_SS_RX_M	AI	USB 3.0 receive data (-)	
36	UIM-PWR	USIM1_VDD	PO	Power supply for (U)SIM1 card	1.8/3.0 V power domain
37	USB3.0-RX+	USB_SS_RX_P	AI	USB 3.0 receive data (+)	
38	N/C	NC		NC	
39	GND	GND		Ground	
40	GPIO_0 (SIM_DET2)	USIM2_DET	DI	(U)SIM2 card insertion detection	Pulled up internally. 1.8 V power domain.
41	PETn0	PCIE_TX_M	AO	PCIe transmit data (-)	
42	GPIO_1 (SIM_DAT2)	USIM2_DATA	IO	(U)SIM2 card data	Pulled up to USIM2_VDD internally
43	PETp0	PCIE_TX_P	AO	PCIe transmit data (+)	
44	GPIO_2 (SIM_CLK2)	USIM2_CLK	DO	(U)SIM2 card clock	1.8/3.0 V power domain

45	GND	GND		Ground	
46	GPIO_3 (SIM_RST2)	USIM2_RST	DO	(U)SIM2 card reset	1.8/3.0 V power domain
47	PERn0	PCIE_RX_M	AI	PCIe receive data (-)	
48	GPIO_4 (SIM_PWR2)	USIM2_VDD	PO	Power supply for (U)SIM2 card	1.8/3.0 V power domain
49	PERp0	PCIE_RX_P	AI	PCIe receive data (+)	
50	PCIE_RST_N	PCIE_RST_N	DI	PCIe reset input. Active low.	3.3 V power domain
51	GND	GND		Ground	
52	PCIE_CLKREQ_N	PCIE_CLKREQ_N	DO	PCIe clock request. Active low.	3.3 V power domain
53	REFCLKn	PCIE_REFCLK_M	AI/AO	PCIe reference clock (-)	
54	PEWAKE#	PCIE_WAKE_N	IO	PCIe wake up the host. Active low.	3.3 V power domain
55	REFCLKp	PCIE_REFCLK_P	AI/AO	PCIe reference clock (+)	
56	N/C	RFFE_CLK	DO	RFFE clock	
57	GND	GND		Ground	
58	N/C	RFFE_DATA	IO	RFFE data	
59	ANTCTL0	ANTCTL0	DO	Antenna tuner control	1.8 V power domain
60	COEX3	COEX3	IO	COEX GPIO	1.8 V power domain
61	ANTCTL1	ANTCTL1	DO	Antenna tuner control	1.8 V power domain
62	COEX2	COEX_RXD	DI	COEX UART receive data	1.8 V power domain
63	ANTCTL2	ANTCTL2	DO	Antenna tuner control	1.8 V power domain
64	COEX1	COEX_TXD	DO	COEX UART transmit data	1.8 V power domain
65	ANTCTL3	ANTCTL3	DO	Antenna tuner control	1.8 V power domain
66	SIM_DETECT	USIM1_DET	DI	(U)SIM1 card insertion detection	Pulled up internally. 1.8 V power

					domain.
67	RESET#	RESET#	DI	WWAN reset input Active low.	Pulled up internally. 1.8 V power domain.
68	SUSCLK (32kHz)	ANT_CONFIG	DI	Antenna configuration	Pulled up internally. 1.8 V power domain.
69	CONFIG_1	CONFIG_1		Connected to GND internally	
70	3.3V	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
71	GND	GND		Ground	
72	3.3V	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
73	GND	GND		Ground	
74	3.3V	VCC	PI	Power supply	Vmin = 3.135 V Vnorm = 3.7 V Vmax = 4.4 V
75	CONFIG_2	CONFIG_2		NC	

NOTE

Please keep all NC, reserved and unused pins unconnected.

3.3. Power Supply

The following table shows definition of VCC pins and ground pins.

Table 4: Pin Definition of VCC and GND

Pin No.	Pin Name	I/O	Power Domain	Description
2, 4, 70, 72, 74	VCC	PI	3.135–4.4 V	3.7 V typical DC supply
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND			Ground

3.3.1. Decrease Voltage Drop

The power supply range of the module is from 3.135 V to 4.4 V. Make sure that the input voltage never drops below 3.135 V, otherwise the module will be powered off automatically. The following figure shows the maximum voltage drop during radio transmission in 3G and 4G networks.

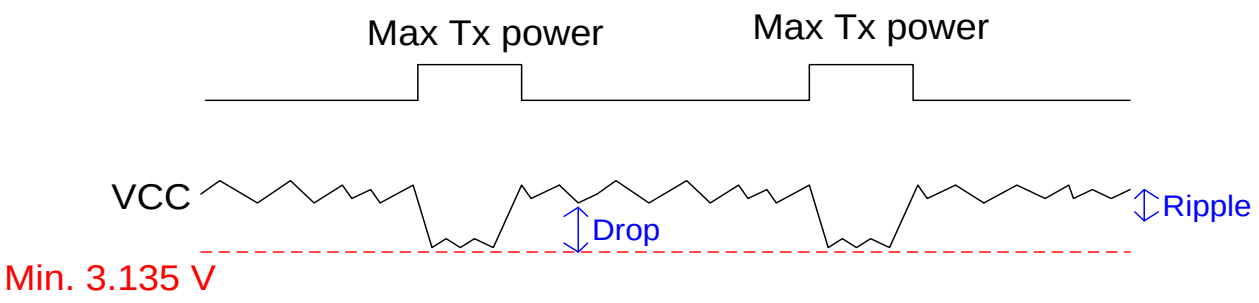


Figure 3: Power Supply Limits during Radio Transmission

To decrease voltage drop, a bypass capacitor of about 220 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The main power supply from an external application must be a single voltage source. The width of VCC trace should be no less than 2 mm. In principle, a longer VCC trace indicates a wider VCC trace.

In addition, in order to get a stable power source, it is recommended to use a zener diode with reverse zener voltage of 5.1 V and dissipation power more than 0.5 W. The following figure shows a reference

circuit of VCC.

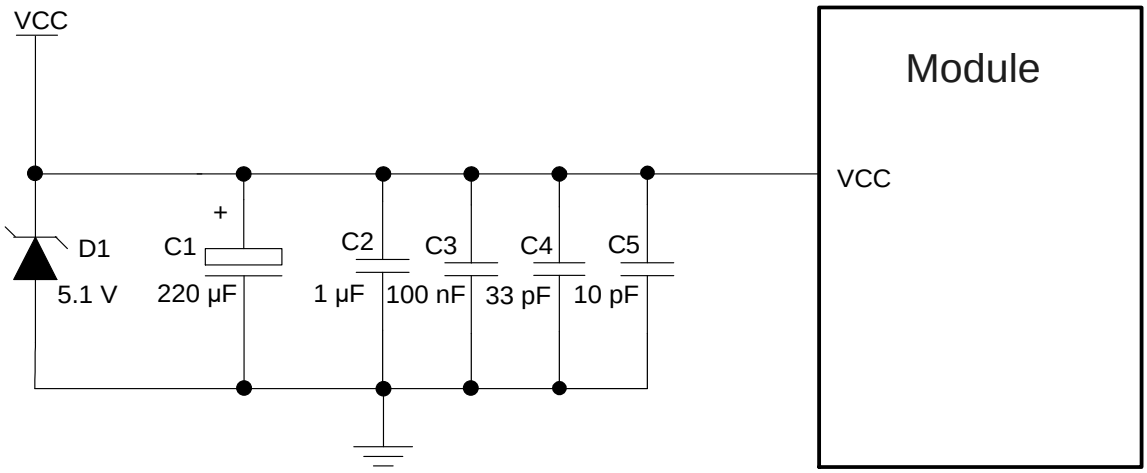


Figure 4: Reference Circuit of VCC

3.3.2. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply can provide sufficient current (at least 2.5 A). If the voltage drop between the input and output is not too high, an LDO is suggested to be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VCC), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.7 V and the maximum load current is 3 A.

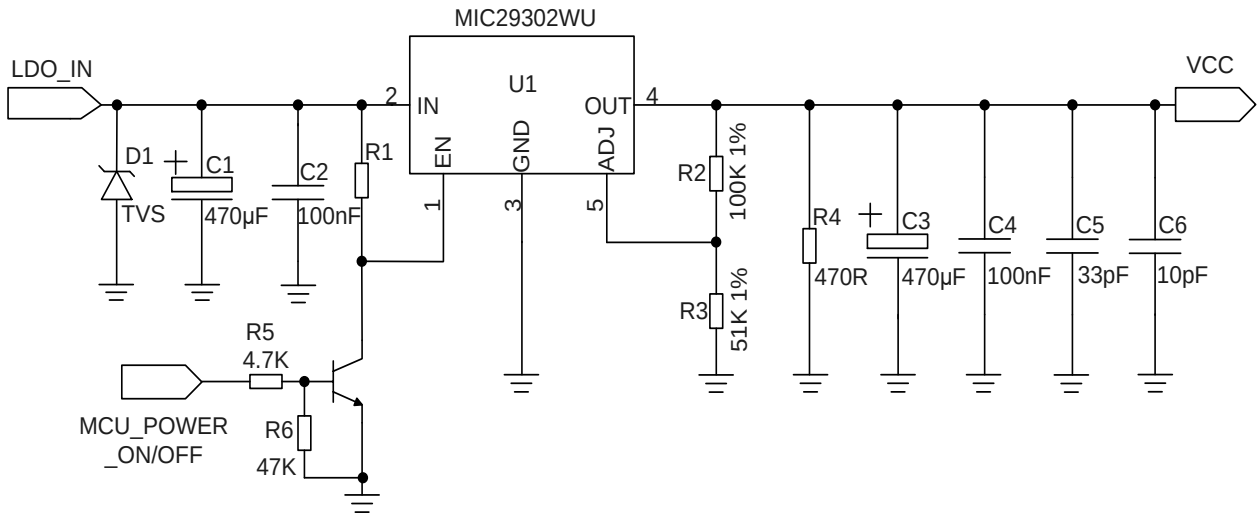


Figure 5: Reference Design of Power Supply

NOTE

In order to avoid damages to the internal flash, do not cut off the power supply directly when the module is working. It is suggested that the power supply should be cut off after the module is shut down.

3.4. Turn-on and Turn-off Scenarios

3.4.1. Turn on the Module

Pulling up the FULL_CARD_POWER_OFF# pin will power on the module. The following table shows the pin definition of FULL_CARD_POWER_OFF#.

Table 5: Pin Definition of FULL_CARD_POWER_OFF#

Pin Name	Pin No.	Description	DC Characteristics	Comment
FULL_CARD_POWER_OFF#	6	Turn on/off the module. When it is at low level, the module is powered off. When it is at high level, the module is powered on.	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Pulled down internally.

3.4.1.1. Turn on the Module with a Host GPIO

It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated in the following figure.

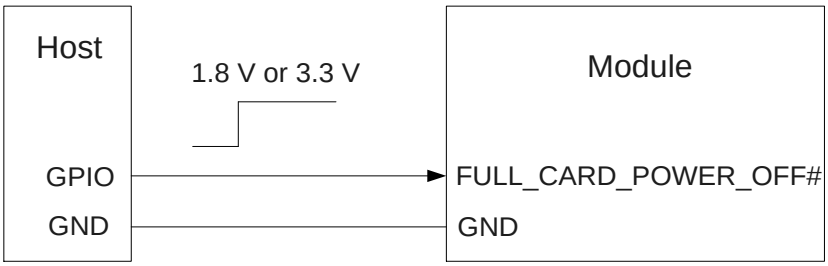
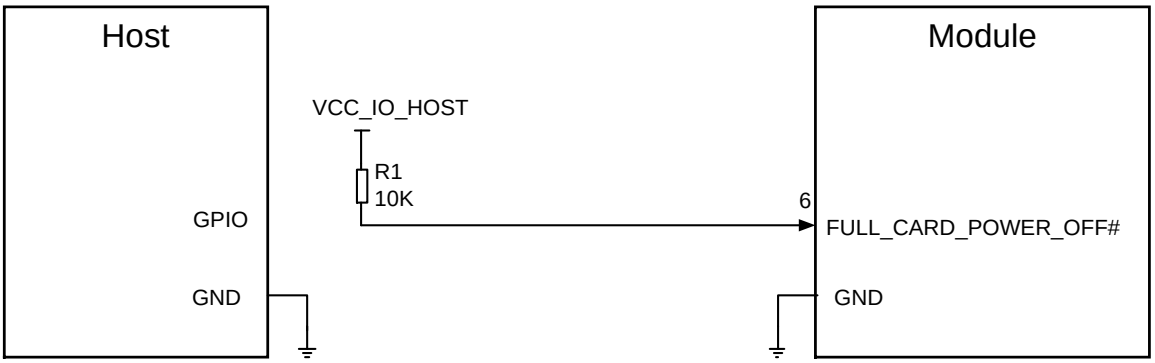


Figure 6: Turn on the Module with a Host GPIO

3.4.1.2. Turn on the Module Automatically

If FULL_CARD_POWER_OFF# is pulled up to VCC with a 5–10 kΩ resistor, the module will be powered on automatically when the power supply for VCC is applied.

A reference circuit is shown in the following figure.

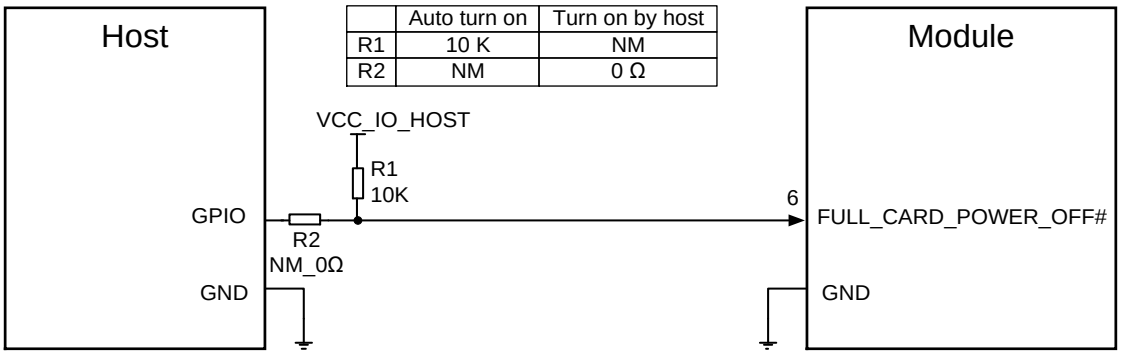


Notes:
1. The voltage of pin 6 should be no less than 1.19 V when it is at HIGH level.
2. The voltage level VCC_IO_HOST could be a 1.8 V or 3.3 V typically.

Figure 7: Turn on the Module Automatically

3.4.1.3. Turn on the Module with Compatible Design

The following figure shows a compatible design to turn on the module automatically after power-up or by host.



	Auto turn on	Turn on by host
R1	10 K	NM
R2	NM	0 Ω

Notes:
1. The voltage of pin 6 should be no less than 1.19 V when it is at HIGH level.
2. The voltage level VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 8: Turn on the Module with Compatible Design

The turn-on scenario is illustrated in the following figure.

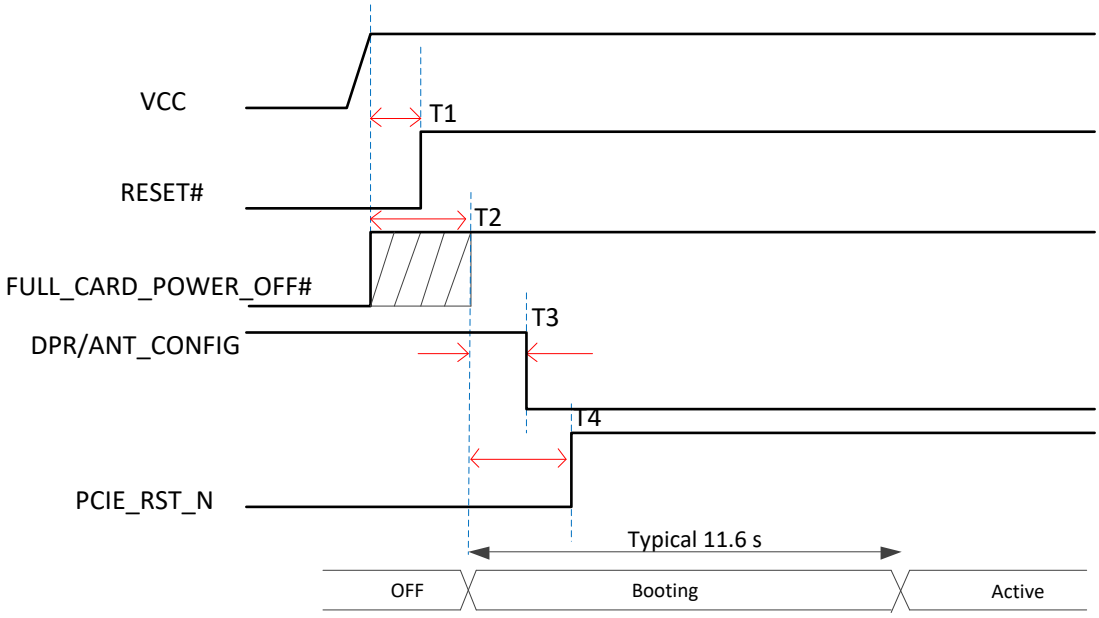


Figure 9: Turn-on Timing of the Module

Table 6: Description of Turn-on Timing of the Module

Index	Min.	Typical	Max.	Comment
T1	0 ms	50 ms	-	RESET# is pulled up internally, and it would be de-asserted 50 ms after VCC is powered on.
T2	0 ms	20 ms	-	FULL_CARD_POWER_OFF# could be de-asserted before or after RESET#, 20 ms is a recommended value when it is controlled by GPIO.
T3	0 ms	15 ms	20 ms	DPR or ANT_CONFIG should be asserted before modem initialize.
T4	-	100 ms	-	PCIE_RST_N should be de-asserted 100 ms after FULL_CARD_POWER_OFF#.

3.4.2. Turn off the Module

3.4.2.1. Turn off the Module through FULL_CARD_POWER_OFF#

Pulling down the FULL_CARD_POWER_OFF# pin will turn off the module. The turn-off scenario is illustrated in the following figure.

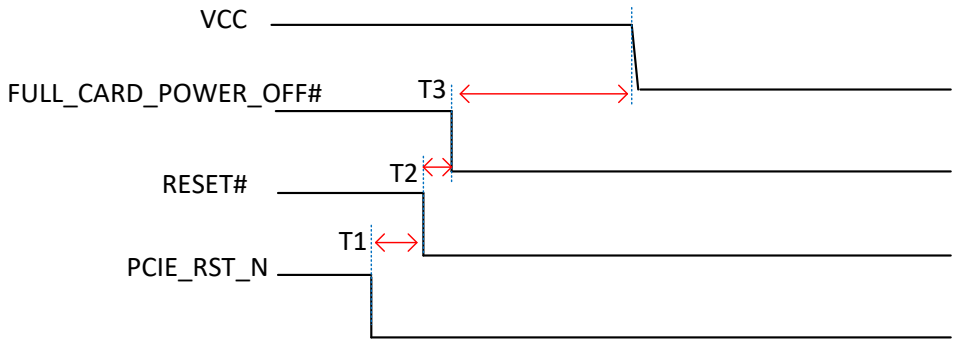


Figure 10: Timing of Turning off the Module through FULL_CARD_POWER_OFF#

Table 7: Description of the Timing of Resetting the Module througn FULL_CARD_POWER_OFF#

Index	Min.	Typical	Max.	Comments
T1	0 ms	20 ms	-	PCIE_RST_N should be asserted before RESET#.
T2	0 ms	10 ms	200 ms	RESET# is recommended to be asserted before FULL_CARD_POWER_OFF#
T3	10 ms	-	-	If power is always on, it could be ignored.

3.4.2.2. Turn off the Module through AT Command

It is a safe way to use **AT+QPOWD** command to turn off the module. For more details about the command, refer to ***document [3]***.

For the circuit design of ***Figure 6***, pull down FULL_CARD_POWER_OFF# pin, or cut off power supply of VCC after the module's USB/PCIe is removed. Otherwise, the module will be powered on again.

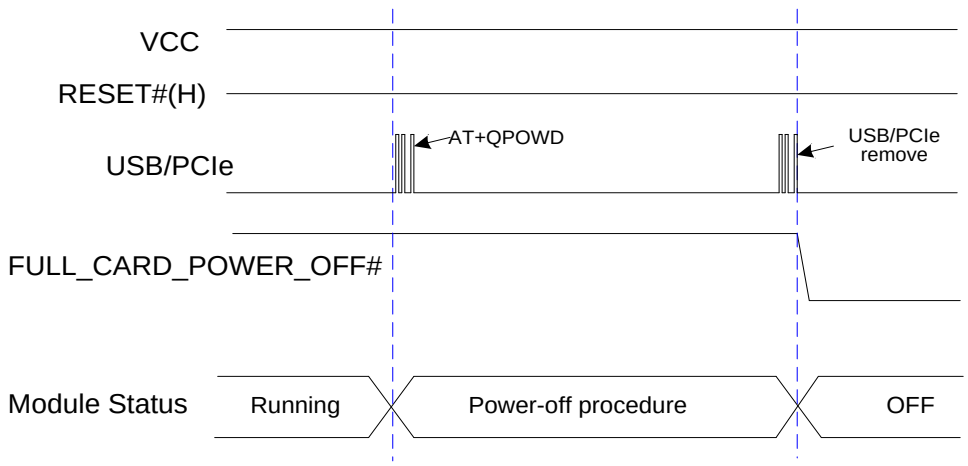


Figure 11: Timing of Turning off the Module through AT Command and FULL_CARD_POWER_OFF#

For the circuit design of ***Figure 7*****,** cut off power supply of VCC after the module's USB/PCIe is removed, as illustrated in ***Figure 11***. Otherwise, the module will be powered on again.

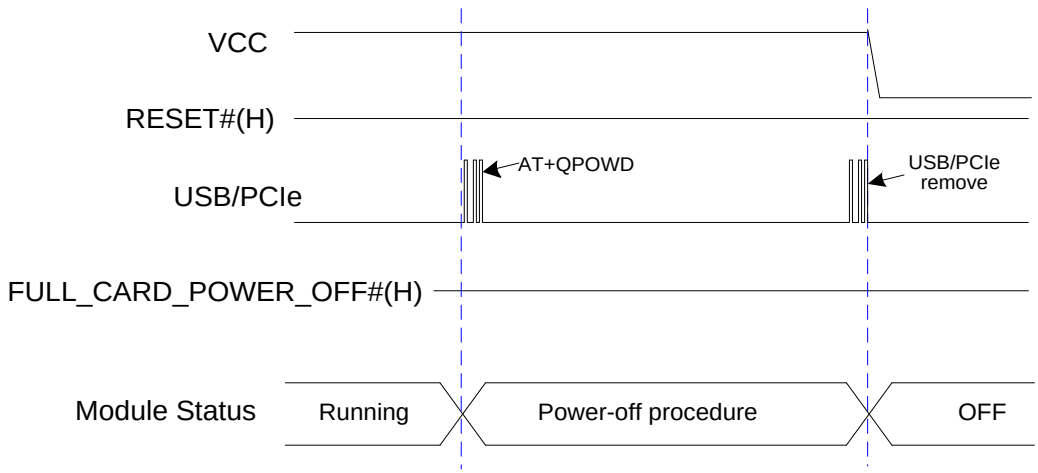


Figure 12: Timing of Turning off the Module through AT Command and Power Supply

NOTE

Please pull down FULL_CARD_POWER_OFF# pin immediately or cut off the power supply of VCC when the host detects that the module is removed.

3.5. Reset

The RESET# pin is used to reset the module. The module can be reset by driving RESET# to a low-level voltage for 200–700 ms.

Table 8: Pin Definition of RESET#

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET#	67	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Pulled up internally. 1.8 V power domain.

An open collector/drain driver or button can be used to control the RESET# pin.

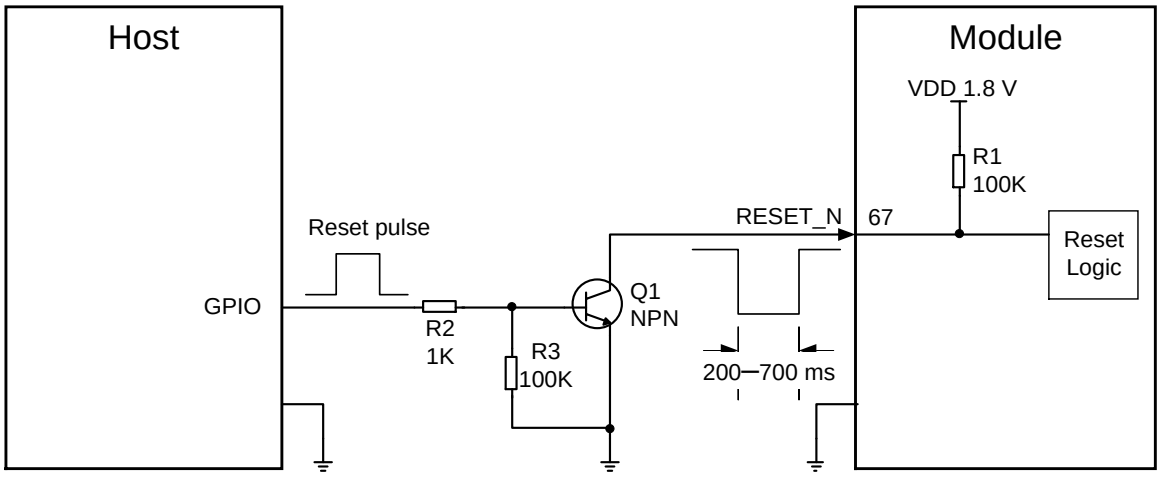


Figure 13: Reference Circuit of RESET_N with NPN Driving Circuit

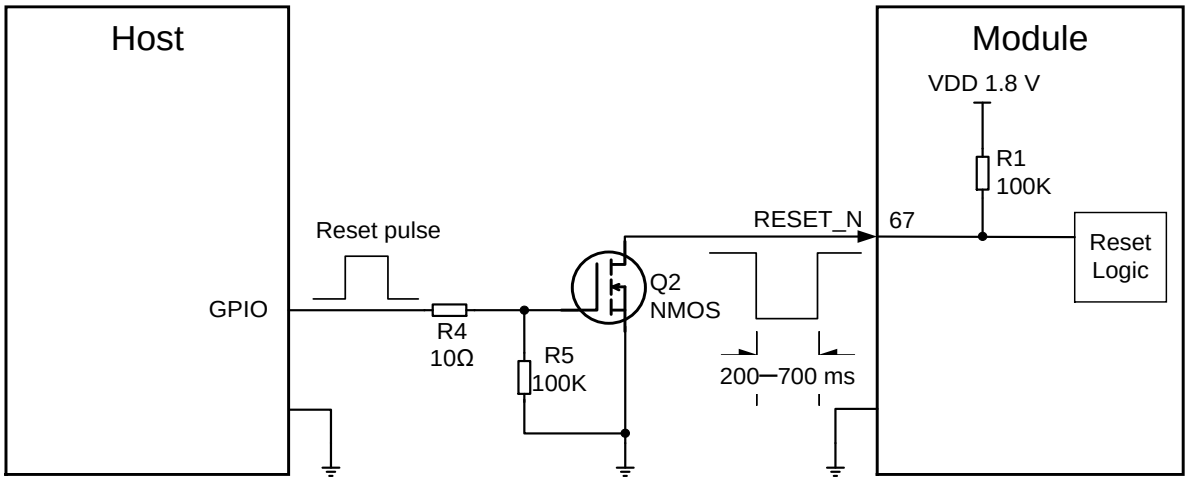
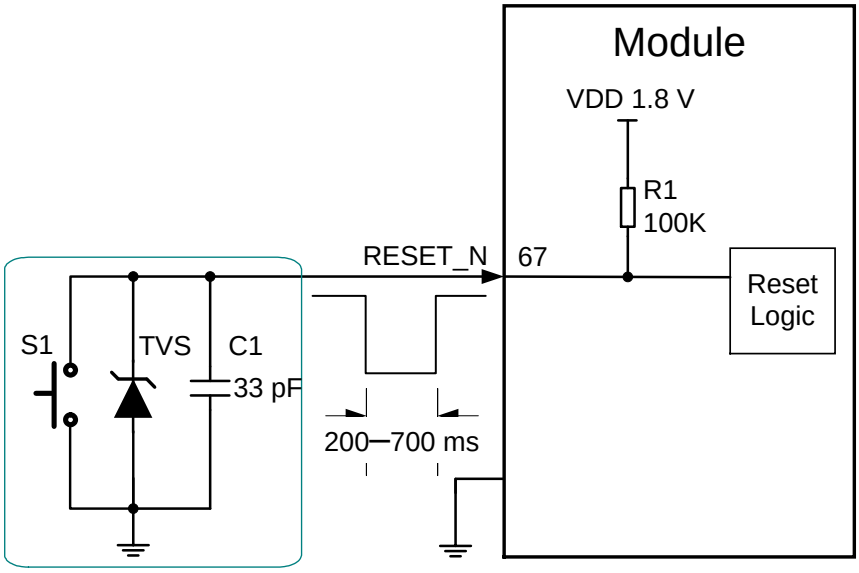


Figure 14: Reference Circuit of RESET_N with NMOS Driving Circuit



Note: The capacitor C1 is recommended to be less than 47 pF.

Figure 15: Reference Circuit of RESET_N with Button

The reset scenario is illustrated in the following figure.

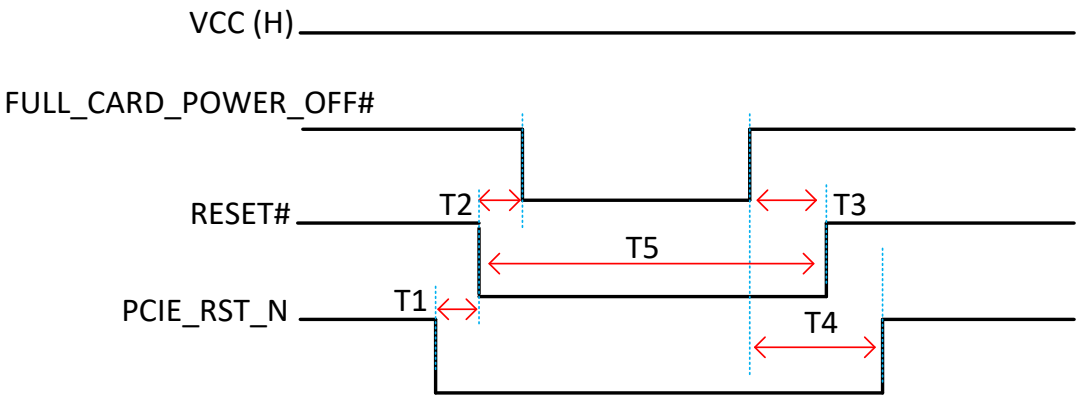


Figure 16: Timing of Resetting the Module

Table 9: Timing of Resetting the Module

Index	Min.	Typical	Max.	Comments
T1	0 ms	20 ms	-	PCIE_RST_N should be asserted before RESET#.
T2	0 ms	10 ms	200 ms	RESET# should be asserted before FULL_CARD_POWER_OFF#.
T3	0 ms	20 ms	200 ms	RESET# should be de-asserted after FULL_CARD_POWER_OFF#
T4	-	100 ms	-	PCIE_RST_N should be de-asserted 100 ms after FULL_CARD_POWER_OFF#.
T5	200 ms	-	700 ms	RESET# should be de-asserted no longer than 700 ms, otherwise the module would reset several times.

NOTE

Please ensure that there is no large capacitance on RESET# pin.

3.6. (U)SIM Interfaces

The (U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported, and Dual SIM Single Standby* function is supported.

Table 10: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	36	PO	Power supply for (U)SIM1 card	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	34	IO	(U)SIM1 card data	
USIM1_CLK	32	DO	(U)SIM1 card clock	
USIM1_RST	30	DO	(U)SIM1 card reset	
USIM1_DET	66	DI	(U)SIM1 card insertion detection. Active high.	Internally pulled up. When (U)SIM1 card is present, it is at high level. When (U)SIM1 card is absent, it is at low level.
USIM2_VDD	48	PO	Power supply for (U)SIM2 card	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	42	IO	(U)SIM2 card data	
USIM2_CLK	44	DO	(U)SIM2 card clock	
USIM2_RST	46	DO	(U)SIM2 card reset	
USIM2_DET	40	DI	(U)SIM2 card insertion detection. Active high.	Internally pulled up. When (U)SIM2 card is present, it is at high level. When (U)SIM2 card is absent, it is at low level.

EM120R-GL&EM160R-GL support (U)SIM card hot-plug via the USIM_DET pin, which is a level trigger pin. The USIM_DET is normally short-circuited to ground when (U)SIM card is not inserted. When the (U)SIM card is inserted, the USIM_DET will change from low to high level. The rising edge will indicate insertion of the (U)SIM card. When the (U)SIM card is removed, the USIM_DET will change from high to low level. This falling edge will indicate the absence of the (U)SIM card.

The following figure shows a reference design for a (U)SIM interface with normally closed (U)SIM card connector.

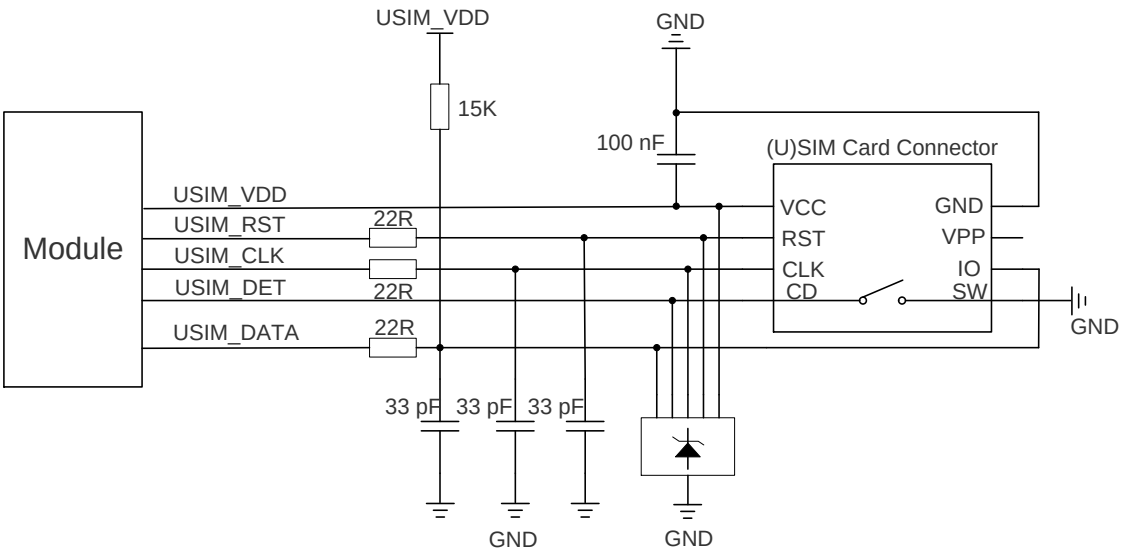


Figure 17: Reference Circuit of Normally Closed (U)SIM1 Card Connector

Normally Closed (U)SIM Card Connector:

- When the (U)SIM is absent, CD is short-circuited to SW and USIM_DET is at low level.
- When the (U)SIM is inserted, CD is open to SW and USIM_DET is at high level.

The following figure shows a reference design for a (U)SIM interface with normally open (U)SIM card connector.

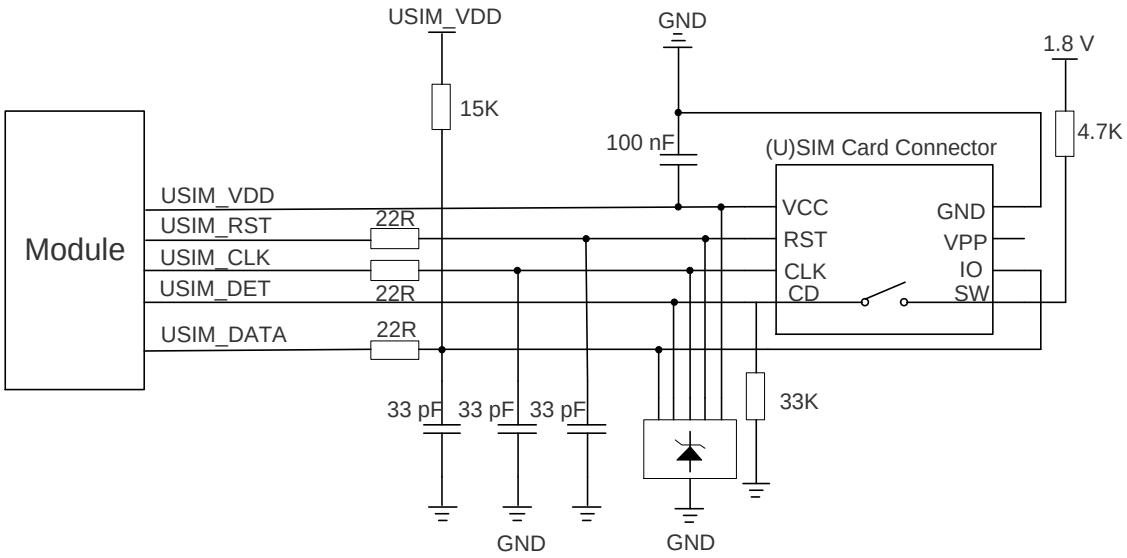


Figure 18: Reference Circuit of Normally Open (U)SIM1 Card Connector

Normally Open (U)SIM Card Connector:

- When the (U)SIM is absent, CD is open to SW and USIM_DET is at low level.
- When the (U)SIM is inserted, CD is short-circuited to SW and USIM_DET is at high level.

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. The following figure shows a reference circuit for a (U)SIM card interface with a 6-pin (U)SIM card connector.

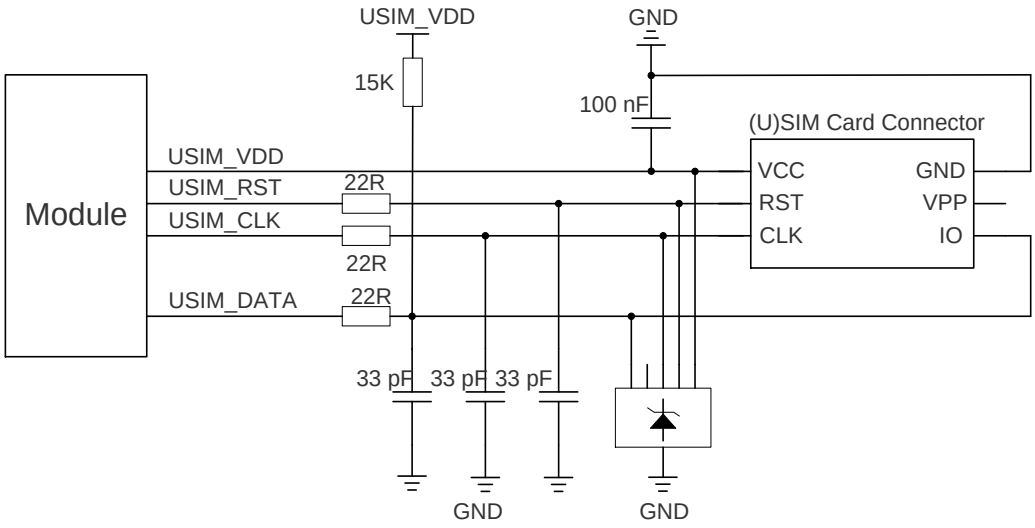
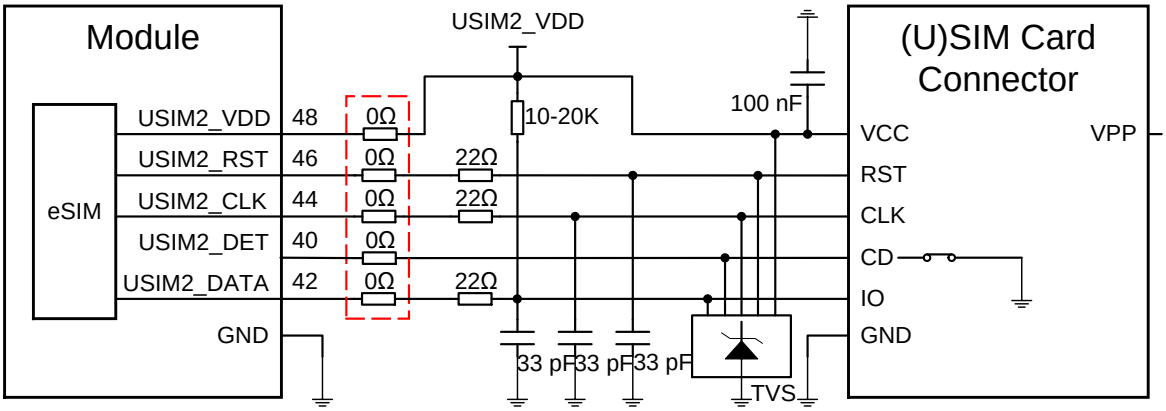


Figure 19: Reference Circuit of a 6-Pin (U)SIM1 Card Connector

EM120R-GL&EM160R-GL provide two (U)SIM interfaces. (U)SIM1 interface is used for external (U)SIM card only, and (U)SIM2 interface is used for external (U)SIM card or internal eSIM card.

It should be noted that, when (U)SIM2 interface is used for an external (U)SIM card, the reference circuits are the same as those of (U)SIM1 interface. When (U)SIM2 interface is used for the internal eSIM card, pins 40, 42, 44, 46 and 48 of the module must be kept open.

A recommended compatible design of (U)SIM2 interface is shown below.



Note: The five 0Ω resistors must be close to M.2 socket connector, and all other components should be close to (U)SIM card connector in PCB layout.

Figure 20: Recommended Compatible Design of (U)SIM2 Interface

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, follow the criteria below when designing the (U)SIM circuit:

- Keep placement of (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VCC traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 10 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used to filter out RF interference. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

NOTE

"*" means under development.

3.7. USB Interface

EM120R-GL&EM160R-GL provide one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0/2.0 specifications and supports super speed (5 Gbps) on USB 3.0, high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*.

The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AI/AO	USB 2.0 differential data bus (+)	Require differential impedance of 90 Ω
9	USB_DM	AI/AO	USB 2.0 differential data bus (-)	
29	USB_SS_TX_M	AO	USB 3.0 transmit data (-)	Require differential impedance of 90 Ω
31	USB_SS_TX_P	AO	USB 3.0 transmit data (+)	
35	USB_SS_RX_M	AI	USB 3.0 receive data (-)	Require differential impedance of 90 Ω
37	USB_SS_RX_P	AI	USB 3.0 receive data (+)	

For more details about the USB 3.0 & 2.0 specifications, visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in customers' designs. The following figure shows a reference circuit of USB 3.0/USB 2.0 interface.

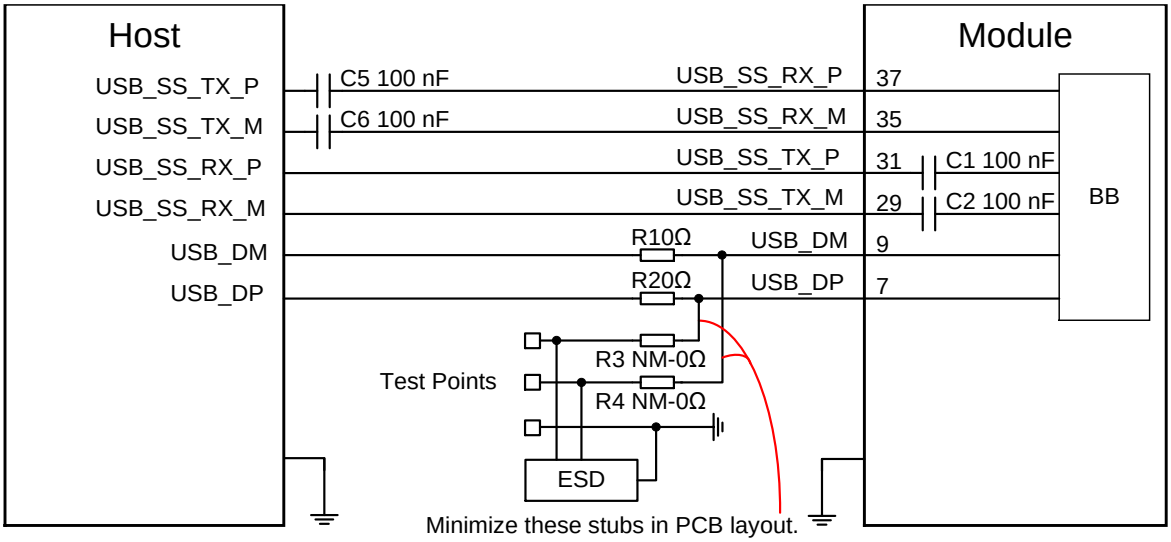


Figure 21: Reference Circuit of USB 3.0/2.0 Interface

AC coupling capacitors C5 and C6 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on customers' schematic and PCB. In order to ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 components must be placed close to the module, and the stubs must be minimized in PCB layout.

In order to ensure that the USB interface designs correspond with USB specifications, comply with the following principles.

- It is important to route the USB 2.0 & 3.0 signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, the trace lengths must be less than 120 mm, and the differential data pair matching is less than 2 mm (15 ps).
- For USB 3.0 signal traces, the maximum length of TX and RX differential data pair is recommended to be less than 100 mm, and the TX and RX differential data pair matching is less than 0.7 mm (5 ps).
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the USB 2.0 & 3.0 differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- If USB connector is used, keep the ESD protection components as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection components on USB 2.0 & 3.0 data traces. Typically, the capacitance value should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- If possible, reserve four 0 Ω resistors (R1–R4) on USB_DP and USB_DM traces, as shown in the above figure.

NOTE

"*" means under development.

3.8. PCIe Interface

EM120R-GL and EM160R-GL provide one integrated PCIe (Peripheral Component Interconnect Express) interface which complies with the *PCI Express Specification, Revision 2.1* and supports 5 Gbps per lane. The PCIe interface is used for data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade.

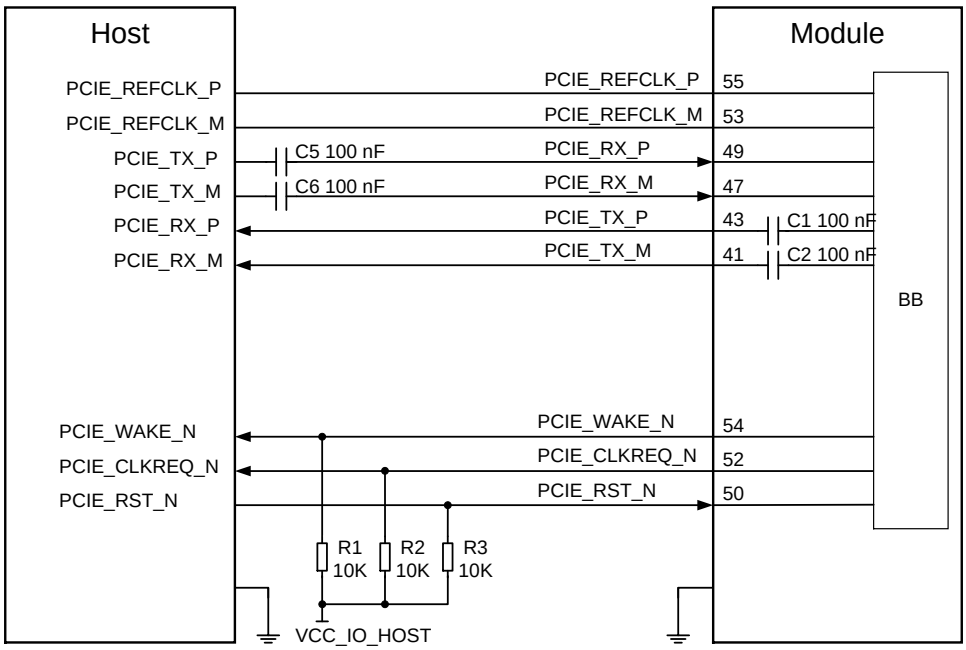
The following table shows the pin definition of PCIe interface.

Table 12: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AI/AO	PCIe reference clock (+)	Require differential impedance of 95 Ω.
53	PCIE_REFCLK_M	AI/AO	PCIe reference clock (-)	
49	PCIE_RX_P	AI	PCIe receive data (+)	Require differential impedance of 95 Ω
47	PCIE_RX_M	AI	PCIe receive data (-)	
43	PCIE_TX_P	AO	PCIe transmit data (+)	Require differential impedance of 95 Ω
41	PCIE_TX_M	AO	PCIe transmit data (-)	
50	PCIE_RST_N	DI	PCIe reset input. Active low.	3.3 V power domain
52	PCIE_CLKREQ_N	DO	PCIe clock request. Active low.	3.3 V power domain
54	PCIE_WAKE_N	DO	PCIe wake up the host. Active low.	3.3 V power domain

3.8.1. Endpoint Mode

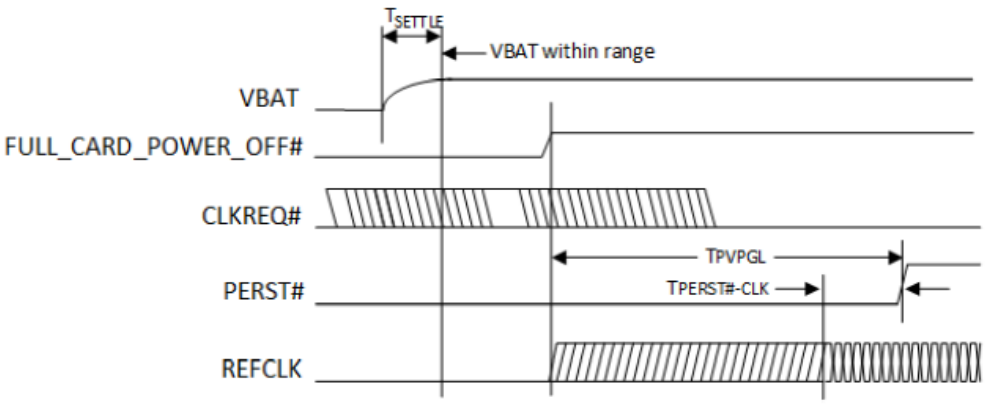
EM120R-GL and EM160R-GL support endpoint (EP) mode. In this mode, the modules are configured as a PCIe EP device. The following figure shows a reference circuit of PCIe endpoint mode.



Note: The voltage level VCC_IO_HOST depends on the host side due to open drain in pin 50, 52 and 54.

Figure 22: PCIe Interface Reference Circuit (EP Mode)

In order to ensure the signal integrity of PCIe interface, AC coupling capacitors C5 and C6 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on customers' schematic and PCB.



Symbol	Parameter	Min	Max	Units
T_{PVPGL}	Power Valid* to PERST# input inactive	Implementation specific; recommended 50 ms		ms
$T_{PERST\#-CLK}$	REFCLK stable before PERST# inactive	100		µs

Figure 23: PCIe Power-on Timing Requirements of M.2 Specification

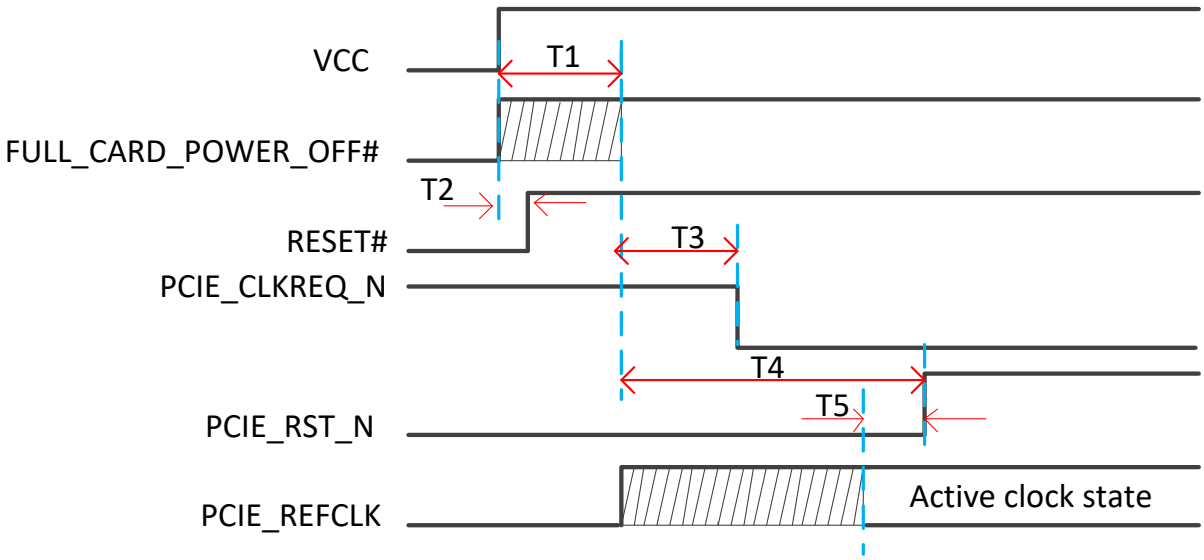


Figure 24: PCIe Power-on Timing Requirements of the Module

Table 13: Description of PCIe Power-on Timing Requirements of the Module

Index	Min.	Typical	Max.	Comment
T1	0 ms	20 ms	-	FULL_CARD_POWER_OFF# could be de-asserted before or after RESET#, 20 ms is a recommended value when it is controlled by GPIO.
T2	-	50 ms	-	RESET# is pulled up internally, and it would be de-asserted 50 ms after VCC is powered on.
T3	-	70 ms	-	PCIE_CLKREQ_N would be asserted 70 ms after FULL_CARD_POWER_OFF#.
T4	-	100 ms	-	PCIE_RST_N should be de-asserted after PCIE_CLKREQ_N.
T5	100 μs	-	-	The host must ensure that the reference clock is in the active clock state for at least a period specified by $T_{PCIE_RST_N\text{-}CLK}$, prior to PCIE_RST_N de-assertion.

The following principles of PCIe interface design should be complied with so as to meet PCIe V2.1 specifications.

- It is important to route the PCIe signal traces as differential pairs with total grounding.
- For PCIe signal traces, the TX and RX differential data pair maximum length is recommended to be less than 250 mm, the TX and RX differential data pair matching are less than 0.7 mm (5 ps).
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the PCIe differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.

3.8.2. USB Version and PCIe Only Version

Beginning with ES2 (engineering samples), EM120R-GL&EM160R-GL support USB version and PCIe only version described as below:

USB version:
- Support all USB 3.0/2.0 features
- Support MBIM/QMI/QRTR/AT
- Support firmware upgrade

PCIe only version:
- Support MBIM/QMI/QRTR/AT
- Support BIOS PCIe early initial
- Support firmware upgrade

If EM120R-GL&EM160R-GL work at PCIe only version by burnt eFuse, the modules cannot switch back to USB version.

3.9. PCM Interface*

EM120R-GL&EM160R-GL support audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256, 512, 1024 or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC only.

EM120R-GL&EM160R-GL support 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

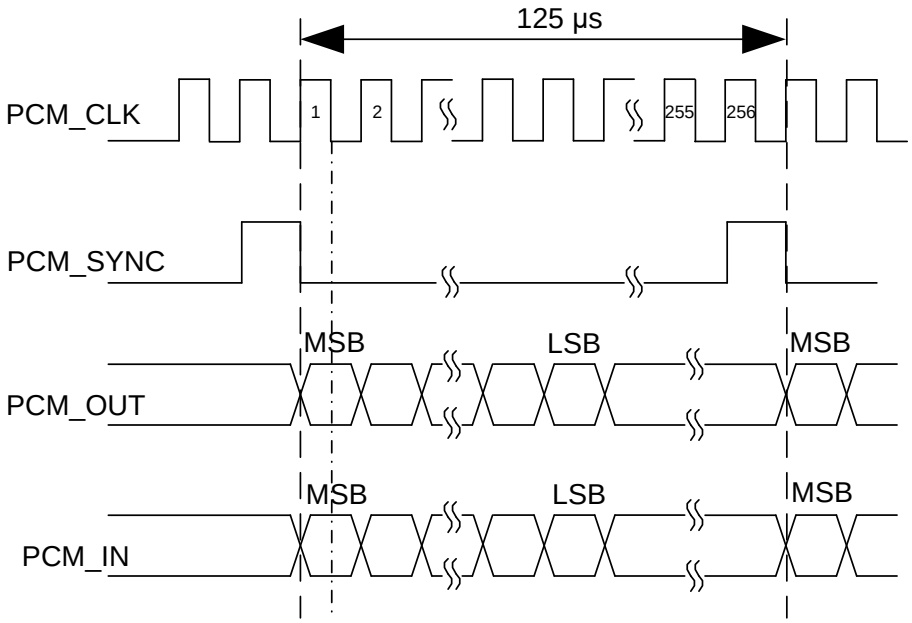


Figure 25: Primary Mode Timing

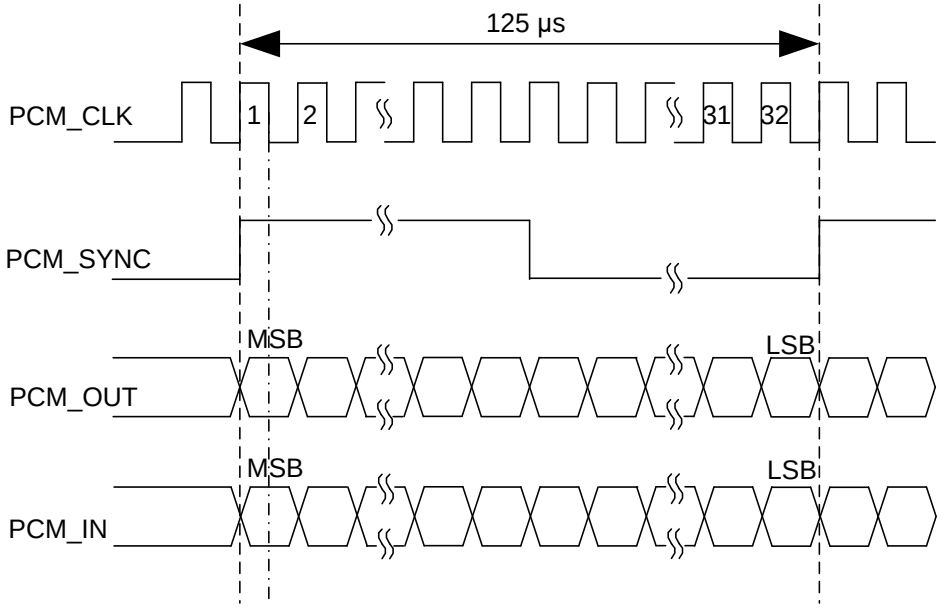


Figure 26: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface which can be applied on audio codec design.

Table 14: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	22	DI	PCM data input	1.8 V power domain
PCM_DOUT	24	DO	PCM data output	1.8 V power domain
PCM_SYNC	28	IO	PCM data frame synchronization	1.8 V power domain
PCM_CLK	20	IO	PCM data bit clock In master mode, it is an output signal. In slave mode, it is an input signal.	1.8 V power domain. If unused, keep it open.

The clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. Refer to ***document [3]*** for details about **AT+QDAI** command.

NOTE

"*" means under development.

3.10. Control and Indicator Signals*

The following table shows the pin definition of control and indicator signals.

Table 15: Definition of Control and Indicator Signals

Pin Name	Pin No.	I/O	Power Domain	Description
WWAN_LED#	10	OD	3.3 V	RF status indication. Active low.
WAKE_ON_WAN#	23	OD	1.8/3.3 V	Wake up the host. Active low.
W_DISABLE1#	8	DI	1.8/3.3 V	Airplane mode control. Active low.
W_DISABLE2#	26	DI	1.8/3.3 V	GNSS enable control. Active low.
DPR	25	DI	1.8 V	Dynamic power reduction. Active low.
ANT_CONFIG	68	DI	1.8 V	Antenna configuration pin.

NOTE

"*" means under development.

3.10.1. W_DISABLE1# Signal

EM120R-GL&EM160R-GL provide a W_DISABLE1# signal to disable or enable airplane mode through hardware operation. The W_DISABLE1# pin is pulled up by default. Driving it to low level will let the module enter airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through software AT commands. The following table shows the RF function status of the modules.

Table 16: RF Function Status

W_DISABLE1# Level	AT Commands	RF Function Status
High Level	**AT+CFUN=1**	Enabled
High Level	**AT+CFUN=0** **AT+CFUN=4**	Disabled
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled

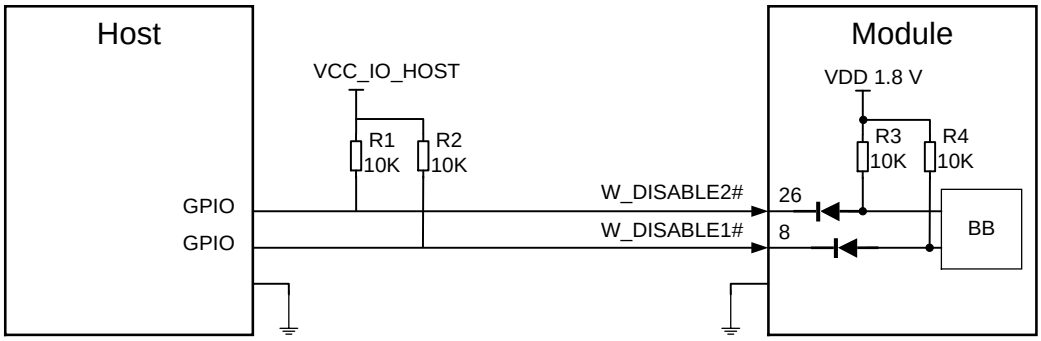
3.10.2. W_DISABLE2# Signal

EM120R-GL&EM160R-GL provide a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it to low level will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands can control the GNSS function.

Table 17: GNSS Function Status

W_DISABLE2# Level	AT Commands	GNSS Function Status
High Level	**AT+QGPS=1**	Enabled
High Level	**AT+QGPSEND**	Disabled
Low Level	**AT+QGPS=1**	
Low Level	**AT+QGPSEND**	

A simple level shifter based on diodes is used on W_DISABLE1# pin and W_DISABLE2# pin which are pulled up to a 1.8 V voltage in the module, as shown in the following figure. So, the control signals (GPIO) of the host device could be a 1.8 V or 3.3 V voltage level and pull-up resistor is not needed on the host side. These two signals are active low, and a reference circuit is shown below.



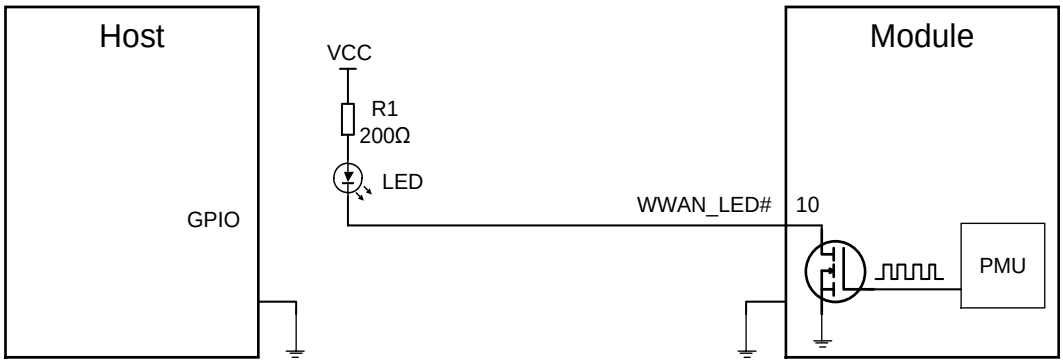
Note:
Host's GPIO could be a 1.8 V or 3.3 V voltage level.

Figure 27: W_DISABLE1# and W_DISABLE2# Reference Circuit

3.10.3. WWAN_LED# Signal

The WWAN_LED# signal is used to indicate RF status of the modules, and its typical current consumption is up to 10 mA.

In order to reduce the current consumption of the LED, a resistor must be placed in series with the LED, as illustrated in the figure below. The LED is ON when the WWAN_LED# signal is at a low voltage level.



Note: This VCC could be the power supply of the module.

Figure 28: WWAN_LED# Signal Reference Circuit

The following table shows the RF status indicated by WWAN_LED# signal.

Table 18: RF Status Indications of WWAN_LED# Signal

WWAN_LED# Level	LED	RF Status
Low Level	On	On
High Level	Off	Off

NOTE

RF function is turned off if any of the following circumstances occurs:

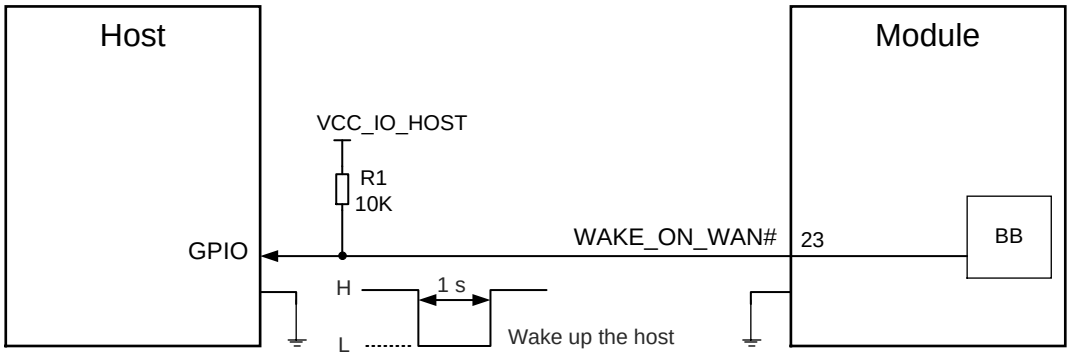
- The (U)SIM card is not working.
- W_DISABLE1# signal is at low level (airplane mode enabled).

3.10.4. WAKE_ON_WAN# Signal

The WAKE_ON_WAN# signal is an open collector signal, which requires a pull-up resistor on the host. When a URC returns, a 1s low level pulse signal will be outputted to wake up the host. The module operation status indicated by WAKE_ON_WAN# is shown as below.

Table 19: State of the WAKE_ON_WAN# Signal

WAKE_ON_WAN# State	Module Operation Status
Output a 1s low level pulse signal	Call/SMS/Data is incoming (to wake up the host)
Always at high level	Idle/Sleep



Note: The voltage level on VCC_IO_HOST depends on the host side due to open drain in pin 23.

Figure 29: WAKE_ON_WAN# Signal Reference Circuit Design

3.10.5. DPR

EM120R-GL&EM160R-GL provide a DPR (Dynamic Power Reduction) signal for body SAR (Specific Absorption Rate) detection. The signal is sent by a host system proximity sensor to EM120R-GL&EM160R-GL modules to provide an input trigger which will reduce the output power in the radio transmission.

Table 20: Function of the DPR Signal

DPR Level	Function
High/Floating	Max transmitting power will NOT back off
Low	Max transmitting power will back off by executing **AT+QCFG="sarcfg"** command

NOTE

Please refer to ***document [3]*** for more details about **AT+QCFG="sarcfg"** command.

3.10.6. ANT_CONFIG Signal

EM160R-GL provides an ANT_CONFIG signal for antenna configuration, however, EM120R-GL does not support it since EM120R-GL only supports 2 antennas. The signal is sent by a host system to EM160R-GL module. ANT_CONFIG is an input port which is pulled high internally by default. The definition of ANT_CONFIG signal is shown as below table.

Table 21: Pin Definition of ANT_COMNFIG of EM160R-GL

ANT_CONFIG Level	Function
High/Floating	Support 2 antennas
Low Level	Support 4 antennas

3.11. COEX UART Interface*

EM120R-GL&EM160R-GL provide one COEX UART interface. The following table shows the COEX UART interface pin definition.

Table 22: Pin Definition of COEX UART Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX3	60	IO	GPIO	1.8 V power domain
COEX_RXD	62	IO	COEX UART Interface	1.8 V power domain
COEX_TXD	64	IO		1.8 V power domain

NOTE

"*" means under development.

3.12. Antenna Tuner Control Interfaces*

ANTCTL [0:3] and RFFE signals are used for antenna tuner control and should be routed to an appropriate antenna control circuit. More details about the interface will be added in a future version of the document.

3.12.1. Antenna Tuner Control Interface through GPIOs

Table 23: Pin Definition of Antenna Tuner Control Interface through GPIOs

Pin Name	Pin No.	I/O	Description	Comment
ANTCTL0	59	DO	Antenna tuner control	1.8 V power domain
ANTCTL1	61	DO	Antenna tuner control	1.8 V power domain
ANTCTL2	63	DO	Antenna tuner control	1.8 V power domain
ANTCTL3	65	DO	Antenna tuner control	1.8 V power domain

3.12.2. Antenna Tuner Control Interface through RFFE

Table 24: Pin Definition of Antenna Tuner Control Interface through RFFE

Pin Name	Pin No.	I/O	Description	Comment
RFFE_CLK	56	DO	RFFE serial interface used for external tuner control	If unused, keep it open.
RFFE_DATA	58	IO		If unused, keep it open.

NOTE

"*" means under development.

3.13. Configuration Pins

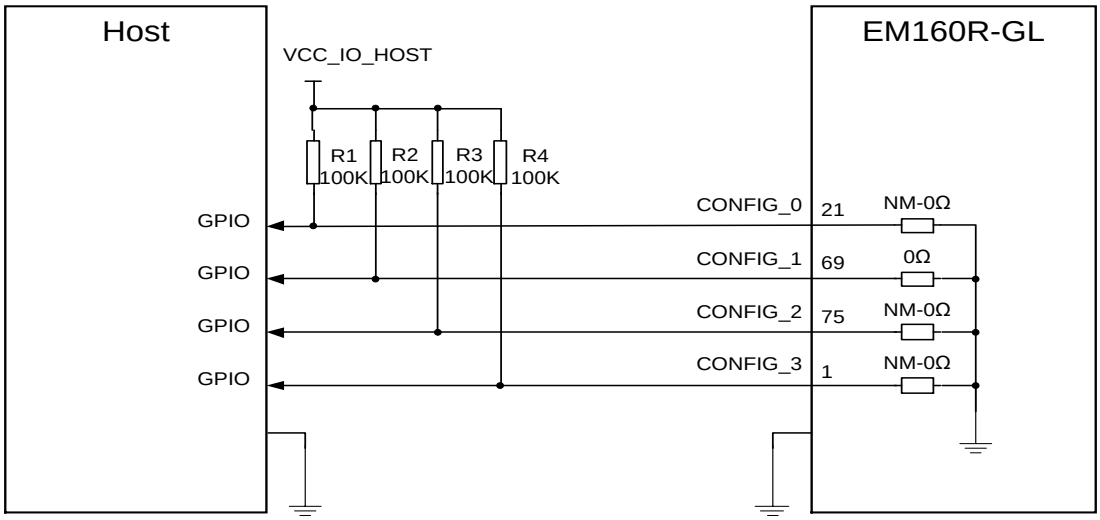
EM120R-GL&EM160R-GL provide four configuration pins which are defined as below.

3.13.1. EM160R-GL configuration pins

Table 25: List of EM160R-GL Configuration Pins

Pin No.	Pin Name	Power Domain	Description
21	CONFIG_0	0	NC
69	CONFIG_1	0	Connected to GND internally.
75	CONFIG_2	0	NC
1	CONFIG_3	0	NC

The following figure shows a reference circuit of these four pins.



Note: The voltage level VCC_IO_HOST depends on the host side, and could be a 1.8 V or 3.3 V voltage level.

Figure 30: Recommended Circuit of EM160R-GL Configuration Pins

Table 26: List of EM160R-GL Configuration Pins

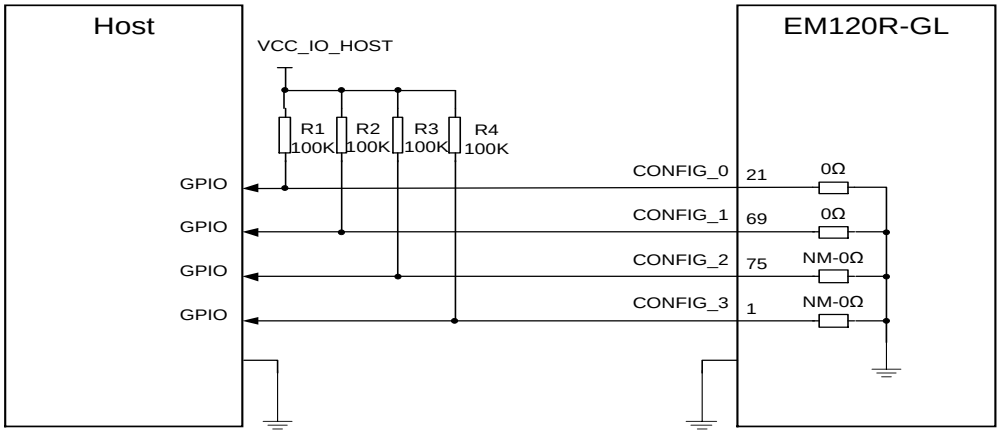
Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	Vender defined	N/A

3.13.2. EM120R-GL configuration pins

Table 27: List of EM120R-GL Configuration Pins

Pin No.	Pin Name	Power Domain	Description
21	CONFIG_0	0	Connected to GND internally.
69	CONFIG_1	0	Connected to GND internally.
75	CONFIG_2	0	NC
1	CONFIG_3	0	NC

The following figure shows a reference circuit of these four pins.



Note: The voltage level VCC_IO_HOST depends on the host side, and could be a 1.8 V or 3.3 V voltage level.

Figure 31: Recommended Circuit of EM120R-GL Configuration Pins

Table 28: List of EM120R-GL Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
GND	GND	NC	NC	Vender defined	N/A

4 GNSS Receiver

4.1. General Description

EM120R-GL&EM160R-GL include a fully integrated global navigation satellite system solution that supports Gen9-Lite of Qualcomm (GPS, GLONASS, BeiDou/Compass and Galileo).

The modules support standard NMEA-0183 protocol, and output NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, EM120R-GL&EM160R-GL GNSS engine is switched off. It can only be switched on via AT command. For more details about GNSS engine technology and configurations, refer to ***document [4]***.

5 Antenna Connection

EM120R-GL and EM160R-GL provide Main, Rx-diversity/GNSS and MIMO antenna connectors [1)] which are used to resist the fall of signals caused by high speed movement and multipath effect. The impedance of antenna ports is 50 Ω.

EM160R-GL provides a Main, an Rx-diversity/GNSS and two MIMO antenna connectors.

EM120R-GL provides a Main and an Rx-diversity/GNSS antenna connectors.

5.1. Antenna Connectors

The antenna connectors are shown below.

Figure 32: Antenna Connectors on the EM160R-GL Module

Figure 33: Antenna Connectors on the EM120R-GL Module

5.1.1. Operating Frequency

Table 29: Operating Frequencies of EM120R-GL&EM160R-GL

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830–840	875–885	MHz
WCDMA B8	880–915	925–960	MHz
WCDAM B19	830–845	875–890	MHz

LTE B1	1920–1980	2110–2170	MHz
LTE B2	1850–1910	1930–1990	MHz
LTE B3	1710–1785	1805–1880	MHz
LTE B4	1710–1755	2110–2155	MHz
LTE B5	824–849	869–894	MHz
LTE B7	2500–2570	2620–2690	MHz
LTE B8	880–915	925–960	MHz
LTE B12	699–716	729–746	MHz
LTE B13	777–787	746–756	MHz
LTE B14	788–798	758–768	MHz
LTE B17	704–716	734–746	MHz
LTE B18	815–830	860–875	MHz
LTE B19	830–845	875–890	MHz
LTE B20	832–862	791–821	MHz
LTE B25	1850–1915	1930–1995	MHz
LTE B26	814–849	859–894	MHz
LTE B28	703–748	758–803	MHz
LTE B29 [1)]	-	717–728	MHz
LTE B30	2305–2315	2350–2360	MHz
LTE B32 [1)]	-	1452–1496	MHz
LTE B38	2570–2620	2570–2620	MHz
LTE B39	1880–1920	1880–1920	MHz
LTE B40	2300–2400	2300–2400	MHz
LTE B41	2496–2690	2496–2690	MHz
LTE B42	3400–3600	3400–3600	MHz

LTE B43	3600–3800	3600–3800	MHz
LTE B46 [1)]	5150–5925	5150–5925	MHz
LTE B48	3550–3700	3550–3700	MHz
LTE B66	1710–1780	2110–2200	MHz

NOTE

[1)] LTE-FDD B29/32 and LTE-TDD B46 support Rx only and are only for secondary component carrier.

5.2. GNSS Antenna Connector

The following table shows frequency specification of GNSS antenna connector.

Table 30: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo	1575.42 ±1.023	MHz
GLONASS	1601.65 ±4.15	MHz
BeiDou/Compass	1561.098 ±2.046	MHz

5.3. Antenna Installation

5.3.1. Antenna Requirements

The following table shows the requirements on Main, Rx-diversity/GNSS and MIMO antennas.

Table 31: Antenna Requirements of EM160R-GL

Type	Requirements	Supported Bands
Main Antenna (Tx/Rx)	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1710–2200 MHz) Cable Insertion Loss: < 2dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19
Rx-diversity/ GNSS Antenna	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19 **GNSS:** GPS; GLONASS; BeiDou/Compass; Galileo
MIMO1 Antenna （Rx）	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz)	**LTE:** B1/B2/B3/B4/B7/B25/ B30/B32/B38/B39/B40/B41/B66

	Cable Insertion Loss: < 2 dB (2300–2690 MHz)	
MIMO2 Antenna (Rx)	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B7/B25/ B30/B32/B38/B39/B40/B41/B66

Table 32: Antenna Requirements of EM120R-GL

Type	Requirements	Supported Bands
Main Antenna (Tx/Rx)	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1710–2200 MHz) Cable Insertion Loss: < 2dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19
Rx-diversity/ GNSS Antenna	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: < 1 dB (699–960 MHz) Cable Insertion Loss: < 1.5 dB (1559–2200 MHz) Cable Insertion Loss: < 2 dB (2300–2690 MHz)	**LTE:** B1/B2/B3/B4/B5/B7/B8/B12/B13/ B14/B17/B18/B19/B20/B25/B26/ B28/B29/B30/B32/B38/B39/B40/ B41/B42/B43/B46/B48/B66 **WCDMA:** B1/B2/B3/B4/B5/B6/B8/B19 **GNSS:** GPS; GLONASS; BeiDou/Compass; Galileo

5.3.2. Recommended RF Connector for Antenna Installation

EM120R-GL and EM160R-GL are mounted with standard 2 mm × 2 mm receptacle RF connectors for convenient antenna connection. The connector dimensions are illustrated below:

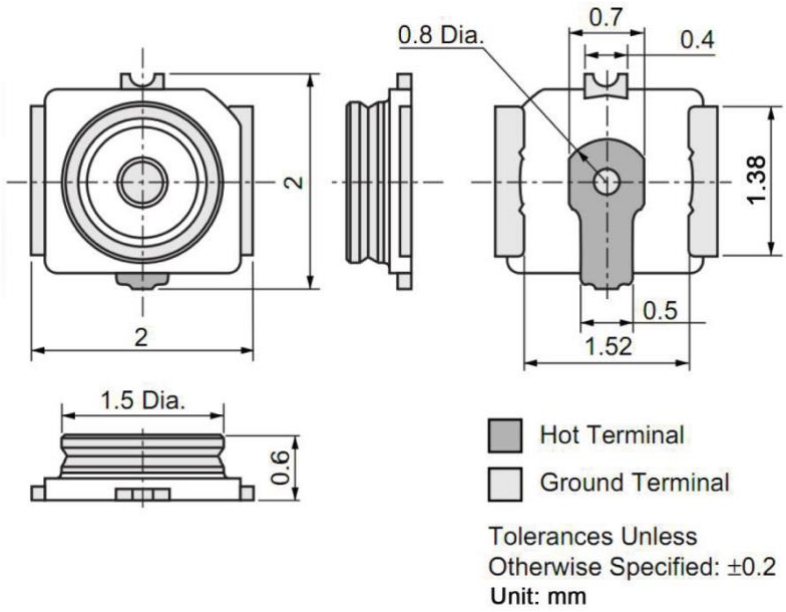


Figure 34: EM120R-GL&EM160R-GL RF Connector Dimensions (Unit: mm)

Table 33: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

The receptacle RF connector used in conjunction with EM120R-GL&EM160R-GL will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø0.81 mm coaxial cable or a maximum height of 1.4 mm utilizing a Ø1.13 mm coaxial cable.

The following figure shows the specifications of mating plugs using Ø0.81 mm coaxial cables.

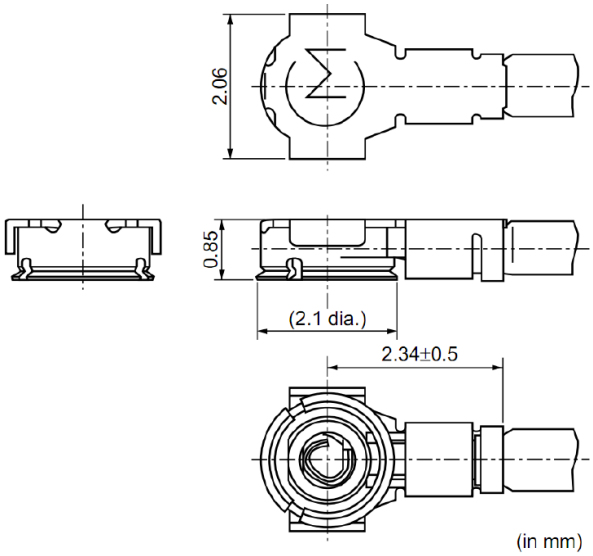


Figure 35: Specifications of Mating Plugs Using Ø0.81 mm Coaxial Cables

The following figure illustrates the connection between the receptacle RF connector on EM120R-GL&EM160R-GL and the mating plug using a Ø0.81 mm coaxial cable.

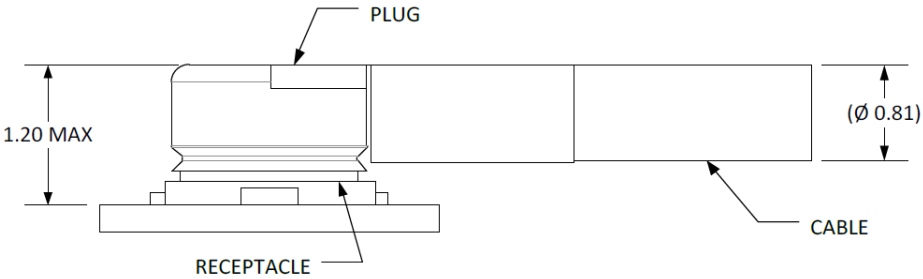


Figure 36: Connection between RF Connector and Mating Plug Using Ø0.81 mm Coaxial Cable

The following figure illustrates the connection between the receptacle RF connector on EM120R-GL&EM160R-GL and the mating plug using a Ø1.13 mm coaxial cable.

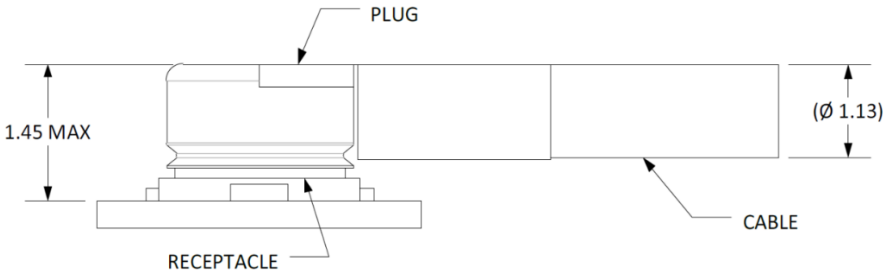


Figure 37: Connection between RF Connector and Mating Plug Using Ø1.13 mm Coaxial Cable

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the modules are listed in the following table.

Table 34: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VCC	-0.3	4.7	V
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Requirements

The typical input voltage of EM120R-GL&EM160R-GL is 3.7 V, as specified by *PCIe M.2 Electromechanical Spec Rev1.0*. The following table shows the power supply requirements of the modules.

Table 35: Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V

6.3. I/O Requirements

Table 36: I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × V_{DD18} [1)]	V_{DD18} + 0.3	V
V_{IL}	Input low voltage	-0.3	0.3 × V_{DD18}	V
V_{OH}	Output high voltage	V_{DD18} - 0.5	V_{DD18}	V
V_{OL}	Output low voltage	0	0.4	V

NOTE

[1)] V_{DD18} refers to I/O power domain.

6.4. Operation and Storage Temperatures

Table 37: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature Range [1)]	-25	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant. For those end devices with bad thermal dissipation condition, a thermal pad or other thermal conductive components may be required between the module and main PCB to achieve the full operating temperature range.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like

P_{out} might reduce in their values and exceed the specified tolerances. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

6.5. Current Consumption

Table 38: EM120R-GL&EM160R-GL Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VCC}	OFF state	Power down	TBD	μA

6.6. RF Output Power

The following table shows the RF output power of EM120R-GL&EM160R-GL.

Table 39: RF Output Power

Frequency	(Quectel SPEC) Max.	Min.
WCDMA band 1, 3, 5, 8	24 dBm +1.5/-3 dB	< -50 dBm
LTE-FDD band 1, 3, 5, 7, 8, 20, 28	23 dBm ±2 dB	< -40 dBm
LTE-TDD band 38, 40, 41, 42, 43	23 dBm ±2 dB	< -40 dBm

6.7. RF Receiving Sensitivity

The following tables show conducted RF min. receiving sensitivity of EM120R-GL and EM160R-GL.

Table 40: EM120R-GL&EM160R-GL Conducted RF Min. Receiving Sensitivity

Frequency	Primary	Diversity	SIMO [1)]	SIMO [2)] (Worst Case)
WCDMA B1	-111	-110	-110.5	-106.7 dBm
WCDMA B2	-109.5	-110	-110	-104.7 dBm
WCDMA B3	-109.5	-110.5	-111	-103.7 dBm
WCDMA B4	TBD	TBD	TBD	-106.7 dBm
WCDMA B5	-111	-111	-112	-104.7 dBm
WCDMA B6	TBD	TBD	TBD	-106.7 dBm
WCDMA B8	-111.5	-110.5	-111	-103.7 dBm
WCDMA B19	TBD	TBD	TBD	-106.7 dBm
LTE-FDD B1 (10 MHz)	-98	-98	-100.7	-96.3 dBm
LTE-FDD B2 (10 MHz)	-97.8	-97.7	-100.3	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98.8	-97.3	-100.8	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97.7	-97.9	-100.6	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.7	-99	-102	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96	-97.2	-99.4	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99	-99.2	-101.7	-93.3 dBm
LTE-FDD B12 (10 MHz)	-99.8	-99.5	-102.3	-93.3 dBm
LTE-FDD B13 (10 MHz)	-100.2	-99.4	-102.5	-93.3 dBm
LTE-FDD B14 (10 MHz)	-99.2	-99.2	-101.8	-93.3 dBm
LTE-FDD B17 (10 MHz)	-99.9	-99.6	-102.3	-93.3 dBm
LTE-FDD B18 (10 MHz)	-99.6	-99.4	-102.2	-96.3 dBm

LTE-FDD B19 (10 MHz)	-99.7	-99	-102	-96.3 dBm
LTE-FDD B20 (10 MHz)	-99.7	-99.5	-102.2	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.8	-97.6	-100.3	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.4	-99.1	-101.9	-93.8 dBm
LTE-FDD B28 (10 MHz)	-99.3	-99.6	-102.1	-94.8 dBm
LTE-FDD B30 (10 MHz)	-96	-97.4	-99.5	-95.3 dBm
LTE-TDD B38 (10 MHz)	-98.4	-97	-100.1	-96.3 dBm
LTE-FDD B39 (10 MHz)	-98.4	-97.5	-100.5	-96.3 dBm
LTE-TDD B40 (10 MHz)	-96.3	-96.9	-99.2	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98.1	-96.1	-99.7	-94.3 dBm
LTE-TDD B42 (10 MHz)	-97.3	-98.7	-100.7	-95.0 dBm
LTE-TDD B43 (10 MHz)	-97.4	-98.4	-100.7	-95.0 dBm
LTE-TDD B48 (10 MHz)	-97.3	-98.5	-100.6	-95.0 dBm
LTE-FDD B66 (10 MHz)	-97.6	-97.8	-100.4	-95.8 dBm

NOTES

1. [1)] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and multiple antennas at the receiver side, which can improve Rx performance.
2. [2)] Per 3GPP specification.

6.8. Characteristics

The modules are not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the modules.

The following table shows the modules' electrostatic discharge characteristics.

Table 41: Electrostatic Discharge Characteristics (Temperature: 25 ºC, Humidity: 40%)

Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	TBD	TBD	kV
Antenna Interfaces	TBD	TBD	kV
Other Interfaces	TBD	TBD	kV

6.9. Thermal Dissipation

EM120R-GL&EM160R-GL are designed to work over an extended temperature range. In order to achieve a better performance while working under extended temperatures or extreme conditions (such as with maximum power or data rate, etc.) for a long time, it is strongly recommended to add a thermal pad or other thermally conductive compounds between the module and the main PCB for thermal dissipation.

The thermal dissipation area (i.e. the area for adding thermal pad) is shown as below. The dimensions are measured in mm.

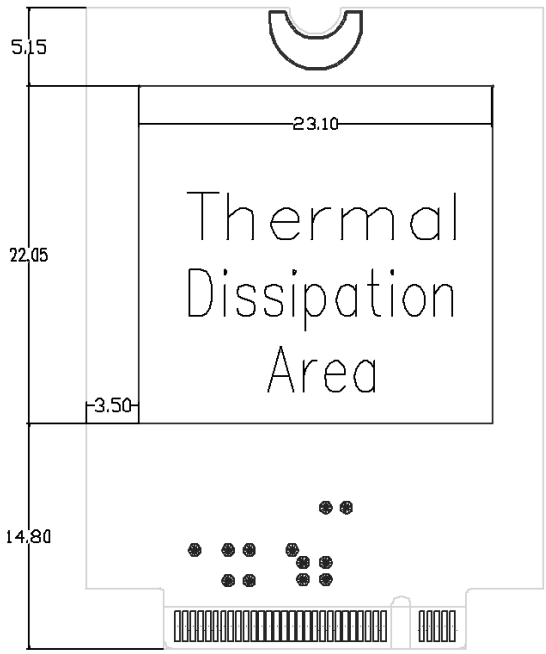


Figure 38: Thermal Dissipation Area on Bottom Side of Module (Top View)

There are some other measures to enhance heat dissipation performance:

- Add ground vias as many as possible on PCB.
- Maximize airflow over/around the module.
- Place the module away from other heating sources.
- Module mounting holes must be used to attach (ground) the device to the main PCB ground.
- It is NOT recommended to apply solder mask on the main PCB where the module's thermal dissipation area is located.
- Select an appropriate material, thickness and surface for the outer housing (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.
- Customers may also need active cooling to pull heat away from the module.
- If possible, add a heatsink on the top of the module. A thermal pad should be used between the heatsink and the module, and the heatsink should be designed with as many fins as possible to increase heat dissipation area.

NOTE

For more detailed guidelines on thermal design, refer to ***document [5]***.

7 Mechanical Dimensions and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of EM120R-GL&EM160R-GL. All dimensions are measured in mm, and the dimensional tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

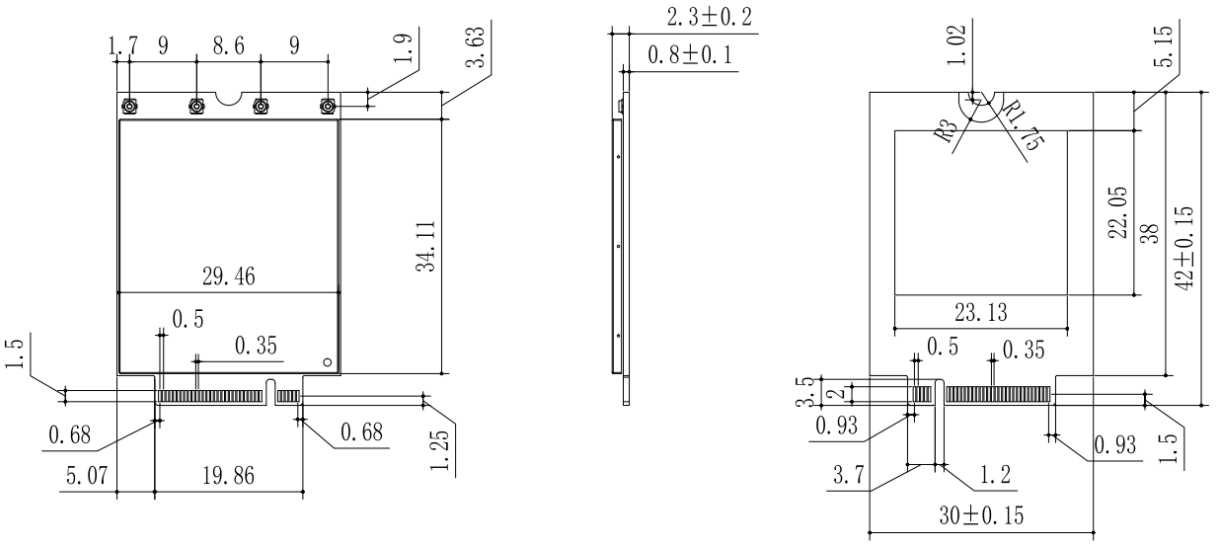


Figure 39: Mechanical Dimensions of EM120R-GL&EM160R-GL (Unit: mm)

7.2. Standard Dimensions of M.2 PCI Express

The following figure shows the standard dimensions of M.2 PCI Express, refer to ***document [6]***.

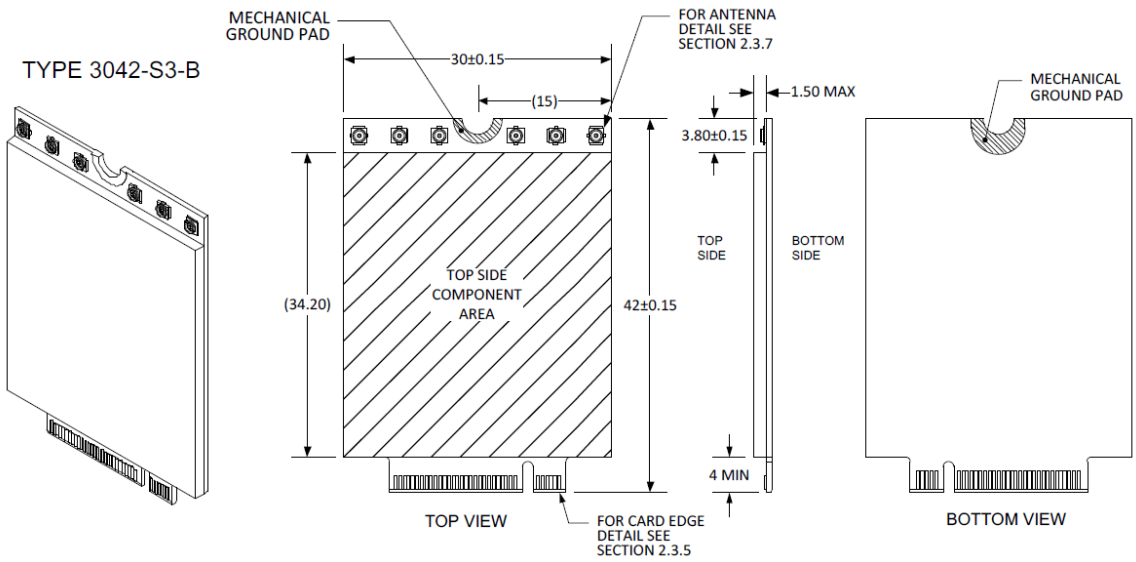
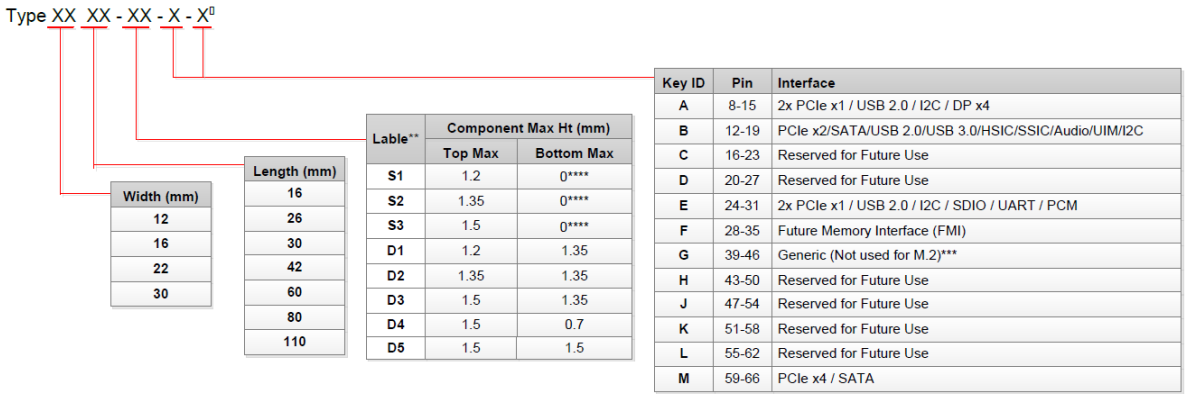


Figure 40: Standard Dimensions of M.2 Type 3042-S3 (Unit: mm)

According to M.2 nomenclature, EM120R-GL&EM160R-GL are Type 3042-S3-B (30.0 mm × 42.0 mm, max component height on the top is 1.5 mm and single-sided, key ID is B).



Width (mm)
12
16
22
30

Length (mm)
16
26
30
42
60
80
110

Lable**	Component Max Ht (mm)	
	Top Max	Bottom Max
S1	1.2	0****
S2	1.35	0****
S3	1.5	0****
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5

Key ID	Pin	Interface
A	8-15	2x PCIe x1 / USB 2.0 / I2C / DP x4
B	12-19	PCIe x2/SATA/USB 2.0/USB 3.0/HSIC/SSIC/Audio/UIM/I2C
C	16-23	Reserved for Future Use
D	20-27	Reserved for Future Use
E	24-31	2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)***
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	PCIe x4 / SATA

* Use ONLY when a double slot is being specified
** Label included in height dimension
*** Key G is intended for custom use. Devices with this key will not be M.2-compliant. Use at your own risk!
**** Insulating label allowed on connector-based designs

Figure 41: M.2 Nomenclature

7.3. Design Effect Drawings of the Module

7.3.1. Design Effect Drawings of EM160R-GL Module

Figure 42: Top View of the Module

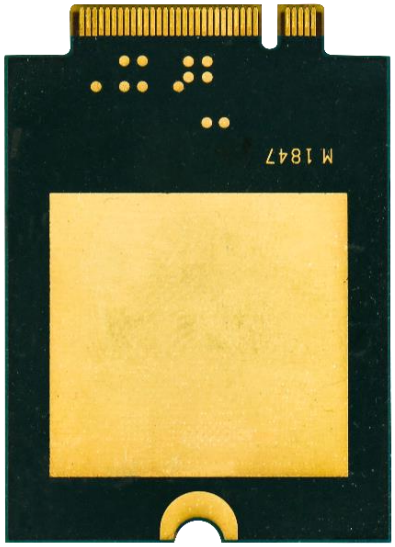


Figure 43: Bottom View of the Module

7.3.2. Design Renderings of EM120R-GL Module

Figure 44: Top View of the Module

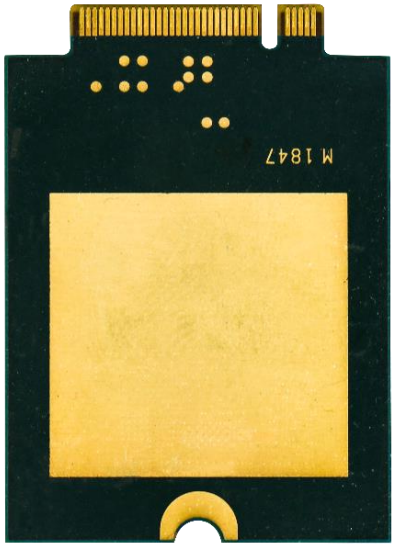


Figure 45: Bottom View of the Module

NOTE

These are renderings of EM120R-GL&EM160R-GL. For authentic appearance, refer to the modules that you receive from Quectel.

7.4. M.2 Connector

EM120R-GL&EM160R-GL adopt a standard PCI Express M.2 connector which compiles with the directives and standards listed in the ***document [6]***.

7.5. Packaging

EM120R-GL&EM160R-GL are packaged in trays. The following figure shows the tray size.

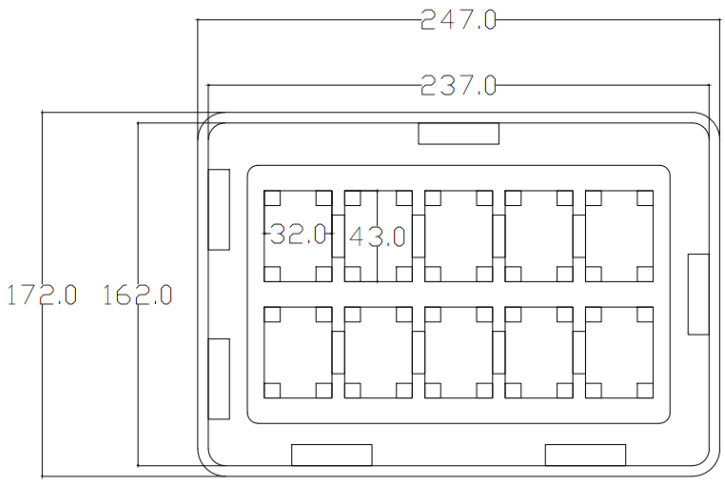


Figure 46: Tray Size (Unit: mm)

Each tray contains 10 modules. The smallest package contains 100 modules. Tray packaging procedures are as below.

1. Use 10 trays to package 100 modules at a time (tray size: 247 mm × 172 mm).
2. Place an empty tray on the top of the 10-tray stack.
3. Fix the stack with masking tape in “#” shape as shown in the following figure.
4. Pack the stack with conductive bag, and then fix the bag with masking tape.
5. Place the list of IMEI No. into a small carton.
6. Seal the carton and then label the seal with sealing sticker (small carton size: 250 mm × 175 mm × 128 mm).

Figure 47: Tray Packaging Procedure

8 Appendix References

Table 42: Related Documents

SN	Document Name	Remark
[1]	Quectel_EM120R-GL&EM160R-GL_CA_Feature	EM120R-GL&EM160R-GL CA Feature
[2]	Quectel_M.2_EVB_User_Guide	M.2 EVB User Guide
[3]	Quectel_EM120R-GL&EM160R-GL_AT_Commands_ Mannual	EM120R-GL&EM160R-GL AT Commands Manual
[4]	Quectel_EM120R-GL&EM160R-GL_GNSS_AT_ Commands_ Manual	EM120R-GL&EM160R-GL GNSS AT Commands Manual
[5]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal Design Guide for LTE Modules
[6]	PCI Express M.2 Specification	

Table 43: Terms and Abbreviations

Abbreviation	Description
bps	Bits Per Second
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRx	Diversity Receive
ESD	Electrostatic Discharge
FDD	Frequency Division Duplexing
GLONASS	Globalnaya Navigatsionnaya Sputnikovaya Sistema (the Russian Global Navigation Satellite System)
GNSS	Global Navigation Satellite System

GPS	Global Positioning System
GSM	Global System for Mobile Communications
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
kbps	Kilo Bits Per Second
LED	Light Emitting Diode
LTE	Long Term Evolution
Mbps	Million Bits Per Second
ME	Mobile Equipment (Module)
MIMO	Multiple-Input Multiple-Output
MLCC	Multiplayer Ceramic Chip Capacitor
MMS	Multimedia Messaging Service
MO	Mobile Originated
MT	Mobile Terminated
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PRx	Primary Receive
RF	Radio Frequency
Rx	Receive
SAR	Specific Absorption Rate
SMS	Short Message Service
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
URC	Unsolicited Result Code

(U)SIM	(Universal) Subscriber Identification Module
WCDMA	Wideband Code Division Multiple Access

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2020EM160RGL2” “Contains IC: XMR2020EM160RGL2”. The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed

Test Mode	Antenna Gain (dBi)	Test Mode	Antenna Gain (dBi)
WCDMA B2	8.00	LTE B14	5.00
WCDMA B4	8.00	LTE B25	8.00
WCDMA B5	5.00	LTE B26	5.00
LTE B2	8.00	LTE B30*	5.00
LTE B4	8.00	LTE B38	8.00
LTE B5	5.00	LTE B41	6.50
LTE B7	8.00	LTE B48*	5.00
LTE B12	5.00	LTE B66	8.00
LTE B13	5.00		

Note: “*” means when using these maximum gain antenna, the host manufacturer should reduce the conducted power to meet the FCC maximum RF output power limit.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.