EG915U Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-12-20	Len CHEN/ Manimo YANG/ Ailsa WANG/ Yunsheng LI	Creation of the document
1.0	2022-01-05	Len CHEN/ Manimo YANG/ Ailsa WANG/ Yunsheng LI	First official release
1.1	2023-01-17	Len CHEN/ Evan WANG	1. Added the description on test points for VDD_EXT, PWRKEY, RESET_N, USB interface, USIM2_DET, Debug UART interface, and USB_BOOT. 2. Updated the information on USB serial drivers; Added SMTP and SMTPS as supported protocols (Table 4). 3. Changed the ADC minimum voltage from 0.1 V to 0 V and updated note 3 (Tables 6 and 22). 4. Added the current requirements for GSM or GSM & LTE and for LTE only; Updated power supply reference design (Chapter 3.5.2). 5. Added a 10 nF capacitor in the reference circuits controlling PWRKEY and RESET_IN with a button (Figures 11 and 16). 6. Added the description of analog output channel used as loudspeaker and handset (Chapter 4.1). 7. Updated the reference design for earpiece interface (Figure 19). 8. Added the timing of the short frame mode of PCM interface; Deleted the external clock scheme of codec chip and added note 3 on clock signal

			(Chapter 4.5). 9. Updated power consumption (Chapter 6.3). 10. Updated the recommended values of ramp-to-soak slope in soak zone, ramp-up slope and cool-down slope in reflow zone and add a note (Chapter 8.2). 11. Added mounting direction (Chapter 8.3.4).
1.2	2024-05-14	Phoebe FU/ Woping WANG	1. Updated the functional diagram (Figure 1). 2. Added the description that the use of VDD_EXT requires a TVS; Added a comment on USB_VBUS pin (Tables 6 and 14). 3. Added a note on VBAT voltage requirement before the module's power-on; Added a note on turn-on scenarios (Chapter 3.6.1). 4. Added a note on RESET_N pin (Chapter 3.8). 5. Updated the reference design for microphone interface (Figure 19). 6. Added a note on UART hardware flow control design (Chapter 4.6). 7. Added two notes on RF antenna design (Chapter 5.1.3). 8. Added two notes specifying that mercury-containing materials and environments containing corrosive gases should be avoided for module processing (Chapter 8.2).
1.3	2025-01-17	Phoebe FU/ Woping WANG/ Kevin WANG	1. Updated pin 123–125 from RESERVED to HP_L, HP_R and HP_DET. 2. Updated reference circuit for RF antenna interface and added relevant notes (Chapter 5.1.3). 3. Updated the maximum voltage on digital pins (Table 33). 4. Updated the power consumption of EG915U-LA (Table 37). 5. Updated the conducted RF Rx sensitivity of EG915U-LA (Table 41). 6. Updated the module coplanarity requirement (Chapter 7.1). 7. Updated the pre-baking time to 24 h (Chapter 8.1).
1.4	2025-07-08	Forest LIN/ Woping WANG/ Kevin WANG	1. Specified that voice functionality is an optional function. 2. Update PSRAM to 128 MB/ 64 Mb (Figure 1). 3. Updated Cat level to Cat 1bis. 4. Added a note specifying that the power consumption data are tested under 50 Ω impedance (Chapter 6.3).

	5. Updated the power consumption of EG915U-EU/LA (Table 36 & Table 37). 6. Updated the conducted RF Rx sensitivity (Chapter 6.5).

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1 Introduction

This document defines the EG915U series module and describes its air interfaces and hardware interfaces which relate to customers' applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

EG915U series module is an LTE and GSM wireless communication module, which provides data connectivity on LTE-FDD, LTE-TDD, and GPRS networks. It also provides voice functionality[1], Bluetooth and Wi-Fi Scan [2] to meet your specific application demands. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Category	
Packaging and Number of Pins	LGA; 126 pins
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm
Weight	2.5 ±0.2 g
Wireless Network Functions	LTE/GSM/Bluetooth [2]/Wi-Fi Scan [2]
Models	EG915U-CN; EG915U-EU; EG915U-LA

2.1. Frequency Bands and Functions

Table 3: Frequency Bands

Wireless Network Type	EG915U-CN	EG915U-EU	EG915U-LA
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28	B2/B3/B4/B5/B7/B8/B28/B66
LTE-TDD	B34/B38/B39/B40/B41	-	-
GSM/GPRS	EGSM900/DCS1800	GSM850/EGSM900/DCS1800/PCS1900	GSM850/EGSM900/DCS1800/PCS1900

[1] Voice functionality is optional. For more details, please contact Quectel Technical Support.
[2] The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.

Bluetooth (Optional) [2]	Bluetooth 4.2 (BR/EDR + LE)	Bluetooth 4.2 (BR/EDR + LE)	Bluetooth 4.2 (BR/EDR + LE)
Wi-Fi Scan (Optional) [2]	2.4 GHz	2.4 GHz	2.4 GHz

NOTE

B41 of EG915U-CN only supports 140 MHz (2535–2675 MHz).

2.2. Key Features

The following table describes the detailed features of EG915U series module.

Table 4: Key Features

Feature	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	**EG915U-CN:** ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB) **EG915U-EU & EG915U-LA:** ● GSM850/EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800/PCS1900: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	**EG915U-CN:** ● Supports up to 3GPP Rel-13 Cat 1 bis FDD/TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK and 16QAM ● Supports downlink QPSK, 16QAM, and 64QAM ● Max. transmission data rates: LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL) **EG915U-EU & EG915U-LA:** ● Supports up to 3GPP Rel-13 Cat 1 bis FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK and 16QAM ● Supports downlink QPSK, 16QAM, and 64QAM

	● Max. transmission data rates: LTE-FDD: 10 Mbps (DL)/5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. transmission data rates: 85.6 kbps (DL)/85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols ● Supports PAP and CHAP protocols, which are usually used for PPP connection
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
(U)SIM Interfaces	● Supports USIM/SIM card: 1.8/3.0 V ● Supports Dual SIM Single Standby by default [3]
USB Interface	● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrade ● Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7, and Android 4.x–13.x
UART Interfaces	**Main UART** ● Used for AT command communication and data transmission ● Baud rates: up to 921600 bps; 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART** ● Used for log output ● Baud rate: 921600 bps ● Cannot be used as a general-purpose UART **Auxiliary UART** The baud rate is the same as that of the main UART
SPI* [4]	Supports one SPI (master mode only)
I2C Interface	● Supports one I2C interface ● Complies with the I2C-bus specification
PCM Interface	● Supports one PCM interface requiring an external codec ● Supports slave mode only
Analog Audio Interfaces	● Supports one analog audio input and two analog audio output channels ● HR/FR/EFR/AMR/AMR-WB

[3] Please contact Quectel Technical Support if Dual SIM Dual Standby is required.
[4] If you need SPI, please contact Quectel Technical Support.

	● Supports echo cancellation and noise suppression
ADC Interfaces	Supports two ADC Interfaces
Indication Signals	● NET_STATUS indicates the module's network activity status ● STATUS indicates the module's operation status ● MAIN_RI indicates URC reporting
AT Commands	● Compliant with *3GPP TS 27.007, 3GPP TS 27.005* ● Quectel enhanced AT commands
USB_BOOT Interface	● Supports one USB_BOOT interface ● Forces the module to enter download mode
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Bluetooth and Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) [5] ● 50 Ω characteristic impedance
Position Fixing	Supports Wi-Fi Scan [5]
Temperature Range	● Operating temperature range: -35 to +75 °C [6] ● Extended temperature range: -40 to +85 °C [7] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Via USB interface or DFOTA
RoHS	All hardware components are fully compliant with *EU RoHS Directive*

[5] The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.

[6] Within this range, the module's indicators comply with 3GPP specification requirements.

[7] Within this range, the module retains the ability to establish and maintain functions such as voice (optional), SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Pin Assignment

The following figure illustrates the pin assignment of the module.

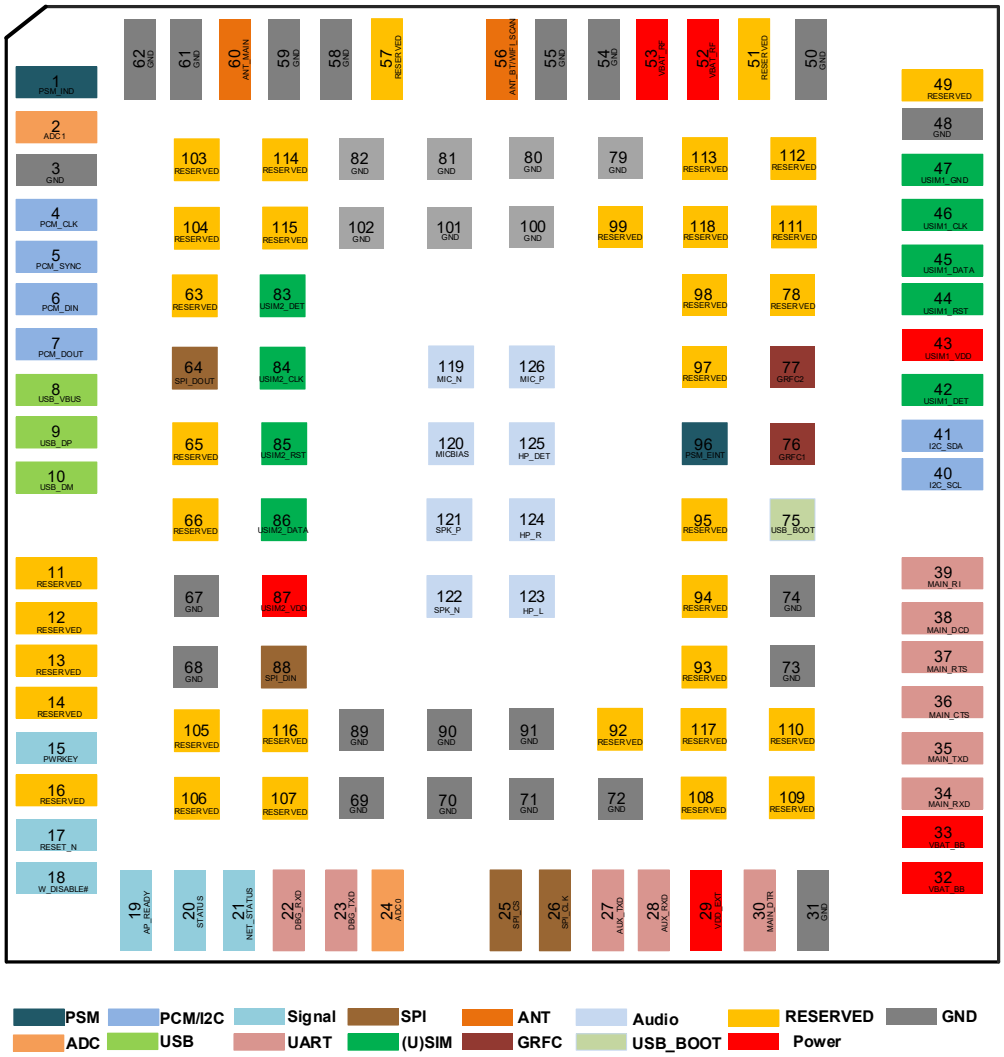


Figure 1: Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up before the module's startup, if forced download mode is not required.
2. Keep unused and RESERVED pins unconnected, and connect all GND pins to ground.
3. The module supports Dual SIM Single Standby by default. For details, please contact Quectel Technical Support.
4. When using pins 18, 19, 30, 38, and 39 (W_DISABLE#, AP_READY, MAIN_DTR, MAIN_DCD and MAIN_RI), please note that these pins will have a period of variable level state (not controllable by

software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

2.4. Pin Description

The following tables show the pin definition of the module.

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of 1 A at least.

					Test points are recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current of at least 2.5 A. Test points are recommended to be reserved.
VDD_EXT	29	PO	Provides 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Used with a 2.2 μF capacitor and a TVS. A test point is recommended to be reserved.
Turn-on/off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turns on/off the module	V_{IL}max = 0.5 V	VBAT power domain. Active low. A test point is recommended to be reserved.
RESET_N	17	DI	Resets the module		VBAT power domain. Active low. A test point is recommended to be reserved if unused.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicates the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep them open.
NET_STATUS	21	DO	Indicates the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_VBUS	8	AI	USB connection detect	Input voltage range: 3.5 V to 5.25 V	A test point must be reserved. The USB_VBUS pin needs to be connected with a 1 kΩ resistor in series if USB_VBUS is connected to power supply and VBAT is powered down.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V	

USIM1_RST	44	DO	(U)SIM1 card reset	V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Specified ground for (U)SIM1 card		
USIM2_VDD	87	PO	(U)SIM2 card power supply	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	84	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. A test point must be reserved for debugging.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	36	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to MCU's CTS.

					1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive		1.8 V power domain. If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_TXD	35	DO	Main UART transmit		
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_TXD	27	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Test points must be reserved for debugging.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM and I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

I2C_SCL	40	OD	I2C serial clock		External pull-up resistor is required. 1.8 V power domain only. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM_SYNC	5	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open. Support slave mode only.
PCM_CLK	4	DI	PCM clock		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_BT/ WIFI_SCAN [8]	56	AIO	The shared antenna interface for Bluetooth and Wi-Fi Scan		Wi-Fi Scan antenna can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.
GRFC Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	76	DO	Generic RF Controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
GRFC2	77	DO			
SPI* [9]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

[8] The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.
[9] If you need SPI, please contact Quectel Technical Support.

SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Supports master mode only. If unused, keep them open.
SPI_CS	25	DO	SPI chip select		
SPI_DIN	88	DI	SPI data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_DOUT	64	DO	SPI data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interfaces	Input voltage range: 0 V to VBAT	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2	AI			
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_N	119	AI	Microphone analog input (-)		If unused, keep them open.
MICBIAS	120	PO	Bias voltage output for microphone	Vmax = 3.0 V Vmin = 2.2 V Vnom = 2.2 V	
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
MIC_P	126	AI	Microphone analog input (+)		
HP_L	123	AO	Headphone left channel output		
HP_R	124	AO	Headphone right channel output		
HP_DET	125	DI	Headphone hot-plug detect		
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_BOOT	75	DI	Forces the module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that enables the module to enter the forced download mode must be reserved. A test point is recommended to be reserved.
PSM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_IND*	1	DO	Indicates the module's power saving mode	1.8 V power domain	If unused, keep it open.
PSM_EINT	96	DI	External interrupt pin. Wakes up the module from PSM		The module will be woken up from PSM when this pin is pulled up externally. If unused, keep it open.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. Driving it low can enable the module into the airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor ready		1.8 V power domain. If unused, keep it

	open.
GND	
Pin Name	**Pin No.**
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102
RESERVED	
Pin Name	**Pin No.**
RESERVED	11–14, 16, 49, 51, 57, 63, 65, 66, 78, 92–95, 97–99, 103–118

NOTE

When using pins 18, 19, 30, 38, and 39 (W_DISABLE#, AP_READY, MAIN_DTR, MAIN_DCD and MAIN_RI), please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

2.5. EVB Kit

Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The following table briefly outlines the operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network and is ready to send and receive data.
	Voice (Optional) /Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or pulling down W_DISABLE# pin can set the module to airplane mode. In this case, RF function is invalid.	
Sleep Mode	In this mode, power consumption of the module is reduced to an ultra-low level. The module remains the ability to receive paging message, SMS, voice calls (Optional) and TCP/UDP data from network normally.	
PSM	In this mode, power consumption of the module is reduced to a minimized level. AT command cannot be sent to the module.	
Power Down Mode	PMU shuts down the power supply. Software is not active. However, operating voltage connected to VBAT pins remains applied.	

NOTE

For more details about AT commands, see ***document [2]***.

3.2. Sleep Mode

With DRX technology, the module is able to reduce its power consumption to an ultra-low level in the sleep mode.

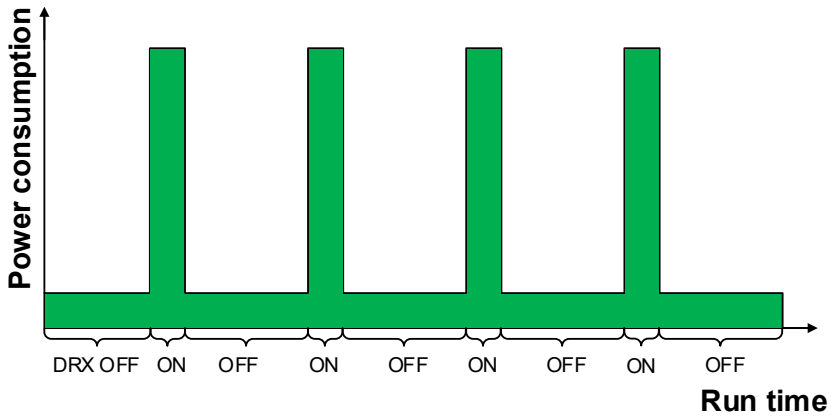


Figure 2: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the MCU communicates with module via UART interface, the following preconditions should be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode. See ***document [3]*** for details.
- Drive MAIN_DTR to high level or keep it unconnected.

The following figure shows the connection between the module and the MCU.

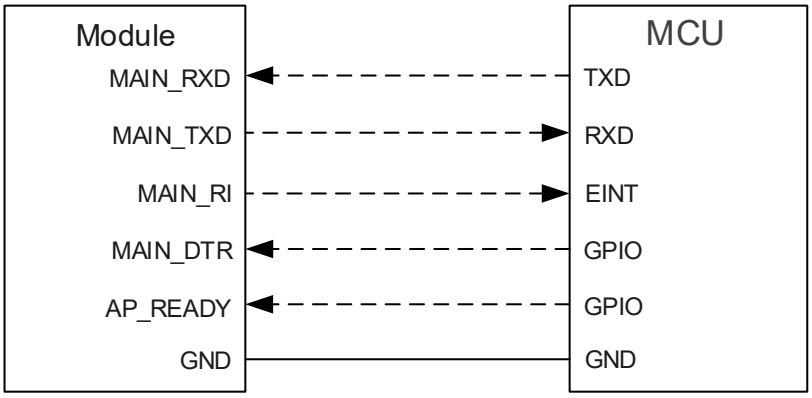


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR low will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 4.9.3*** for details about MAIN_RI behaviors.

NOTE

When using pins 19, 30 and 39 (AP_READY, MAIN_DTR and MAIN_RI), please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

3.2.2. USB Application Scenarios

For the scenarios mentioned in ***Chapters 3.2.2.1*** and ***3.2.2.2***, three preconditions must be met to make the module enter the sleep mode:

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at a high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters Suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function

The following figure illustrates the connection between the module and the host if the host supports USB Suspend/Resume and remote wakeup function.

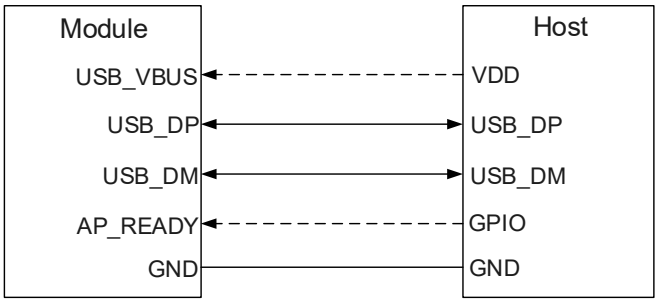


Figure 4: Sleep Mode Application with USB Remote Wakeup

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the module will send remote wake-up signals to USB bus to wake up the host.

NOTE

USB Suspend is supported on Linux system but not on Windows system.

3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend/Resume, but does not support remote wake-up function, the MAIN_RI signal is needed to wake up the host.

The following figure illustrates the connection between the module and the host.

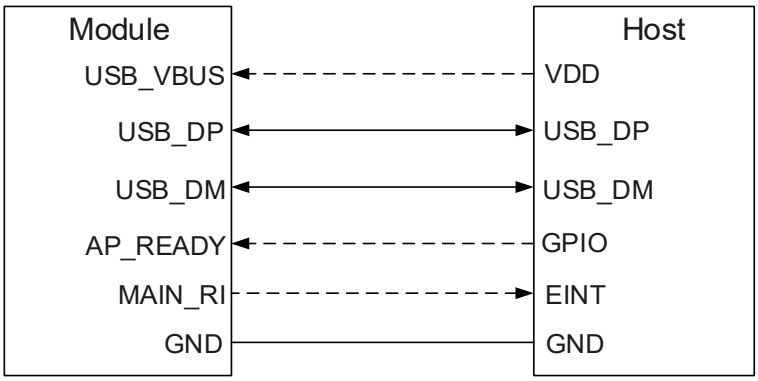


Figure 5: Sleep Mode Application with MAIN_RI

- You can wake up the module by sending data to it through USB.

- When the module has a URC to report, the URC will trigger the behaviors of MAIN_RI pin. See ***Chapter 4.9.3*** for details about MAIN_RI behaviors.

NOTE

USB Suspend is supported on Linux system but not on Windows system.

3.2.2.3. USB Application Without USB Suspend Function

If the host does not support USB Suspend function, disconnect USB_VBUS with an externally-controlled circuit to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at a high level or keep it open.
- Disconnect the USB_VBUS.

The following figure illustrates the connection between the module and the host.

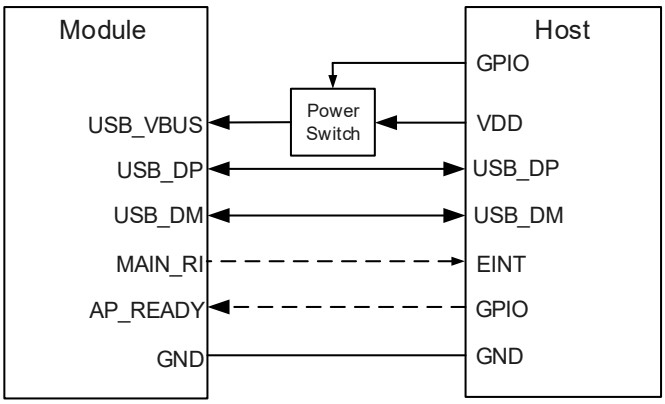


Figure 6: Sleep Mode Application Without Suspend Function

You can wake up the module by restoring the power supply to USB_VBUS.

NOTE

1. Please pay attention to the level match shown in dotted line between the module and the host.
2. When using pins 19 and 39 (AP_READY and MAIN_RI), please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

3.3. Airplane Mode

When the module enters airplane mode, the RF function is disabled and all AT commands related to it are inaccessible. This mode can be set via the following ways.

Hardware:

Driving W_DISABLE# to low level can make the module enter airplane mode. See ***Chapter 4.10*** for details.

Software:

AT+CFUN=<fun> provides the choice of functionality level through setting **<fun>** to 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality. Both RF function and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality (by default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled).

3.4. PSM

The module supports power saving mode (PSM). It enters the PSM through executing the following AT commands sequentially when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling up the PSM_EINT pin externally or setting the timer by software will enable the module to exit PSM.

Table 8: Pin Definition of PSM_IND and PSM_EINT

Pin Name	Pin No.	I/O	Description	Comment
PSM_IND*	1	DO	Indicates the module's power saving mode	If unused, keep it open.
PSM_EINT	96	DI	External interrupt pin. Wakes up the module from PSM	The module will be woken up from PSM when this pin is pulled up externally. If unused, keep it open.

3.5. Power Supply

3.5.1. Power Supply Pins

The module provides four VBAT pins for connection with an external power supply.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 9: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	52, 53	PI	Power supply for the module's RF part	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.5.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3.0 A when the GSM or both GSM and LTE are available and provide sufficient current of 2.0 A when only LTE is available. If the voltage drop between input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for 5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

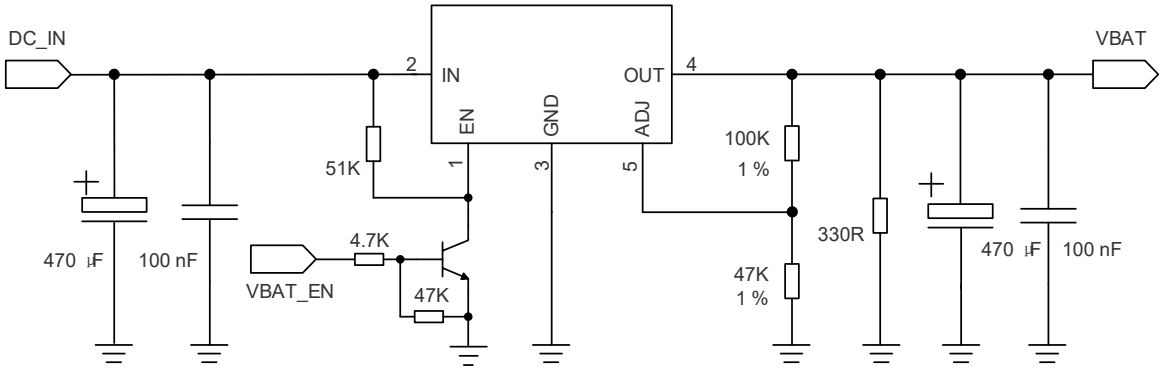


Figure 7: Reference Design of Power Supply

3.5.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage never drops below 3.3 V.

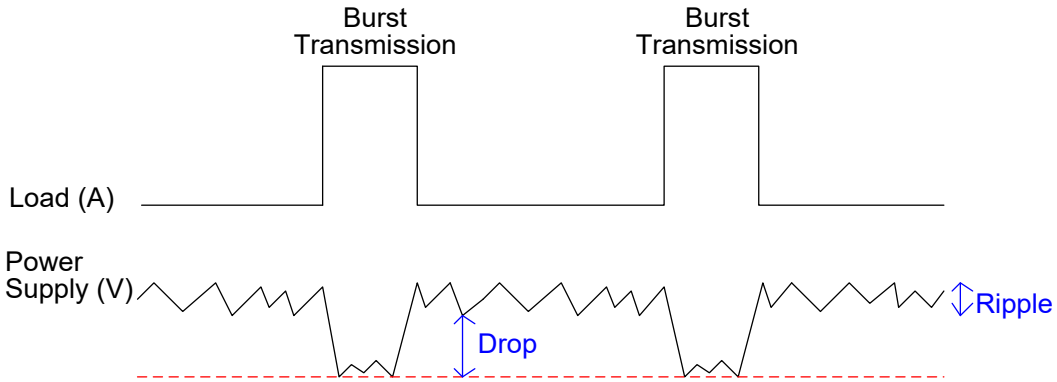


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage drop, a filter capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be at least 2 mm; and the width of VBAT_RF trace should be at least 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The reference circuit is shown as below.

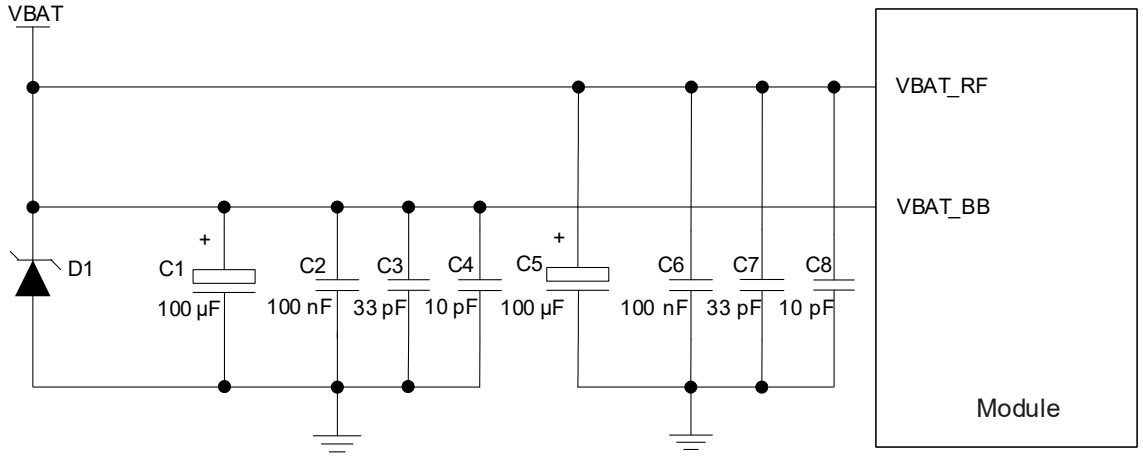


Figure 9: Power Supply

3.6. Turn-on

3.6.1. Turn-on with PWRKEY

Table 10: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turns on/off the module	VBAT power domain. Active low. A test point is recommended to be reserved.

When the module is in turn-off mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

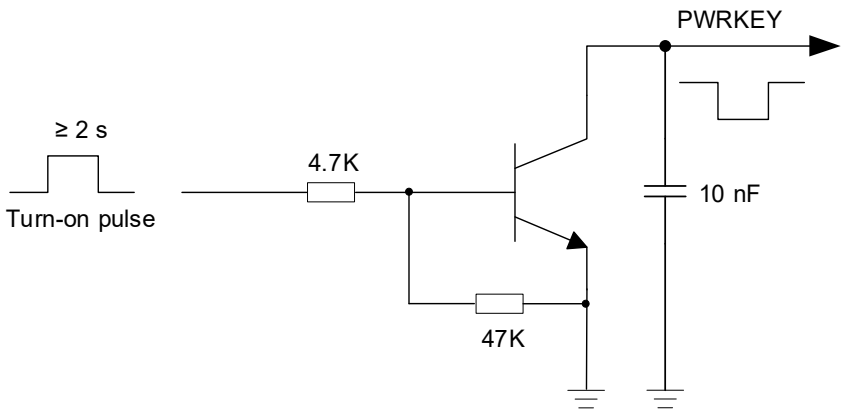


Figure 10: Turning On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the button, electrostatic strike may be generated from finger. Therefore, you must place a TVS nearby the button for ESD protection. A reference circuit is shown in the following figure.

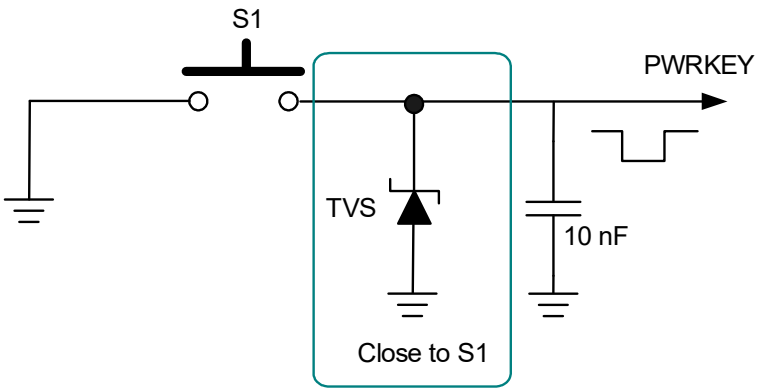


Figure 11: Turning On the Module Using Button

If the module needs to turn on automatically, PWRKEY can be driven low directly to ground with a recommended resistor less than 1 kΩ. However, ensure that the voltage of VBAT_BB and VBAT_RF pins is below 0.5 V before power-up.

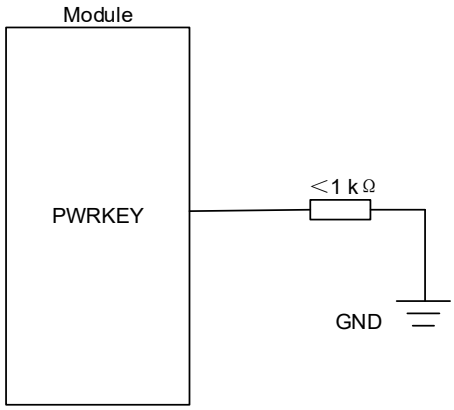


Figure 12: Turning On the Module Automatically

The turn-on timing is illustrated in the following figure.

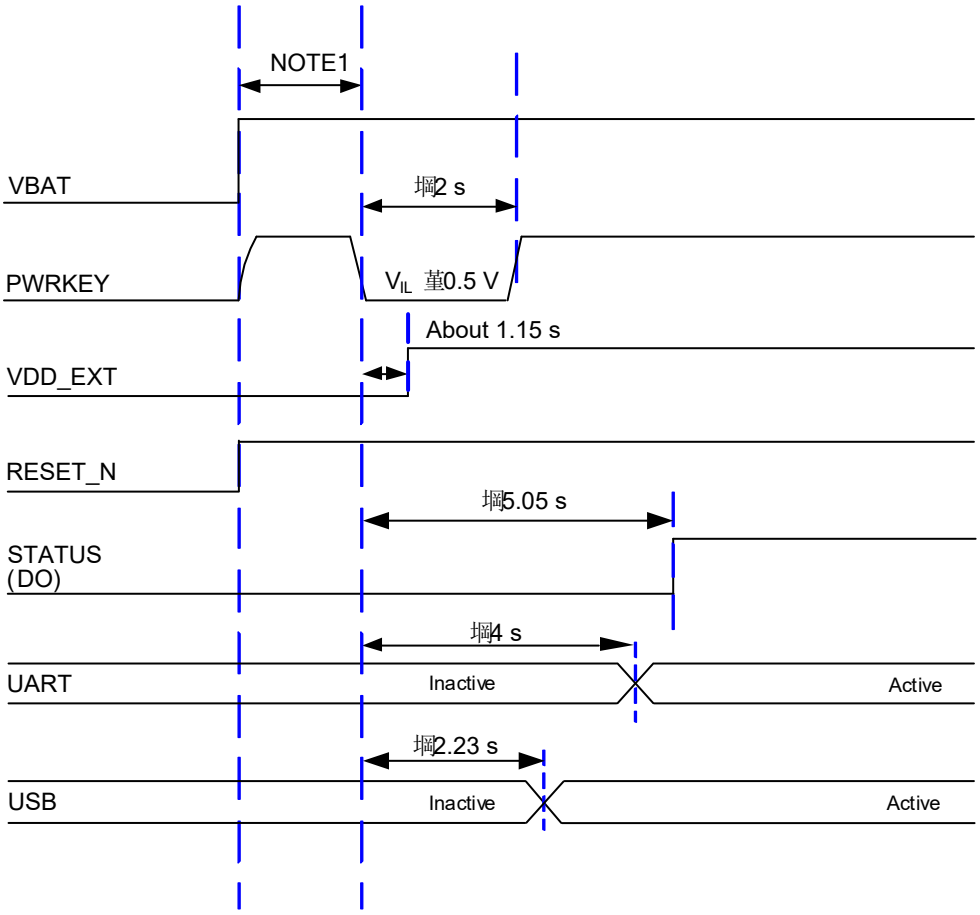


Figure 13: Turn-on Timing

NOTE

1. Before pulling down the PWRKEY, ensure that the VBAT voltage is stable within the recommended range of 3.3–4.3 V. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. When PWRKEY is connected to GND with a pull-down resistor, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and power up the module again. Therefore, it is recommended to use a control circuit to control the PWRKEY to turn on/off the module.
3. Ensure that the VBAT voltage is less than 0.5 V before powering up the module again. If MOSFET is used to control the VBAT power supply, a discharge circuit must be designed to ensure that the VBAT voltage can be released quickly after the module is turned off and powered down.
4. Pay special attention to the following two turn-on scenarios:
   - In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is powered up later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered up stably for at least 2 s before PWRKEY is pulled down;
   - In the scenario where VBAT is powered up first (or has always been powered up), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.

3.7. Turn-off

The following methods can be used to turn off the module normally:

- Use the PWRKEY pin.
- Execute **AT+QPOWD**. See ***document [2]*** for details.

3.7.1. Turn-off with PWRKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY. After this, the module executes power-down procedure. The turn-off timing is illustrated in the following figure.

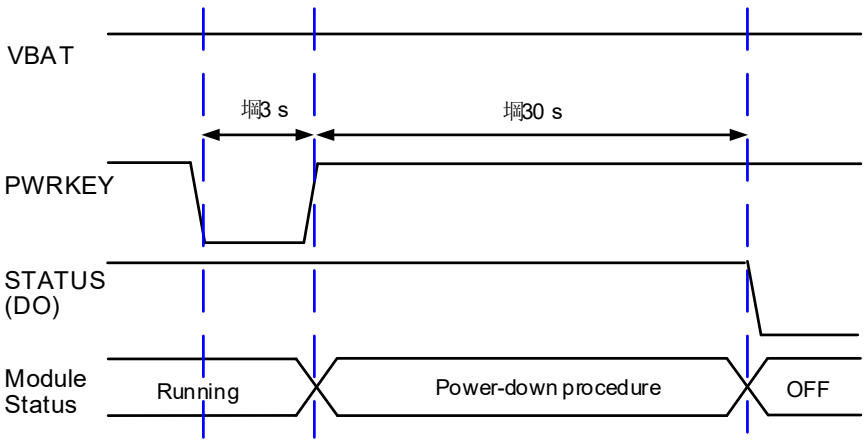


Figure 14: Turn-off Timing

3.7.2. Turn-off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.

3.8. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Resets the module	VBAT power domain. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

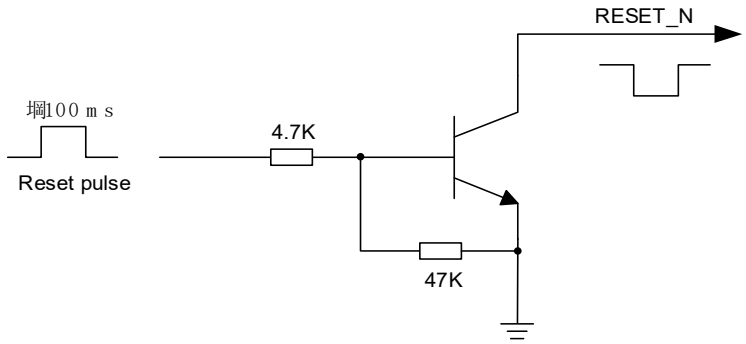


Figure 15: Reference Circuit of RESET_N by Using Driving Circuit

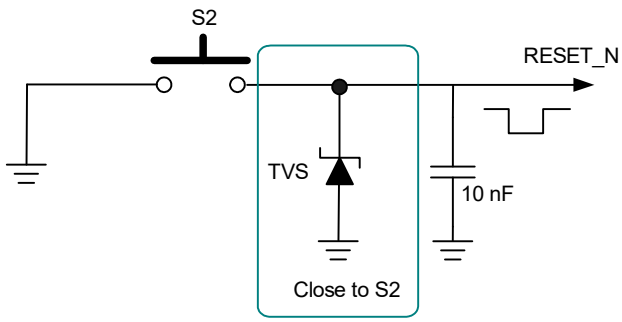


Figure 16: Reference Circuit of RESET_N by Using Button

The reset timing is illustrated in the following figure.

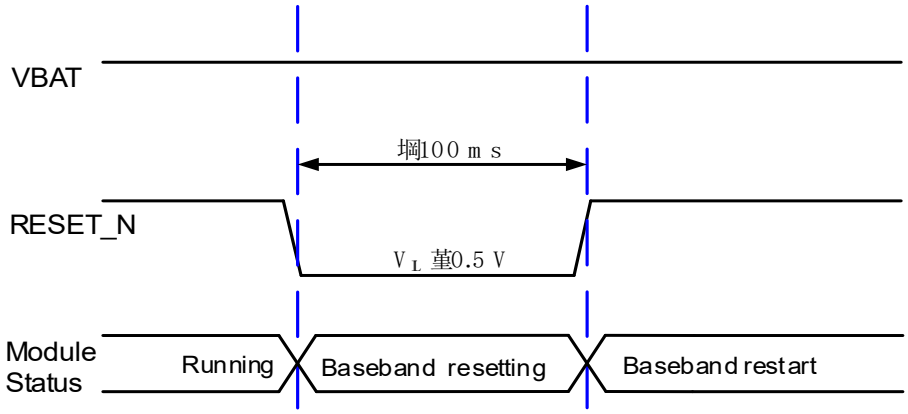


Figure 17: Timing of Resetting the Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when you fail to turn off the module with the **AT+QPOWD** or PWRKEY pin.
3. The RESET_N pin performs a soft reset which only resets the baseband, not the PMU.

4 Application Interfaces

4.1. Analog Audio Interfaces

The module provides one analog audio input channel and two analog audio output channels. The pin definition is shown in the following table.

Table 12: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_N	119	AI	Microphone analog input (-)	If unused, keep them open.
MICBIAS	120	PO	Bias voltage output for microphone	
SPK_P	121	AO	Analog audio differential output (+)	
SPK_N	122	AO	Analog audio differential output (-)	
MIC_P	126	AI	Microphone analog input (+)	
HP_L	123	AO	Headphone left channel output	
HP_R	124	AO	Headphone right channel output	
HP_DET	125	DI	Headphone hot-plug detect	

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of handset, earpiece and loudspeaker. (Since the module has no built-in PA, the analog audio output channels SPK_P and SPK_N can be directly applied for output of earpiece function, and if connected with external PA, they can be used as loudspeaker function.)

4.1.1. Audio Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing noise. Note that the resonant frequency point of a capacitor

largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitors on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitors should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.1.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

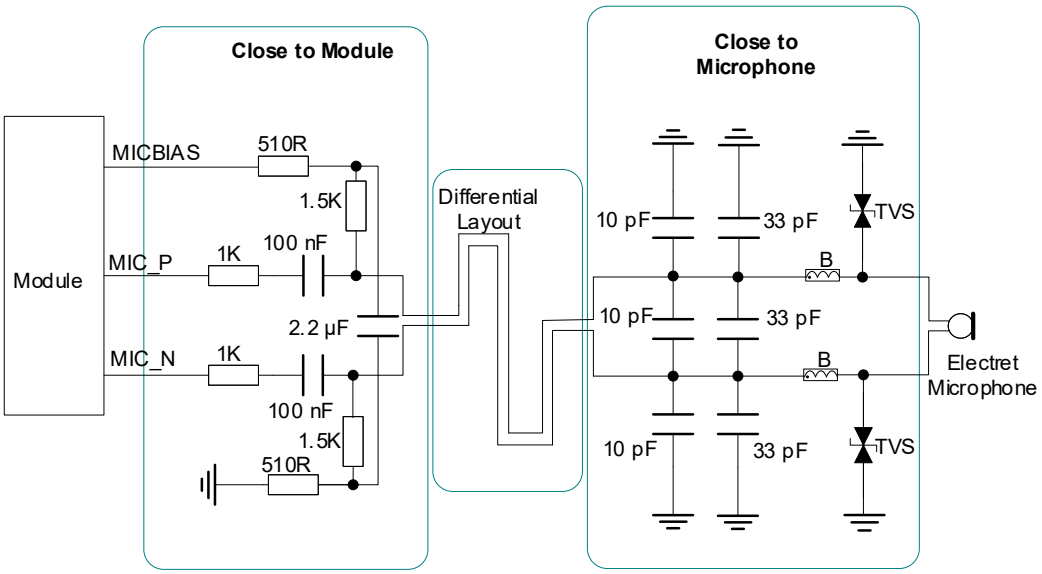


Figure 18: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

4.1.3. Headphone Interface Design

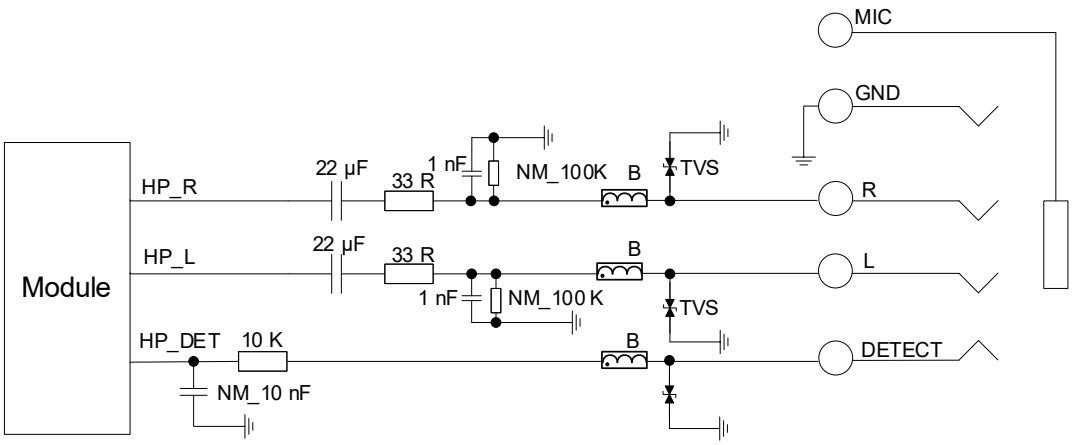


Figure 19: Reference Design for Headphone Interface

4.1.4. Earpiece Interface Design

The earpiece channel reference circuit is shown in the following figure:

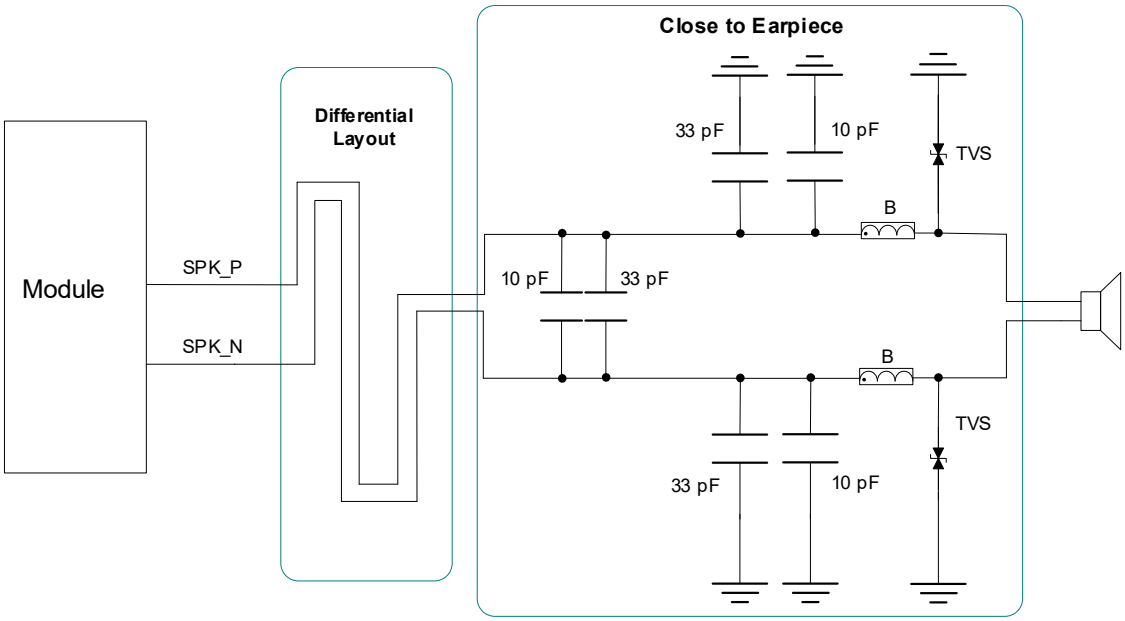


Figure 20: Reference Design for Earpiece Interface

4.2. USB Interface

The module provides an integrated Universal Serial Bus (USB) interface compliant with the USB 2.0 specification and supporting full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device.

Table 13: Functions of USB Interface

Function	
AT command communication	√
Data transmission	√
Software debugging	√
Firmware upgrade	√

Table 14: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Input voltage range: 3.5 V to 5.25 V. A test point must be reserved. The USB_VBUS pin needs to be connected with a 1 kΩ resistor in series if USB_VBUS is connected to power supply and VBAT is powered down.
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

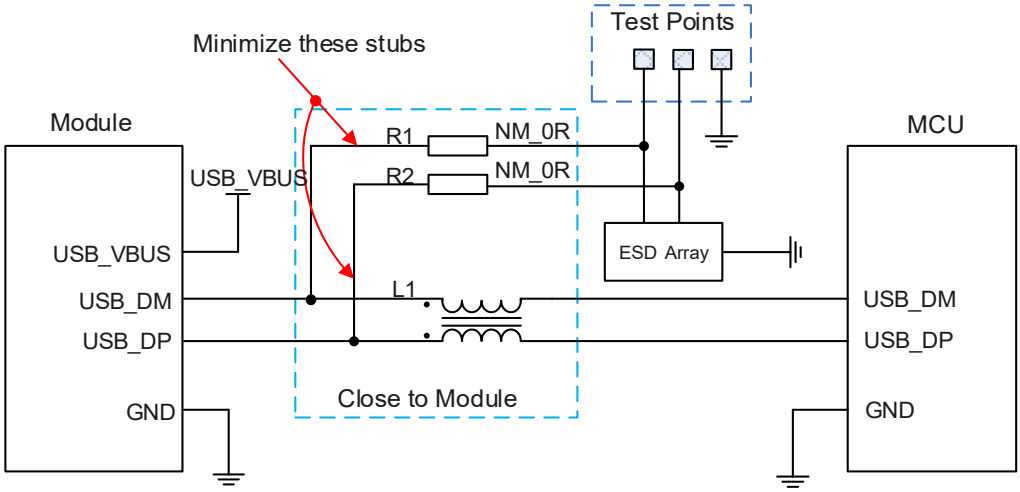


Figure 21: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R1, and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under or near crystals, oscillators, magnetic devices, and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Pay attention to the selection of the ESD component on the USB data line. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

4.3. USB_BOOT Interface

The module provides a USB_BOOT interface. Pull up USB_BOOT to VDD_EXT before powering on the module, and the module will enter the forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 15: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Forces the module to enter download mode	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

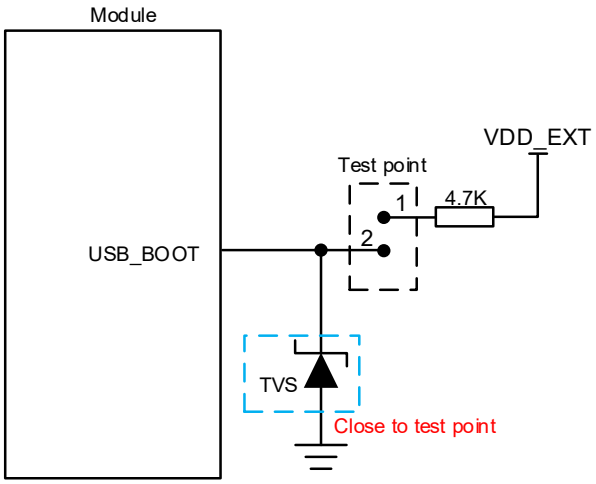


Figure 22: Reference Circuit of USB_BOOT Interface

4.4. (U)SIM Interfaces

The module provides two (U)SIM interfaces that support Dual SIM Single Standby by default [10]. The (U)SIM interface circuitry meets ETSI requirement and IMT-2000 specification. Either 1.8 V or 3.0 V (U)SIM card is supported.

[10] Please contact Quectel Technical Support if Dual SIM Dual Standby is required.

Table 16: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Specified ground for (U)SIM1 card	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. A test point must be reserved for debugging.

The module supports (U)SIM card hot-plug via the USIM_DET pin and both high- and low-level detections are supported. By default, the function is disabled, and see **AT+QSIMDET** in ***document [2]*** for more details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

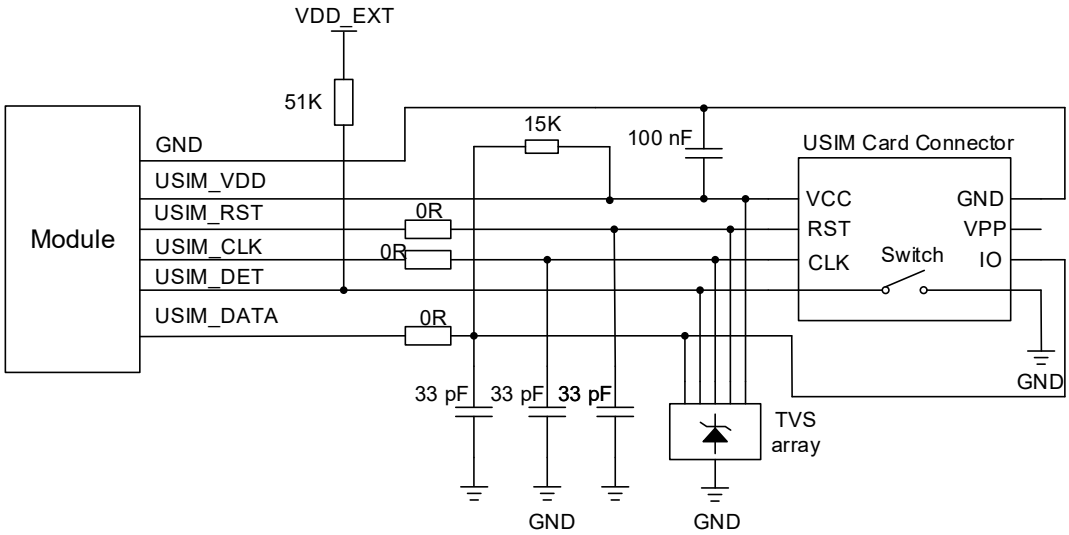


Figure 23: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

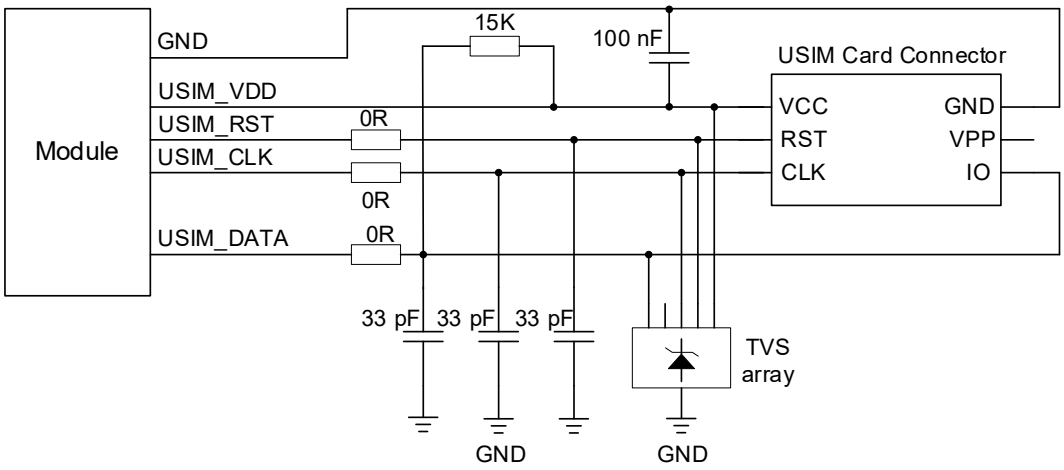


Figure 24: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM_VDD and GND does not exceed 1 μF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and

shield them with surrounded ground.

- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering out RF interference. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.5. I2C and PCM Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface. The PCM interface of the module only supports slave mode, therefore, the master clock signal of the codec IC needs to be provided externally.

PCM interface supports the short frame mode, in which PCM_CLK = the number of channels × PCM_SYNC × 16 bits, where the number of channels supports 1–4 channels, but the module will only take the data on the first channel; PCM_SYNC is equal to the audio sampling rate, which supports 8–44.1 kHz.

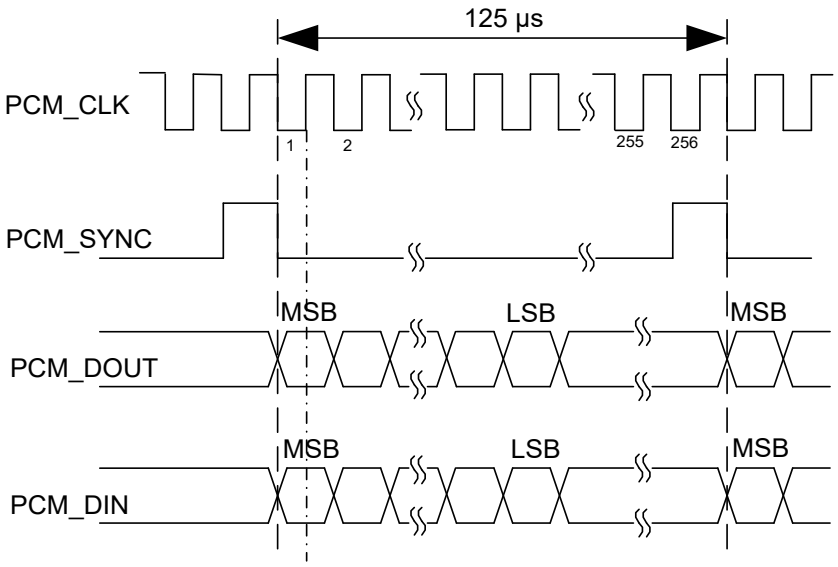


Figure 25: Timing of PCM Short Frame Mode

NOTE

The clocks of PCM_SYNC and PCM_CLK are provided by the codec IC, but the provided PCM_SYNC frequency must be equal to the sampling frequency of the audio file played by the module.

Table 17: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	External pull-up resistor is required. 1.8 V power domain only. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

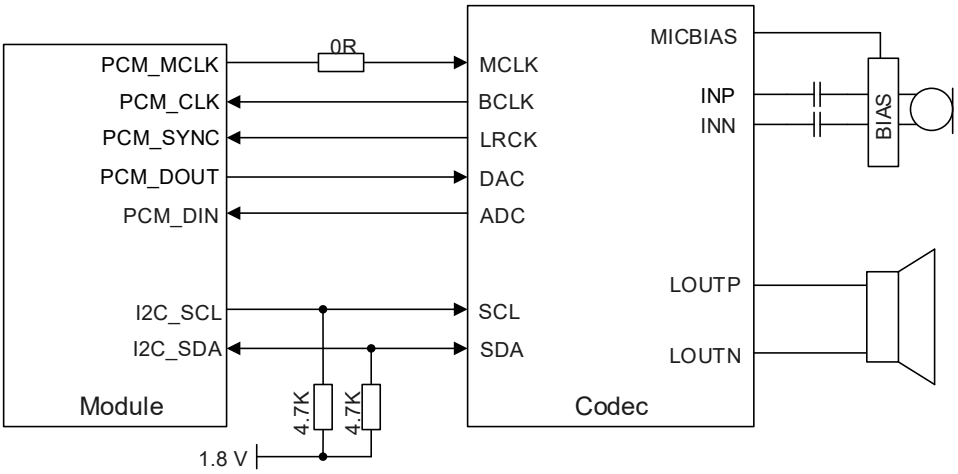


Figure 26: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve a termination resistor and a filter capacitor on the PCM traces, especially for PCM_CLK.
2. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.
3. For PCM external codec solution, it is recommended to use the clock signal provided by the module. If you need to use the PCM_MCLK function of the module, please consult Quectel Technical Support for details.

4.6. UART Interfaces

The module provides three UART interfaces: main UART, debug UART, and auxiliary UART. Their features are described as follows.

- Main UART interface supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, and 921600 bps, and the default setting is 115200 bps. It supports RTS and CTS hardware flow control. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 921600 bps baud rate. It is used for log output and cannot be used as a general-purpose UART.
- Auxiliary UART interface supports the same baud rates as the main UART interface.

Table 18: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Clear to send signal from the module (connect to MCU's CTS)	1.8 V power domain. If unused, keep them open.
MAIN_RTS	37	DI	Request to send signal to the module (connect to MCU's RTS)	
MAIN_RXD	34	DI	Main UART receive	
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	

Table 19: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. Test points must be reserved for debugging.
DBG_TXD	23	DO	Debug UART transmit	

Table 20: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	

The module provides 1.8 V UART interfaces. Use a voltage-level translator if the application is equipped with a 3.3 V UART interface.

A level-shifting chip TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

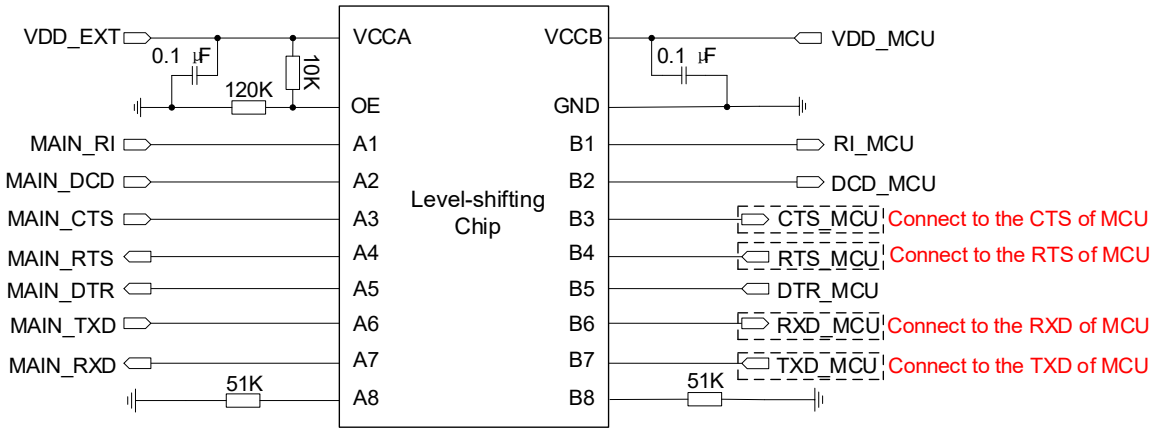


Figure 27: Reference Circuit with A Level-shifting Chip (Main UART)

Please visit http://www.ti.com for more information.

Another example with level-shifting circuit is shown as follows. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

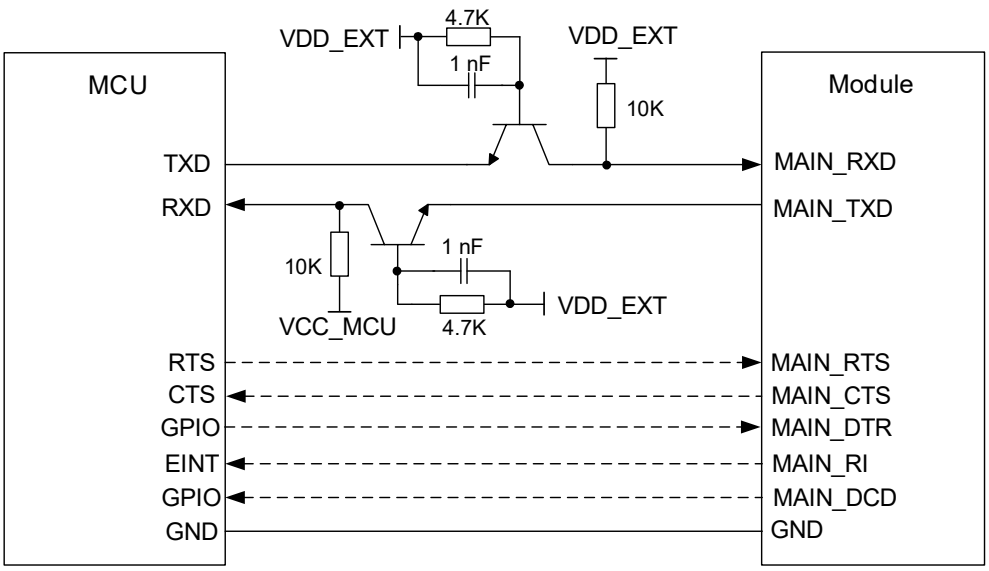


Figure 28: Reference Circuit with Transistor Circuit (Main UART)

NOTE

1. Transistor solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. The level-shifting circuits (***Figure* 27** and ***Figure 28***) take the main UART as an example. The circuits of the auxiliary UART are connected in the same way as the main UART.
4. When using pins 30, 38, and 39 (MAIN_DTR, MAIN_DCD and MAIN_RI), please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.
5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.7. ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces. You can use **AT+QADC=0** and **AT+QADC=1** to read the voltage values on ADC0 and ADC1 respectively. See ***document [2]*** for more details.

To improve the measurement accuracy of ADC, surround the traces of ADC with ground.

Table 21: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interfaces	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2	AI		

Table 22: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0	-	VBAT	V
ADC1 Input Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. Do not supply any voltage to ADC pins when VBAT is removed.
3. Considering the difference of ADC input voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistance in series.

4.8. SPI *

The module provides one SPI that only supports master mode. It has a working voltage of 1.8 V. If you need SPI, please contact Quectel Technical Support.

Table 23: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain. Supports master mode only. If unused, keep them open.
SPI_CS	25	DO	SPI chip select	

SPI_DIN	88	DI	SPI data input
SPI_DOUT	64	DO	SPI data output

4.9. Indication Signals

Table 24: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicates the module's network activity status	1.8 V power domain. If unused, keep them open.
STATUS	20	DO	Indicates the module's operation status	
MAIN_RI	39	DO	Main UART ring indication	

4.9.1. NET_STATUS

The network indication pin NET_STATUS can drive the network activity status indicator. The following table describes its pin definition and working states in different network status.

Table 25: Working States of Network Connection Status/Activity Indication

Pin Name	State	Network Status
NET_STATUS	Blink slowly (200 ms high/1800 ms low)	Network searching
	Blink quickly (234 ms high/266 ms low)	Registered on network and idle
	Blink rapidly (63 ms high/62 ms low)	Data transmission is ongoing
	Always high	Voice calling

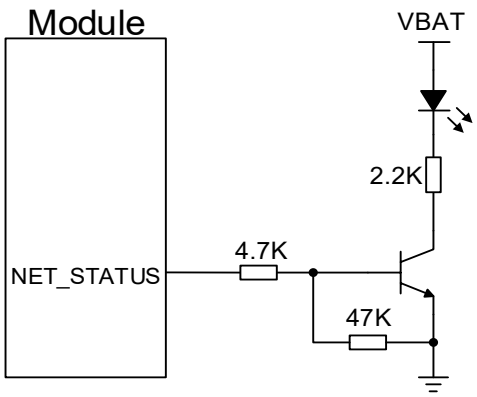


Figure 29: Reference Circuit of Network Status Indication

4.9.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It will output high level when module is turned on successfully.

A reference circuit is shown as below.

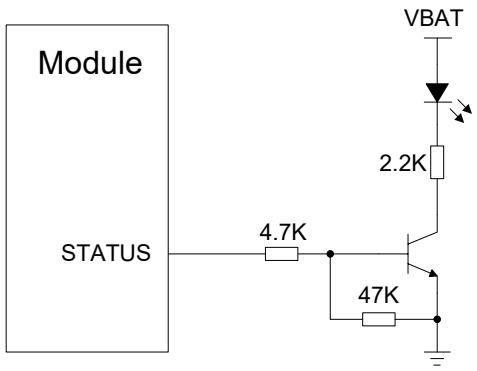


Figure 30: Reference Circuit of STATUS

4.9.3. MAIN_RI

You can configure MAIN_RI behaviors with **AT+QCFG="risignaltype","physical"**. No matter on which port (main UART, USB AT port and USB modem port) a URC is presented, the URC will trigger the behaviors of MAIN_RI.

MAIN_RI behavior can be configured flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 26: Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The MAIN_RI behaviors can be changed via **AT+QCFG="urc/ri/ring"**.

NOTE

1. The URC can be output via UART port, USB AT port, and USB modem port, which can be set by **AT+QURCCFG**. The default setting is USB AT port.
2. See ***document [2]*** for details on the above-mentioned AT commands.
3. When using pin 39 (MAIN_RI), please note that it will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before it can be configured as 1.8 V output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

4.10. W_DISABLE#

The module provides W_DISABLE# to enable or disable RF function. The W_DISABLE# pin is pulled up by default. Its control function for airplane mode, which is disabled by default, can be enabled through **AT+QCFG="airplanecontrol",1**. When such a control function is enabled, you can drive it to low level to make the module enter airplane mode. See ***document [2]*** for details on the AT command.

Table 27: Pin Definition of W_DISABLE#

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain. Pulled up by default. Driving it low can enable the module into the airplane mode. If unused, keep it open.

NOTE

When using pin 18 (W_DISABLE#), please note that it will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before it can be configured as 1.8 V input. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.

5 Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides a main antenna interface and a Bluetooth/Wi-Fi Scan antenna interface [11]. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna and Bluetooth/Wi-Fi Scan Antenna Interfaces

5.1.1. Pin Definition

Table 28: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_BT/ WIFI_SCAN [11]	56	AIO	The shared antenna interface for Bluetooth and Wi-Fi Scan	Wi-Fi Scan can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.

5.1.2. Operating Frequency

Table 29: Operating Frequency of EG915U-CN

Operating Frequency	Transmit (Unit: MHz)	Receive (Unit: MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880

[11] The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.

LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

B41 of EG915U-CN only supports 140 MHz (2535–2675 MHz).

Table 30: Operating Frequency of EG915U-EU

Operating Frequency	Transmit (Unit: MHz)	Receive (Unit: MHz)
GSM850	824–849	869–894
PCS1900	1850–1910	1930–1990
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821

LTE-FDD B28	703–748	758–803

Table 31: Operating Frequency of EG915U-LA

Operating Frequency	Transmit (Unit: MHz)	Receive (Unit: MHz)
GSM850	824–849	869–894
PCS1900	1850–1910	1930–1990
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180

5.1.3. Reference Design

A reference design of ANT_MAIN and ANT_BT/WIFI_SCAN is shown as below.

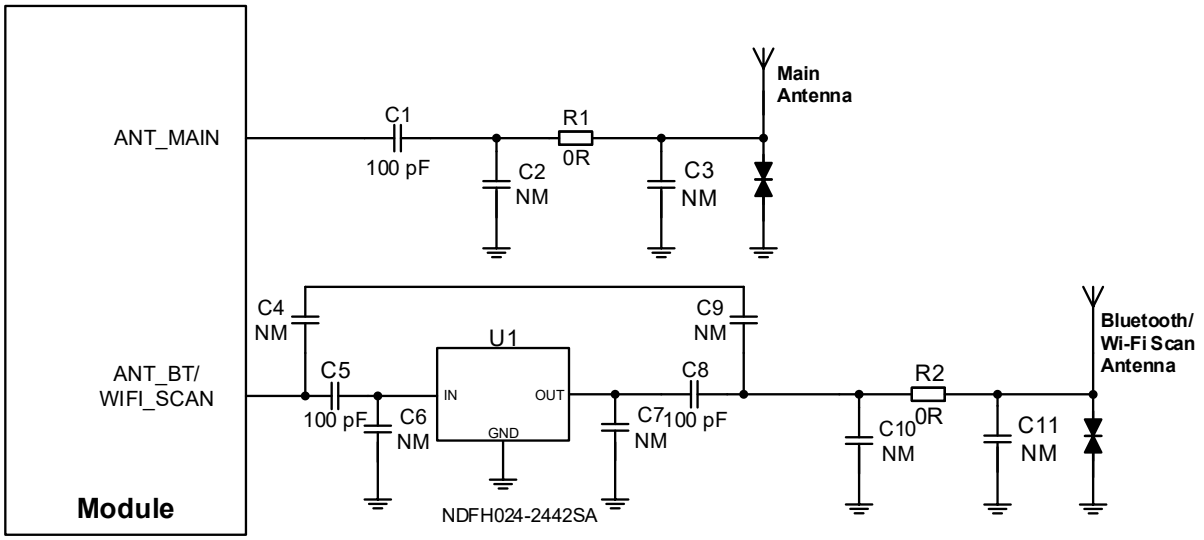


Figure 31: Reference Circuit of RF Antennas

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Place the DC-blocking capacitors (C1 and C8 (or C9)) and π-type matching components (C2, R1, C3 and C10, R2, C11) to antennas as close as possible.
3. The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.
4. If there is DC power at the antenna ports, C1 and C8 (or C9) must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C1 and C8 (or C9) should not be reserved.
5. For EG915U-EU/-LA, it is recommended to reserve a filter at Wi-Fi Scan/Bluetooth antenna port. When the isolation between main antenna and Wi-Fi Scan/Bluetooth antenna is greater than 20 dB, the compatible design (C4 and C9) can be used first. However, for EG915U-CN, there is no need to use the filter, so C5–C8 should be not mounted. And you can use the compatible design (C4 and C9).

5.1.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

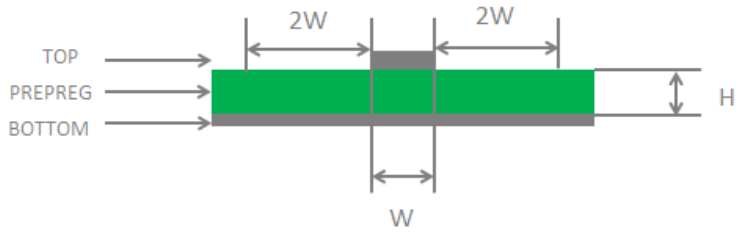


Figure 32: Microstrip Design on a 2-layer PCB

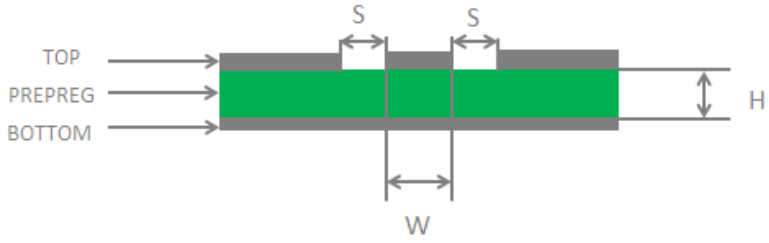


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

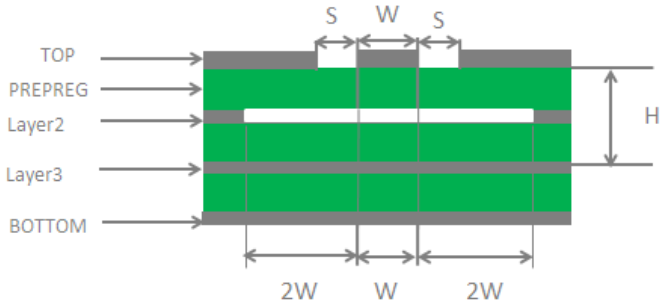


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

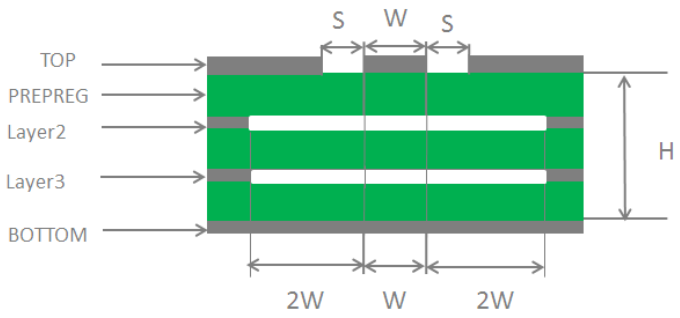


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

5.2. Antenna Installation

5.2.1. Antenna Design Requirement

Table 32: Requirements for Antenna Design

Type	Requirement
Cellular	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss:

	< **1 dB:** LB (< 1 GHz) < **1.5 dB:** MB (1–2.3 GHz) < **2 dB:** HB (> 2.3 GHz)

5.2.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

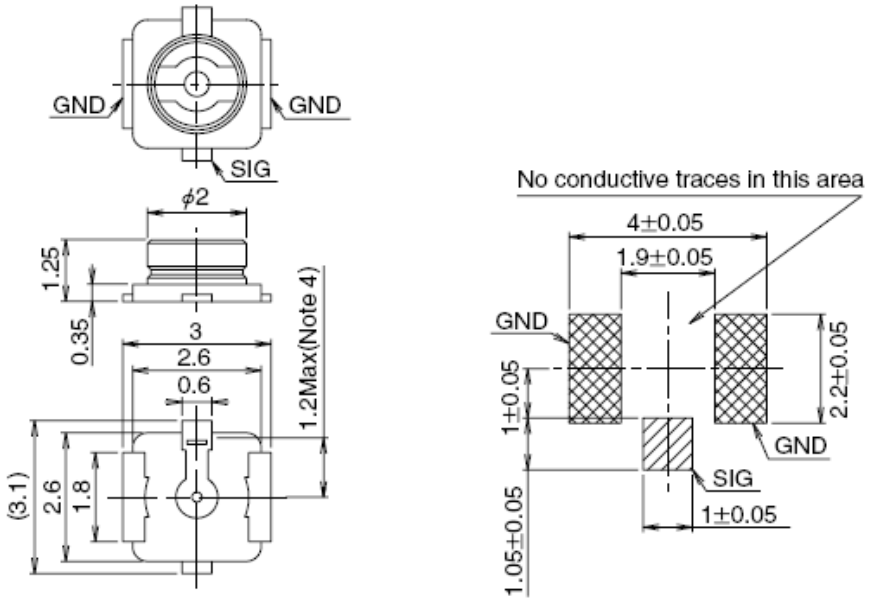


Figure 36: Dimensions of Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

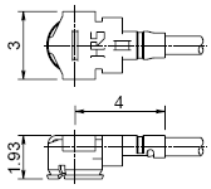
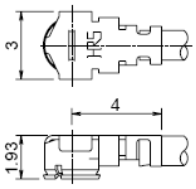
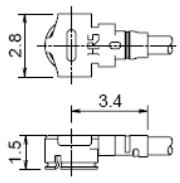
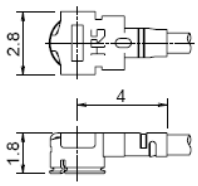
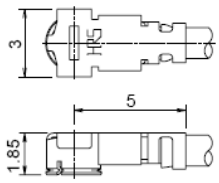
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

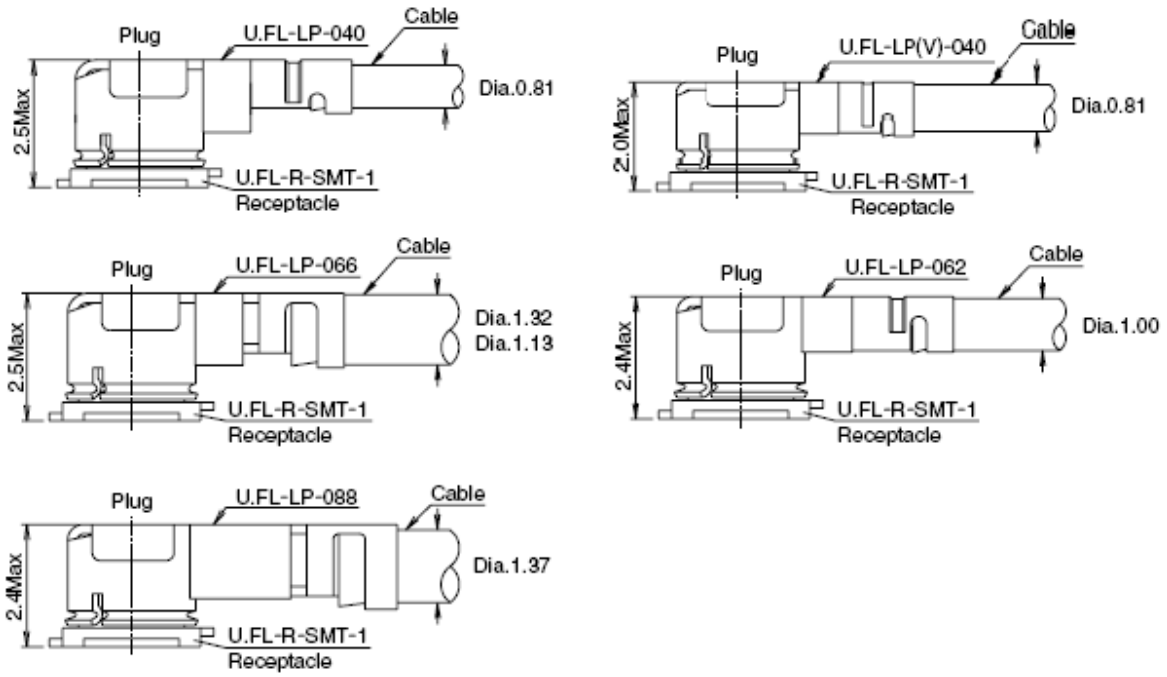


Figure 38: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 33: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	2.5	A
Voltage on Digital Pins	-0.3	2.1	V
Input Voltage at ADC0	0	VBAT	V
Input Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 34: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum	3.3	3.8	4.3	V

		and maximum values.				
	Voltage drop during transmitting burst	At maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current	At maximum power control level	-	1.7	2.5	A
USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

6.3. Power Consumption

Table 35: EG915U-CN Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	32	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.0	mA
	AT+CFUN=0 (USB connected)	2.2	mA
	AT+CFUN=4 (USB disconnected)	1.0	mA
	AT+CFUN=4 (USB connected)	2.3	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.0	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.5	mA
	EGSM900 @ DRX = 5 (USB connected)	2.7	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.3	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.0	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.5	mA
	DCS1800 @ DRX = 5 (USB connected)	2.7	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.3	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.8	mA
	LTE-FDD @ PF = 64 (USB connected)	3.0	mA

	LTE-FDD @ PF = 128 (USB disconnected)	1.4	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.2	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.8	mA
	LTE-TDD @ PF = 64 (USB connected)	3.1	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.4	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.2	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.6	mA
	EGSM900 @ DRX = 5 (USB connected)	28.6	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.0	mA
	LTE-FDD @ PF = 64 (USB connected)	29.0	mA
	LTE-TDD @ PF = 64 (USB disconnected)	13.0	mA
	LTE-TDD @ PF = 64 (USB connected)	29.0	mA
LTE data transmission	LTE-FDD B1 @ 22.94 dBm	587	mA
	LTE-FDD B3 @ 23.01 dBm	615	mA
	LTE-FDD B5 @ 23.54 dBm	527	mA
	LTE-FDD B8 @ 22.83 dBm	564	mA
	LTE-TDD B34 @ 23.14 dBm	280	mA
	LTE-TDD B38 @ 23.34 dBm	326	mA
	LTE-TDD B39 @ 23.25 dBm	247	mA
	LTE-TDD B40 @ 23.81 dBm	297	mA
	LTE-TDD B41 @ 23.06 dBm	311	mA
GPRS data transmission	EGSM900 4DL/1UL @ 32.87 dBm	234	mA
	EGSM900 3DL/2UL @ 30.86 dBm	348	mA
	EGSM900 2DL/3UL @ 28.90 dBm	401	mA
	EGSM900 1DL/4UL @ 26.74 dBm	415	mA

	DCS1800 4DL/1UL @ 30.13 dBm	160	mA
	DCS1800 3DL/2UL @ 28.12 dBm	221	mA
	DCS1800 2DL/3UL @ 26.01 dBm	249	mA
	DCS1800 1DL/4UL @ 23.94 dBm	258	mA
GSM voice call	EGSM900 PCL = 5 @ 32.89 dBm	256	mA
	EGSM900 PCL = 12 @ 19.41 dBm	101	mA
	EGSM900 PCL = 19 @ 6.33 dBm	72	mA
	DCS1800 PCL = 0 @ 29.99 dBm	178	mA
	DCS1800 PCL = 7 @ 16.09 dBm	84	mA
	DCS1800 PCL = 15 @ 1.26 dBm	67	mA
GSM voice call (Max. current)	EGSM900 PCL = 5 @ 32.83 dBm	1.78	A
	EGSM900 PCL = 12 @ 18.94 dBm	0.45	A
	EGSM900 PCL = 19 @ 6.18 dBm	0.19	A
	DCS1800 PCL = 0 @ 30.12 dBm	1.11	A
	DCS1800 PCL = 7 @ 15.97 dBm	0.30	A
	DCS1800 PCL = 15 @ 0.28 dBm	0.15	A

Table 36: EG915U-EU Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	32	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
	AT+CFUN=0 (USB connected)	2.3	mA
	AT+CFUN=4 (USB disconnected)	1.2	mA
	AT+CFUN=4 (USB connected)	2.4	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.1	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.8	mA

	EGSM900 @ DRX = 5 (USB connected)	2.8	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.5	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.1	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.8	mA
	DCS1800 @ DRX = 5 (USB connected)	2.7	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.5	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.7	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.1	mA
	LTE-FDD @ PF = 64 (USB connected)	3.3	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.6	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.5	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.5	mA
	EGSM900 @ DRX = 5 (USB connected)	28.1	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-FDD @ PF = 64 (USB connected)	28.1	mA
LTE data transmission	LTE-FDD B1 @ 22.82 dBm	737	mA
	LTE-FDD B3 @ 23.53 dBm	732	mA
	LTE-FDD B5 @ 22.73 dBm	663	mA
	LTE-FDD B7 @ 23dBm	819	mA
	LTE-FDD B8 @ 22.32 dBm	574	mA
	LTE-FDD B20 @ 22.75 dBm	634	mA
	LTE-FDD B28 @ 22.4 dBm	655	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.7 dBm	250	mA
	GSM850 3DL/2UL @ 31.22 dBm	386	mA
	GSM850 2DL/3UL @ 30.12 dBm	499	mA

	GSM850 1DL/4UL @ 28.92 dBm	582	mA
	EGSM900 4DL/1UL @ 32.68 dBm	259	mA
	EGSM900 3DL/2UL @ 31.01 dBm	390	mA
	EGSM900 2DL/3UL @ 29.93 dBm	501	mA
	EGSM900 1DL/4UL @ 28.12 dBm	574	mA
	DCS1800 4DL/1UL @ 29.68 dBm	151	mA
	DCS1800 3DL/2UL @ 28.18 dBm	226	mA
	DCS1800 2DL/3UL @ 26.22 dBm	263	mA
	DCS1800 1DL/4UL @ 24.4 dBm	299	mA
	PCS1900 4DL/1UL @ 29.84 dBm	166	mA
	PCS1900 3DL/2UL @ 28.47 dBm	254	mA
	PCS1900 2DL/3UL @ 27.25 dBm	321	mA
	PCS1900 1DL/4UL @ 26.08 dBm	383	mA
GSM voice call	GSM850 PCL = 5 @ 32.62 dBm	256	mA
	GSM850 PCL = 12 @ 18.71 dBm	91	mA
	GSM850 PCL = 19 @ 5.04 dBm	60	mA
	EGSM900 PCL = 5 @ 32.11 dBm	249	mA
	EGSM900 PCL = 12 @ 18.76 dBm	100	mA
	EGSM900 PCL = 19 @ 5.30 dBm	69	mA
	DCS1800 PCL = 0 @ 29.43 dBm	171	mA
	DCS1800 PCL = 7 @ 15.91 dBm	81	mA
	DCS1800 PCL = 15 @ 0.21 dBm	63	mA
	PCS1900 PCL = 0 @ 29.88 dBm	179	mA
	PCS1900 PCL = 7 @ 16.03 dBm	83	mA
	PCS1900 PCL = 15 @ 0.72 dBm	64	mA

GSM voice call (Max. current)	GSM850 PCL = 5 @ 32.82 dBm	1.88	A
	GSM850 PCL = 12 @ 19.08 dBm	0.46	A
	GSM850 PCL = 19 @ 6.12 dBm	0.19	A
	EGSM900 PCL = 5 @ 32.34 dBm	1.72	A
	EGSM900 PCL = 12 @ 19.06 dBm	0.44	A
	EGSM900 PCL = 19 @ 5.39 dBm	0.19	A
	DCS1800 PCL = 0 @ 29.89 dBm	1.13	A
	DCS1800 PCL = 7 @ 15.96 dBm	0.30	A
	DCS1800 PCL = 15 @ 0.95 dBm	0.16	A
	PCS1900 PCL = 0 @ 29.66 dBm	1.10	A
	PCS1900 PCL = 7 @ 15.59 dBm	0.33	A
	PCS1900 PCL = 15 @ 0.58 dBm	0.15	A

Table 37: EG915U-LA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	36.8	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.94	mA
	AT+CFUN=0 (USB connected)	2.39	mA
	AT+CFUN=4 (USB disconnected)	1.02	mA
	AT+CFUN=4 (USB connected)	2.45	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.90	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.85	mA
	EGSM900 @ DRX = 5 (USB connected)	2.86	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.55	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.95	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.44	mA

	DCS1800 @ DRX = 5 (USB connected)	2.85	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.25	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.75	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.95	mA
	LTE-FDD @ PF = 64 (USB connected)	3.24	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.55	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.35	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.80	mA
	EGSM900 @ DRX = 5 (USB connected)	30.2	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.15	mA
	LTE-FDD @ PF = 64 (USB connected)	30.6	mA
LTE data transmission	LTE-FDD B2 @ 22.82 dBm	666	mA
	LTE-FDD B3 @ 23.61 dBm	733	mA
	LTE-FDD B4 @ 23.06 dBm	714	mA
	LTE-FDD B5 @ 22.92 dBm	683	mA
	LTE-FDD B7 @ 23.20 dBm	820	mA
	LTE-FDD B8 @ 22.62 dBm	590	mA
	LTE-FDD B28 @ 22.86 dBm	660	mA
	LTE-FDD B66 @ 22.82 dBm	690	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.7 dBm	250	mA
	GSM850 3DL/2UL @ 31.22 dBm	386	mA
	GSM850 2DL/3UL @ 30.12 dBm	499	mA
	GSM850 1DL/4UL @ 28.92 dBm	582	mA
	EGSM900 4DL/1UL @ 32.68 dBm	259	mA
	EGSM900 3DL/2UL @ 31.01 dBm	390	mA
	EGSM900 2DL/3UL @ 29.93 dBm	501	mA

	EGSM900 1DL/4UL @ 28.12 dBm	574	mA
	DCS1800 4DL/1UL @ 29.68 dBm	151	mA
	DCS1800 3DL/2UL @ 28.18 dBm	226	mA
	DCS1800 2DL/3UL @ 26.22 dBm	263	mA
	DCS1800 1DL/4UL @ 24.4 dBm	299	mA
	PCS1900 4DL/1UL @ 29.84 dBm	166	mA
	PCS1900 3DL/2UL @ 28.47 dBm	254	mA
	PCS1900 2DL/3UL @ 27.25 dBm	321	mA
	PCS1900 1DL/4UL @ 26.08 dBm	383	mA
GSM voice call	GSM850 PCL = 5 @ 32.82 dBm	288	mA
	GSM850 PCL = 12 @ 19.08 dBm	113	mA
	GSM850 PCL = 19 @ 6.12 dBm	80	mA
	EGSM900 PCL = 5 @ 32.34 dBm	261	mA
	EGSM900 PCL = 12 @ 19.06 dBm	112	mA
	EGSM900 PCL = 19 @ 5.39 dBm	79	mA
	DCS1800 PCL = 0 @ 29.89 dBm	187	mA
	DCS1800 PCL = 7 @ 15.96 dBm	91	mA
	DCS1800 PCL = 15 @ 0.95 dBm	72	mA
	PCS1900 PCL = 0 @ 29.66 dBm	196	mA
	PCS1900 PCL = 7 @ 15.59 dBm	94	mA
	PCS1900 PCL = 15 @ 0.58 dBm	72	mA
GSM voice call (Max. current)	GSM850 PCL = 5 @ 32.08 dBm	1.92	A
	GSM850 PCL = 12 @ 19.08 dBm	0.47	A
	GSM850 PCL = 19 @ 5.09 dBm	0.19	A
	EGSM900 PCL = 5 @ 31.99 dBm	1.82	A
	EGSM900 PCL = 12 @ 18.98 dBm	0.47	A

	EGSM900 PCL = 19 @ 5.39 dBm	0.19	A
	DCS1800 PCL = 0 @ 29.34 dBm	1.07	A
	DCS1800 PCL = 7 @ 16.86 dBm	0.32	A
	DCS1800 PCL = 15 @ 1.84 dBm	0.15	A
	PCS1900 PCL = 0 @ 29.30 dBm	1.07	A
	PCS1900 PCL = 7 @ 16.36 dBm	0.32	A
	PCS1900 PCL = 15 @ 1.42 dBm	0.15	A

NOTE

The above power consumption data are tested under 50 Ω impedance.

6.4. Tx Power

Table 38: RF Tx Power

Frequency Band	Max. RF Tx Power	Min. RF Tx Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE bands	23 dBm ±2 dB	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 6.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.

6.5. Rx Sensitivity

Table 39: EG915U-CN Conducted RF Rx Sensitivity

Frequency	Rx Sensitivity (Typ.)	3GPP
	Primary	
EGSM900	-108.0 dBm	-102 dBm
DCS1800	-107.5 dBm	-102 dBm
LTE-FDD B1 (10 MHz)	-97.3 dBm	-93.3dbm
LTE-FDD B3 (10 MHz)	-98 dBm	-90.3
LTE-FDD B5 (10 MHz)	-99 dBm	-91.8
LTE-FDD B8 (10 MHz)	-99 dBm	-90.8
LTE-TDD B34 (10 MHz)	-98 dBm	-93.8
LTE-TDD B38 (10 MHz)	-97.6 dBm	-93.3
LTE-TDD B39 (10 MHz)	-98.4 dBm	-93.8
LTE-TDD B40 (10 MHz)	-98.3 dBm	-93.8
LTE-TDD B41 (10 MHz)	-97 dBm	-91.8

Table 40: EG915U-EU Conducted RF Rx Sensitivity

Frequency	Rx Sensitivity (Typ.)	3GPP
	Primary	
GSM850	-108 dBm	-102 dBm
EGSM900	-106.5 dBm	-102 dBm
DCS1800	-107.5 dBm	-102 dBm
PCS1900	-107 dBm	-102 dBm
LTE-FDD B1 (10 MHz)	-97	-93.3

LTE-FDD B3 (10 MHz)	-97.1	-90.3
LTE-FDD B5 (10 MHz)	-97.4	-91.8
LTE-FDD B7 (10 MHz)	-96.1	-91.3
LTE-FDD B8 (10 MHz)	-98.2	-90.8
LTE-FDD B20 (10 MHz)	-98.3	-90.8
LTE-FDD B28 (10 MHz)	-97.7	-92.3

Table 41: EG915U-LA Conducted RF Rx Sensitivity

Frequency	Rx Sensitivity (Typ.)	3GPP
	Primary	
GSM850	-108 dBm	-102 dBm
EGSM900	-106.8 dBm	-102 dBm
DCS1800	-107.5 dBm	-102 dBm
PCS1900	-107.2 dBm	-102 dBm
LTE-FDD B2 (10 MHz)	-96.7	-91.3
LTE-FDD B3 (10 MHz)	-97.1	-90.3
LTE-FDD B4 (10 MHz)	-96.9	-93.3
LTE-FDD B5 (10 MHz)	-97.8	-91.8
LTE-FDD B7 (10 MHz)	-96	-91.3
LTE-FDD B8 (10 MHz)	-98.2	-90.8
LTE-FDD B28 (10 MHz)	-97.7	-92.3
LTE-FDD B66 (10 MHz)	-96.9	-92.8

6.6. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 42: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.7. Operating and Storage Temperatures

Table 43: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [12]	-35	+25	+75	ºC
Extended Operating Range [13]	-40	+25	+85	ºC
Storage Temperature Range	-40	+25	+90	ºC

[12] Within this range, the module's indicators comply with 3GPP specification requirements.
[13] Within this range, the module retains the ability to establish and maintain functions such as voice (optional), SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

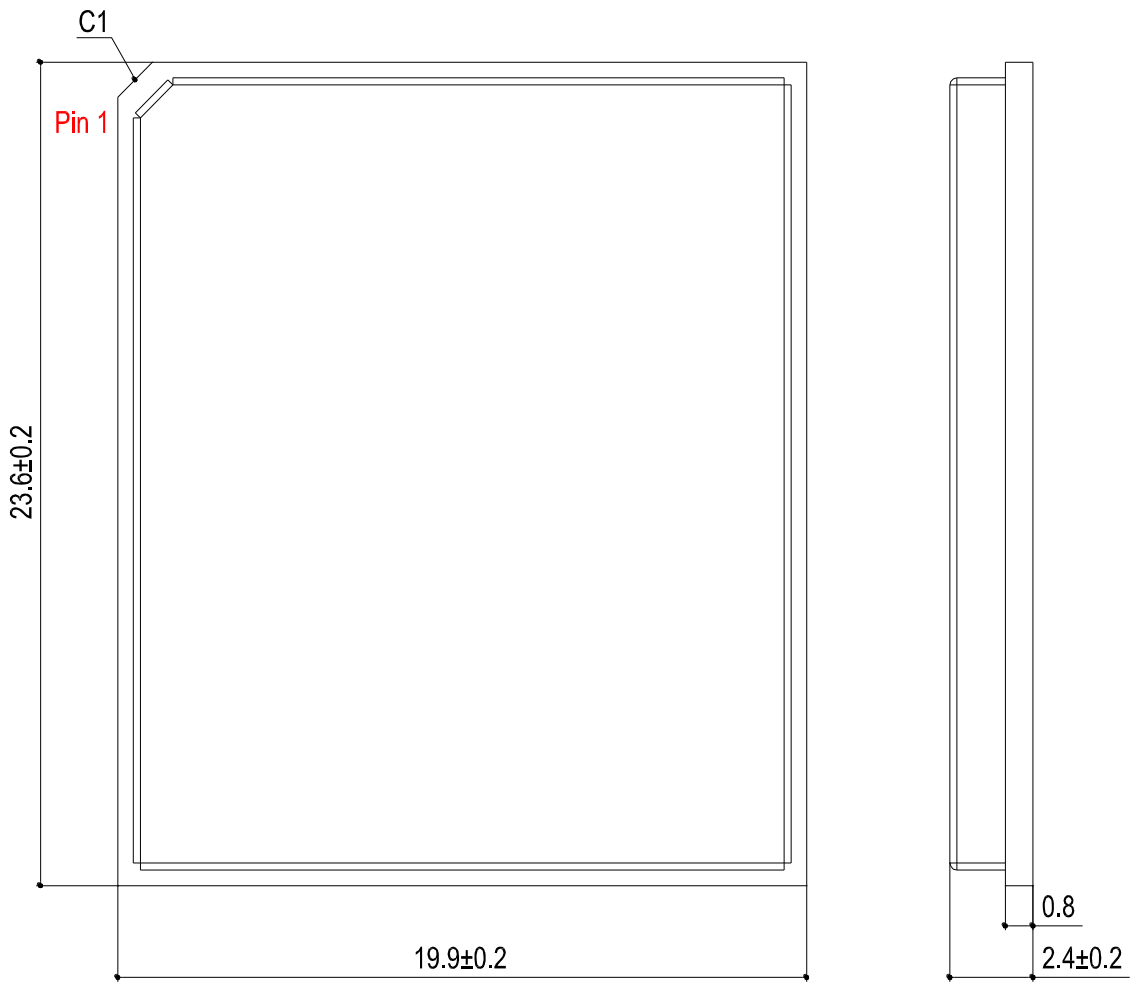


Figure 39: Module Top and Side Dimensions (Unit: mm)

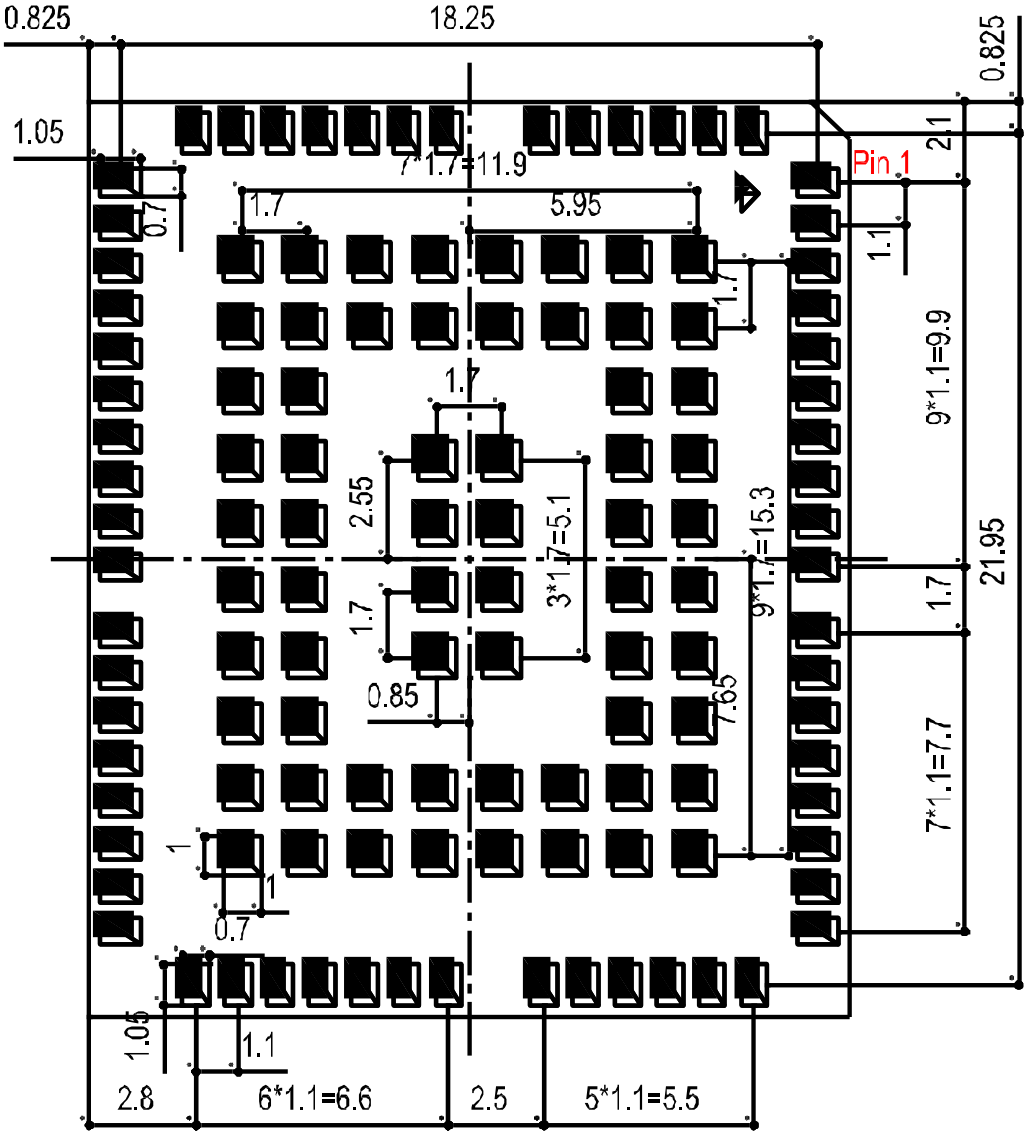


Figure 40: Module Bottom Dimensions

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

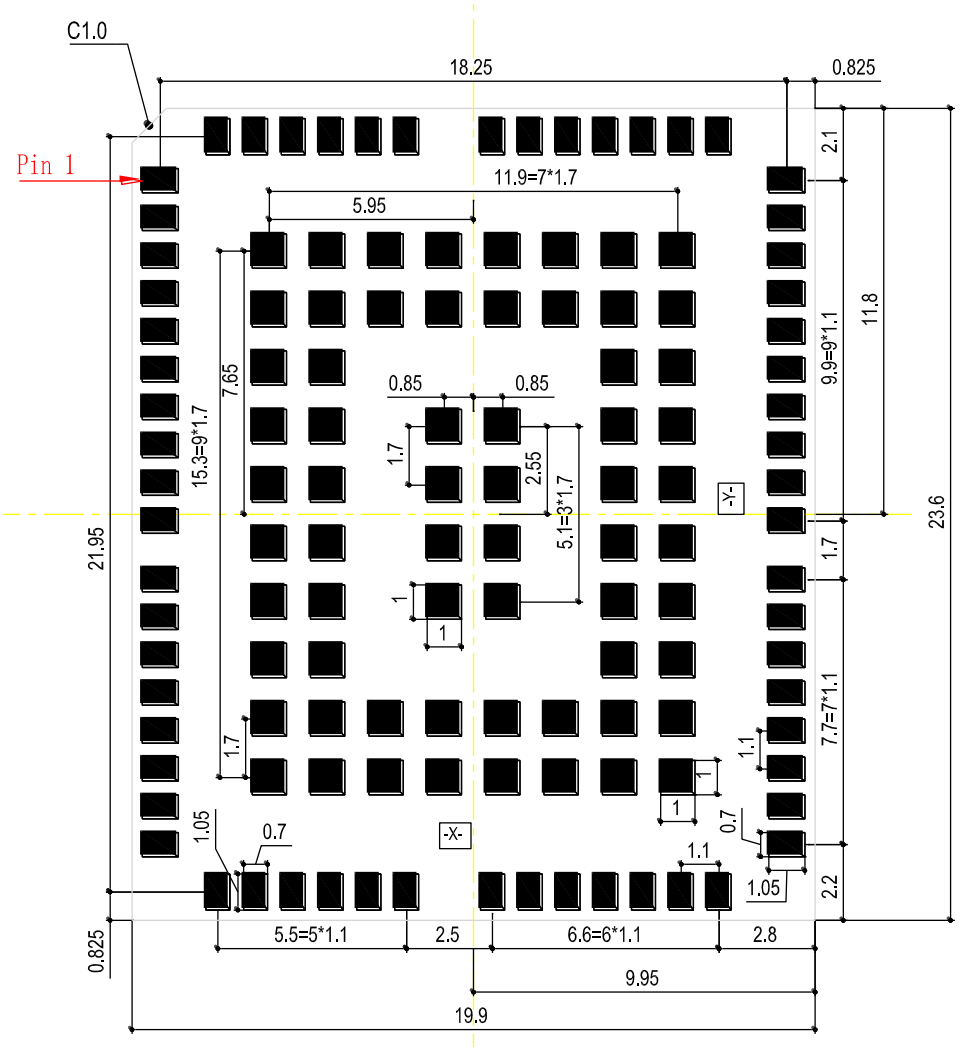


Figure 41: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

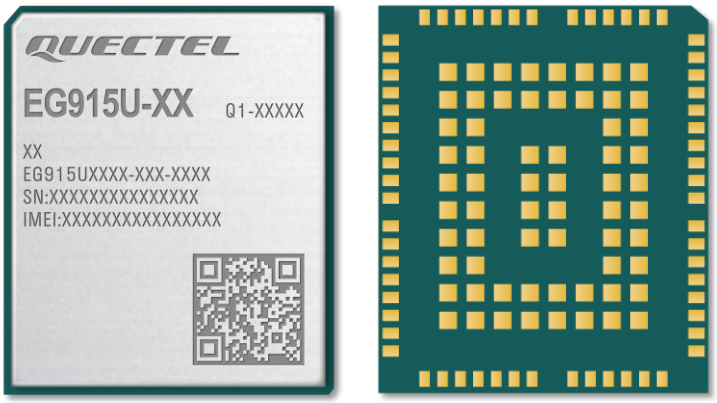


Figure 42: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing, and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [14] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[14] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [5]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

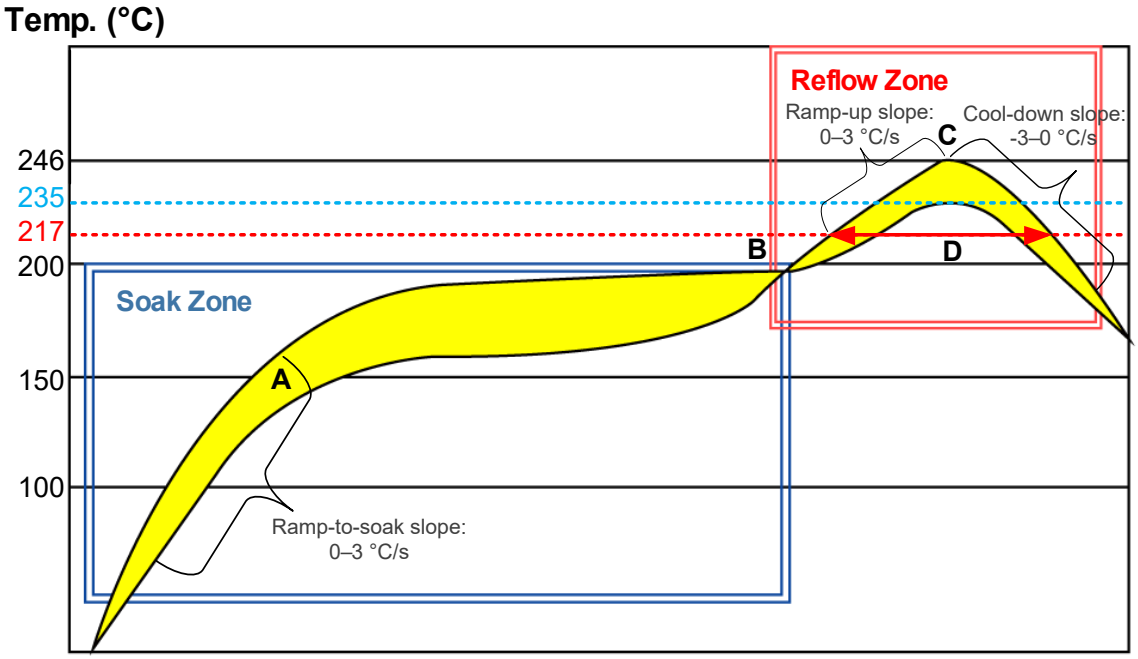


Figure 43: Recommended Reflow Soldering Thermal Profile

Table 44: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol and trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic

soldering) that is not mentioned in ***document [6]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

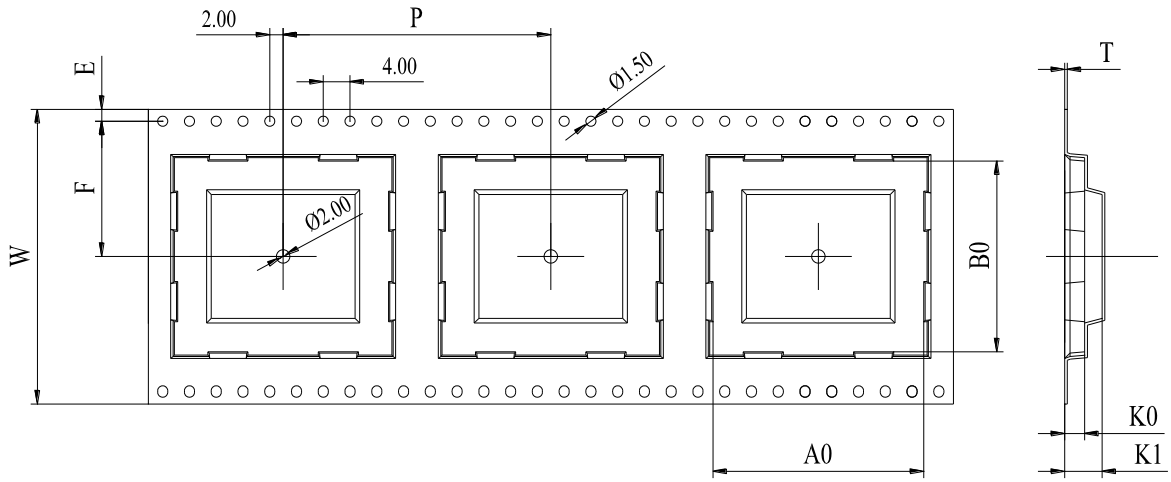


Figure 44: Carrier Tape Dimension Drawing (Unit: mm)

Table 45: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

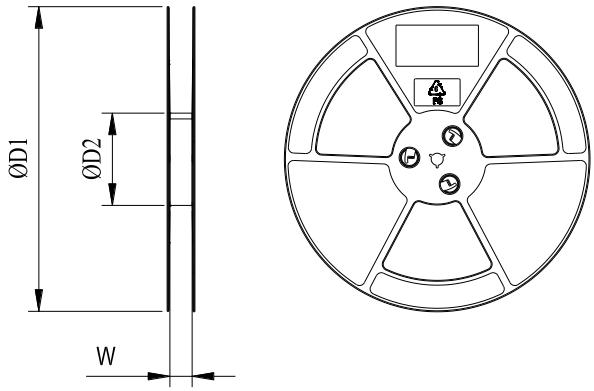


Figure 45: Plastic Reel Dimension Drawing

Table 46: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

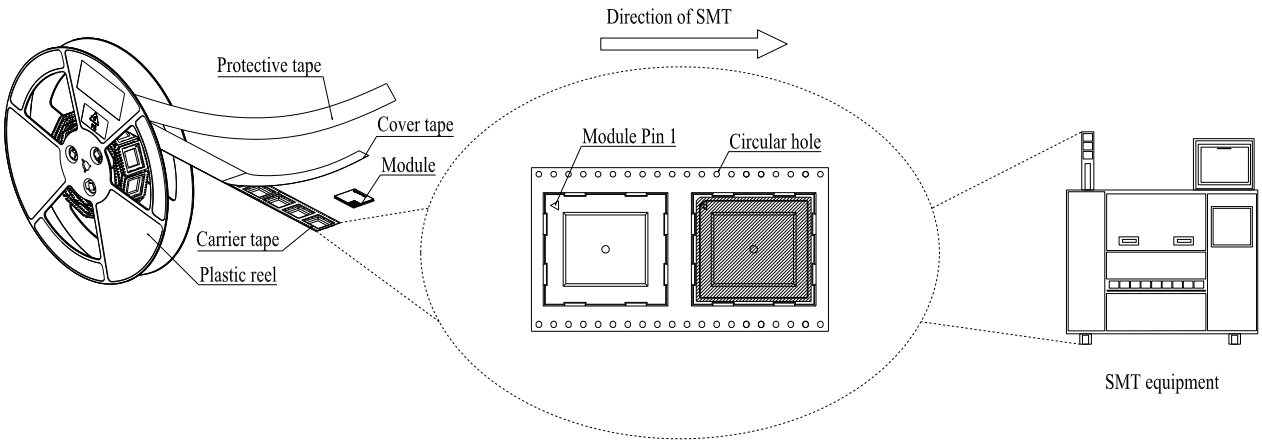
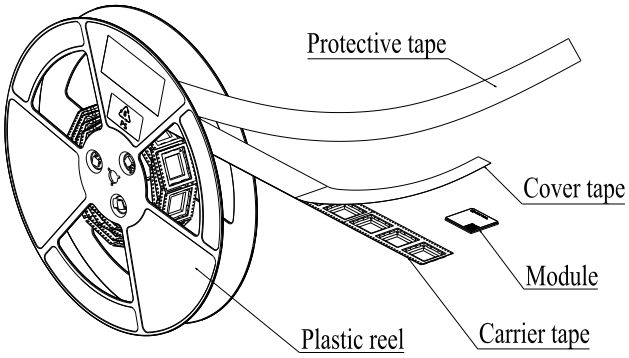


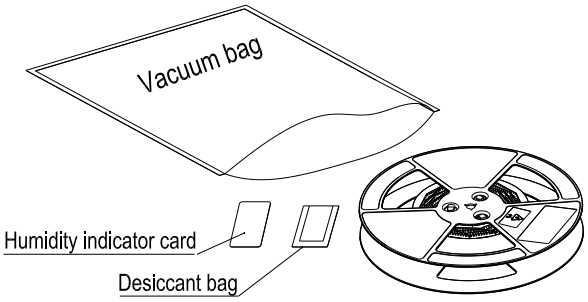
Figure 46: Mounting Direction

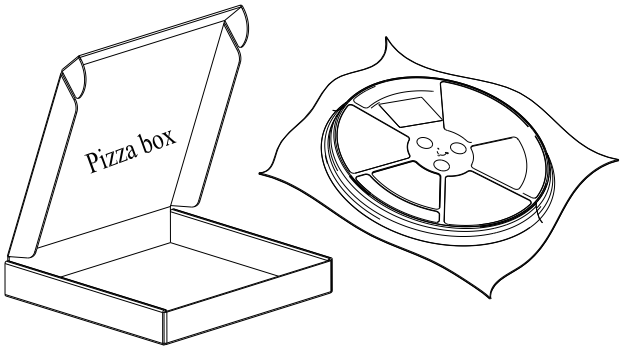
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

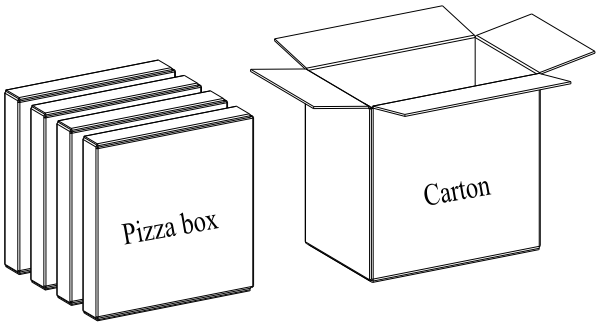


Figure 47: Packaging Process

9 Appendix References

Table 47: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200U&EG800G&EG91xU&EG915G_Series_AT_Commands_Manual
[3] Quectel_EC200U&EG800G&EG91xU&EG915G_Series_Low_Power_Mode_Application_Note
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Stencil_Design_Requirements
[6] Quectel_Module_SMT_Application_Note

Table 48: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception

DRX	Diversity Receive
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GRFC	General RF Control
HB	High Band
HR	Half Rate
I/O	Input/Output
LB	Low Band
LGA	Land Grid Array
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MT	Mobile Terminated
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Rx	Receive
SIMO	Single Input Multiple Output

SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

FCC ID: XMR202111EG915ULA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: XMR202111EG915ULA”
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for

re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Antenna Type	Max Gain (dBi)
Dipole	GSM850: 2.53; GSM1900: 1.59 LTE B2: 1.59; B4: 2.00; B5: 2.53; B7: 3.00; B66: 2.00; BT: 5.38

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 and Part 15C requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.