

EG912U Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-08-04	Anla HUANG/ Chris LIANG	Creation of the document
1.0	2023-01-16	Anla HUANG/ Chris LIANG/ Loft XU	First official release
1.1	2023-08-17	Anla HUANG/ Chris LIANG/ Loft XU	- Updated pin 51 from RESERVED to 1PPS. - Updated the USB serial driver information (Table 4). - Updated the functional diagram (Figure 1). - Added the description that the use of VDD_EXT requires a TVS; Changed the PSM_IND voltage domain from 3.3 V to 1.8 V (Table 6). - Updated the recommended value of the pull-down resistor required in the automatic turn-on scenario; Added a note on power-on scenarios; Added a note to specify that VBAT voltage should be lower than 0.5 V before power-on (Chapter 3.6.1). - Optimized the reference design for microphone interface (Figure 27). - Specified that the GNSS data update rate for positioning is 1 Hz (Chapter 5.2). - Added antenna isolation requirement (Table 37).
1.2	2024-10-09	Phoebe FU/ Chris LIANG/ Dony ZHAO	- Added the applicable module EG912U-EAL. - Added AGNSS feature description and AGNSS parameters (Tables 4 and 37). - Specified the description of dual (U)SIM functions (Table 4 and Chapter 4.3). - Added the notification on USB_VBUS design (Tables 6 & 12).

			- Added the recommended value for VBAT_BB trace width (Chapter 3.5.3). - Added the notification on VBAT design (Chapter 3.6). - Added the description on reset function (Chapter 3.8). - Added the notification on firmware upgrade function of USB interface (Chapter 4.2). - Added the notification on UART hardware flow control design (Chapter 4.4). - Deleted the truth table of GRFC interface (Chapter 5.1.2). - Updated the 3GPP requirement for LTE-FDD B66 receiver sensitivity (Table 33). - Updated the reference design of main antenna and Bluetooth antenna/Wi-Fi Scan antenna interfaces and added relevant note (Chapter 5.1.5). - Updated the reference design of GNSS antenna and added relevant note (Chapter 5.2.3). - Updated the requirements for antenna design (Table 38). - Added a note specifying that mercury-containing materials should be avoided for module processing; Added a note prohibiting storage or use of unprotected modules in environments containing corrosive gases (Chapter 8.2).
1.3	2025-01-21	Phoebe FU/ Chris LIANG	- Updated the maximum voltage value on digital pins (Table 39). - Updated the module coplanarity requirement (Chapter 7.1). - Updated the pre-baking time to 24 h (Chapter 8.1).

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1 Introduction

This document defines the EG912U series module and describes its air interfaces and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[...]	Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is an SMD module with compact packaging.

Table 2: Brief Introduction of Module

Category	EG912U-GL	EG912U-EAL
Package	LGA	LGA
Number of Pins	126	126
Dimensions	(29.0 ±0.2) mm × (25.0 ±0.2) mm × (2.4 ±0.2) mm	(29.0 ±0.2) mm × (25.0 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 3.67 g	Approx. 3.5 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Technology	EG912U-GL	EG912U-EAL
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B18/B19/B20/B25/B26/B28/B66	B1/B2/B3/B4/B5/B7/B8/B20/B28/B66
LTE-TDD	B34/B38/B39/B40/B41	B38/B40/B41
GSM	GSM850/EGSM900/DCS1800/PCS1900	GSM850/EGSM900/DCS1800/PCS1900
GNSS	Optional, GPS/GLONASS/BDS/Galileo/QZSS	-
Bluetooth ¹	Optional, Bluetooth 4.2 (BR/EDR + BLE)	-
Wi-Fi Scan ¹	Optional, 2.4 GHz 802.11b (Rx)	-

¹ The Wi-Fi Scan function utilizes the same antenna interface as the Bluetooth antenna. Due to this shared interface, the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported. For details, contact Quectel Technical Support.

2.2. Key Features

Table 4: Key Features

Feature	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● GSM850: Class 4 (33 dBm $\pm$2 dB) ● EGSM900: Class 4 (33 dBm $\pm$2 dB) ● DCS1800: Class 1 (30 dBm $\pm$2 dB) ● PCS1900: Class 1 (30 dBm $\pm$2 dB) ● LTE-FDD band: Class 3 (23 dBm $\pm$2 dB) ● LTE-TDD band: Class 3 (23 dBm $\pm$2 dB)
LTE Features	● Supports up to 3GPP Rel-13 Cat1 bis FDD/TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Modulations: – DL: QPSK, 16QAM and 64QAM – UL: QPSK and 16QAM ● Max. transmission data rates: - LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) - LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL)
GSM Features	GPRS: ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. transmission data rates: 85.6 kbps (DL)/85.6 kbps (UL)
GNSS (Optional)	● Constellations: GPS, GLONASS, BDS, Galileo and QZSS ● The module complies with NMEA 0183 protocol ● Data update rate: 1 Hz ● Supports AGNSS. For more details, see document [1]
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
USB Interface	● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7, and

	Android 4.x–13.x
USB_BOOT Interface	- Supports one USB_BOOT interface - Forces the module into download mode
(U)SIM Interfaces	- Supports (U)SIM card: 1.8/3.0 V - Supports Dual SIM Single Standby by default ²
UART	Main UART - Used for AT command communication and data transmission - Baud rates: up to 921600 bps; 115200 bps by default - Supports RTS and CTS hardware flow control Debug UART - Used for log output and Linux console - Baud rate: 921600 bps - Used as debug UART only, and cannot be used as a general-purpose UART Auxiliary UART - The baud rate is the same as that of the main UART
PCM Interface	- Supports one PCM interface (slave mode only) - Used for audio data transmission between the module and the external codec
I2C Interface	- Supports one I2C interface - Complies with the I2C-bus Specification
Audio Features	- Supports one analog audio input and one analog audio output - HR/FR/EFR/AMR/AMR-WB - Supports echo cancellation and noise suppression
ADC Interfaces	Supports two ADC Interfaces
SPI*	- Supports one SPI (master mode only) - Maximum clock frequency: 25 MHz 1.8 V voltage domain
Indication Signals	- STATUS indicates the module's operation status - NET_STATUS indicates the network activity status - MAIN_RI indicates URC reporting
AT Commands	- Compliant with 3GPP TS 27.007 and 3GPP TS 27.005 - Quectel enhanced AT commands
Antenna Interfaces	- Main antenna interface (ANT_MAIN) - Bluetooth antenna /Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) (optional) ³ - GNSS antenna interface (ANT_GNSS) (optional) ³ 50 Ω impedance

² Please contact Quectel Technical Support if Dual SIM Dual Standby is required.

³ EG912U-EAL does not support GNSS, Bluetooth and Wi-Fi Scan functions. For EG912U-GL, these functions are optional. The Wi-Fi Scan function utilizes the same antenna interface as the Bluetooth antenna. Due to this shared interface, the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported. For details, contact Quectel Technical Support.

Position Fixing	Supports Wi-Fi Scan (optional) and GNSS (optional)
Temperature Range	● Operating temperature range: -35 °C to +75 °C ⁴ ● Extended temperature range: -40 °C to +85 °C ⁵ ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Via USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS Directive

⁴ Within this range, the module's indicators comply with 3GPP specification requirements.

⁵ Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out} , may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Pin Assignment

The following figure illustrates the pin assignment of the module.

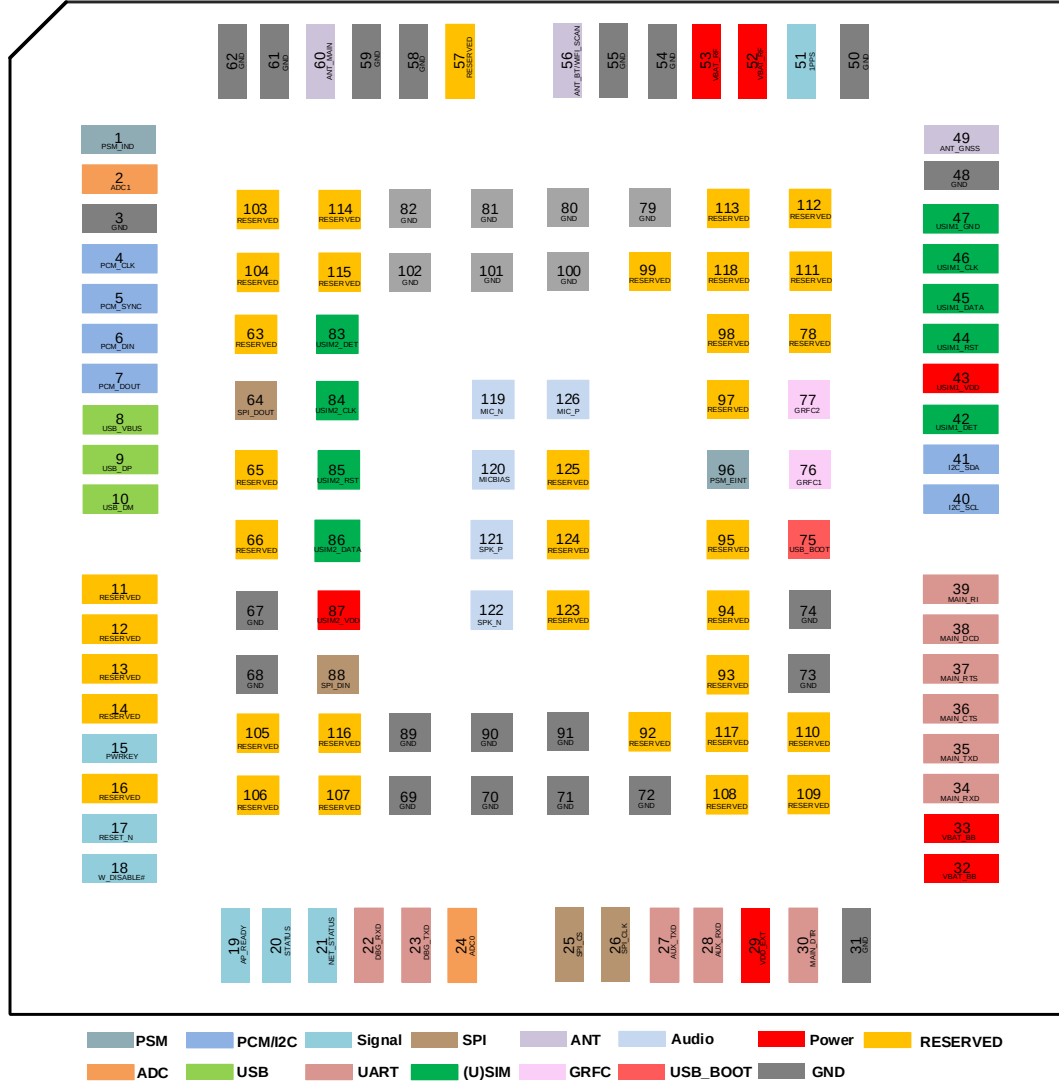


Figure 1: Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up to high level before the module starts up if forced download function is not required.
2. Keep all RESERVED pins and unused pins unconnected, and connect all GND pins to ground.
3. When using pins 18, 19, 30, 38, and 39 (W_DISABLE#, AP_READY, MAIN_DTR, MAIN_DCD, MAIN_RI), note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for

1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.4. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	32, 33	PI	Power supply for the module's BB part	V _{max} = 4.3 V V _{min} = 3.3 V V _{nom} = 3.8 V	External power supply must be provided with at least 1.0 A current.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		External power supply must be provided with at least

					2.5 A current.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V I _o max = 50 mA	Used with a 2.2 µF capacitor and TVS. It is recommended to reserve a test point.

Turn-on/off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on/off the module	V _{IL} max = 0.5 V VBAT power domain	Active low. It is recommended to reserve a test point.
RESET_N	17	DI	Reset the module		Active low. A test point is recommended to be reserved if unused.

Indication Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain	If unused, keep them open.
NET_STATUS	21	DO	Indicate the module's network activity status		

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	AI	USB connection detect	Input voltage range: 3.5 V to 5.25 V	A test point must be reserved. The USB_VBUS pin needs to be connected with a 1 kΩ resistor in series if USB_VBUS is connected to power supply and VBAT is powered down.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		Test points must be reserved.

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	I _o max = 50 mA	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data		
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain	If unused, keep it open.
USIM1_GND	47	-	Specified ground for (U)SIM1 card		
USIM2_VDD	87	PO	(U)SIM2 card power supply	I _o max = 50 mA	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data		
USIM2_CLK	84	DO	(U)SIM2 card clock		
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain	A test point must be reserved.

Main UART

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_CTS	36	DO	Clear to send signal from the module	1.8 V power domain	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive		If unused, keep them

MAIN_DCD	38	DO	Main UART data carrier detect	open.	
MAIN_TXD	35	DO	Main UART transmit		
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready		
Auxiliary UART					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain	If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive		
Debug UART					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit		
I2C Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	OD	I2C serial clock		External 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_SYNC	5	DI	PCM data frame sync	1.8 V power domain	If unused, keep them open. Support slave mode only.
PCM_CLK	4	DI	PCM clock		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		
Antenna Interfaces					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment

ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_BT/ WIFI_SCAN ⁶	56	AIO/ AI	Bluetooth antenna/Wi-Fi Scan antenna interface	When Wi-Fi Scan is used, only receiving is supported. 50 Ω impedance. If unused, keep it open.
ANT_GNSS ⁶	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Antenna Tuner Control Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC1	76	DO	Generic RF controller	1.8 V power domain	If unused, keep them open.
GRFC2	77	DO			

SPI*

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain	If unused, keep them open. Support master mode only.
SPI_CS	25	DO	SPI chip select		
SPI_DIN	88	DI	SPI data input		
SPI_DOUT	64	DO	SPI data output		

ADC Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	24	AI	General-purpose ADC interfaces	Input voltage range: 0 V to VBAT	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2	AI			

Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC_N	119	AI	Microphone analog		If unused, keep them

⁶ EG912U-EAL does not support GNSS, Bluetooth and Wi-Fi Scan functions and pins 49 and 56 should be kept reserved. For EG912U-GL, these functions are optional. The Wi-Fi Scan function utilizes the same antenna interface as the Bluetooth antenna. Due to this shared interface, the two functions cannot be used simultaneously. For details, contact Quectel Technical Support.

			input (-)	open.
MICBIAS	120	PO	Bias voltage output for microphone	Vmax = 3.0 V Vmin = 2.2 V Vnom = 2.2 V
SPK_P	121	AO	Analog audio differential output (+)	
SPK_N	122	AO	Analog audio differential output (-)	
MIC_P	126	AI	Microphone analog input (+)	

USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	75	DI	Force the module into download mode	1.8 V power domain	Active high. A circuit that can set the module into forced download mode should be reserved during design. It is recommended to reserve a test point.

Other Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain	Pulled up by default. Driving it low can enable the module into airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor ready		If unused, keep it open.
PSM_IND*	1	DO	Indicate the module's power saving mode		If unused, keep it open.
PSM_EINT	96	DI	Wake up the module from PSM		Pull it up externally to exit power saving mode. If unused, keep it open.

1PPS	51	DO	Pulse signal output	If unused, keep it open.
GND				
Pin Name	Pin No.			
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102			
RESERVED pins				
Pin Name	Pin No.			
RESERVED	11–14, 16, 57, 63, 65, 66, 78, 92–95, 97–99, 103–118, 123–125			

NOTE

When using pins 18, 19, 30, 38, and 39 (W_DISABLE#, AP_READY, MAIN_DTR, MAIN_DCD, MAIN_RI), note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.5. EVB Kit

Quectel supplies an evaluation board (UMTS<E EVB) with accessories to develop and test the module. For more details, see [document \[2\]](#).

3 Operating Characteristics

3.1. Operating Modes

The following table briefly outlines the operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details
Full Functionality Mode	Idle Software is active. The module remains registered on the network and is ready to send and receive data.
	Voice/Data Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	● AT+CFUN=0 can set the module to a minimum functionality mode without removing the power supply. ● In this case, both RF function and (U)SIM card are invalid.
Airplane Mode	● AT+CFUN=4 or pulling down W_DISABLE# pin can set the module to airplane mode. ● In this mode, RF function is invalid.
Sleep Mode	In this mode, power consumption of the module is reduced to an ultra-low level. The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from network normally.
PSM	In this mode, power consumption of the module is reduced to a minimized level, and AT command cannot be sent.
Power Down Mode	PMU shuts down the power supply. Software is not active. However, operating voltage connected to VBAT_BB/VBAT_RF pins remains applied.

NOTE

For more details about the AT command, see *document [3]*.

3.2. Sleep Mode

The module can reduce its power consumption to an ultra-low level in the sleep mode. The following chapters describe the procedures of entering sleep mode.

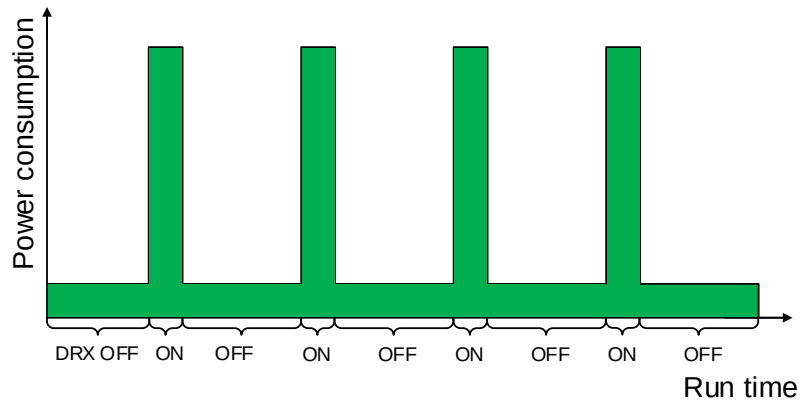


Figure 2: Power Consumption During Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the MCU communicates with module via UART interface, the following preconditions should be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode. For more details about the AT command, see *document [4]*.
- Drive MAIN_DTR to high level or keep it open.

The following figure shows the connection between the module and the MCU.

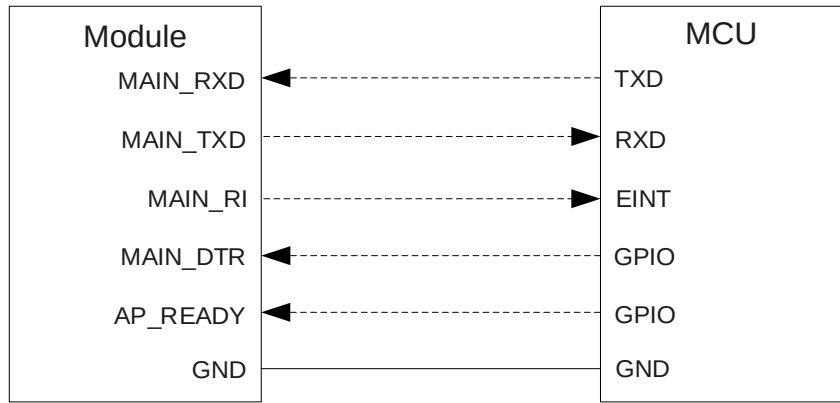


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR low will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See **Chapter 4.9.3** for details about MAIN_RI behaviors.

NOTE

When using pins 19, 30 and 39 (AP_READY, MAIN_DTR, and MAIN_RI), note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.2.2. USB Application Scenario

For the scenarios mentioned in **Chapters 3.2.2.1** and **3.2.2.2**, three preconditions must be met to make the module enter the sleep mode:

- Execute **AT+QSCCLK=1** to enable the sleep mode.
- Drive MAIN_DTR to high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters Suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function

The following figure illustrates the connection between the module and the host.

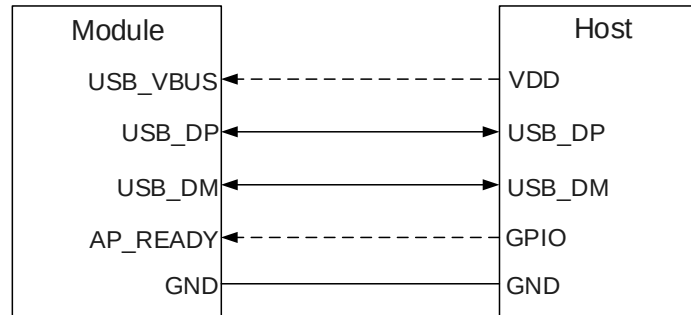


Figure 4: Sleep Mode Application with USB Remote Wakeup

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the module will send remote wake-up signals to USB bus to wake up the host.

NOTE

USB Suspend is supported on Linux system but not on Windows system.

3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend/Resume, but does not support remote wake-up function, the MAIN_RI signal is needed to wake up the host.

The following figure illustrates the connection between the module and the host.

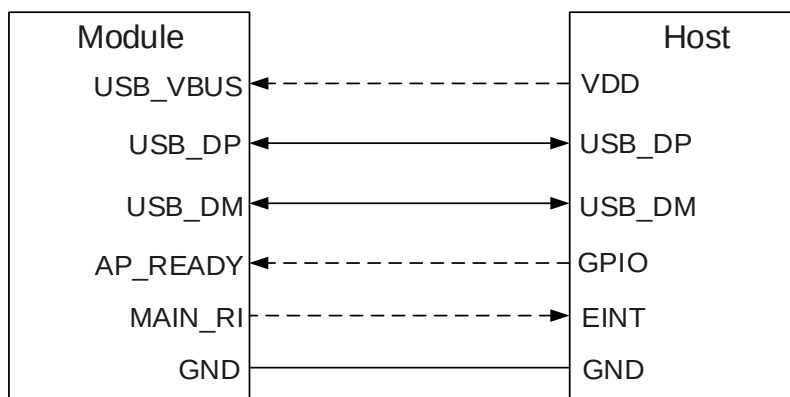


Figure 5: Sleep Mode Application with MAIN_RI

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the URC will trigger the behaviors of MAIN_RI pin. See **Chapter 4.9.3** for details about MAIN_RI behaviors.

NOTE

USB Suspend is supported on Linux system but not on Windows system.

3.2.2.3. USB Application Without USB Suspend Function

If the host does not support USB Suspend function, disconnect USB_VBUS with an external control circuit to make the module enter sleep mode.

- Execute **AT+QSClk=1** to enable sleep mode.
- Drive MAIN_DTR to high level or keep it open.
- Disconnect the USB_VBUS power supply.

The following figure illustrates the connection between the module and the host.

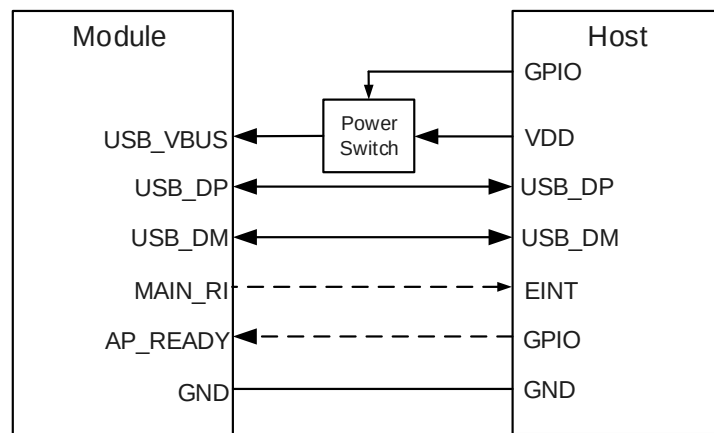


Figure 6: Sleep Mode Application Without Suspend Function

You can wake up the module by turning on the power switch to supply power to USB_VBUS.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the MCU/host.
2. When using pins 19, 30 and 39 (AP_READY, MAIN_DTR, and MAIN_RI), note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V

input or output. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

Driving W_DISABLE# pin low can make the module enter airplane mode. See **Chapter 4.10** for details.

Software:

AT+CFUN=<fun> provides the choice of functionality level through setting <fun> to 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both RF and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

When using pin 18 (W_DISABLE#), note that it will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before it can be configured as 1.8 V input. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.4. PSM

The module supports power saving mode (PSM). It enters the PSM through executing the following AT commands sequentially when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling up the PSM_EINT pin externally or setting the timer by software will enable the module to exit PSM.

Table 8: Pin Definition of PSM_IND and PSM_EINT

Pin Name	Pin No.	I/O	Description	Comment
PSM_IND*	1	DO	Indicate the module's power saving mode	If unused, keep it open.
PSM_EINT	96	DI	Wake up the module from PSM	Pull it up externally to exit power saving mode. If unused, keep it open.

3.5. Power Supply

3.5.1. Power Supply Pins

The module provides four VBAT pins for connection with an external power supply.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 9: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	PI	Power supply for the module's BB part	3.3	3.8	4.3	V
VBAT_RF	52, 53		Power supply for the module's RF part				
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.5.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 3.0 A when the GSM or both GSM and LTE are available and provide sufficient current of at least 2.0 A when only LTE is available. If the voltage drop between input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for 5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

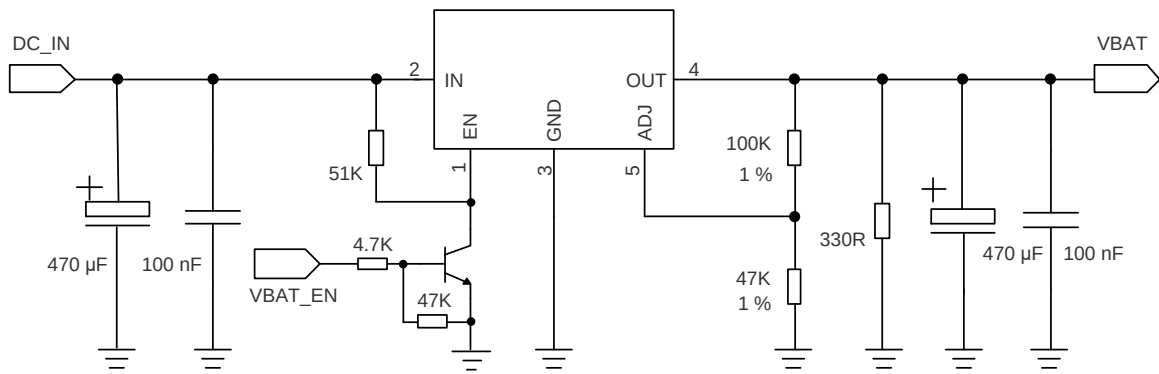


Figure 7: Reference Design of Power Supply

3.5.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure the input voltage never drops below 3.3 V.

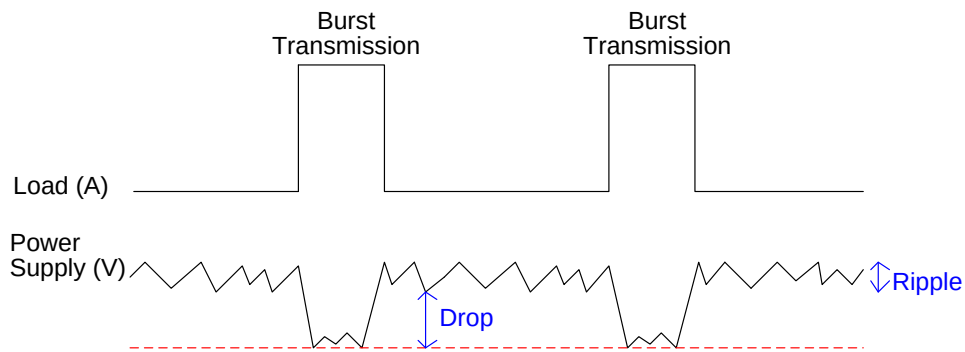


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage drop, a filter capacitor of about 100 µF with low ESR ($ESR \leq 0.7 \Omega$) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application should be a single voltage source and must be expanded to two sub paths with the star configuration. The width of VBAT_BB trace should be at least 1 mm; and the width of VBAT_RF trace should be at least 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The reference circuit is shown as below.

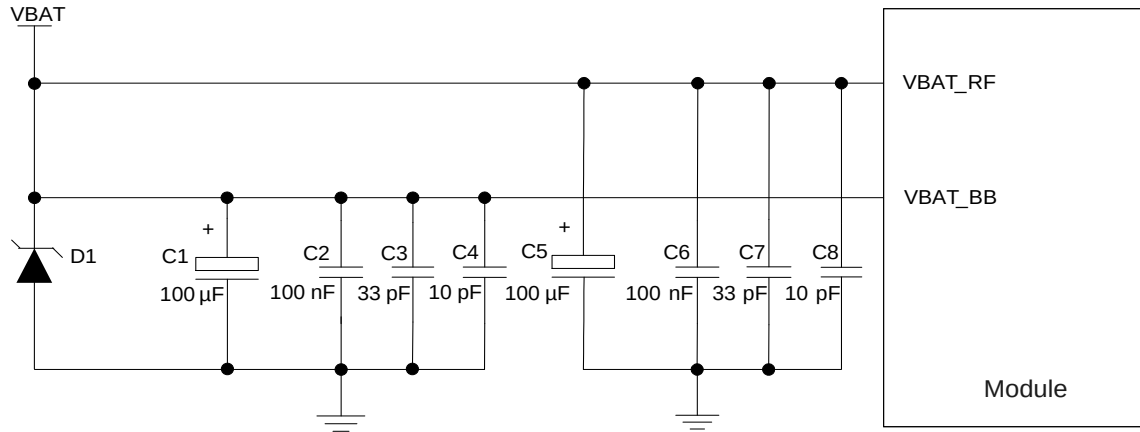


Figure 9: Reference Design of Power Supply

3.6. Turn-on

3.6.1. Turn-on with PWRKEY

Table 10: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain. Active low. It is recommended to reserve a test point.

When the module is in power down mode, driving the PWRKEY pin low for at least 2 s can turn on the module. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

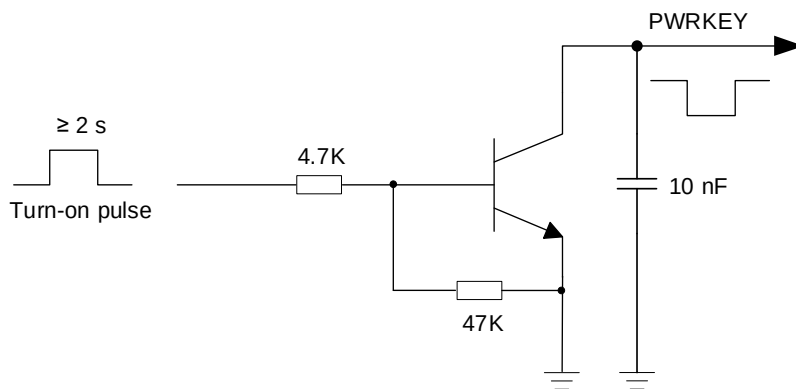


Figure 10: Reference Circuit for Driving PWRKEY

Another way to control the PWRKEY is using a button directly. When you are pressing the button, electrostatic strike may be generated from finger. Therefore, you must place a TVS nearby the button for ESD protection. A reference circuit is shown in the following figure.

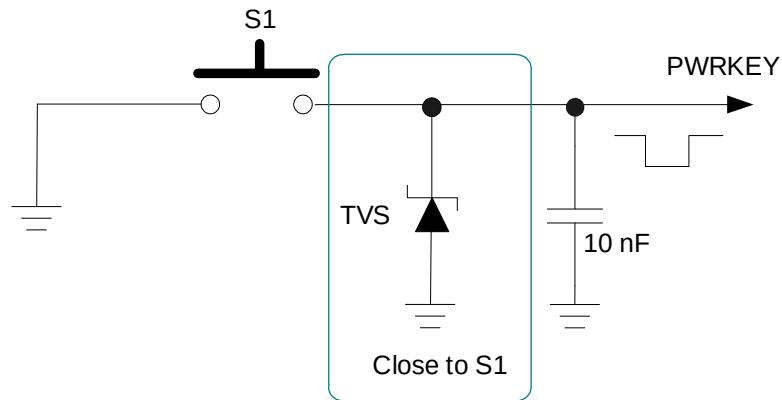


Figure 11: Reference Circuit with A Button

If the module needs to be turned on automatically when powered up, PWRKEY can be driven low directly to ground with a recommended resistor less than 1 k Ω . Ensure that the VBAT voltage is lower than 0.5 V before power-up.

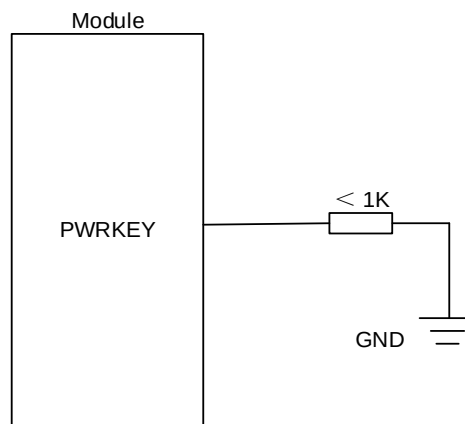


Figure 12: Turning On Module Automatically

The turn-on timing is illustrated in the following figure.

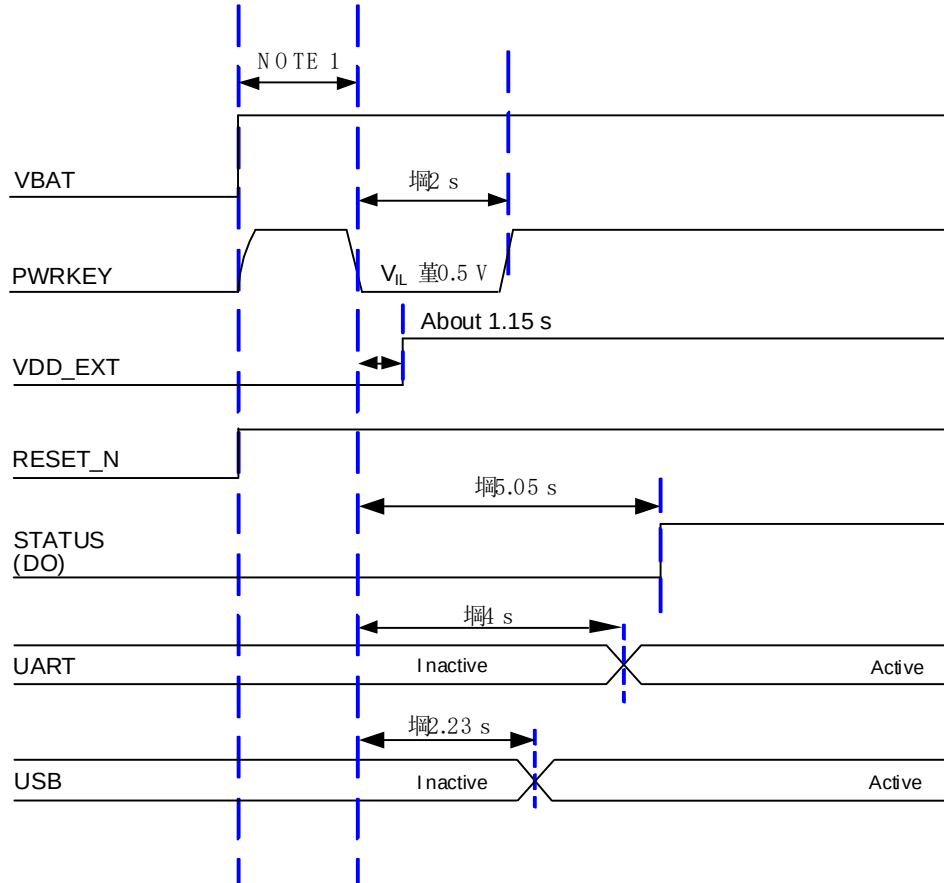


Figure 13: Turn-on Timing

NOTE

- Before pulling down the PWRKEY, ensure that the VBAT voltage is stable within the recommended range of 3.3–4.3 V. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
- When PWRKEY is connected to GND with a pull-down resistor, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and power up the module again. Therefore, it is recommended to use a control circuit to control the PWRKEY to turn on/off the module.
- Pay special attention to the following two power-on scenarios:
 - In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is powered on later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered on stably for at least 2 s before PWRKEY is pulled down;
 - In the scenario where VBAT is powered on first (or has always been powered on), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.
- Ensure that the voltage of VBAT is less than 0.5 V before powering up the module. If MOSFET is

used to control the VBAT power supply, a discharge circuit must be designed to ensure that the VBAT voltage can be released quickly after the module is shut down and powered down.

3.7. Turn-off

Both the following methods can be used to turn off the module:

- Use the PWRKEY pin.
- Use **AT+QPOWD**. See *document [3]* for details.

3.7.1. Turn-off with PWRKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY, and the module will execute power-down procedure. The turn-off timing is illustrated in the following figure.

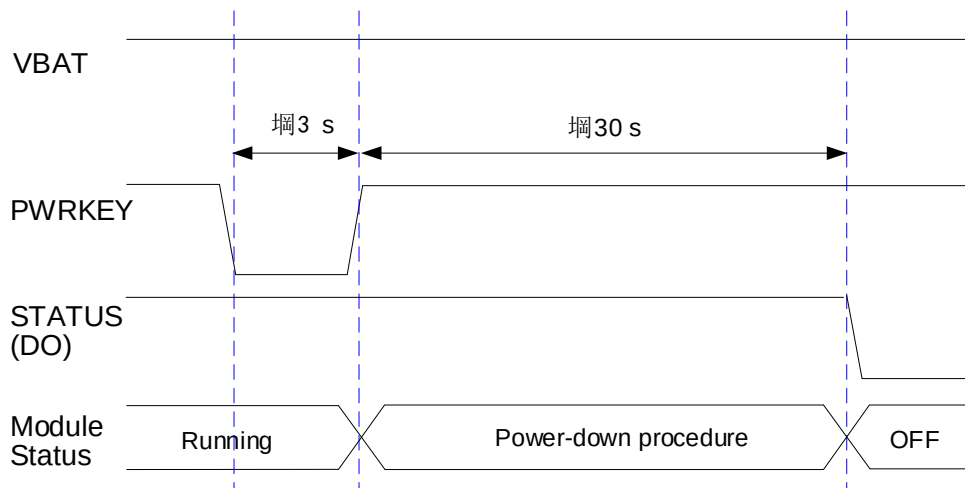


Figure 14: Turn-off Timing

3.7.2. Turn-off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

- During the shutdown, the module will log out of the network. The time for logging out relates to its network status. Thus, pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.

3.8. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	VBAT power domain. Active low. It is recommended to reserve a test point.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

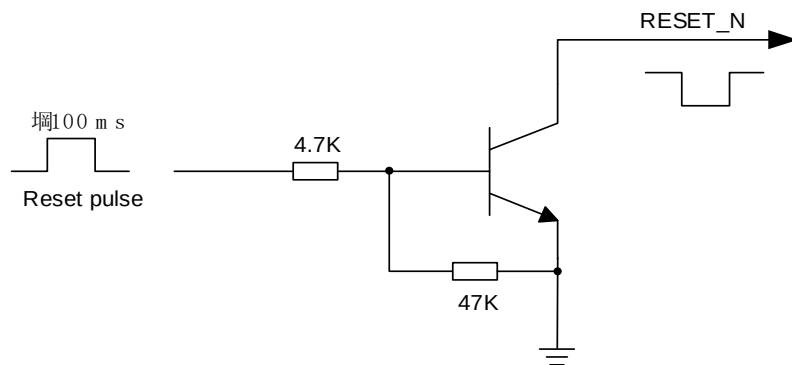


Figure 15: Reference Circuit of RESET_N by Using Driving Circuit

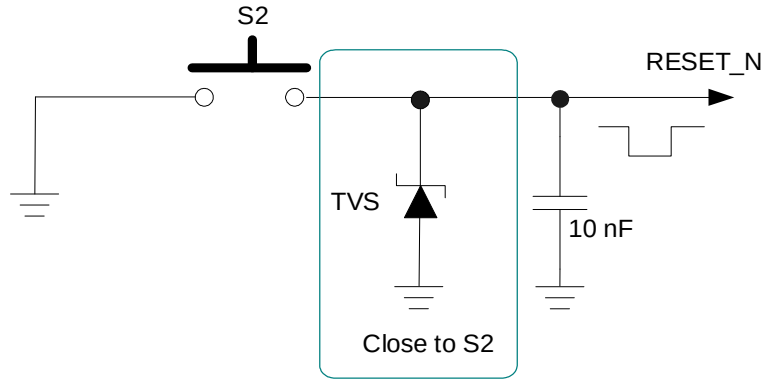


Figure 16: Reference Circuit of RESET_N by Using Button

The reset timing is illustrated in the following figure.

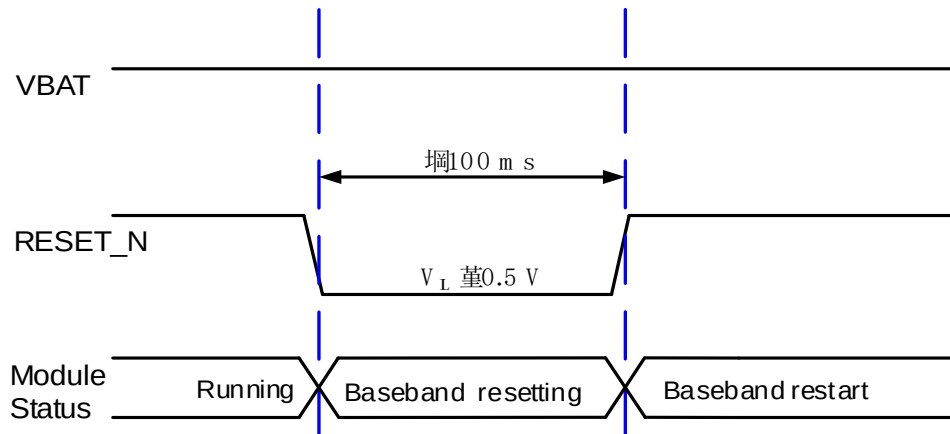


Figure 17: Reset Timing

NOTE

1. Ensure the capacitance on PWRKEY and RESET_N does not exceed 10 nF.
2. Use RESET_N only when you fail to turn off the module with **AT+QPOWD** and PWRKEY.
3. The RESET_N pin performs a soft reset which only resets the baseband, not the PMU.

4 Application Interfaces

4.1. USB Interface

The module provides an integrated Universal Serial Bus (USB) interface, which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device. The USB interface can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Input voltage range: 3.5 V to 5.25 V. A test point must be reserved. The USB_VBUS pin needs to be connected with a 1 k Ω resistor in series if USB_VBUS is connected to power supply and VBAT is powered down.
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω .
USB_DM	10	AIO	USB differential data (-)	Test points must be reserved.

Test points must be reserved for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

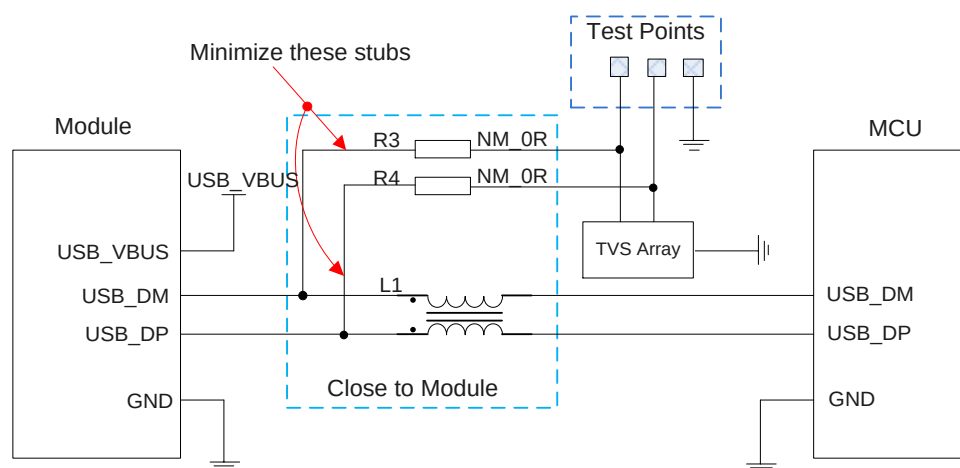


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data traces, L1, R3, and R4 must be placed close to the module, and resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. The impedance of USB differential traces is 90 Ω .
- Do not route signal traces under or near crystals, oscillators, magnetic devices, and RF signal traces.
- Pay attention to the selection of the TVS array on the USB data traces. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

For more details about the USB 2.0 specification, visit <http://www.usb.org/home>.

4.2. USB_BOOT Interface

The module provides a USB_BOOT interface. Pull up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter the forced download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 13: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into download mode	1.8 V power domain. Active high. A circuit that can set the module into forced download mode should be reserved during design. It is recommended to reserve a test point.

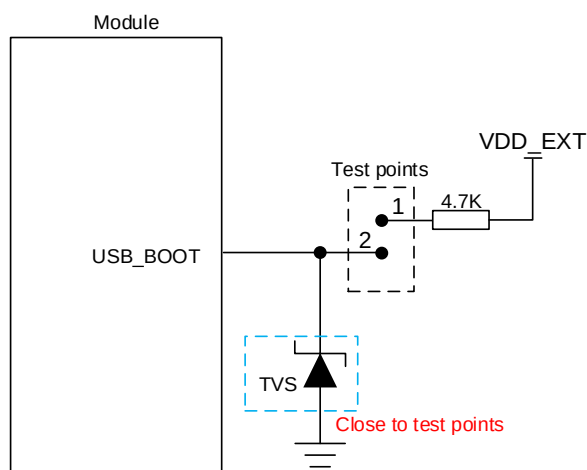


Figure 19: Reference Circuit of USB_BOOT Interface

NOTE

1. If you need to manually force the module to enter download mode, directly connect the test points shown in **Figure 19**.
2. The firmware upgrade function of USB interface can be used in forced download mode. It is strongly recommended to lead out USB_BOOT and VDD_EXT together with the USB interface.

4.3. (U)SIM Interfaces

The module provides two (U)SIM interfaces meeting ETSI requirement and IMT-2000 specification. Either 1.8 V or 3.0 V (U)SIM card is supported. Dual SIM Single Standby is supported by default and please contact Quectel Technical Support if Dual SIM Dual Standby is required.

Table 14: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Specified ground for (U)SIM1 card	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. A test point must be reserved.

The module supports (U)SIM card hot-plug via the USIM_DET pin and both high- and low-level detections are supported. By default, the function is disabled, and see **AT+QSIMDET** in **document [3]** for more details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

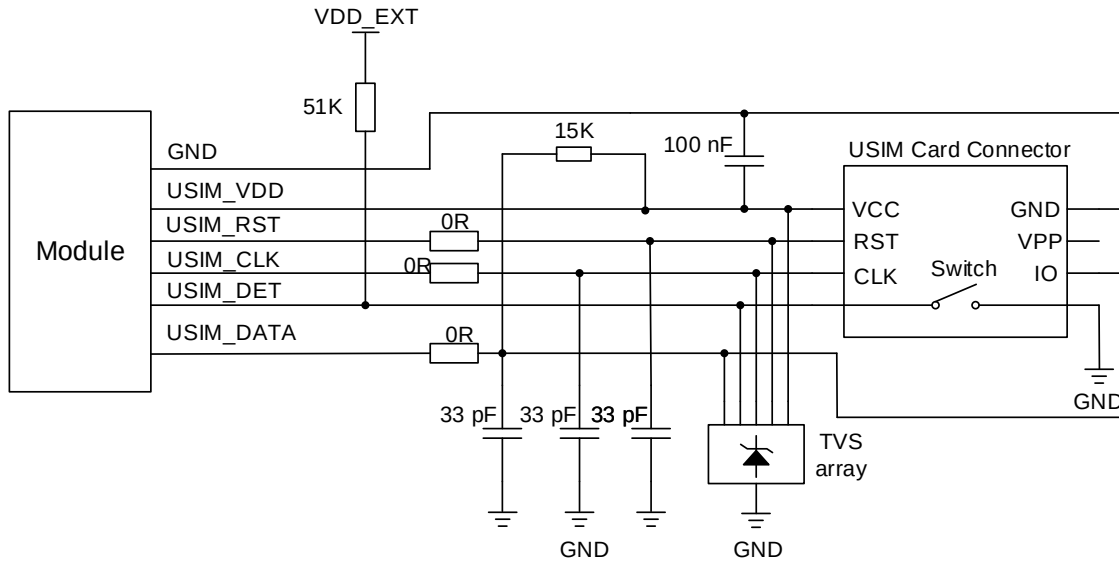


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

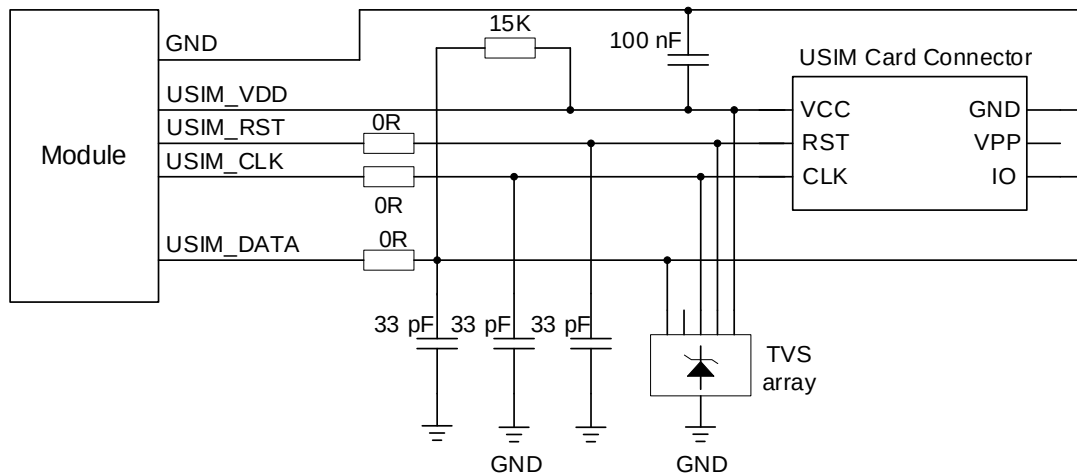


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM_VDD and GND not exceed 1 μ F, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and

shield them with surrounded ground.

- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should not exceed 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. The 33 pF capacitors are used for filtering RF interference. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.4. UARTs

The module provides three UARTs: main UART, debug UART, and auxiliary UART. Their features are described as follows.

- Main UART: supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, and 921600 bps, and the default is 115200 bps. It supports RTS and CTS hardware flow control. This interface is used for data transmission and AT command communication.
- Debug UART: supports 921600 bps baud rate only. It is used for log output and Linux console. It can only be used for debugging.
- Auxiliary UART: the baud rate is the same as that of the main UART.

Table 15: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Clear to send signal from the module	1.8 V power domain. Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module	1.8 V power domain. Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	1.8 V power domain. If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	

Table 16: Pin Definition of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain.
DBG_TXD	23	DO	Debug UART transmit	Test points must be reserved.

Table 17: Pin Definition of Auxiliary UART

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain.
AUX_RXD	28	DI	Auxiliary UART receive	If unused, keep them open.

The module provides 1.8 V UART. Use a level-shifting circuit if the application is equipped with a 3.3 V UART.

A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

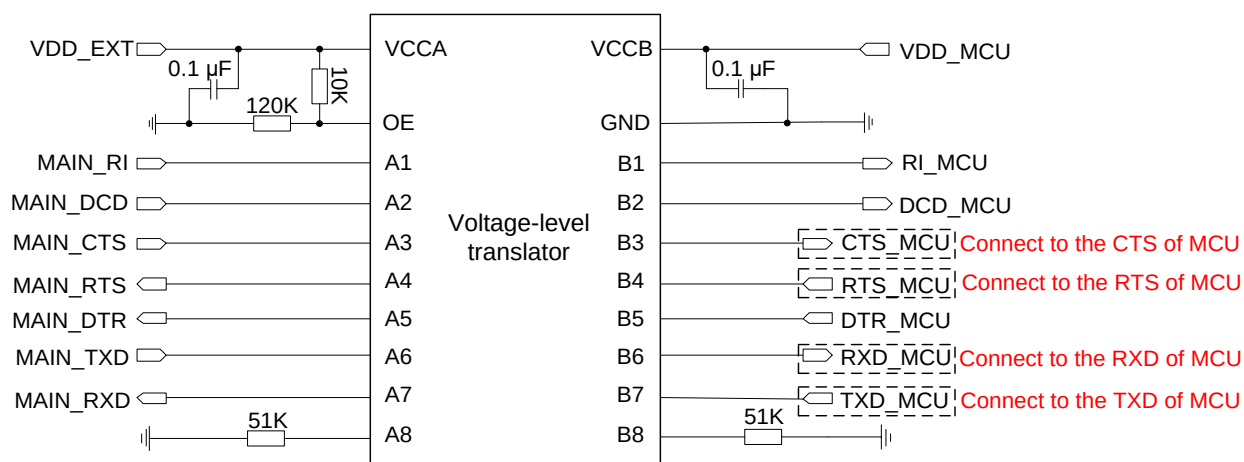


Figure 22: Reference Circuit with Voltage-level Translator (Main UART)

Visit <http://www.ti.com> for more information.

Another example with transistor circuit is shown as follows. For the design of circuits in dotted lines, refer to that of the circuits in solid lines, but pay attention to the direction of connection.

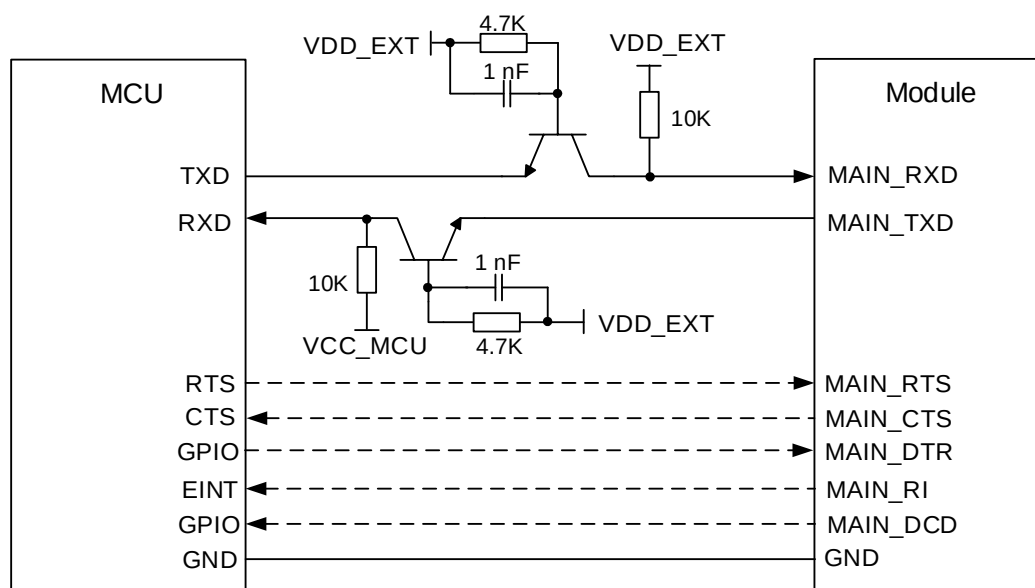


Figure 23: Reference Circuit with Transistor (Main UART)

NOTE

1. Transistor solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. The level-shifting circuits (**Figure 22** and **Figure 23**) take the main UART as an example. The circuits of the auxiliary UART are connected in the same way as the main UART.
4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.
5. When using pins 30, 38, and 39 (MAIN_DTR, MAIN_DCD, MAIN_RI), note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

4.5. PCM and I2C Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface. The PCM interface of the module only supports slave mode. The clock signal of the external codec IC needs to be provided externally.

PCM interface supports the short frame mode and the module can be used as the slave mode only. In short frame mode, $\text{PCM_CLK} = \text{the number of channels} \times \text{PCM_SYNC} \times 16 \text{ bit}$, where PCM_CLK

indicates PCM clock; the number of channels supports 1–4 channels, but the module will only take the data on the first channel; PCM_SYNC is equal to the audio sampling rate, which supports 8–44.1 KHz.

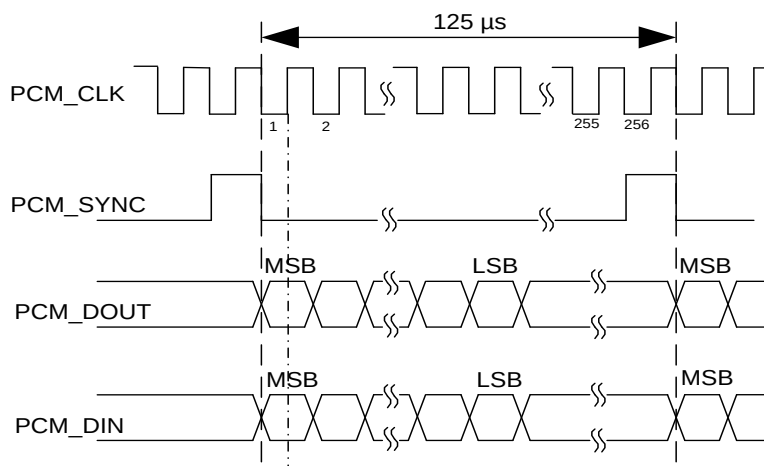


Figure 24: Timing of PCM Short Frame Mode

NOTE

The clocks of PCM_SYNC and PCM_CLK are provided by the external codec IC, but the PCM_SYNC frequency must be equal to the sampling frequency of the audio file played by the module.

Table 18: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	External 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep them open. Support slave mode only.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

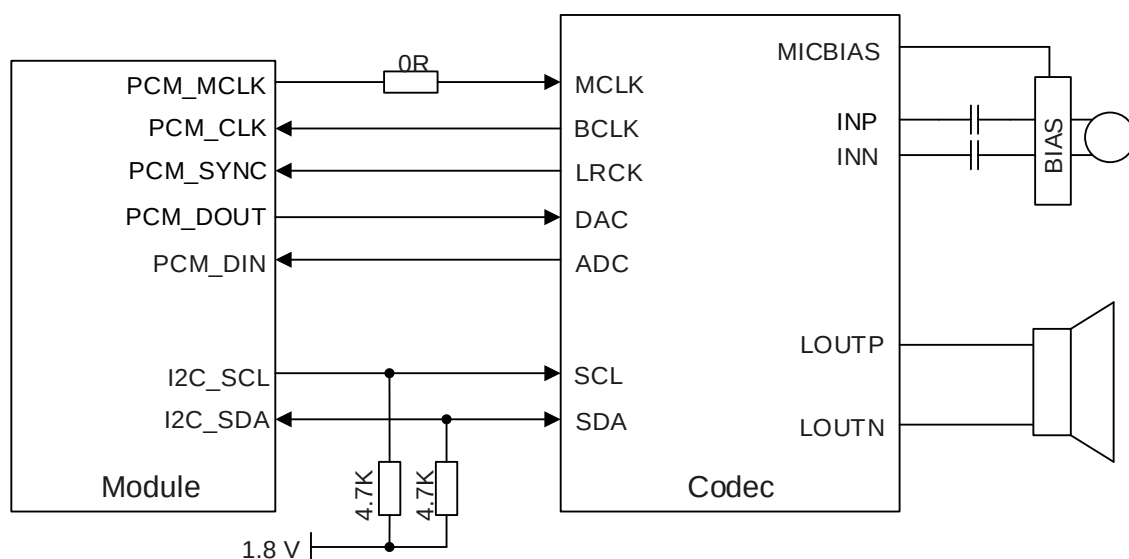


Figure 25: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve a termination resistor and a filter capacitor on the PCM traces (especially PCM_CLK trace).
2. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC, i.e., if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.
3. For PCM external codec solution, if you need to use the PCM_MCLK function of the module, contact Quectel Technical Support for details.

4.6. Analog Audio Interfaces

The module provides one analog audio input channel and one analog audio output channel. The pin definitions are shown in the following table.

Table 19: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description
MIC_N	119	AI	Microphone analog input (-)
MICBIAS	120	PO	Bias voltage output for microphone
SPK_P	121	AO	Analog audio differential output (+)

SPK_N	122	AO	Analog audio differential output (-)
MIC_P	126	AI	Microphone analog input (+)

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of handset, earpiece, and loudspeaker. (Since the module has no built-in PA, the analog audio output SPK can be directly used as earpiece, and if connected with external PA, it can be used as loudspeaker.)

4.6.1. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

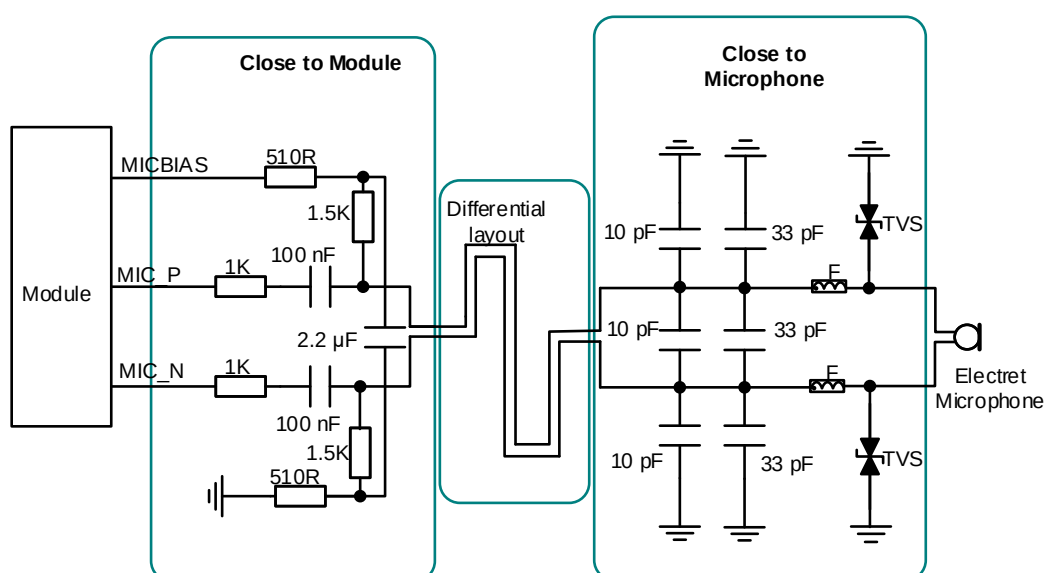


Figure 26: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components (TVS) used for protecting the MIC.

4.6.2. Earpiece Interface Design

The earpiece channel reference circuit is shown in the following figure:

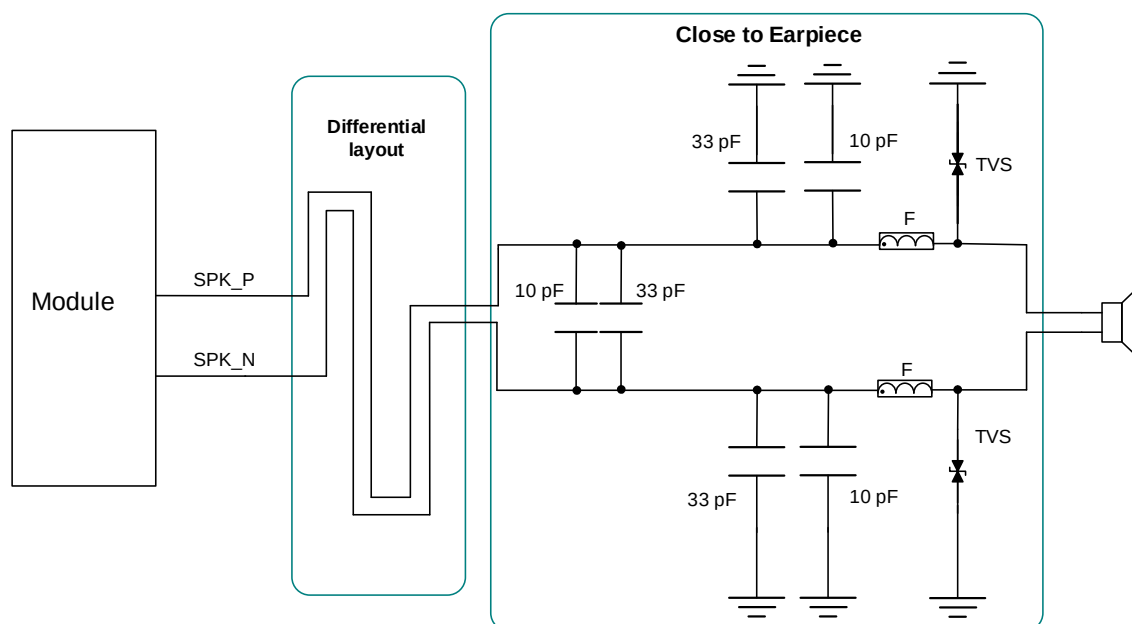


Figure 27: Reference Design for Earpiece Interface

4.6.3. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without these capacitors, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitors on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitors should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.7. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interfaces	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2	AI		

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC[0:1] Input Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

With **AT+QADC=<port>**, you can read the voltage values on ADC pins.

- **AT+QADC=0:** read the voltage values on ADC0
- **AT+QADC=1:** read the voltage values on ADC1

See **document [3]** for more details about the AT command.

NOTE

1. The input voltage of ADC pins should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.

4.8. SPI*

The module provides one SPI that only supports master mode. The voltage domain is 1.8 V. The maximum clock frequency is 25 MHz.

Table 22: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	
SPI_CS	25	DO	SPI chip select	1.8 V power domain. If unused, keep them open. Support master mode only.
SPI_DIN	88	DI	SPI data input	
SPI_DOUT	64	DO	SPI data output	

4.9. Indication Signals

Table 23: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep them open.
NET_STATUS	21	DO	Indicate the module's network activity status	
MAIN_RI	39	DO	Main UART ring indication	

4.9.1. STATUS

The STATUS pin indicates the module's operation status. It will output high level when module is powered on successfully.

A reference circuit is shown as below.

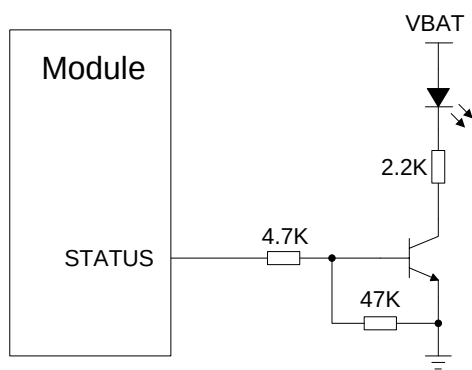


Figure 28: Reference Circuit of STATUS

4.9.2. NET_STATUS

The network activity status indication pin NET_STATUS can drive the network status indicator. The following table describes its working states in different network status.

Table 24: Working States of NET_STATUS

Pin Name	State	Network Status
NET_STATUS	Blink slowly (200 ms high/1800 ms low)	Network searching
	Blink quickly (234 ms high/266 ms low)	Registered on network and idle
	Blink rapidly (63 ms high /62 ms low)	Data transmission is ongoing
	Always high	Voice calling

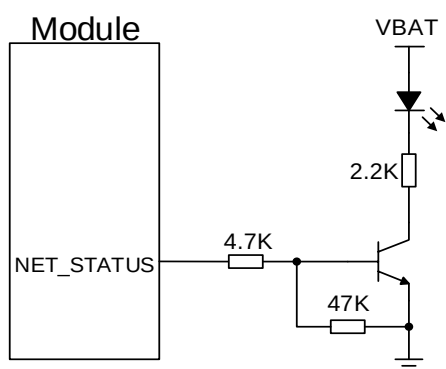


Figure 29: Reference Circuit of Network Activity Status Indication

4.9.3. MAIN_RI

You can configure MAIN_RI behaviors with **AT+QCFG="risignalttype","physical"**. No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI. MAIN_RI behavior can be configured flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 25: Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The MAIN_RI behaviors can be changed via **AT+QCFG="urc/ri/ring"**.

NOTE

1. The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The default port is USB AT port.
2. See **document [3]** for details on the above-mentioned AT commands.
3. When using pin 39 (MAIN_RI), note that it will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before it can be configured as 1.8 V output. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

4.10. W_DISABLE#

The module provides W_DISABLE# to enable or disable airplane mode.

Table 26: Pin Definition of W_DISABLE#

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain. Pulled up by default. Driving it low can enable the module into airplane mode. If unused, keep it open.

Set the W_DISABLE# pin into low level, and the module will enter airplane mode. Release the pin and the module will exit airplane mode. Its control function for airplane mode, which is disabled by default, can be enabled through **AT+QCFG="airplanecontrol",1**. For more details about AT command, see *document [3]*.

NOTE

When using pin 18 (W_DISABLE#), note that it will have a period of variable level state (not controllable by software) after the module is powered on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before it can be configured as 1.8 V input. Evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Main Antenna and Bluetooth Antenna/Wi-Fi Scan Antenna

5.1.1. Antenna Interface & Frequency Bands

Table 27: Pin Definition of Main and Bluetooth Antenna/Wi-Fi Scan Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_BT/ WIFI_SCAN	56	AIO/ AI	Bluetooth antenna/Wi-Fi Scan antenna interface	When Wi-Fi Scan is used, only receiving is supported. 50 Ω impedance. If unused, keep it open.

NOTE

EG912U-EAL does not support Bluetooth and Wi-Fi Scan functions, and pin 56 should be kept reserved. For EG912U-GL, these functions are optional. The Wi-Fi Scan function utilizes the same antenna interface as the Bluetooth antenna. Due to this shared interface, the two functions cannot be used simultaneously. For details, contact Quectel Technical Support.

Table 28: EG912U-GL Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
GSM850	824–849	869–894
EGSM900	880–915	925–960

DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B17	704–716	734–746
LTE-FDD B18	815–830	860–875
LTE-FDD B19	830–845	875–890
LTE-FDD B20	832–862	791–821
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–850	859–894
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

Table 29: EG912U-EAL Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

5.1.2. Antenna Tuner Control Interfaces

The module can use GRFC (generic RF control) interfaces to control external antenna tuner.

Table 30: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	76	DO	Generic RF controller	1.8 V power domain.

GRFC2	77	DO	If unused, keep them open.
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Table 31: Digital Characteristics of GRFC Interface (Unit: V)

Parameter	Min.	Max.
V _{OL}	0	0.36
V _{OH}	1.44	1.8

5.1.3. Output Power

Table 32: RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD bands	23 dBm ±2 dB	< -39 dBm
LTE-TDD bands	23 dBm ±2 dB	< -39 dBm

5.1.4. Receiver Sensitivity

Table 33: EG912U-GL Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP Requirements (SIMO)
	Primary	
GSM850	-108.6	-102.0
EGSM900	-108.4	-102.0
DCS1800	-108.1	-102.0
PCS1900	-108.3	-102.0

LTE-FDD B1 (10 MHz)	-97.8	-93.3
LTE-FDD B2 (10 MHz)	-98.6	-91.3
LTE-FDD B3 (10 MHz)	-98.7	-90.3
LTE-FDD B4 (10 MHz)	-97.9	-93.3
LTE-FDD B5 (10 MHz)	-99.0	-91.8
LTE-FDD B7 (10 MHz)	-96.0	-91.3
LTE-FDD B8 (10 MHz)	-98.9	-90.8
LTE-FDD B12 (10 MHz)	-98.0	-90.3
LTE-FDD B13 (10 MHz)	-99.0	-90.3
LTE-FDD B17 (10 MHz)	-97.5	-93.3
LTE-FDD B18 (10 MHz)	-98.7	-93.8
LTE-FDD B19 (10 MHz)	-99.2	-96.3
LTE-FDD B20 (10 MHz)	-98.6	-90.8
LTE-FDD B25 (10 MHz)	-98.0	-92.8
LTE-FDD B26 (10 MHz)	-98.6	-91.3
LTE-FDD B28 (10 MHz)	-99.1	-92.8
LTE-FDD B66 (10 MHz)	-97.8	-92.8
LTE-TDD B34 (10 MHz)	-98.7	-96.3
LTE-TDD B38 (10 MHz)	-98.7	-96.3
LTE-TDD B39 (10 MHz)	-99.4	-93.8
LTE-TDD B40 (10 MHz)	-99.0	-96.3
LTE-TDD B41 (10 MHz)	-98.3	-91.8

Table 34: EG912U-EAL Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP Requirements (SIMO)
	Primary	
GSM850	-108.2	-102.0
EGSM900	-108.3	-102.0
DCS1800	-108.1	-102.0
PCS1900	-107.8	-102.0
LTE-FDD B1 (10 MHz)	-97.4	-93.3
LTE-FDD B2 (10 MHz)	-97.5	-91.3
LTE-FDD B3 (10 MHz)	-97.9	-90.3
LTE-FDD B4 (10 MHz)	-97.5	-93.3
LTE-FDD B5 (10 MHz)	-98.5	-91.8
LTE-FDD B7 (10 MHz)	-95.3	-91.3
LTE-FDD B8 (10 MHz)	-98.5	-90.8
LTE-FDD B20 (10 MHz)	-98.9	-90.8
LTE-FDD B28 (10 MHz)	-98.8	-92.3
LTE-FDD B66 (10 MHz)	-97.3	-92.8
LTE-TDD B38 (10 MHz)	-98.3	-96.3
LTE-TDD B40 (10 MHz)	-98.6	-96.3
LTE-TDD B41 (10 MHz)	-98.1	-91.8

5.1.5. Reference Design

A reference design of ANT_MAIN and ANT_BT/WIFI_SCAN is shown as below.

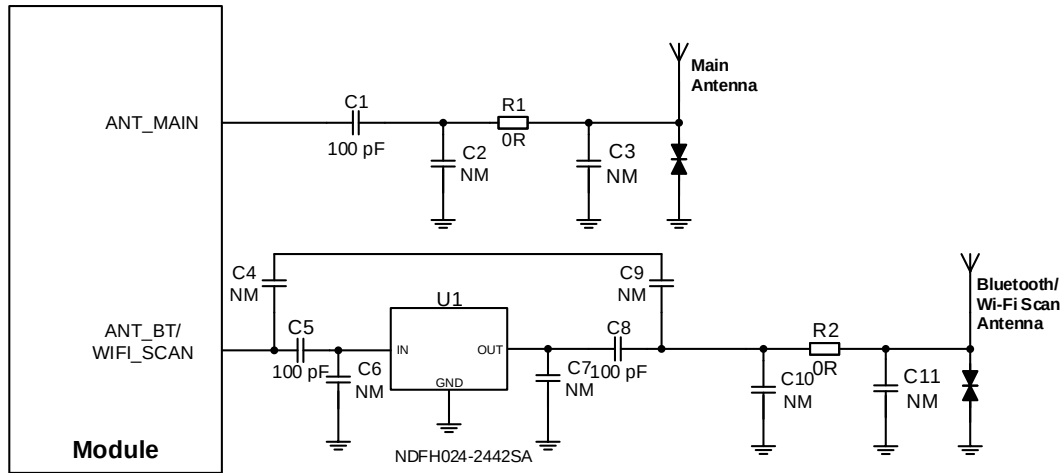


Figure 30: Reference Circuit of RF Antennas

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Place the DC-blocking capacitors (C1 and C8 (or C9)) and π -type matching components (C2, R1, C3 and C10, R2, C11) to antennas as close as possible.
3. EG912U-EAL does not support Bluetooth and Wi-Fi Scan functions. For EG912U-GL, these functions are optional. The Wi-Fi Scan function utilizes the same antenna interface as the Bluetooth antenna. Due to this shared interface, the two functions cannot be used simultaneously. For details, contact Quectel Technical Support.
4. If there is DC power at the antenna ports, C1 and C8 (or C9) must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C1 and C8 (or C9) should not be reserved.
5. It is recommended to reserve a filter at Wi-Fi Scan/Bluetooth antenna port. When the isolation between main antenna and Wi-Fi Scan/Bluetooth antenna is greater than 20 dB, the compatible design (C4 and C9) can be applied first.

5.2. GNSS (Optional)

Only EG912U-GL supports GNSS function. The information is as follows:

- Supports GPS, GLONASS, BDS, Galileo, QZSS constellations.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1 Hz).
- The module's GNSS function is disabled by default. It can be enabled via AT commands. See [document \[1\]](#) for details.

5.2.1. Antenna Interface & Frequency Bands

Table 35: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 36: GNSS Frequency (Unit: MHz)

GNSS Constellation Type	Frequency
GPS	1575.42 $\pm$ 1.023
GLONASS	1597.5–1605.8
Galileo	1575.42 $\pm$ 2.046
BDS	1561.098 $\pm$ 2.046
QZSS	1575.42 $\pm$ 1.023

5.2.2. GNSS Performance

Table 37: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-145	dBm
	Reacquisition		-160	
	Tracking		-159	
TTFF	Cold start @ open sky	Autonomous	28	s
		AGNSS start	6.86	
	Warm start @ open sky	Autonomous	28	
		AGNSS start	3.86	
	Hot start @ open sky	Autonomous	4	
		AGNSS start	0.51	

Accuracy	CEP-50	Autonomous @ open sky	2.5	m
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NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π -type attenuation circuit and use a high-performance LDO in the power system design.

A reference design of GNSS antenna is shown as below:

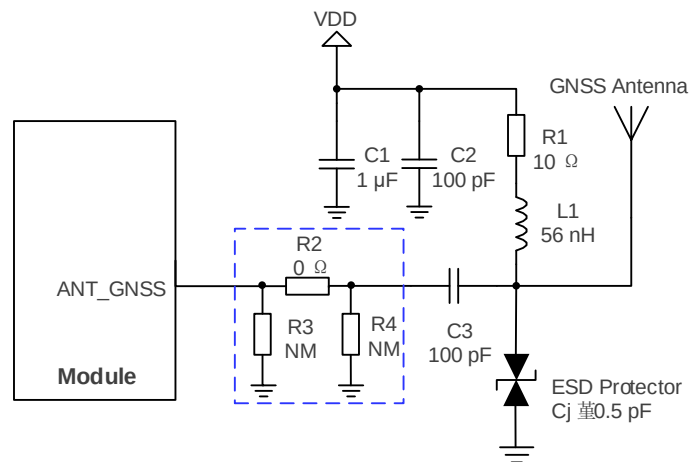


Figure 31: Reference Circuit of GNSS Antenna

NOTE

1. The active antenna requires an external power supply. VDD is recommended to be 3.3 V @ 30 mA.
2. The VDD circuit is not needed if you use the passive antenna.
3. It is recommended to use a passive antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.
4. For passive antenna, if there is DC power at the antenna ports, C3 must be used for DC-blocking

to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3 should not be reserved.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω . The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

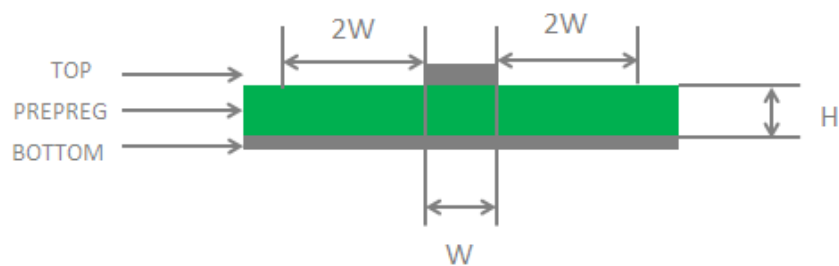


Figure 32: Microstrip Design on a 2-layer PCB

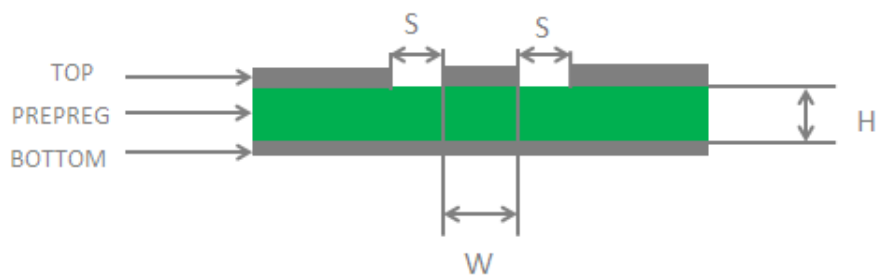


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

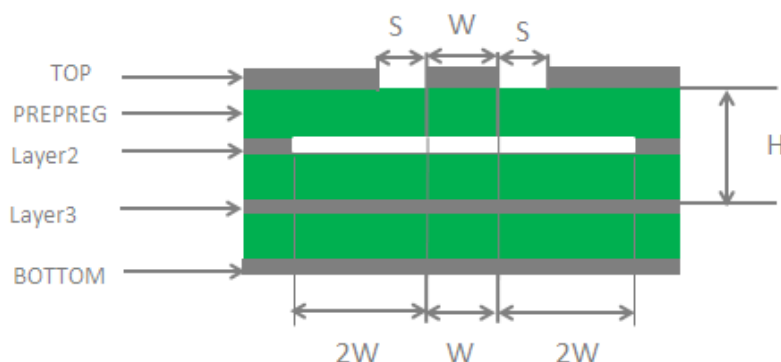


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

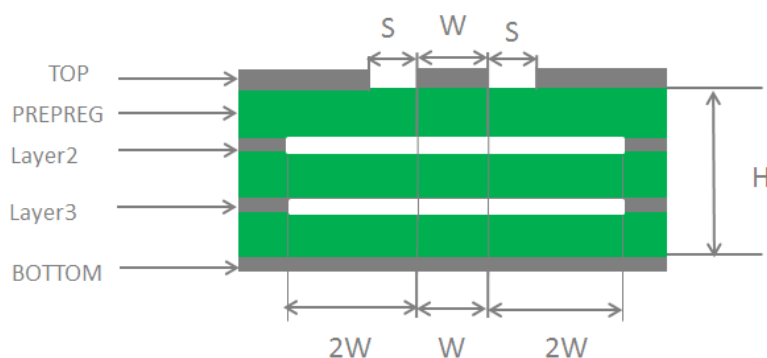


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to $50\ \Omega$.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135° .
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces ($2 \times W$).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document [5]**.

5.4. Requirements for Antenna Design

Table 38: Requirements for Antenna Design

Type	Requirement
GNSS (optional)	● Frequency range: 1559–1609 MHz ● RHCP or linear polarization ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: ● Passive antenna gain: > 0 dBi
	For active antenna usage: ● Active antenna noise coefficient: < 1.5 dB ● Active antenna embedded LNA gain: < 24 dB
Cellular	● VSWR: ≤ 2 ● Efficiency: $> 30\%$ ● Max. input power: 50 W ● Input impedance: 50 Ω ● Polarization: vertical direction ● Cable insertion loss: < 1 dB: LB (< 1 GHz) < 1.5 dB: MB (1–2.3 GHz) < 2 dB: HB (> 2.3 GHz)
Bluetooth/Wi-Fi Scan (optional)	● VSWR: ≤ 3 ● Gain: 1 dBi ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: < 1 dB

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

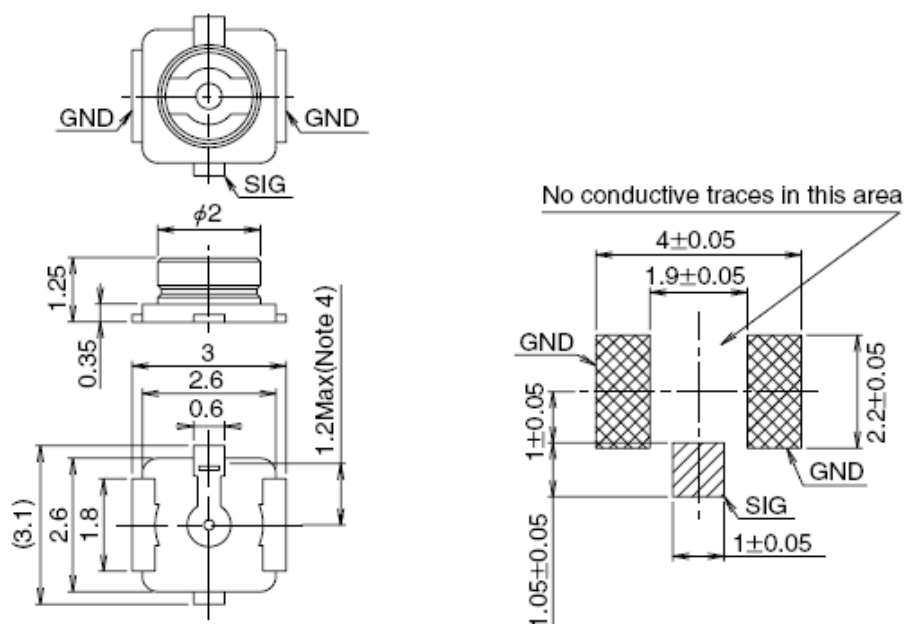


Figure 36: Dimensions of Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

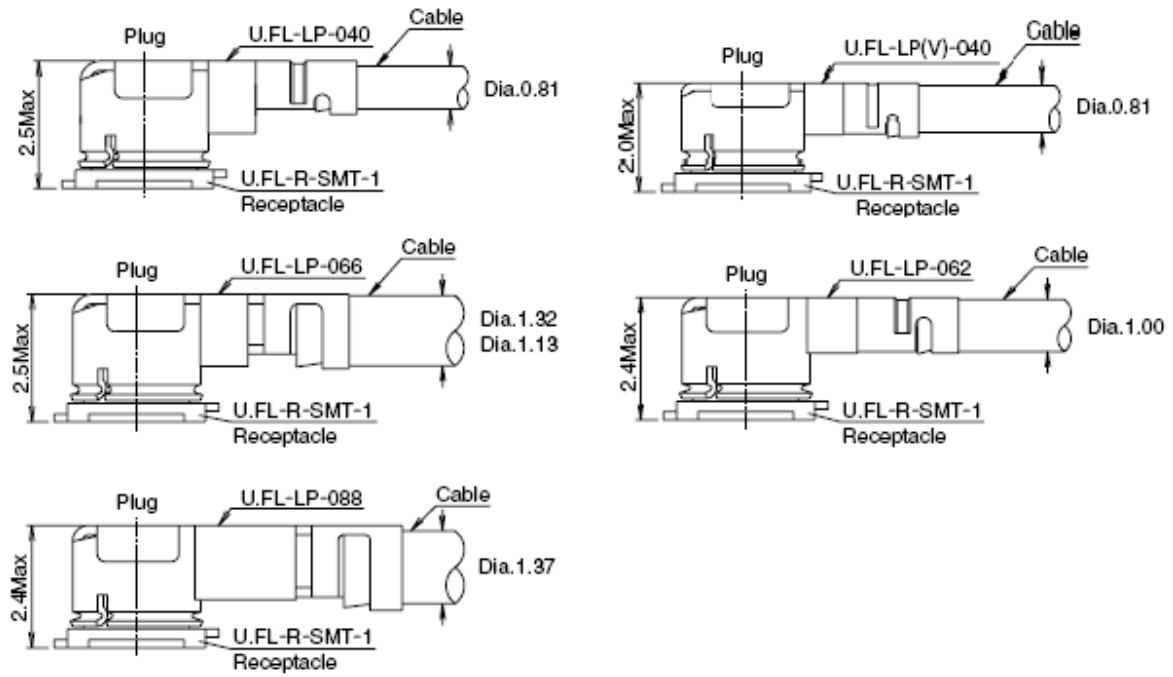


Figure 38: Space Factor of Mated Connector (Unit: mm)

For more details, visit <http://hirose.com>.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 39: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	2.5	A
Voltage on Digital Pins	-0.3	2.1	V
Voltage at ADC[0:1]	0	VBAT	V

6.2. Power Supply Ratings

Table 40: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	At maximum power control level	-	-	400	mV
I _{VBAT}	Peak power	At maximum power control	-	1.7	2.5	A

	consumption	level				
USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

6.3. Power Consumption

Table 41: EG912U-GL Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	34	μA
	Minimum functionality mode (USB disconnected)	1.4	mA
	Minimum functionality mode (USB connected)	2.5	mA
	Airplane mode (USB disconnected)	1.5	mA
	Airplane mode (USB connected)	2.6	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.3	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.8	mA
	EGSM900 @ DRX = 5 (USB connected)	3.3	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.6	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.3	mA
Sleep state	DCS1800 @ DRX = 5 (USB disconnected)	1.8	mA
	DCS1800 @ DRX = 5 (USB connected)	3.3	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.6	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.9	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.1	mA
	LTE-FDD @ PF = 64 (USB connected)	3.6	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.7	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.5	mA

	LTE-TDD @ PF = 32 (USB disconnected)	3.0	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.1	mA
	LTE-TDD @ PF = 64 (USB connected)	3.6	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.7	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.5	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	14.1	mA
	EGSM900 @ DRX = 5 (USB connected)	30	mA
	LTE-FDD @ PF = 64 (USB disconnected)	14.2	mA
	LTE-FDD @ PF = 64 (USB connected)	30.2	mA
	LTE-TDD @ PF = 64 (USB disconnected)	14.3	mA
	LTE-TDD @ PF = 64 (USB connected)	30.2	mA
LTE data transmission	LTE-FDD B1 @ 23.20 dBm	635	mA
	LTE-FDD B2 @ 22.24 dBm	604	mA
	LTE-FDD B3 @ 23.20 dBm	634	mA
	LTE-FDD B4 @ 22.80 dBm	694	mA
	LTE-FDD B5 @ 22.01 dBm	622	mA
	LTE-FDD B7 @ 22.62 dBm	919	mA
	LTE-FDD B8 @ 23.21 dBm	710	mA
	LTE-FDD B12 @ 24.13 dBm	656	mA
	LTE-FDD B13 @ 23.39 dBm	605	mA
	LTE-FDD B17 @ 23.53 dBm	649	mA
	LTE-FDD B18 @ 22.33 dBm	608	mA
	LTE-FDD B19 @ 22.05 dBm	596	mA
	LTE-FDD B20 @ 23.01 dBm	652	mA
	LTE-FDD B25 @ 22.62 dBm	624	mA
	LTE-FDD B26 @ 23.17 dBm	658	mA

	LTE-FDD B28 @ 23.43 dBm	666	mA
	LTE-FDD B66 @ 22.45 dBm	732	mA
	LTE-TDD B34 @ 22.91 dBm	274	mA
	LTE-TDD B38 @ 23.19 dBm	407	mA
	LTE-TDD B39 @ 23.41 dBm	255	mA
	LTE-TDD B40 @ 23.71 dBm	394	mA
	LTE-TDD B41 @ 23.71 dBm	384	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.95 dBm	234	mA
	GSM850 3DL/2UL @ 30.94 dBm	338	mA
	GSM850 2DL/3UL @ 29.02 dBm	396	mA
	GSM850 1DL/4UL @ 27.03 dBm	417	mA
	EGSM900 4DL/1UL @ 32.27 dBm	230	mA
	EGSM900 3DL/2UL @ 31.01 dBm	378	mA
	EGSM900 2DL/3UL @ 29.20 dBm	447	mA
	EGSM900 1DL/4UL @ 27.41 dBm	488	mA
	DCS1800 4DL/1UL @ 30.95 dBm	189	mA
	DCS1800 3DL/2UL @ 28.76 dBm	272	mA
	DCS1800 2DL/3UL @ 26.64 dBm	310	mA
	DCS1800 1DL/4UL @ 24.35 dBm	322	mA
	PCS1900 4DL/1UL @ 30.17 dBm	168	mA
	PCS1900 3DL/2UL @ 28.08 dBm	238	mA
	PCS1900 2DL/3UL @ 26.13 dBm	276	mA
	PCS1900 1DL/4UL @ 24.10 dBm	288	mA
GSM voice call	GSM850 PCL = 5 @ 32.88 dBm	239	mA
	GSM850 PCL = 12 @ 18.87 dBm	90	mA
	GSM850 PCL = 19 @ 4.77 dBm	63	mA

EGSM900 PCL = 5 @ 32.72 dBm	257	mA
EGSM900 PCL = 12 @ 19.35 dBm	99	mA
EGSM900 PCL = 19 @ 4.82 dBm	64	mA
DCS1800 PCL = 0 @ 30.35 dBm	188	mA
DCS1800 PCL = 7 @ 16.39 dBm	80	mA
DCS1800 PCL = 15 @ 1.29 dBm	61	mA
PCS1900 PCL = 0 @ 30.06 dBm	172	mA
PCS1900 PCL = 7 @ 16.01 dBm	78	mA
PCS1900 PCL = 15 @ 1.29 dBm	61	mA

Table 42: EG912U-EAL Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	30	μA
	Minimum functionality mode (USB disconnected)	0.9	mA
	Minimum functionality mode (USB connected)	1.9	mA
	Airplane mode (USB disconnected)	1.0	mA
	Airplane mode (USB connected)	2.0	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.97	mA
Sleep state	EGSM900 @ DRX = 5 (USB disconnected)	1.48	mA
	EGSM900 @ DRX = 5 (USB connected)	2.79	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.37	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.90	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.40	mA
	DCS1800 @ DRX = 5 (USB connected)	2.68	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.34	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.4	mA

	LTE-FDD @ PF = 64 (USB disconnected)	1.7	mA
	LTE-FDD @ PF = 64 (USB connected)	2.8	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.2	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.5	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.7	mA
	LTE-TDD @ PF = 64 (USB connected)	2.8	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.3	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.1	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.04	mA
	EGSM900 @ DRX = 5 (USB connected)	27.77	mA
	LTE-FDD @ PF = 64 (USB disconnected)	11.8	mA
	LTE-FDD @ PF = 64 (USB connected)	27.6	mA
	LTE-TDD @ PF = 64 (USB disconnected)	11.8	mA
	LTE-TDD @ PF = 64 (USB connected)	27.6	mA
LTE data transmission	LTE-FDD B1 @ 23.43 dBm	668	mA
	LTE-FDD B2 @ 23.52 dBm	662	mA
	LTE-FDD B3 @ 23.71 dBm	688	mA
	LTE-FDD B4 @ 23.02 dBm	695	mA
	LTE-FDD B5 @ 23.68 dBm	685	mA
	LTE-FDD B7 @ 23.66 dBm	933	mA
	LTE-FDD B8 @ 23.30 dBm	733	mA
	LTE-FDD B20 @ 23.62 dBm	695	mA
	LTE-FDD B28 @ 23.47 dBm	688	mA
	LTE-FDD B66 @ 23.57 dBm	735	mA
	LTE-TDD B38 @ 23.72 dBm	411	mA

	LTE-TDD B40 @ 23.89 dBm	395	mA
	LTE-TDD B41 @ 23.83 dBm	420	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.71 dBm	206	mA
	GSM850 3DL/2UL @ 31.90 dBm	345	mA
	GSM850 2DL/3UL @ 30.09 dBm	409	mA
	GSM850 1DL/4UL @ 28.97 dBm	482	mA
	EGSM900 4DL/1UL @ 32.96 dBm	233	mA
	EGSM900 3DL/2UL @ 32.20 dBm	395	mA
	EGSM900 2DL/3UL @ 30.57 dBm	478	mA
	EGSM900 1DL/4UL @ 29.55 dBm	579	mA
	DCS1800 4DL/1UL @ 29.85 dBm	154	mA
	DCS1800 3DL/2UL @ 28.34 dBm	240	mA
	DCS1800 2DL/3UL @ 27.38 dBm	308	mA
	DCS1800 1DL/4UL @ 26.24 dBm	363	mA
	PCS1900 4DL/1UL @ 29.91 dBm	149	mA
	PCS1900 3DL/2UL @ 29.15 dBm	246	mA
	PCS1900 2DL/3UL @ 27.31 dBm	290	mA
	PCS1900 1DL/4UL @ 26.36 dBm	343	mA
GSM voice call	GSM850 PCL = 5 @ 32.87 dBm	230	mA
	GSM850 PCL = 12 @ 19.24 dBm	89	mA
	GSM850 PCL = 19 @ 5.24 dBm	60	mA
	EGSM900 PCL = 5 @ 32.93 dBm	256	mA
	EGSM900 PCL = 12 @ 19.52 dBm	95	mA
	EGSM900 PCL = 19 @ 5.86 dBm	62	mA
	DCS1800 PCL = 0 @ 29.79 dBm	171	mA
	DCS1800 PCL = 7 @ 16.12 dBm	76	mA

DCS1800 PCL = 15 @ 0.76 dBm	58	mA
PCS1900 PCL = 0 @ 30.01 dBm	165	mA
PCS1900 PCL = 7 @ 16.25 dBm	77	mA
PCS1900 PCL = 15 @ 0.76 dBm	58	mA

6.4. Digital I/O Characteristic

Table 43: 1.8 V I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	$0.7 \times VDDIO$	$VDDIO + 0.2$
V_{IL}	Low-level input voltage	-0.3	$0.3 \times VDDIO$
V_{OH}	High-level output voltage	$VDDIO - 0.2$	-
V_{OL}	Low-level output voltage	-	0.2

NOTE

VDDIO is the power domain of the module's I/O pins.

Table 44: (U)SIM Low-voltage I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
USIM_VDD	Power supply	1.62	1.98
V_{IH}	High-level input voltage	$0.7 \times USIM_VDD$	USIM_VDD
V_{IL}	Low-level input voltage	0	$0.2 \times USIM_VDD$
V_{OH}	High-level output voltage	$0.7 \times USIM_VDD$	USIM_VDD
V_{OL}	Low-level output voltage	0	$0.15 \times USIM_VDD$

Table 45: (U)SIM High-voltage I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
USIM_VDD	Power supply	2.9	3.3
V _{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V _{IL}	Low-level input voltage	0	0.15 × USIM_VDD
V _{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V _{OL}	Low-level output voltage	0	0.15 × USIM_VDD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 46: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 47: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Operating Temperature Range ⁷	-35	+25	+75
Extended Operation Range ⁸	-40	+25	+85
Storage Temperature Range	-40	+25	+90

⁷ Within this range, the module's indicators comply with 3GPP specification requirements.

⁸ Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out} , may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

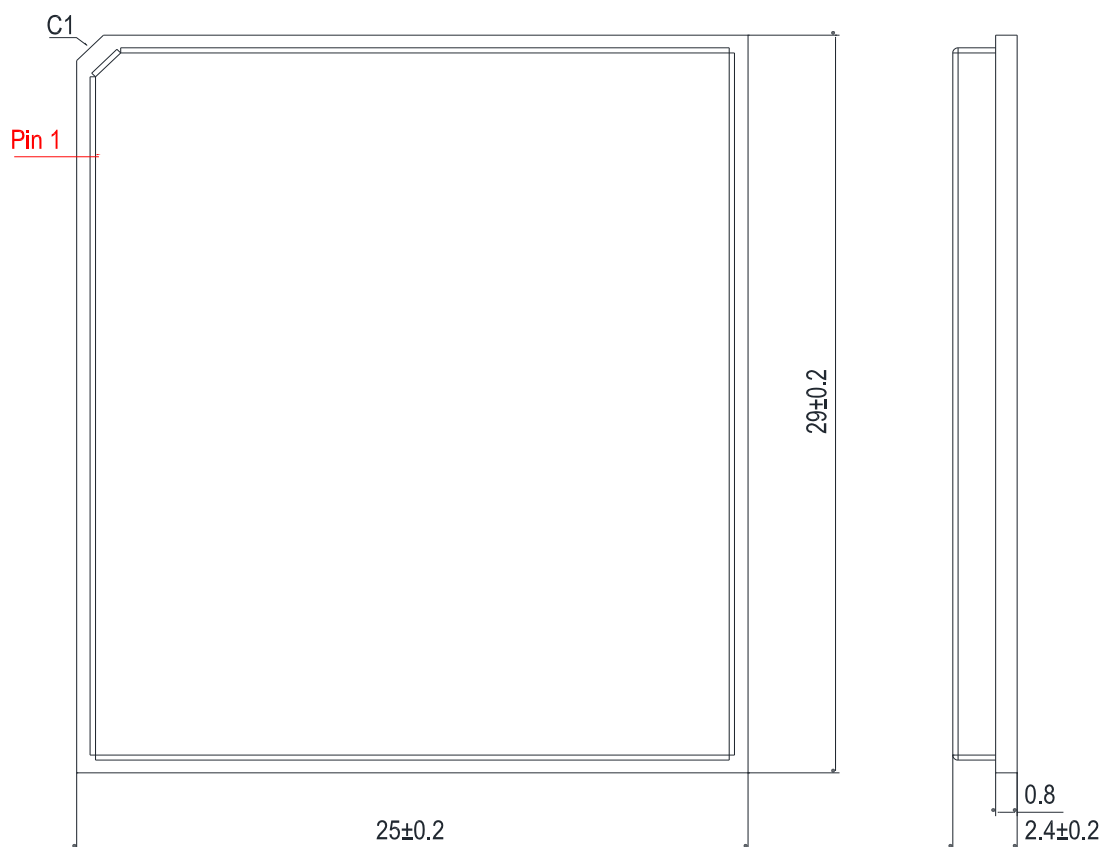


Figure 39: Module Top and Side Dimensions (Unit: mm)

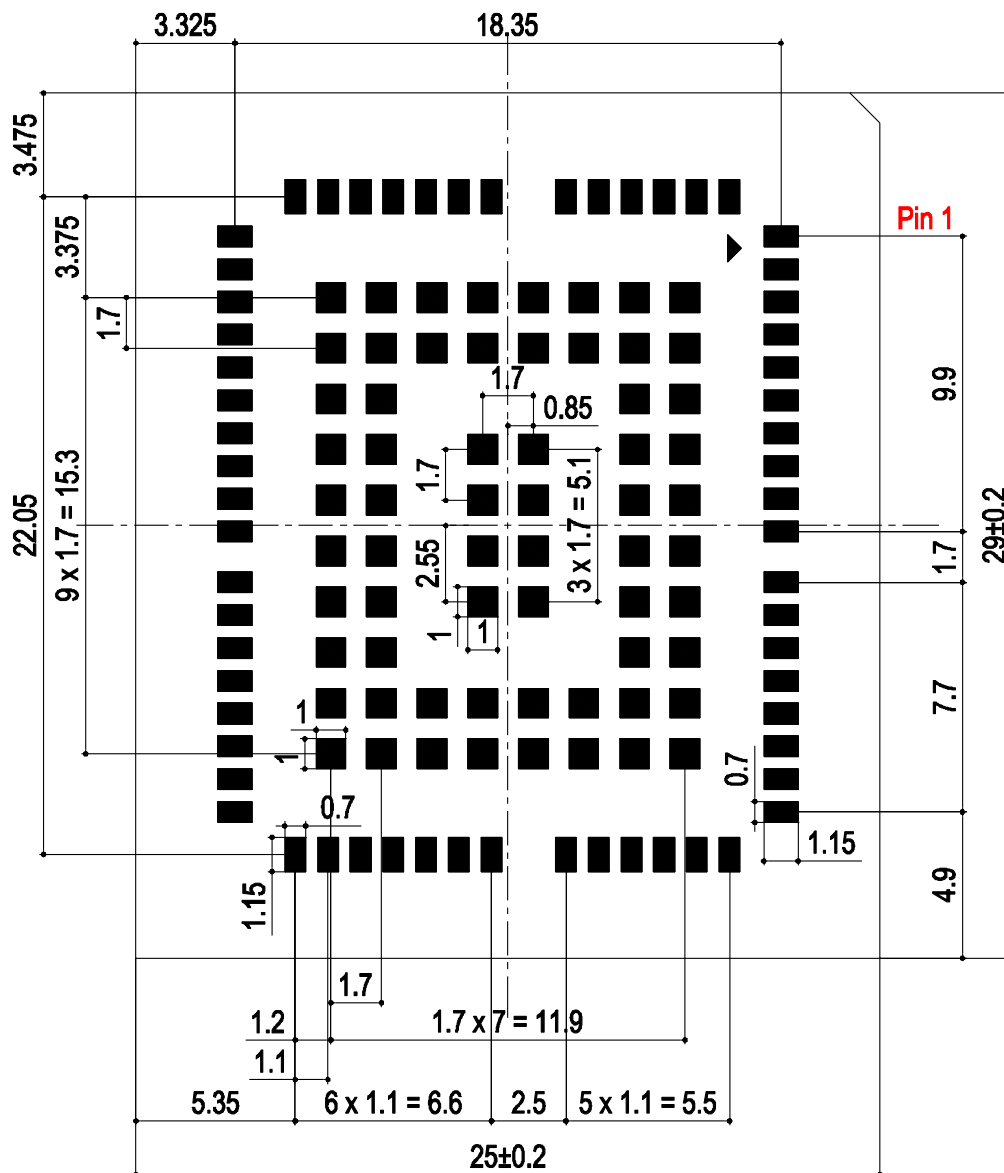
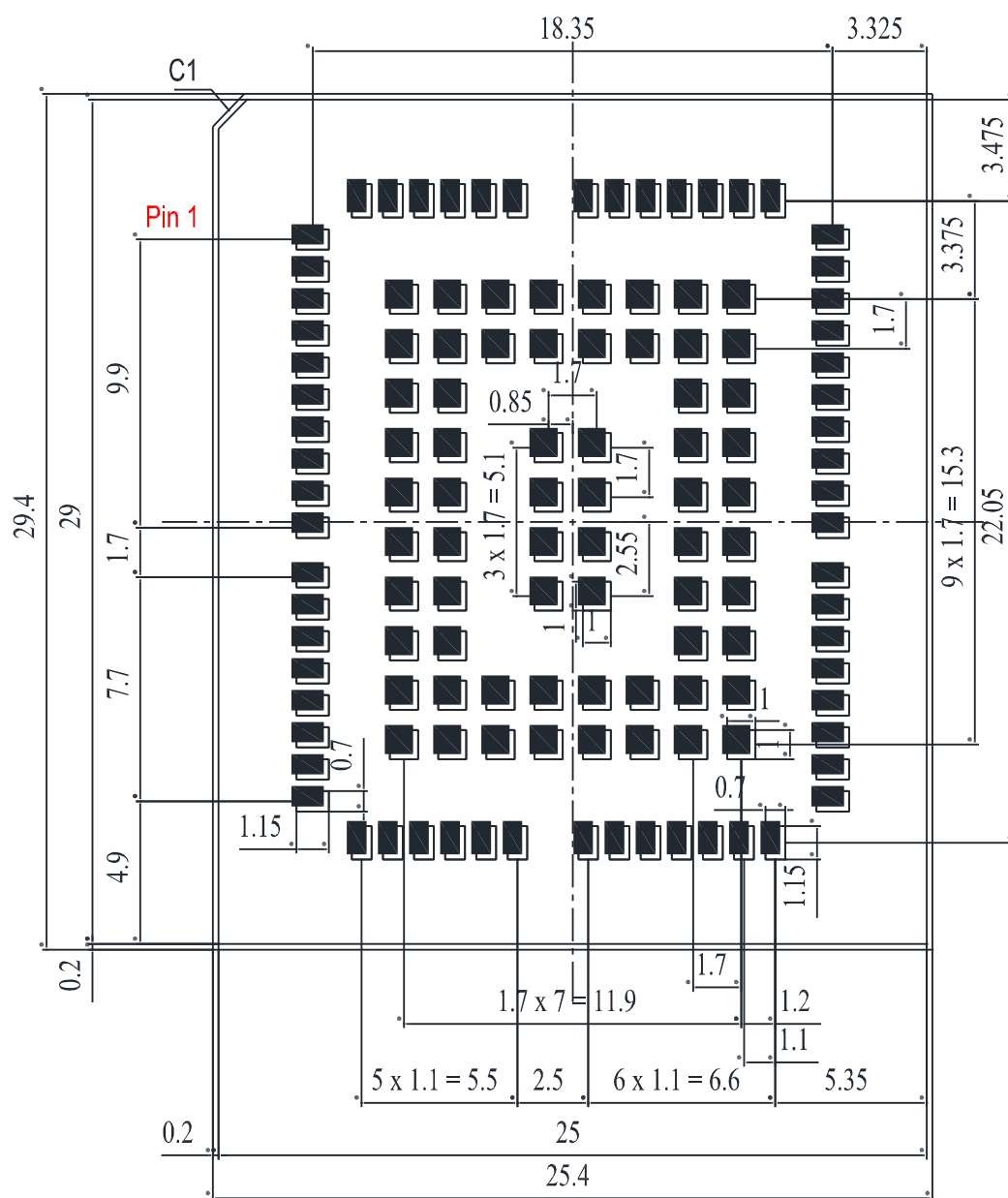


Figure 40: Bottom Dimension (Bottom View)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint



Unlabeled tolerance: +/-0.2mm

Figure 41: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

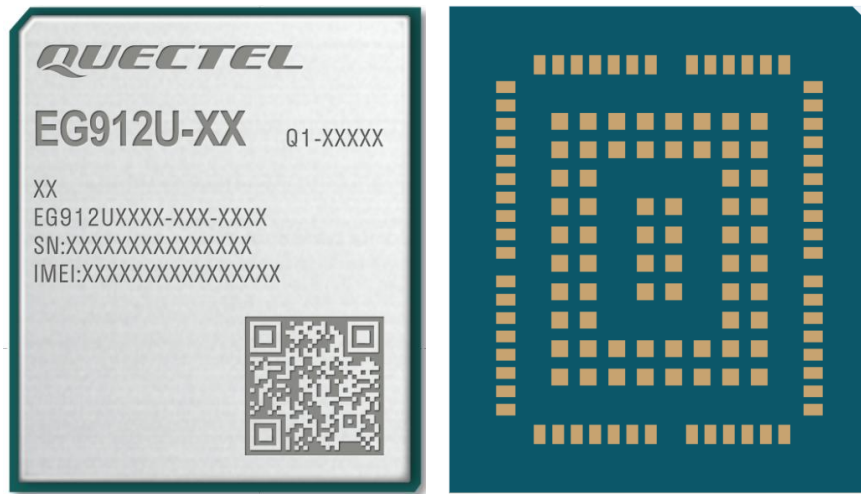


Figure 42: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing, and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours ⁹ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 24 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

⁹ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see **document [6]**.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

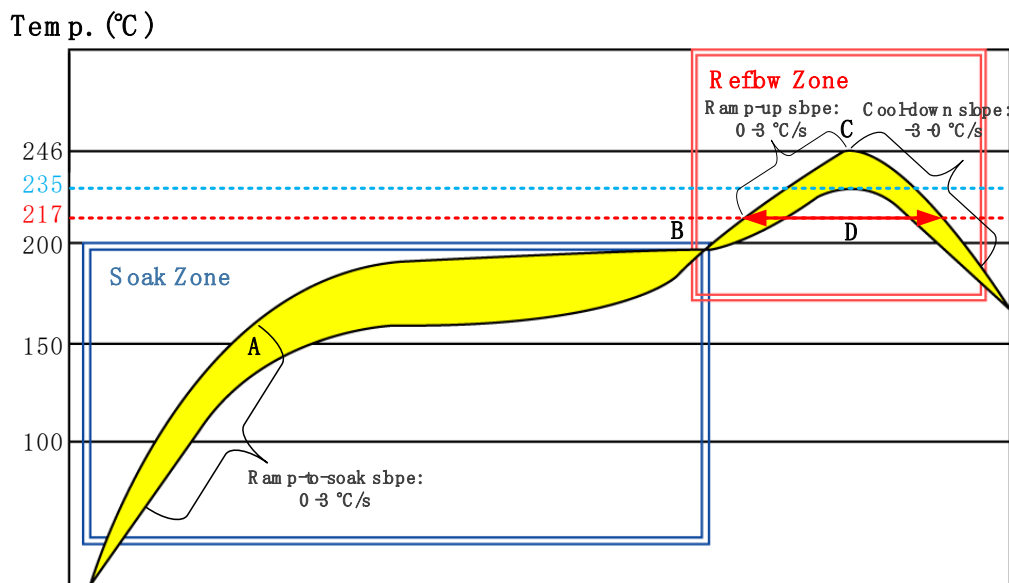


Figure 43: Recommended Reflow Soldering Thermal Profile

Table 48: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic

soldering) that is not mentioned in *document [7]*.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

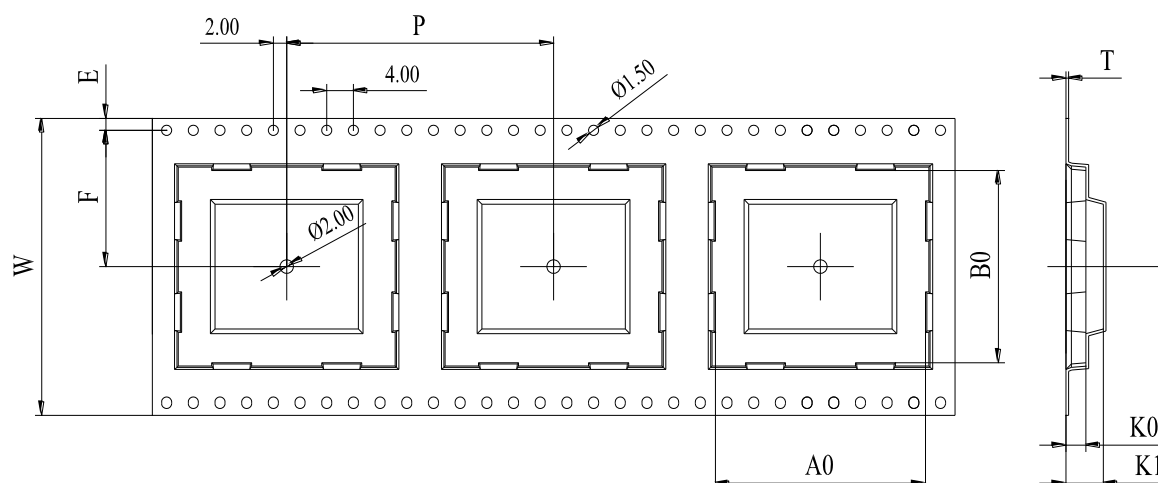


Figure 44: Carrier Tape Dimension Drawing (Unit: mm)

Table 49: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

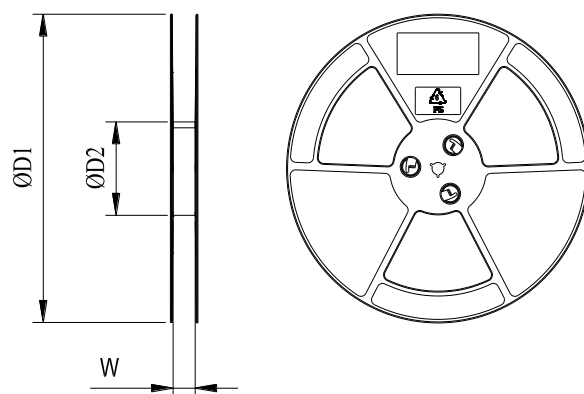


Figure 45: Plastic Reel Dimension Drawing

Table 50: Plastic Reel Dimension Table (Unit: mm)

ØD1	ØD2	W
330	100	44.5

8.3.3. Mounting Direction

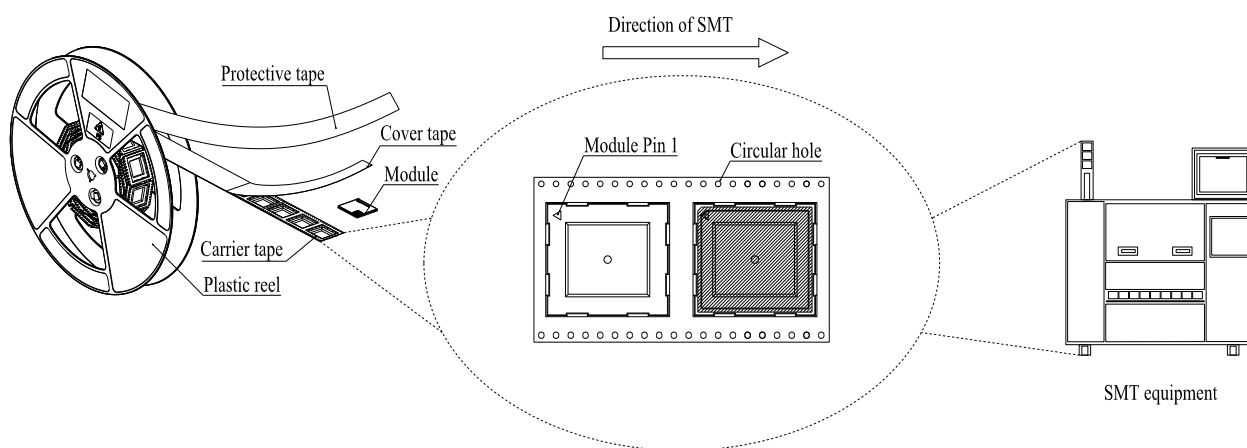
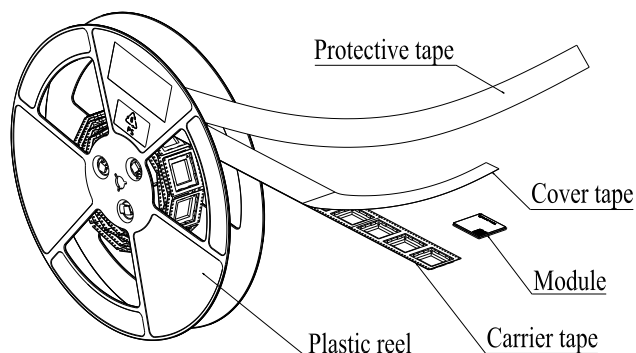


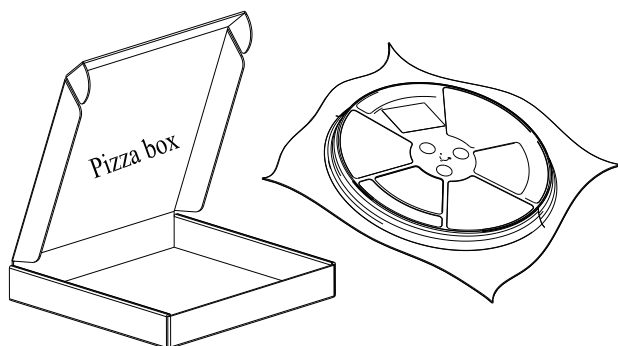
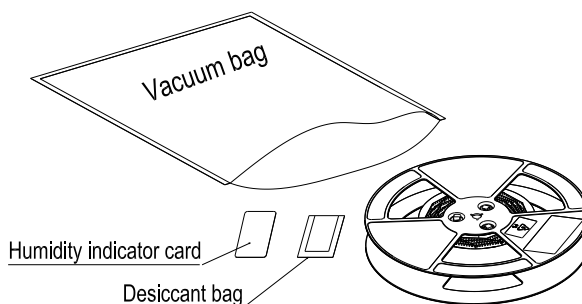
Figure 46: Mounting Direction

8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

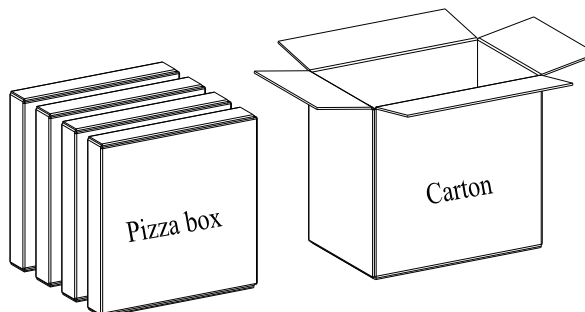


Figure 47: Packaging Process

9 Appendix References

Table 51: Related Documents

Document Name
[1] Quectel_EC200U_Series&EG912U-GL_GNSS_Application_Note
[2] Quectel_UMTS<E_EVB_User_Guide
[3] Quectel_EC200U&EG800G&EG91xU&EG915G_Series_AT_Commands_Manual
[4] Quectel_EC200U&EG800G&EG91xU&EG915G_Series_Low_Power_Mode_Application_Note
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_Stencil_Design_Requirements
[7] Quectel_Module_SMT_User_Guide

Table 52: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
BDS	BeiDou Navigation Satellite System
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
C _j	junction capacitance

CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL / FTP Secure
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GRFC	General RF Control
GSM	Global System for Mobile Communications
HB	High Band

HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000
I/O	Input/Output
LB	Low Band
LDO	Low-dropout Regulator
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long-Term Evolution
MB	Medium Band
MCU	Microcontroller Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Levels
NITZ	Network Identity and Time Zone/Network Informed Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation

PDU	Protocol Data Unit
PING	Packet Internet Groper
PMU	Power Management Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RTS	Ready To Send/Request to Send
SAW	Surface Acoustic Wave
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
Tx	Transmit/Transmission
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink

UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V _{max}	Maximum Voltage Value
V _{nom}	Nominal Voltage Value
V _{min}	Minimum Voltage Value
V _{IH}	High-level Input Voltage
V _{IL}	Low-level Input Voltage
V _{OH}	High-level Output Voltage
V _{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID XMR2023EG912UEAL procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: XMR2023EG912UEAL"

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

- (1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
- (2) The transmitter module may not be co-located with any other transmitter or antenna.
- (3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Gain	GSM: GSM850: 2.13dBi PCS1900: 1.59dBi LTE: LTE Band 2: 1.59dBi LTE Band 4: 2.00dBi LTE Band 5: 2.13dBi LTE Band 7: 3.00dBi LTE Band 38: 2.06dBi LTE Band 41: 3.00dBi LTE Band 66: 2.00dBi
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In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.247 & 15.209 & 15.407.

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 3.00dBi antenna. The host manufacturer installing this module into their product must ensure that the final compos it product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules,

including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

2.4 Limited module procedures

Not applicable. The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable. The module has its own antenna, and doesn't need a host's printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and user's body; and if RF exposure statement or module layout is changed, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: External Antenna

Gain: 3.00 dBi Max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a "unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2023EG912UEAL " with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, etc. according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15.209 & 15.407 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.