EG915Q-NA

Hardware Design

LTE Standard Module Series

Version: 1.0

Date: 2023-02-07

Status: Released

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-11-28	Lex LI/Lena HUANG	Creation of the document
1.0	2023-02-07	Lex LI/Barry DENG	First official release

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1 Introduction

This document describes the EG915Q-NA features, performance, and air interfaces and hardware interfaces connected to your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, and other module information, as well.

1.1. Special Marks

Table 1: Special Marks

Marks	Definitions
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

EG915Q-NA is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M and IoT applications, such as asset management, commercial telematics, payment, RMAC (Remote Monitoring and Control applications), security and automation, smart metering and smart grid.

Table 2: Basic Information

EG915Q-NA	
Packaging type	LGA
Pin counts	126
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 2.3 g

2.1. Frequency Bands

Table 3: Frequency Bands

Network Type	EG915Q-NA
LTE-FDD	B2/B4/B5/B12/B13/B66

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Supply Voltage	● 3.3–4.3 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interface	1.8 V and 3.0 V
PCM Interface*	● Supports one digital audio interface: PCM interface ● Used for audio function with external Codec
I2C Interface*	● One I2C interface ● Comply with I2C-bus specification
SPI Interface*	● One SPI ● 1.8 V voltage domain ● Clock rate: up to 25.6 MHz
Camera SPI Interface*	● Supports one camera SPI Interface ● Supports the 2-data-line transmission of SPI
USB Interface	● Compliant with USB 2.0 specifications (only supports slave mode) ● Data rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrade and the output of partial logs ● USB serial driver: supports USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.18*, Android 4.x–12.x* systems
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs ● Baud rate: up to 3 Mbps, 115200 bps by default
Network Indication	**NET_STATUS:** ● Use: network connectivity status indication
AT Commands	● Complies with the AT commands defined in *3GPP TS 27.007* and *3GPP TS 27.005* ● Complies with Quectel enhanced AT commands
Antenna Interface	● Main antenna interface (ANT_MAIN) ● 50 Ω characteristic impedance

Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Complies with 3GPP Rel-14 FDD ● Max. LTE category: Cat 1 bis ● 1.4/3/5/10/15/20 MHz RF bandwidth ● DL modulations: QPSK, 16QAM and 64QAM ● UL modulations: QPSK, 16QAM ● LTE-FDD max. data rates: – DL: 10 Mbps – UL: 5 Mbps
Internet Protocol Features	● Complies with TCP, UDP, PPP, NTP, NITZ, FTP, HTTP, PING, CMUX*, HTTPS, FTPS, SSL, FILE, MQTT protocols ● Complies with PPP protocol's PAP and CHAP authentication
Temperature Ranges	● Normal operating temperature [1]: -35 °C to +75 °C ● Extended operating temperature [2]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Via USB 2.0 interface or DFOTA
RoHS	All hardware components fully comply with EU RoHS directive

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Radio frequency part
- Peripheral interfaces

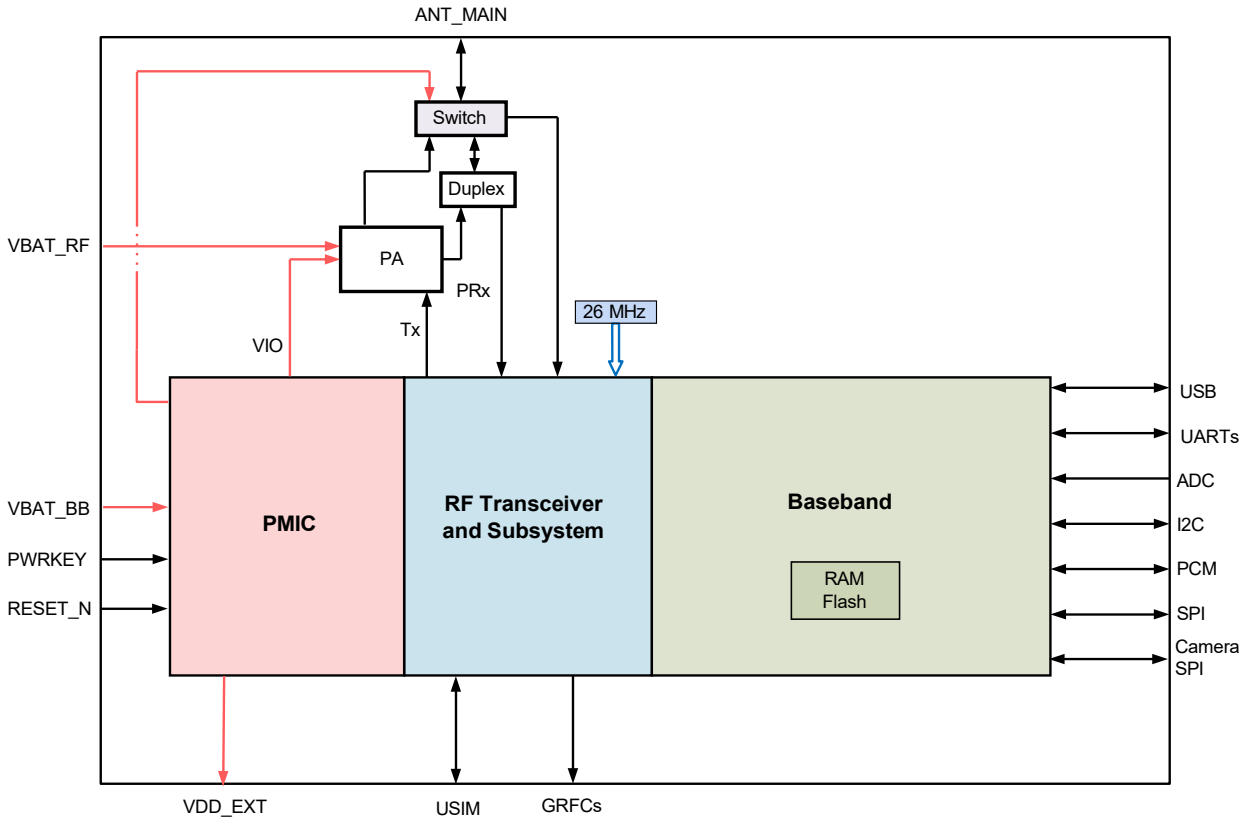


Figure 1: Functional Diagram

2.4. Pin Assignment

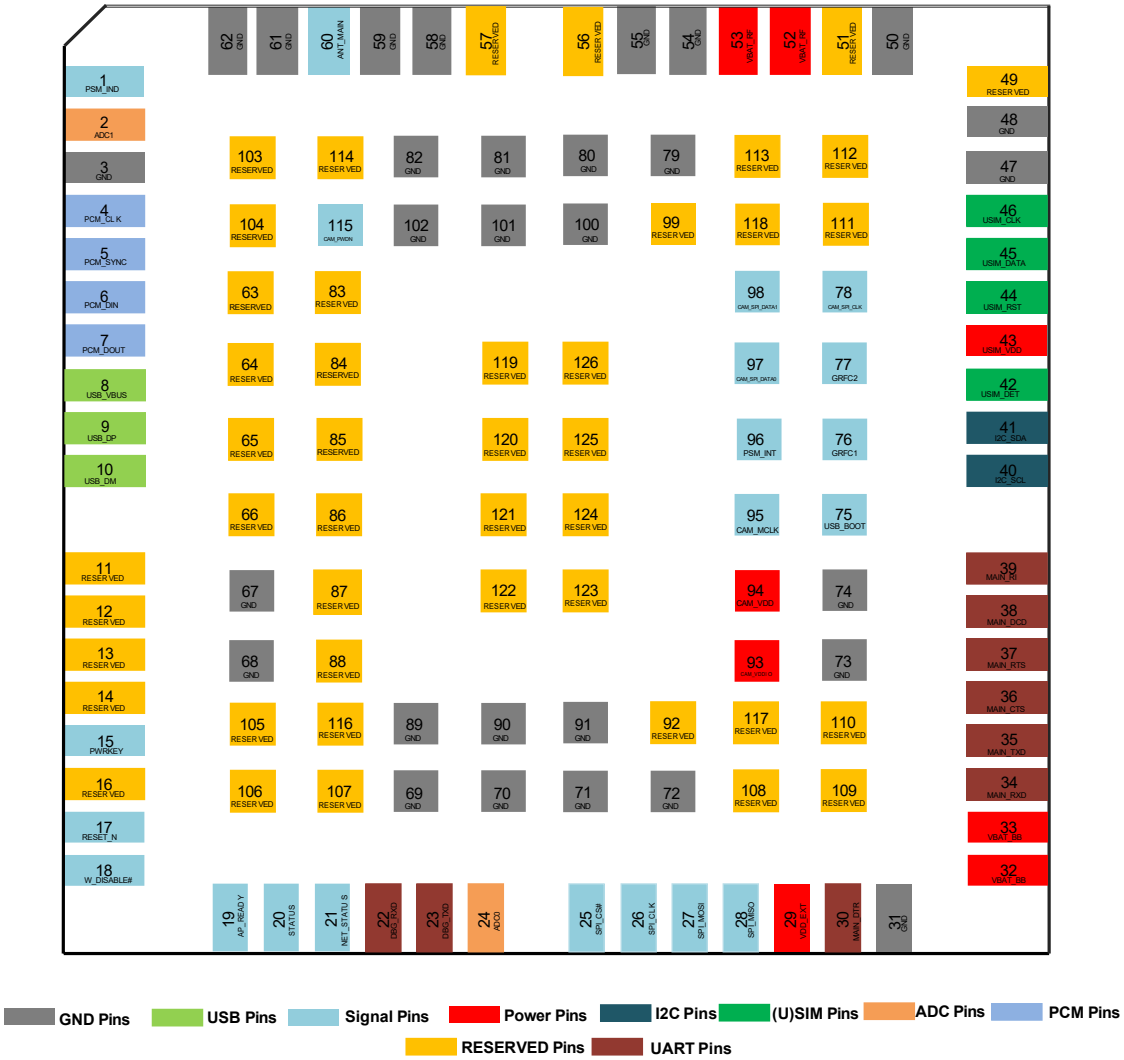


Figure 2: Pins Assignment (Top View)

NOTE

1. If the module does not need to enter emergency download mode, USB_BOOT (pin 75) should not be pulled up to VDD_EXT before the module successfully starts up.
2. In sleep mode, some pins of the main UART interface (pins 34–37), debug UART interface (pins 22, 23), USB_BOOT (pin 75), PCM interface* (pins 4–7), I2C interface* (pins 40, 41), and SPI interface* (pins 25-28) are powered down. The driving capacity will be lost and the functions of status indication and data transmission are disabled. Pay attention to it when designing circuits.
3. Keep all RESERVED pins and unused pins unconnected.

2.5. Pin Description

The following table shows the pin descriptions. DC characteristics include power domain, rate current, etc.

Table 5: Parameter Definition

Parameters	Descriptions
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of 0.5 A at least.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 1.5 A.
VDD_EXT	29	PO	Provides 1.8 V for external circuit	Vnom = 1.8 V I_{o} max = 50 mA	Power supply for external GPIO's pull-up circuits. It is recommended to reserve test points.
GND	3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn On/Off					

Pin Name	Pin No.	I/O	Description	DC Characteristic	Comment
PWRKEY	15	DI	Turns on/off the module	V_{IL}max = 0.5 V	Active low.
RESET_N	17	DI	Resets the module		Active low. Test points are recommended to be reserved if unused.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
STATUS	20	DO	Indicates the module's operation status	VDD_EXT	If unused, keep them open.
NET_STATUS	21	DO	Indicates the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Test points must be reserved.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)		
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USIM_VDD	43	PO	USIM card power supply	$I_O$max = 50 mA **Low-voltage:** Vmax = 1.85 V Vmin = 1.75 V **High-voltage:** Vmax = 3.05 V Vmin = 2.95 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DATA	45	DIO	USIM card data	USIM_VDD	
USIM_CLK	46	DO	USIM card clock		

USIM_RST	44	DO	USIM card reset		
USIM_DET	42	DI	USIM card hot-plug detect	VDD_EXT	If unused, keep it open.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
MAIN_CTS	36	DO	DTE clear to send signal from DCE	VDD_EXT	Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	37	DI	DTE request to send signal to DCE		Connect to DTE's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive		If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect		
MAIN_TXD	35	DO	Main UART transmit		
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
DBG_RXD	22	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit		
I2C Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
I2C_SCL	40	DO	I2C serial clock	VDD_EXT	External pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	DIO	I2C serial data		
PCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**

PCM_SYNC	5	DO	PCM data frame sync	VDD_EXT	If unused, keep them open.
PCM_CLK	4	DO	PCM clock		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
ANT_MAIN [3]	60	AIO	Main antenna interface		50 Ω impedance.
GRFC Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
GRFC1	76	DO	Generic RF controller	VDD_EXT	If unused, keep them open.
GRFC2	77	DO	Generic RF controller		
Camera SPI Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
CAM_MCLK	95	DO	Master clock of the camera	VDD_EXT	If unused, keep them open.
CAM_SPI_CLK	78	DI	Camera SPI clock		
CAM_SPI_DATA0	97	DI	Camera SPI data bit 0		
CAM_SPI_DATA1	98	DI	Camera SPI data bit 1		
CAM_PWDN	115	DO	Power down of the camera		
CAM_VDD	94	PO	Camera analog power supply	Vnom = 2.8 V	
CAM_VDDIO	93	PO	Camera digital power supply	VDD_EXT	
SPI Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
SPI_CLK	26	DO	SPI clock	VDD_EXT	If unused, keep them

[3] ANT_MAIN only supports passive antennas.

SPI_CS	25	DO	SPI chip selection		open.
SPI_MISO	28	DI	SPI master-in slave-out		
SPI_MOSI	27	DO	SPI master-out slave-in		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0–1.2 V	If unused, keep them open.
ADC1	2	AI	General-purpose ADC interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USB_BOOT	75	DI	Forces the module into emergency download mode		Active high before power-up. Test points must be reserved.
W_DISABLE#*	18	DI	Airplane mode control		
PSM_IND*	1	DO	Indicates the module's power saving mode	VDD_EXT	
PSM_INT*	96	DI	External interrupt; wakes up the module from power saving mode		If unused, keep them open.
AP_READY*	19	DI	Application processor ready		
RESERVED Pins					
Pin Name	**Pin No.**				**I/O**
RESERVED	11–14, 16, 49, 51, 56, 57, 63–66, 83–88, 92, 99, 103–114, 116–126				Keep these pins open.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Operating Modes Overview

Modes	Descriptions	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but has no data interaction with the network.
	Data	Network connection is ongoing. Power consumption is decided by network setting and data rate.
Minimum Functionality Mode	● **AT+CFUN=0** can set the module to the minimum functionality mode when the power is on. ● Both RF function and USIM card will be invalid.	
Airplane Mode	● **AT+CFUN=4** or driving W_DISABLE#* low can set the module to airplane mode. ● RF function will be invalid.	
Sleep Mode	Power consumption of the module will be reduced to a minimal level. The module can still receive paging, SMS and TCP/UDP data from the network.	
Power Down Mode	The VBAT_BB and VBAT_RF pins are constantly turned on and the software stops working.	

NOTE

For more details about **AT+CFUN**, see ***document [2]***.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to a minimal level.

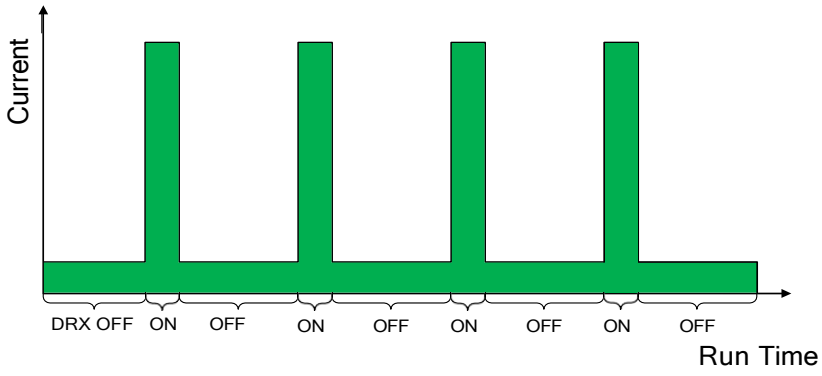


Figure 3: Power Consumption During Sleep Mode

3.2.1. UART Application Scenario

If the module communicates with the host via main UART, both the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**. For more details, see ***document [2]***.
- Ensure MAIN_DTR is held high or is kept unconnected.

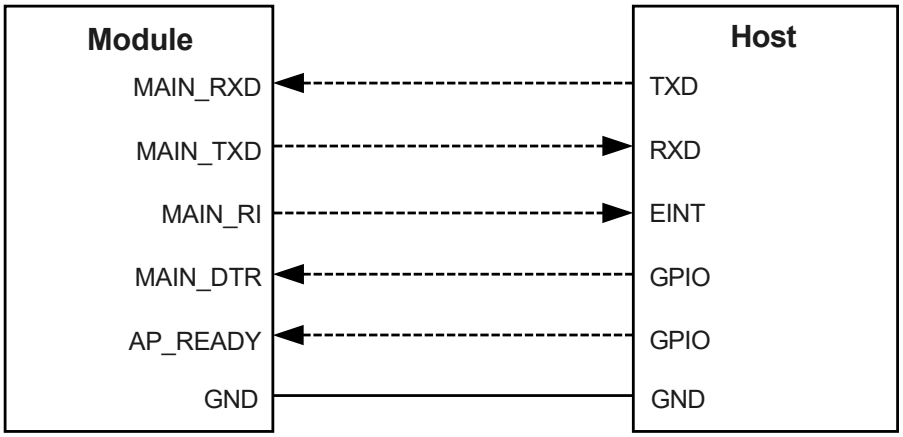


Figure 4: Sleep Mode Application via UART

- Driving MAIN_DTR low with the host will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the host. See ***Chapter 4.11.3*** for details about MAIN_RI.

3.2.2. USB Application Scenarios*

For the two situations ("USB application with USB remote wakeup function" and "USB application with USB suspend/resume and MAIN_RI function") below, three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters suspend state.

3.2.2.1. USB Application with USB Suspend/Resume and Remote Wakeup Function

The following figure illustrates the connection between the module and the host when the host supports USB suspend, resume and remote wakeup function.

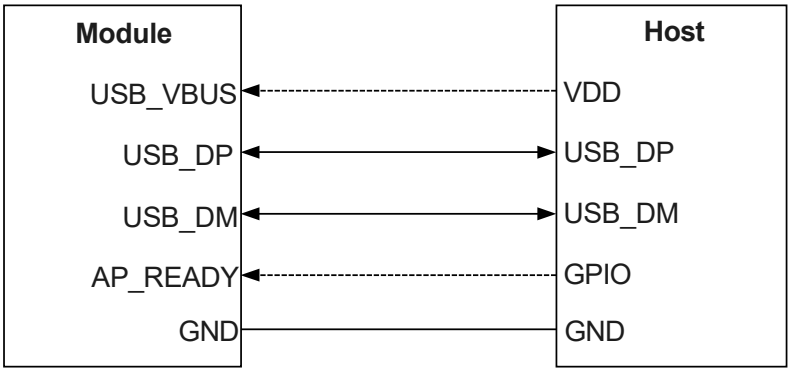


Figure 5:Sleep Mode Application with USB Suspend/Resume and Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

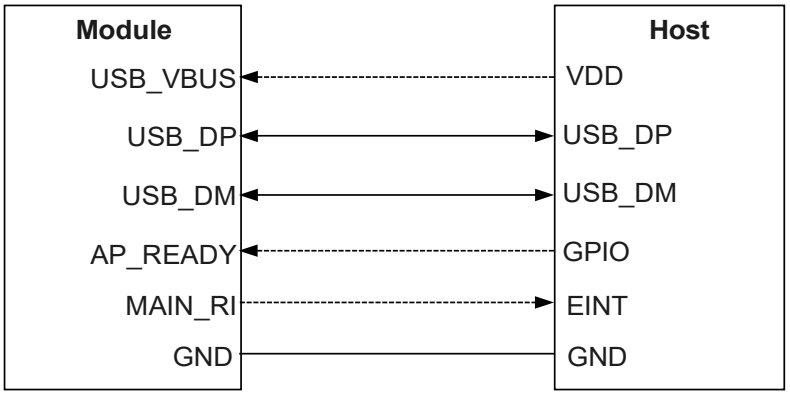


Figure 6: Sleep Mode Application with USB Suspend/Resume and MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal. See ***Chapter 4.11.3*** for details about MAIN_RI behavior.

3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure USB_VBUS is disconnected via the external control circuit.

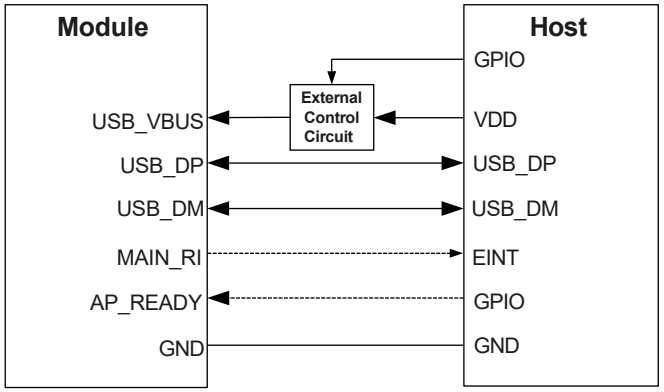


Figure 7: Sleep Mode Application without USB Suspend

Restore the power supply of USB_VBUS will wake up the module.

NOTE

Pay attention to the level match shown in the dotted line between the module and the host.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following methods.

Hardware:

W_DISABLE#* is pulled up by default. Driving it low makes the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level via setting **<fun>** to 0, 1 or 4. For more details, see ***document [2]***.

- **AT+CFUN=0**: Minimum functionality mode. (Both USIM and RF functions are disabled.)
- **AT+CFUN=1**: Full functionality mode. (By default.)
- **AT+CFUN=4**: Airplane mode. (RF function is disabled.)

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides four VBAT pins dedicate to connecting with the external power supply:

Table 8: Pin Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Units
VBAT_BB	32, 33	PI	Power supply for the module's BB part	3.3	3.8	4.3	V
VBAT_RF	52, 53	PI	Power supply for the module's RF part	3.3	3.8	4.3	V
VDD_EXT	29	PO	Provide 1.8 V for external circuit	-	1.8	-	V
GND	3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of 2 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for +5 V input power supply. The circuit is designed using the LDO of Microchip's MIC29302WU.

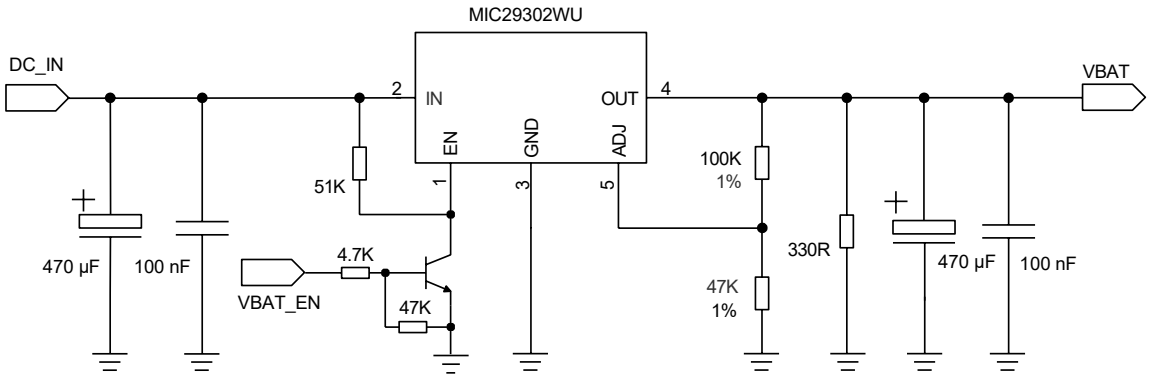


Figure 8: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Voltage Stability Requirements

The power supply range of the module is 3.3–4.3 V. Ensure the input voltage never drops below 3.3 V.

To decrease the voltage drop, use a bypass capacitor of about 100 µF with low ESR for VBAT_BB and VBAT_RF respectively and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use three ceramic capacitors (100 nF, 33 pF and 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT pins. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths with the star configuration. The width of VBAT_BB trace and VBAT_RF trace should be at least 1 mm and 2 mm respectively. In principle, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and to ensure the stability of the power supply to the module, it is

recommended to add a TVS with V_{RWM} = 4.7 V, low clamping voltage and high reverse peak pulse current Ipp at the front end of the power supply.

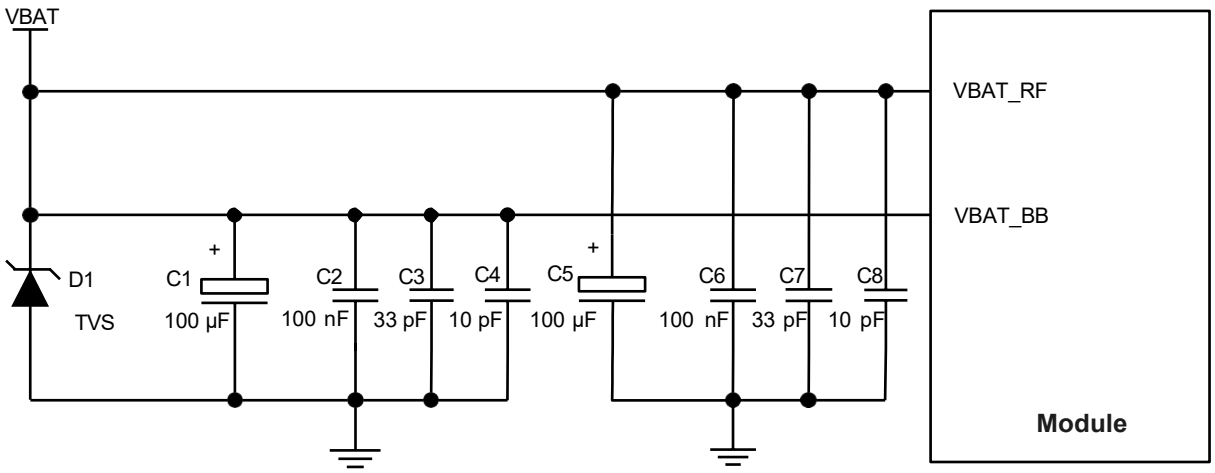


Figure 9: Reference Design of Power Supply

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	Active low.

When the module is in power-down mode, it can be turned on by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

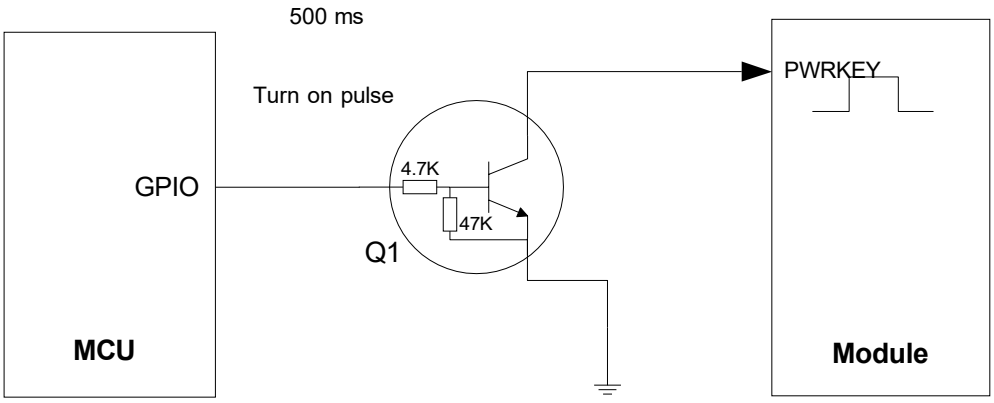


Figure 10: Reference Design of Turn On with Driving Circuit

Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the keystroke for ESD protection.

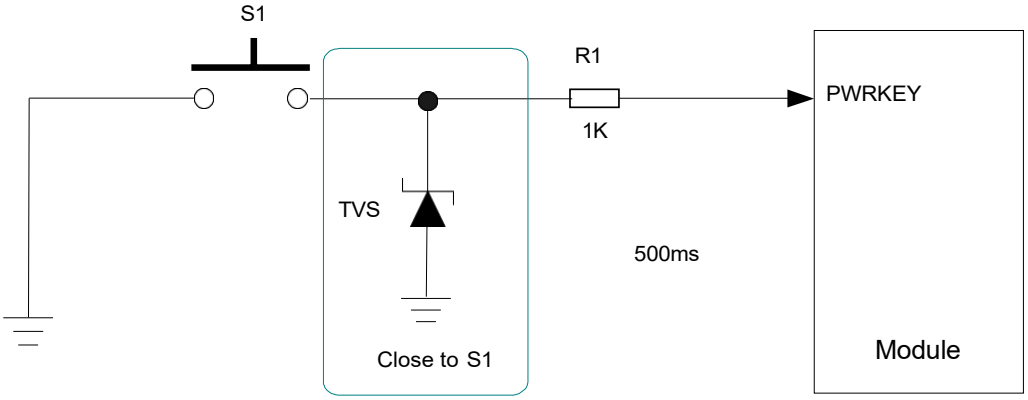


Figure 11: Reference Design of Turn On with Keystroke

The power-up timing is illustrated in the following figure.

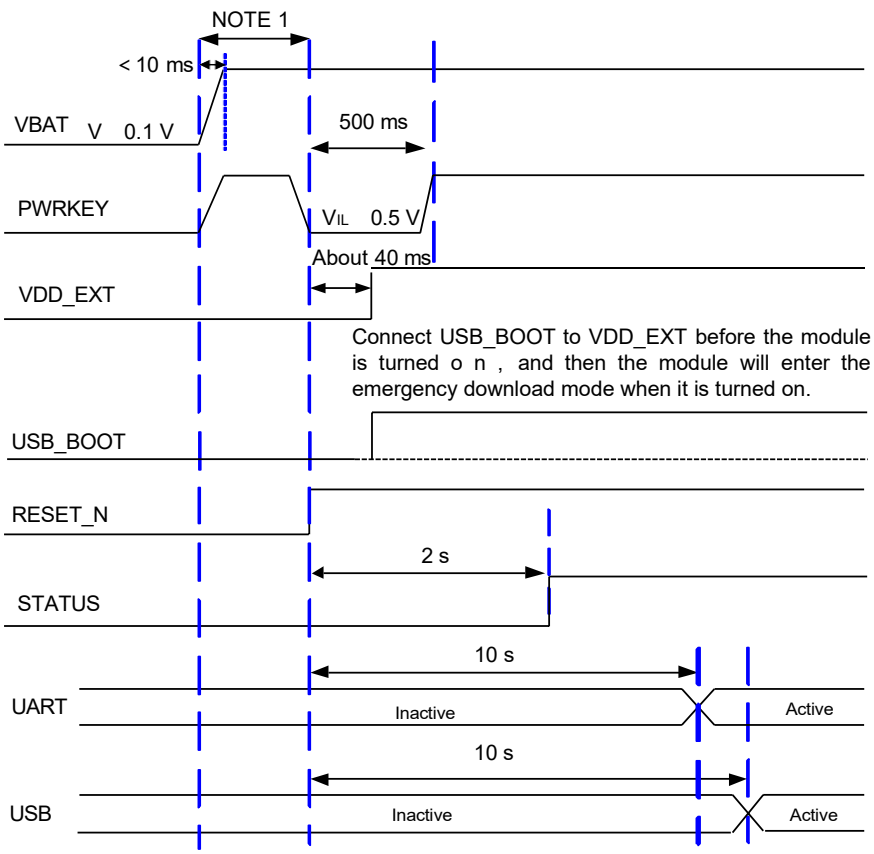


Figure 12: Power-up Timing with PWRKEY

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need the turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn Off

The following procedures can be used to turn off the module normally.

3.6.1. Turn Off with PWRKEY

Drive the PWRKEY low for at least 650 ms and then release it. Then, the module will execute the turn-off procedure.

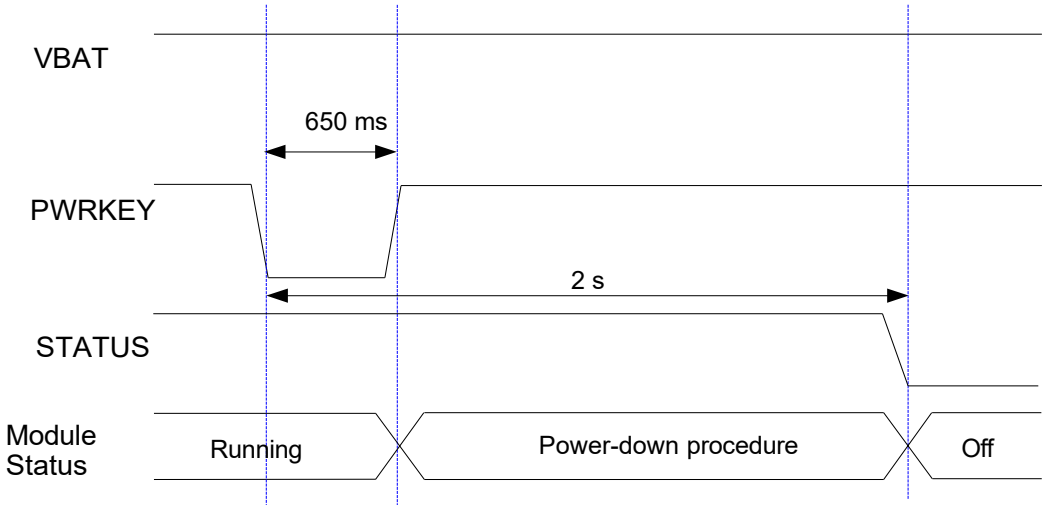


Figure 13: Power-down Timing with PWRKEY

3.6.2. Turn Off with AT Command

For proper shutdown procedure, execute **AT+QPOWD**, which has similar timing and effect as turning off the module through driving PWRKEY low. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

3.7. Reset

The reset function requires the PWRKEY and RESET_N pins to work together to complete. Pulling down PWRKEY when RESET_N is at low level can reset the module. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Active low. Test points are recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N and PWRKEY pins.

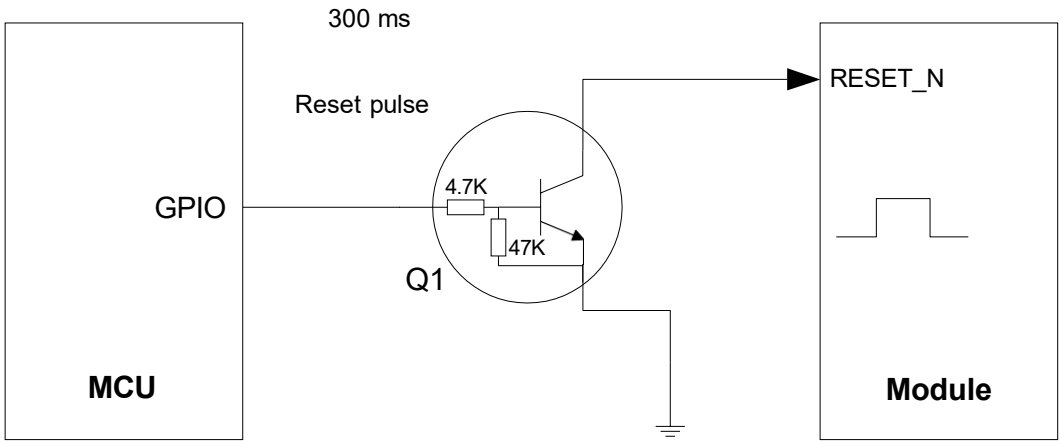


Figure 14: Reference Design of Reset with Driving Circuit

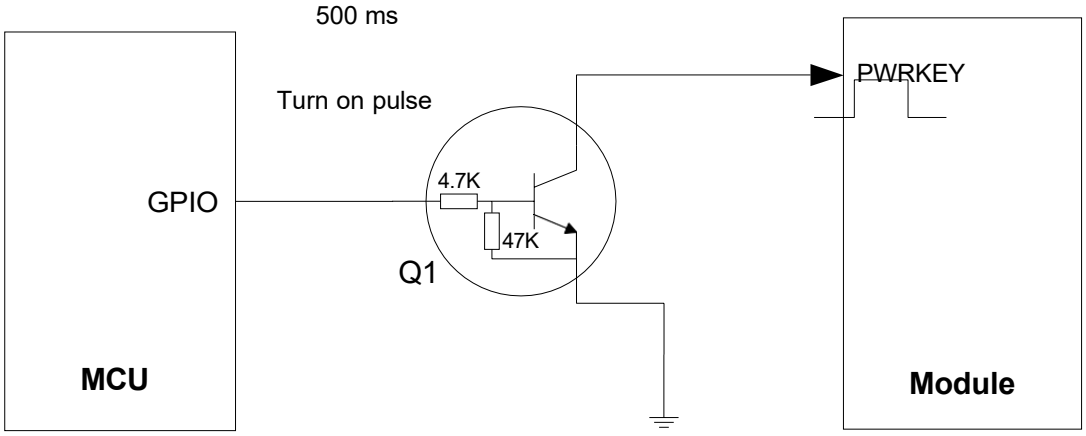


Figure 15: Reference Design of PWRKEY with Driving Circuit

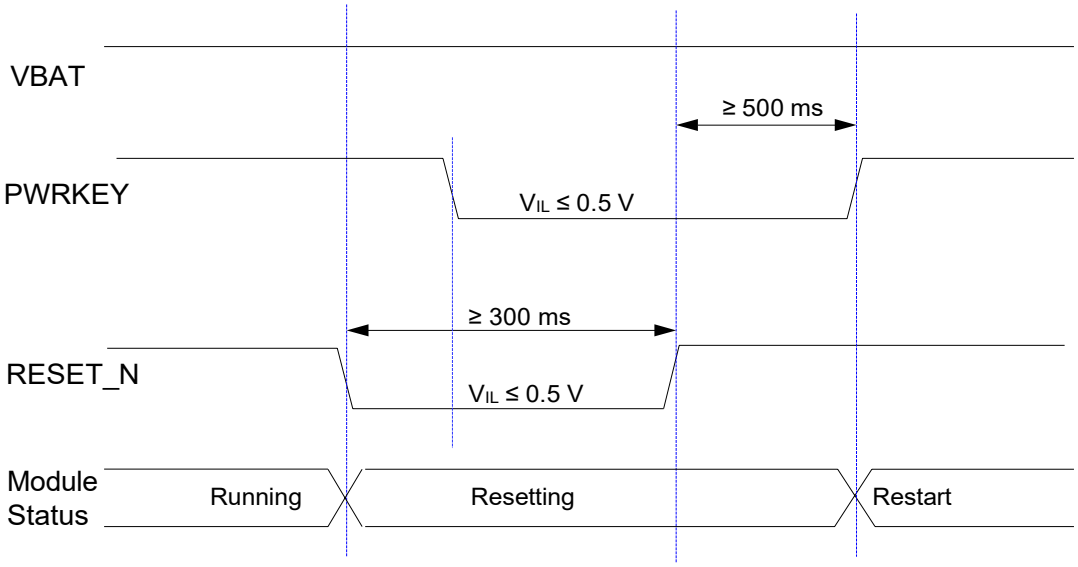


Figure 16: Reset Timing

NOTE

1. In reset timing, pull down PWRKEY when RESET_N is at low level.
2. Ensure the capacitance on PWRKEY and RESET_N is not more than 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports high-speed (480 Mbps) and full-speed (12 Mbps) for USB 2.0. The module only supports USB slave mode. The USB interface can be used for AT command communication, data transmission, software debugging, firmware upgrade and the output of partial logs.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Test points must be reserved.
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	

Test points of USB 2.0 interface must be reserved, which can be used for firmware upgrading and debugging.

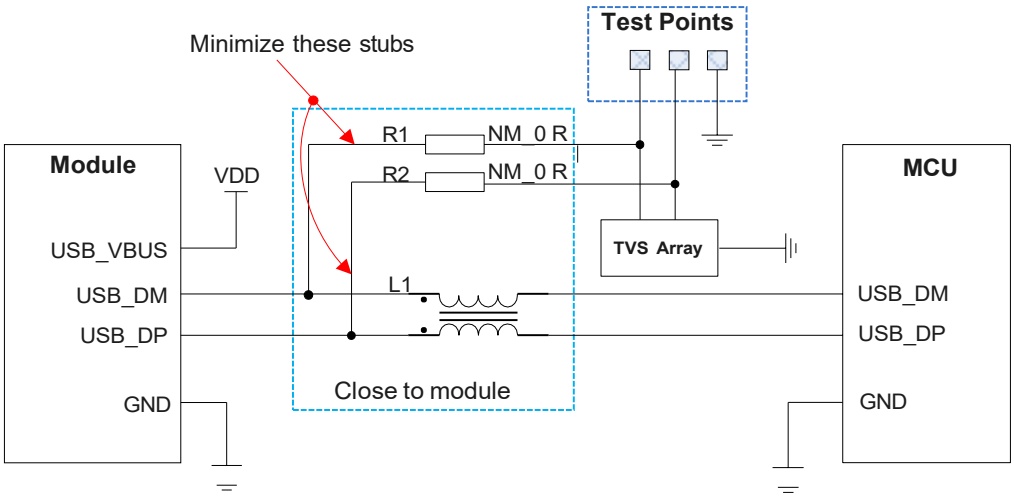


Figure 17: Reference Design of USB 2.0 Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI spurious transmission. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, you should place L1, R1 and R2 close to the module, and keep these resistors close to each other. Moreover, keep extra stubs of trace as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. For signal traces, provide clearance from VBAT traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 2 pF for USB 2.0.
- Keep the ESD protection components as close to the USB port as possible.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. USB_BOOT

The module provides a USB_BOOT pin for emergency download. Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 12: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Forces the module into emergency download mode	Active high before power-up. Test points must be reserved.

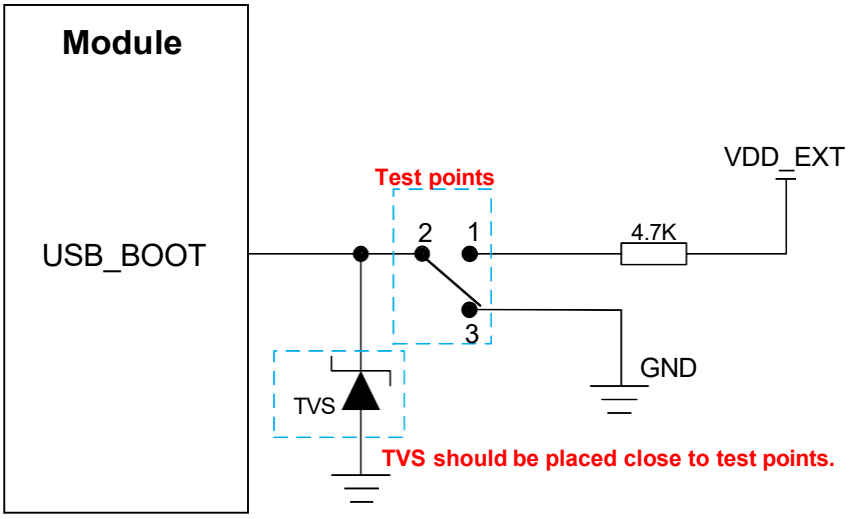


Figure 18: Reference Design of USB_BOOT

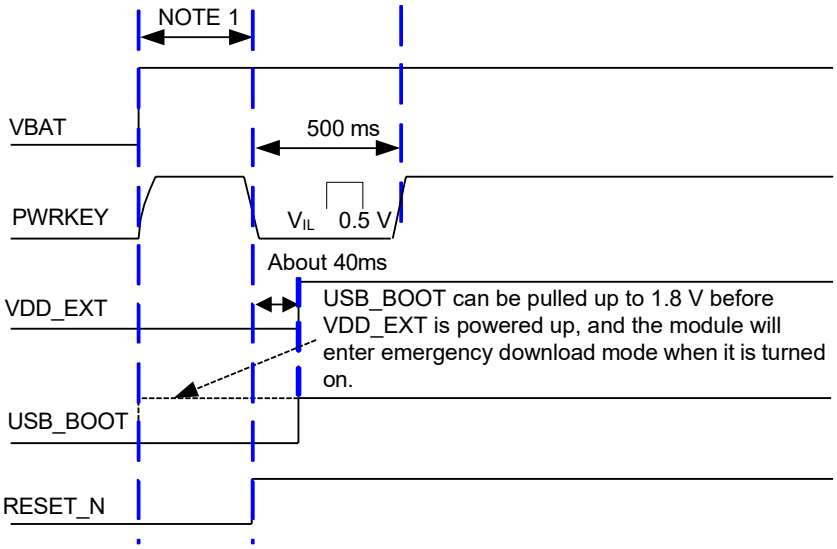


Figure 19: Timing of Entering Emergency Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low.
2. Follow the above timing when using MCU control the module to enter the emergency download mode.
3. If you need to manually force the module to enter emergency download mode, directly connect the test points shown in ***Figure 18***.

4.3. USIM Interface

The USIM interface meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported.

Table 13: Pin Description of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	43	PO	USIM card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DATA	45	DIO	USIM card data	
USIM_CLK	46	DO	USIM card clock	
USIM_RST	44	DO	USIM card reset	
USIM_DET	42	DI	USIM card hot-plug detect	If unused, keep it open.

The module supports USIM card hot-plug via the USIM_DET, and both high-level and low-level detections are supported. Hot-plug function is disabled by default and you can use **AT+QSIMDET** to configure this function. See ***document [2]*** for more details.

The following figure illustrates a reference design for USIM card interface with an 8-pin USIM card connector.

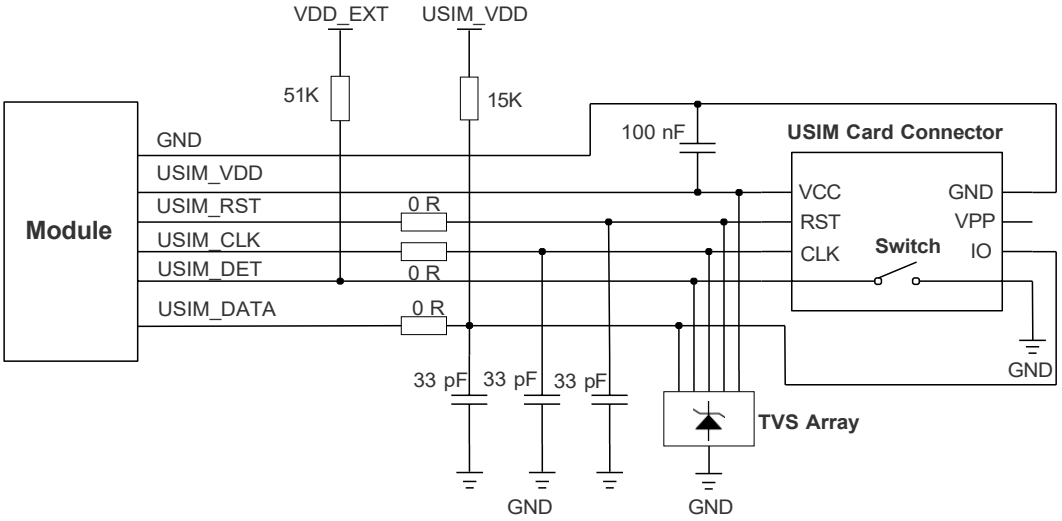


Figure 20: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the function of USIM card hot-plug is not needed, keep USIM_DET disconnected. A reference design for USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

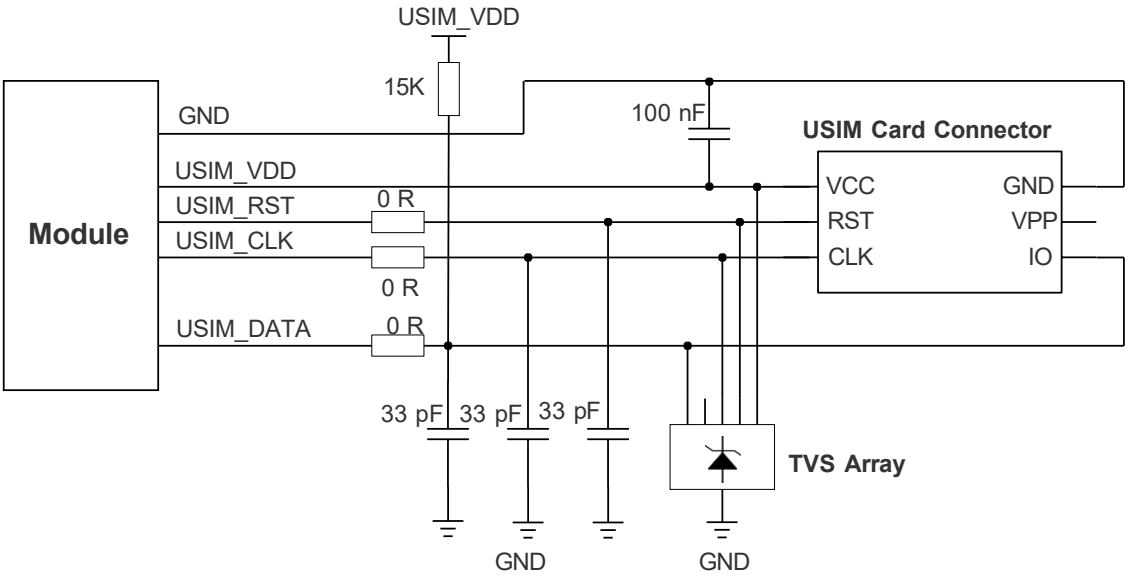


Figure 21: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the principles below in the USIM circuit design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible and at most 200 mm.
- Route USIM card differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from VBAT traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Ensure the tracing between the USIM card connector and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array of which parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. The 33 pF capacitors are used for filtering out RF interference. Additionally, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the USIM card connector.

4.4. UART Interfaces

The module serves as DCE (Data Communication Equipment), which is connected in the traditional DCE-DTE (Data Terminal Equipment) mode. The module provides two UART Interfaces.

Table 14: UART Information (Unit: bps)

UART Types	Supported Baud Rates	Default Baud Rates	Functions
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	AT command communication and data transmission
Debug UART	115200, 3000000	115200	The output of partial logs

Table 15: Pin Description of UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	DTE clear to send signal from DCE	Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	37	DI	DTE request to send signal to DCE	Connect to DTE's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	
DBG_RXD	22	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit	

The module provides 1.8 V UART interfaces. You can use a level-shifting chip between the module and host's UART if the host is equipped with a 3.3 V UART.

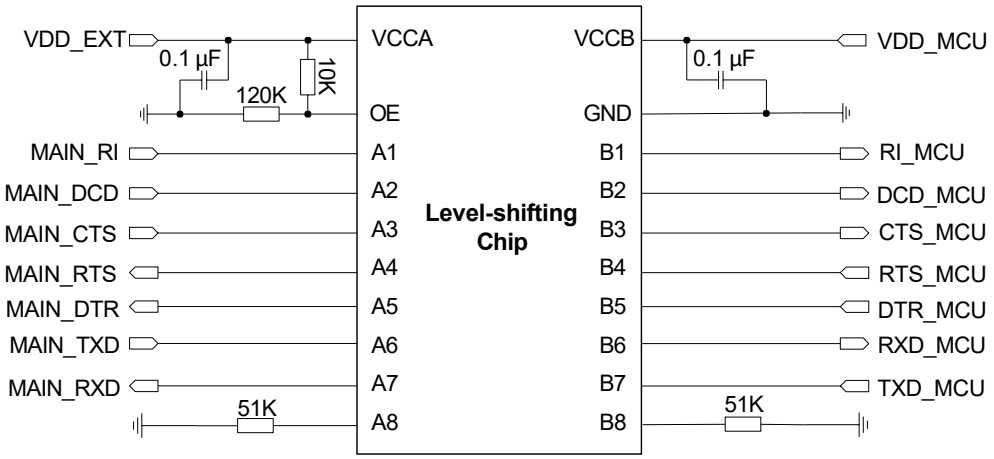


Figure 22: Reference Design of UART with Level-shifting Chip

Another example of level-shifting circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

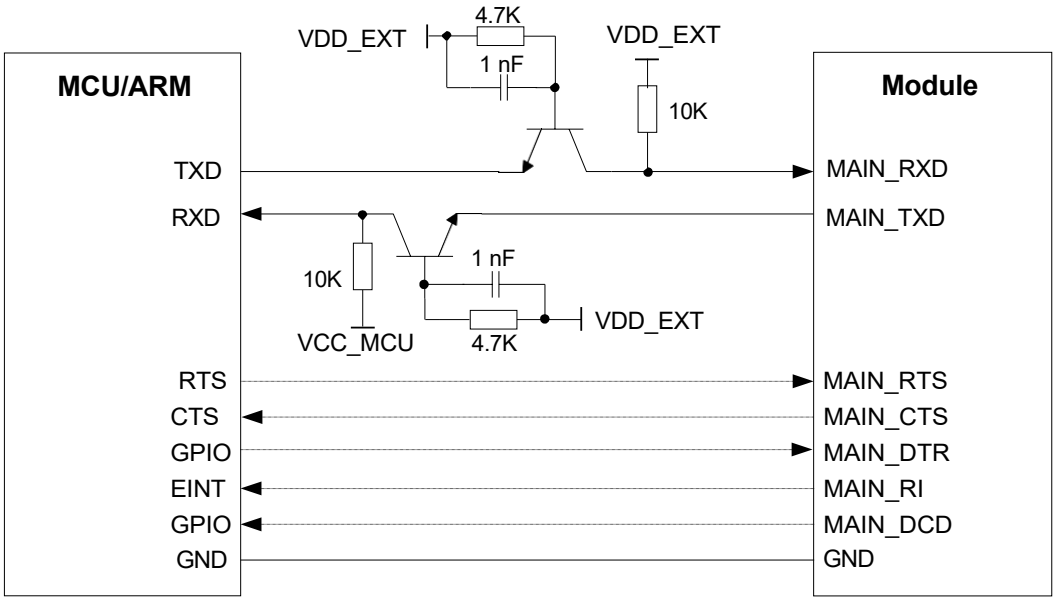


Figure 23: Reference Design of UART with Transistor Level-shifting Circuit

NOTE

1. Transistor circuit solution above is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module's CTS is connected to the host CTS, and the module's RTS is connected to the host RTS.

4.5. PCM and I2C Interfaces*

The module provides one Pulse Code Modulation (PCM) digital interface and one I2C interface.

Table 16: Pin Description of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	5	DO	PCM data frame sync	If unused, keep them open.
PCM_CLK	4	DO	PCM clock	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	DO	I2C serial clock	External pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	DIO	I2C serial data	

The reference design is illustrated as follows.

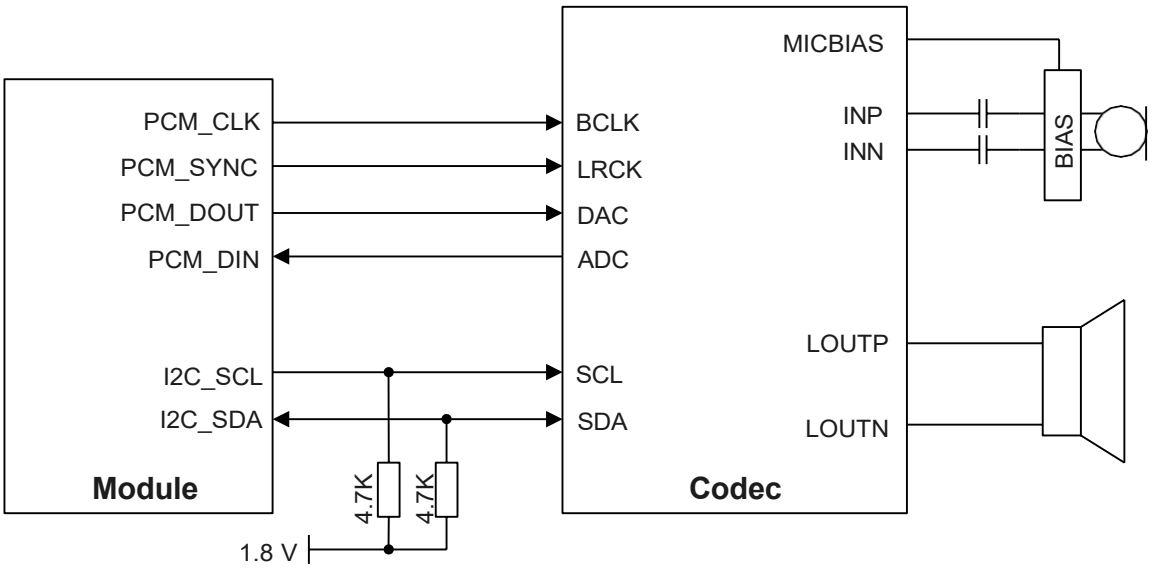


Figure 24: Reference Design of PCM and I2C Interfaces

4.6. ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 17: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	2	AI	General-purpose ADC interface	

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see ***document [2]***.

Table 18: Characteristics of ADC Interfaces

Parameters	Min.	Typ.	Max.	Units
ADC0 voltage range	0	-	1.2	V
ADC input resistance	0.26	-	0.75	MΩ
ADC resolution	-	12	-	bits

NOTE

1. The input voltage of every ADC interface should not exceed 1.2 V.
2. It is prohibited to directly supply any voltage to ADC Interfaces when the module is not powered by the VBAT.
3. It is recommended to use resistor divider circuit for ADC interface application. Resistance of the external resistor divider should not exceed 100 kΩ, or the measurement accuracy of ADC would be significantly reduced.

4.7. SPI Interface*

The module provides one SPI interface with a maximum clock frequency up to 25.6 MHz.

Table 19: Pin Description of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	
SPI_CS	25	DO	SPI chip selection	If unused, keep them open.
SPI_MISO	28	DI	SPI master-in slave-out	
SPI_MOSI	27	DO	SPI master-out slave-in	

The voltage domain of the module's SPI is 1.8 V. Use a level-shifting chip between the module and the host if the voltage domain of the external host system is 3.3 V. A level-shifting chip that supports SPI data rate is recommended. The following figure shows a reference design:

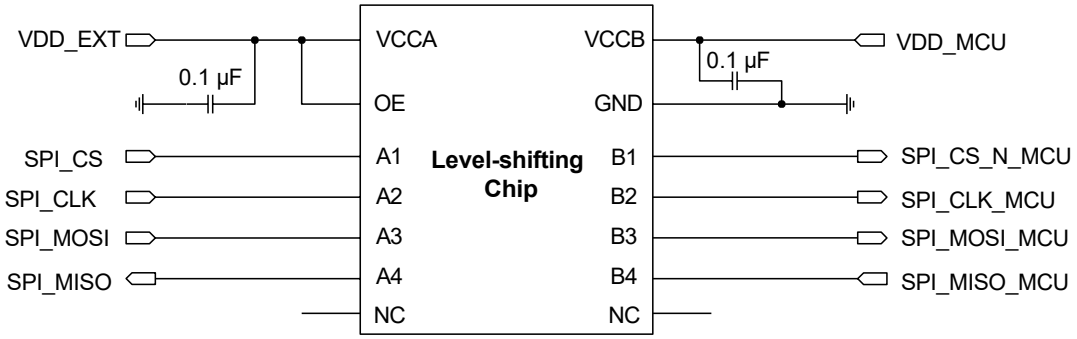


Figure 25: Reference Design of SPI with a Level-Shifting Chip

4.8. Camera SPI Interface*

The module provides one camera SPI interface supporting 2-bit data transmission of SPI.

Table 20: Pin Description of Camera SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	95	DO	Master clock of the camera	If unused, keep them open.
CAM_SPI_CLK	78	DI	Camera SPI clock	
CAM_SPI_DATA0	97	DI	Camera SPI data bit 0	
CAM_SPI_DATA1	98	DI	Camera SPI data bit 1	
CAM_PWDN	115	DO	Power down of the camera	
CAM_VDD	94	PO	Camera analog power supply	
CAM_VDDIO	93	PO	Camera digital power supply	

4.9. GRFC Interfaces*

The module provides two GRFC (generic RF control) interfaces for the control of external antenna tuners.

Table 21: Pin Description of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	76	DO	Generic RF controller	If unused, keep them open.
GRFC2	77	DO	Generic RF controller	

4.10. Control Signals

Table 22: Pin Description of Control Signals

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#*	18	DI	Airplane mode control	If unused, keep them open.
PSM_IND*	1	DO	Indicate the module's power saving mode	

PSM_INT*	96	DI	External interrupt; wake up the module from power saving mode
AP_READY*	19	DI	Application processor ready

4.10.1. W_DISABLE#*

The module provides W_DISABLE# to enable or disable RF function. When the voltage level of W_DISABLE# is high, you can send **AT+CFUN=<fun>** to set the module's operating mode. Driving W_DISABLE# low will set the module to airplane mode.

Table 23: W_DISABLE# AT Command Configuration Information

Level Status	AT Command	RF Function	Operating Mode
High level	**AT+CFUN=1**	Enabled	Full functionality mode
	AT+CFUN=0	Disabled	Minimum functionality mode
	AT+CFUN=4	Disabled	Airplane mode
Low level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled	Airplane mode

NOTE

W_DISABLE# is a control function for airplane mode, which is disabled in software by default. It can be enabled through **AT+QCFG="airplanecontrol",1**. For the details of this command, please contact Quectel Technical Support.

4.11. Indication Signals

Table 24: Pin Description of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	If unused, keep them open.
NET_STATUS	21	DO	Indicate the module's network activity status	

4.11.1. Network Status Indication

The module provides one network status indication pins: the NET_STATUS for the module's network operation status indication, which can drive corresponding LEDs.

Table 25: Network Status Indication Pin Level and Module Network Status

Pin Name	NET_STATUS Level Status	Module Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transmission is ongoing

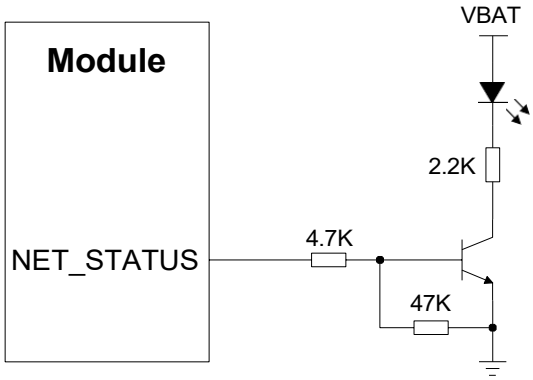


Figure 26: Reference Design of NET_STATUS Indication

4.11.2. STATUS

The STATUS is used for indicating the module's operation status. It will output high level when the module is turned on.

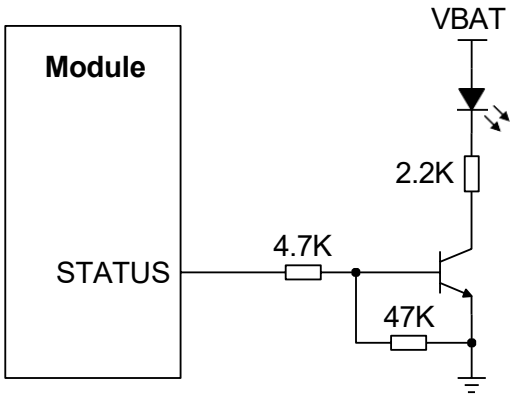


Figure 27: Reference Design of STATUS

4.11.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" can be used to configure MAIN_RI behavior. No matter on which port a URC information is presented, the URC information will trigger the behavior of the MAIN_RI. For the details of **AT+QCFG**, please contact Quectel Technical Support.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. For more details about **AT+QURCCFG**, see ***document [2]***.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 26: MAIN_RI Level and Module Status

Module Status	MAIN_RI Level Status
Idle	High level
When a new URC information returns	MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high.

Indication behavior for MAIN_RI can be configured via **AT+QCFG="urc/ri/ring"**.

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

Table 27: Pin Description of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN [4]	60	AIO	Main antenna interface	50 Ω impedance.

Table 28: Operating Frequency of EG915Q-NA (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B66	1710–1780	2110–2180

[4] ANT_MAIN only supports passive antennas.

5.1.2. Tx Power

Table 29: RF Transmitting Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
LTE-FDD bands	23 dBm ±2 dB	< -39 dBm

5.1.3. Rx Sensitivity

Table 30: Conducted RF Receiver Sensitivity of EG915Q-NA (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
LTE-FDD B2 (10 MHz)	-98 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-98.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-98.5dBm	-93.3 dBm
LTE-FDD B66 (10 MHz)	-98.5 dBm	-95.8 dBm

5.1.4. Reference Design

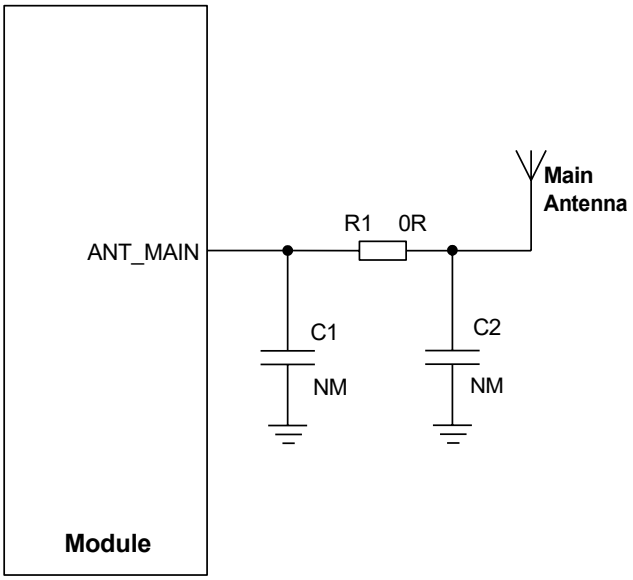


Figure 28: Reference Design of Main Antenna

NOTE

1. Use a π-type matching circuit for the antenna interface for better cellular performance and for the ease of debugging.
2. Capacitors are not mounted by default.
3. Place the π-type matching components (R1 & C1 & C2) to the antenna as close as possible.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

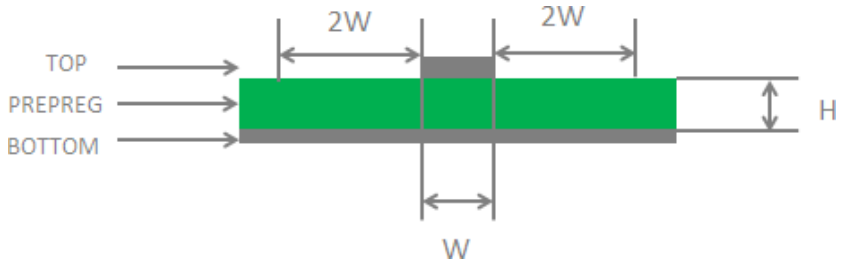


Figure 29: Microstrip Design on a 2-layer PCB

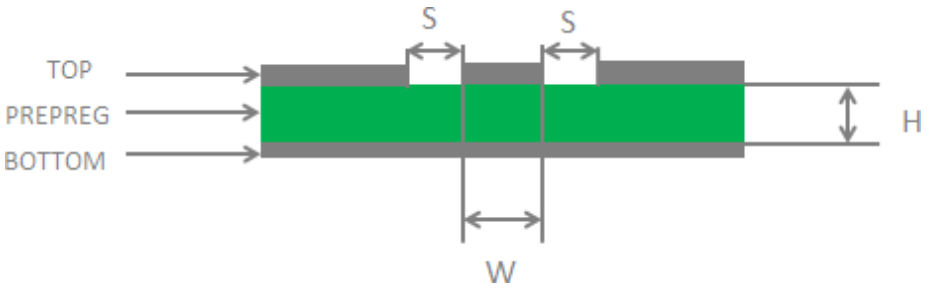


Figure 30: Coplanar Waveguide Design on a 2-layer PCB

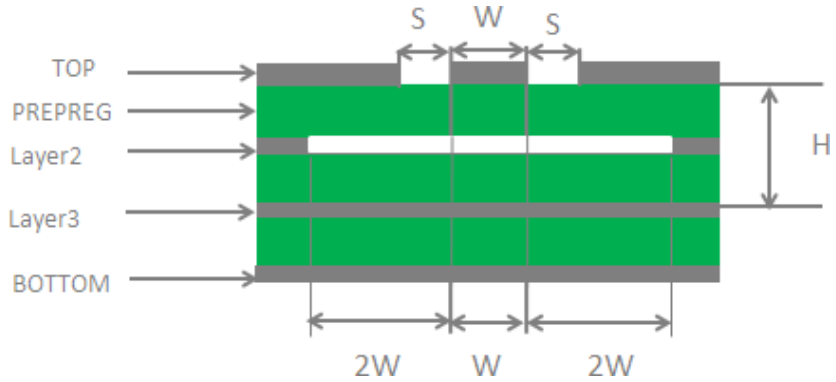


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

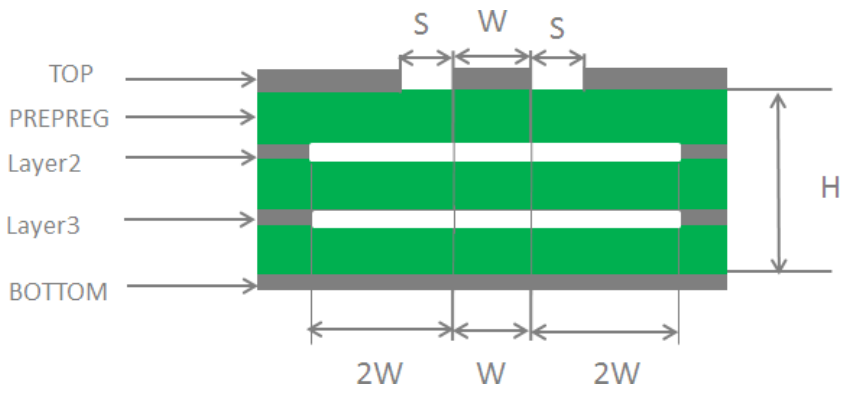


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.3. Antenna Design Requirements

Table 31: Requirements for Antenna Design

Antenna Types	Requirements
LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max. input power: 50 W ● Input impedance: 50 Ω ● Vertical polarization ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

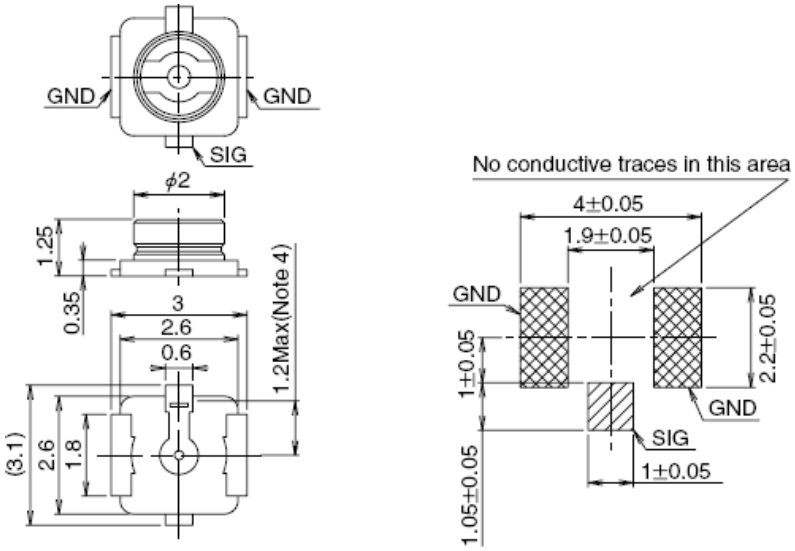


Figure 33: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

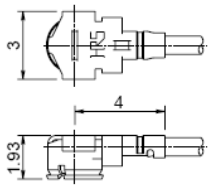
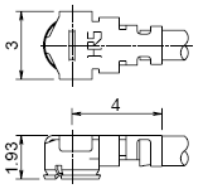
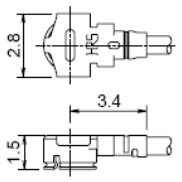
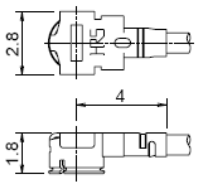
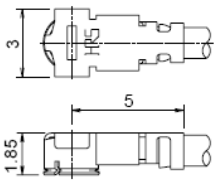
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 34: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

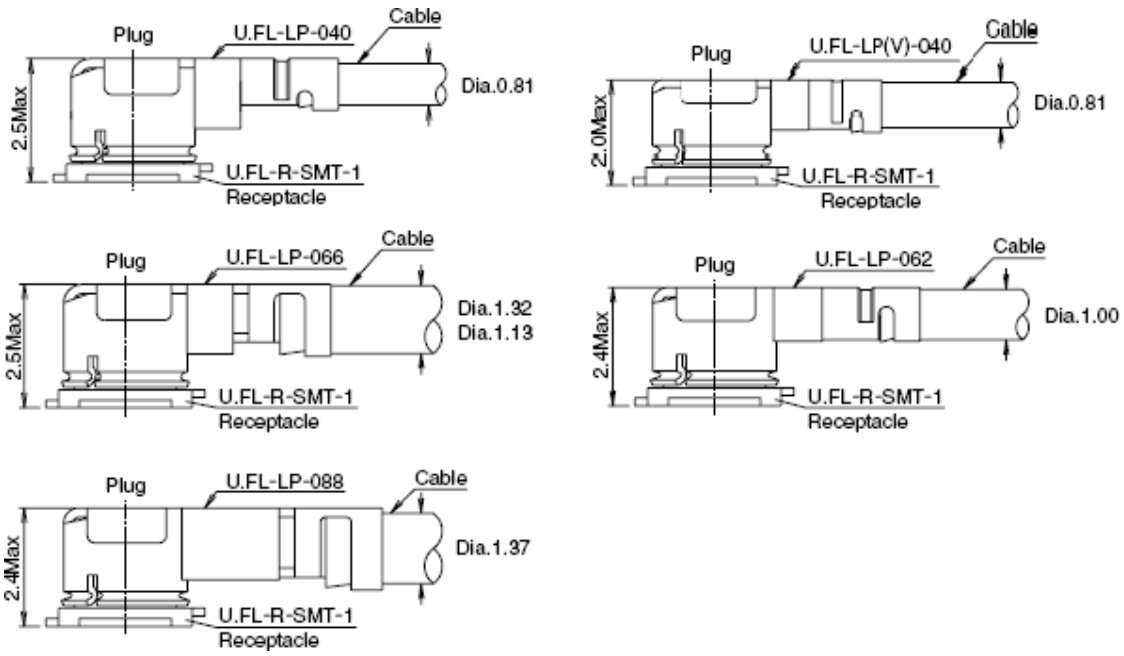


Figure 35: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 32: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT_RF & VBAT_BB	-0.3	5	V
Voltage at USB_VBUS	-0.3	5.25	V
Voltage at digital pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 33: Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	VBAT_BB & VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak power consumption	At maximum power control level	-	1.5	2	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 34: Power Consumption

Description	Conditions	Typ.	Units
OFF state	Power down	0.4	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	54	uA
	AT+CFUN=4 (USB disconnected)	130	uA
	LTE-FDD @ PF = 32 (USB disconnected)	1.24	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.68	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.41	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.3	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	4.55	mA
	LTE-FDD @ PF = 64 (USB connected)	28.22	mA
LTE data transfer	LTE-FDD B2	629	mA
	LTE-FDD B4	570	mA
	LTE-FDD B5	544	mA
	LTE-FDD B12	571	mA
	LTE-FDD B13	657	mA
	LTE-FDD B66	543	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 35: VDD_EXT I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.2	2
V_{IL}	Low-level input voltage	-0.3	0.6
V_{OH}	High-level output voltage	1.35	-
V_{OL}	Low-level output voltage	-	0.45

Table 36: USIM Low-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.2	-
V_{IL}	Low-level input voltage	-	0.6
V_{OH}	High-level output voltage	1.35	-
V_{OL}	Low-level output voltage	-	0.45

Table 37: USIM High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.95	-
V_{IL}	Low-level input voltage	-	1.0
V_{OH}	High-level output voltage	2.55	-
V_{OL}	Low-level output voltage	-	0.45

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 38: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±8	±12
Antenna interface	±5	±10
Other interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 39: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [5]	-35	+25	+75
Extended Operating Temperature [6]	-40	-	+85
Storage Temperature	-40	-	+90

[5] Within the operating temperature range, the module meets 3GPP specifications.
[6] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

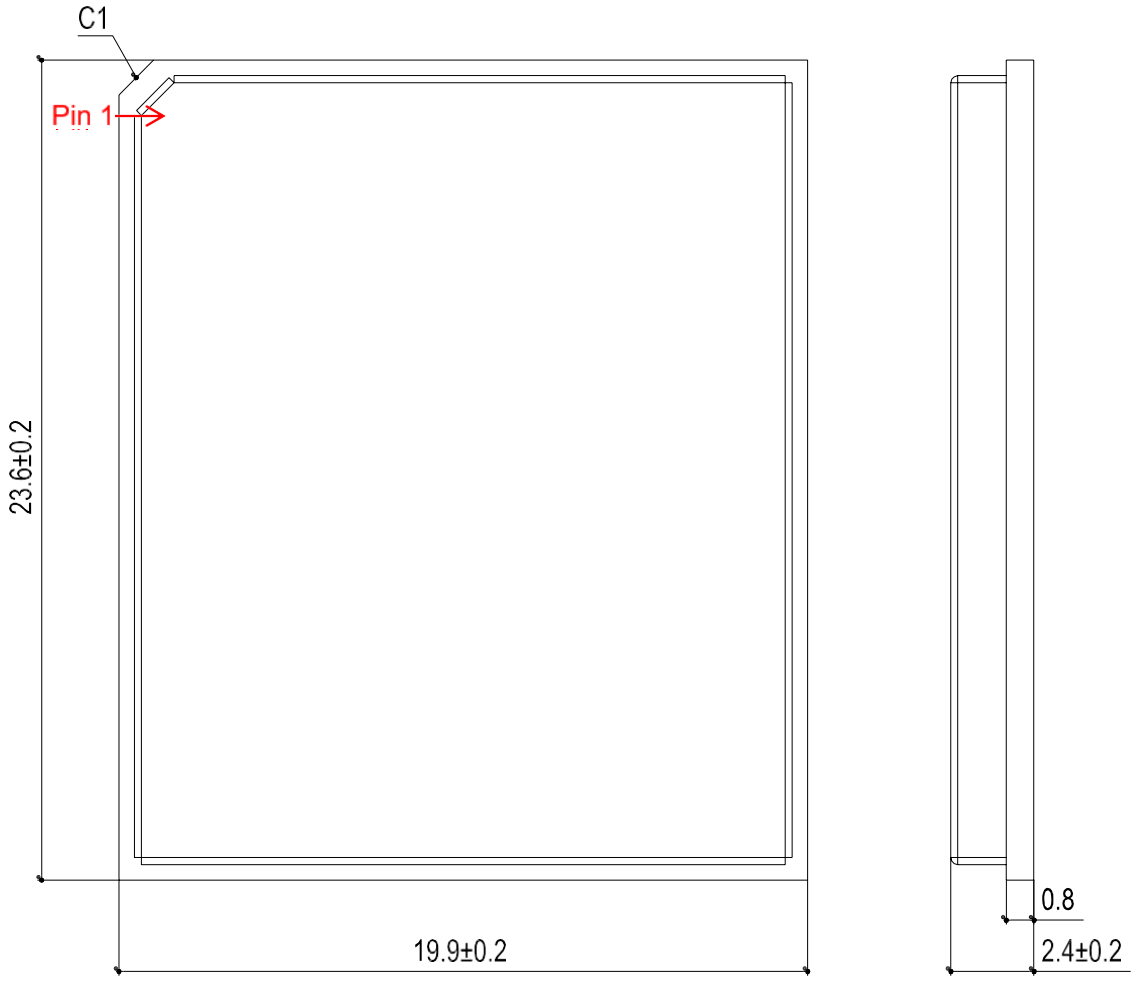


Figure 36: Top and Side Dimensions (Unit: mm)

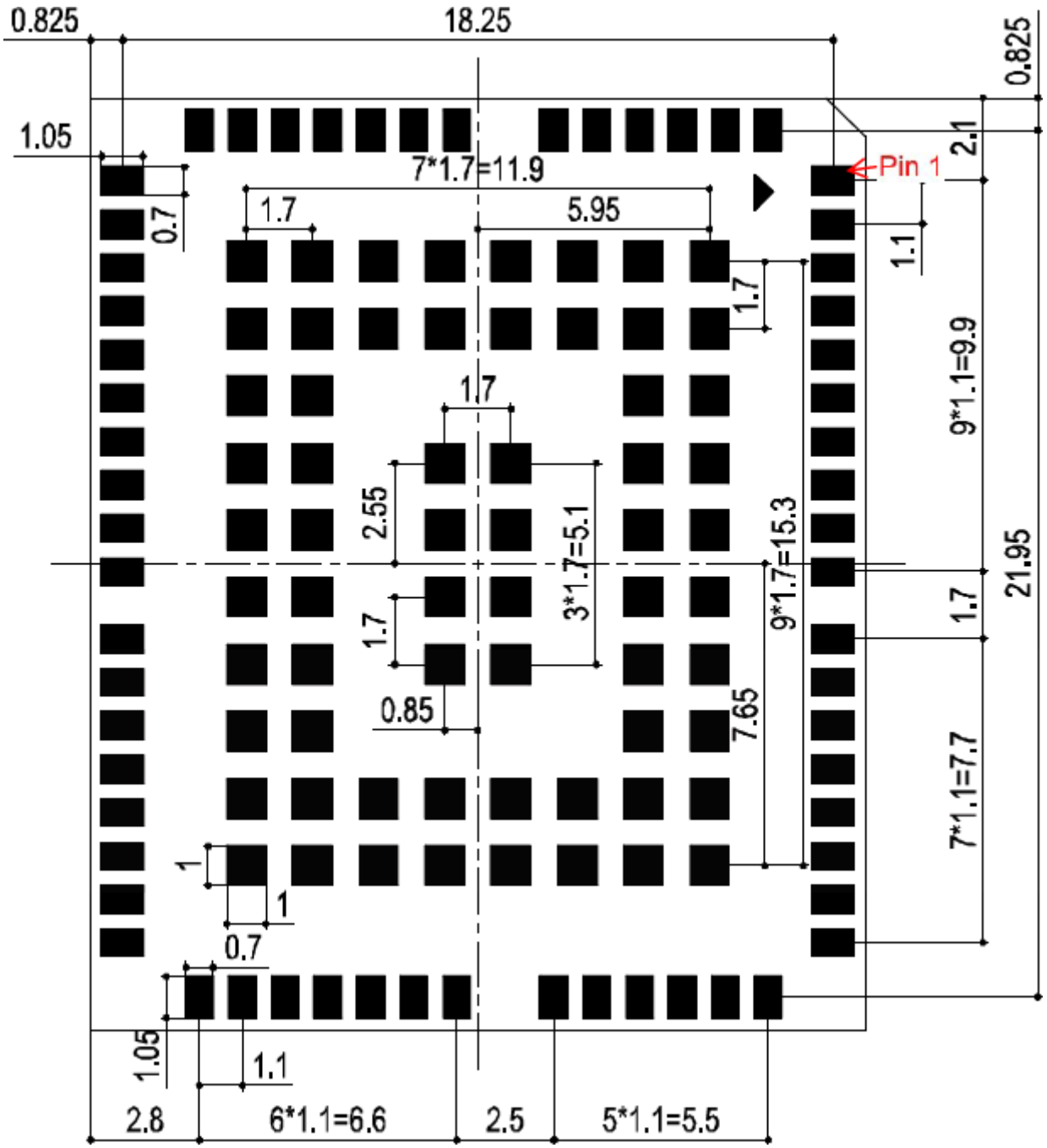


Figure 37: Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

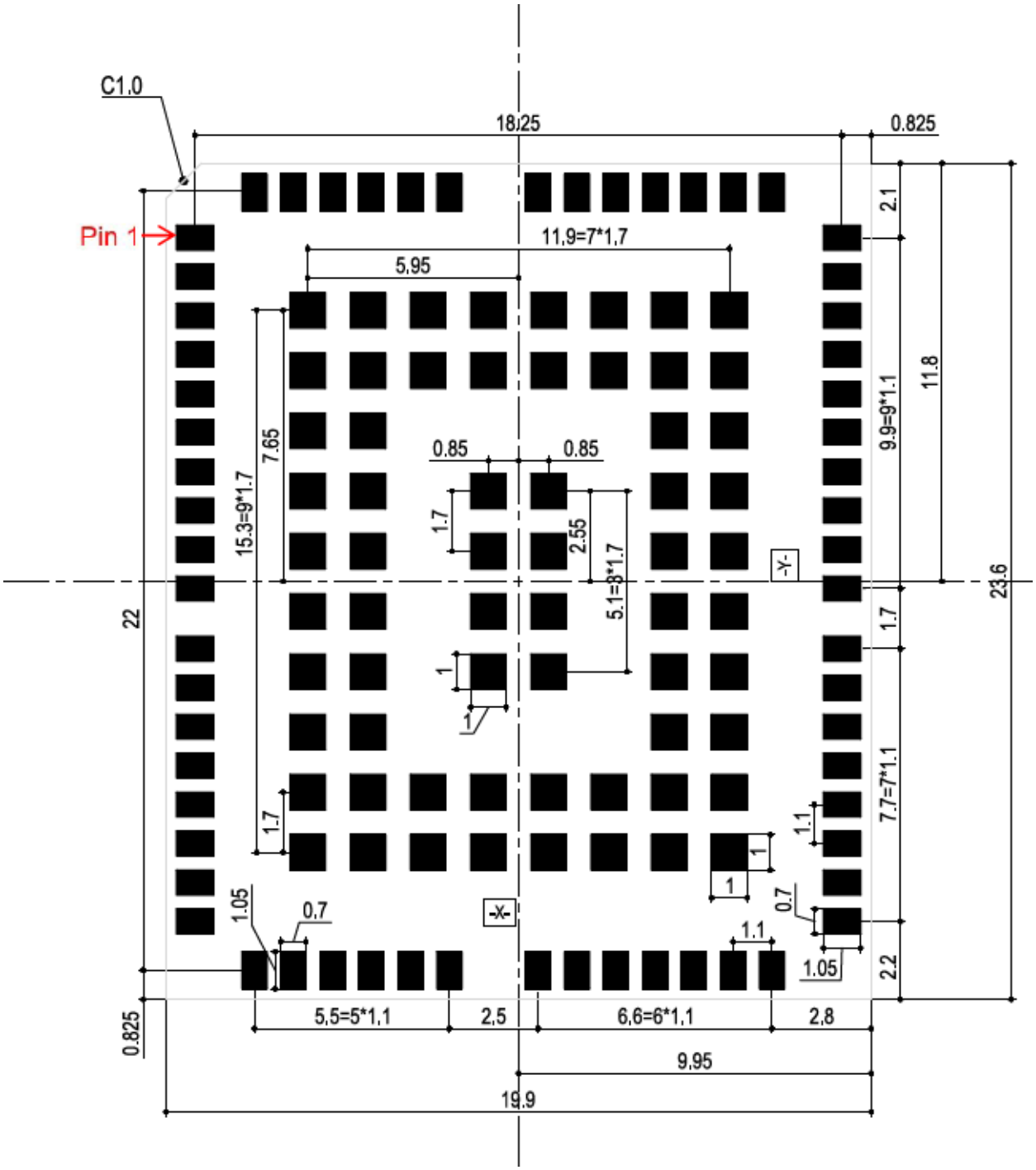


Figure 38: Recommended Footprint (Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

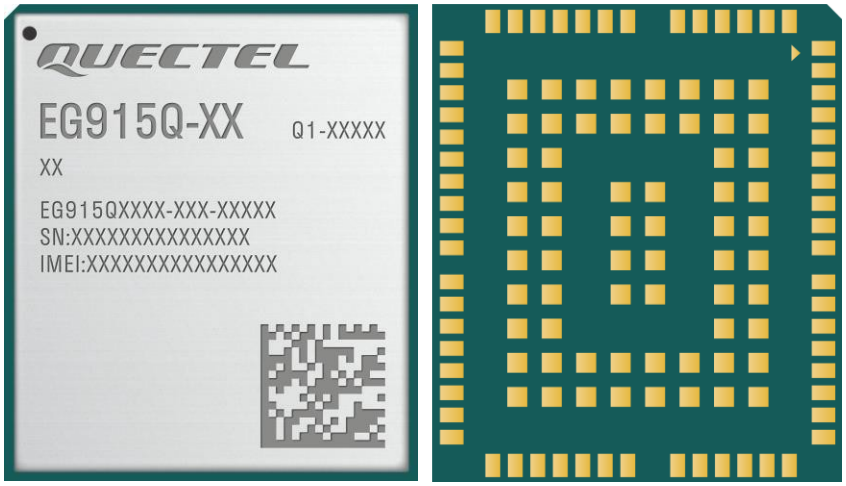


Figure 39: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

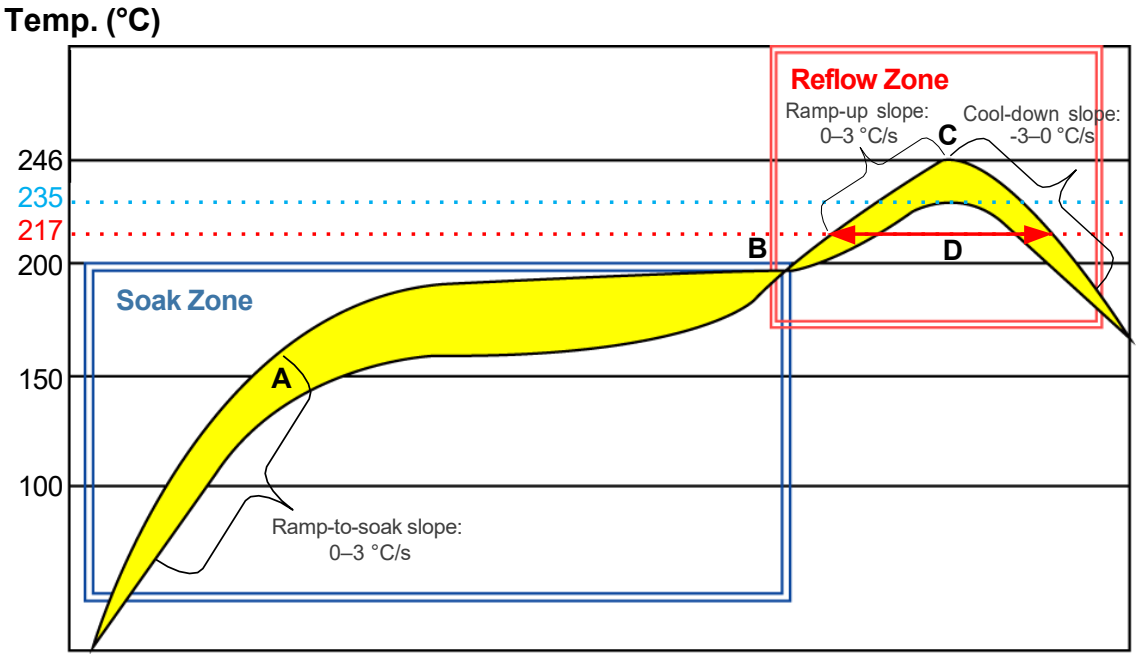


Figure 40: Recommended Reflow Soldering Thermal Profile

Table 40: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, never wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

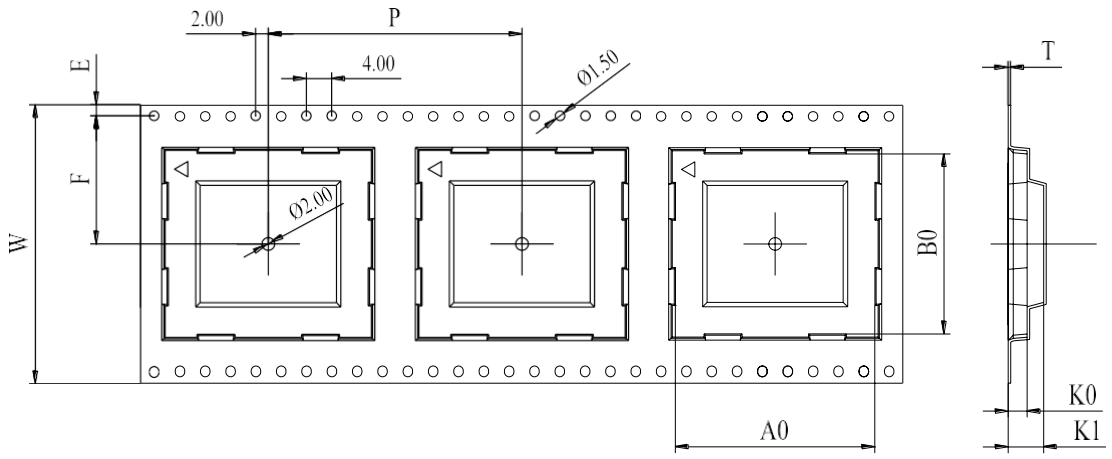


Figure 41: Carrier Tape Dimension Drawing

Table 41: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

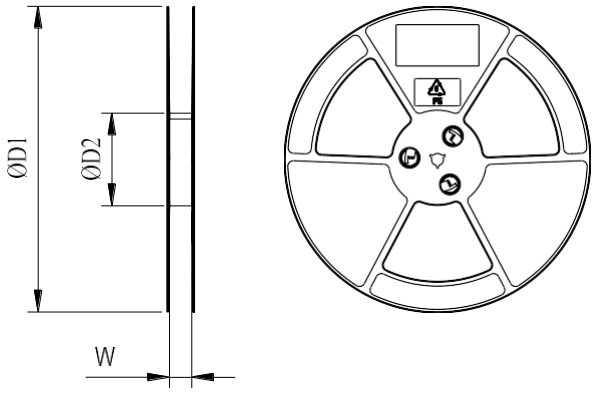


Figure 42: Plastic Reel Dimension Drawing

Table 42: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

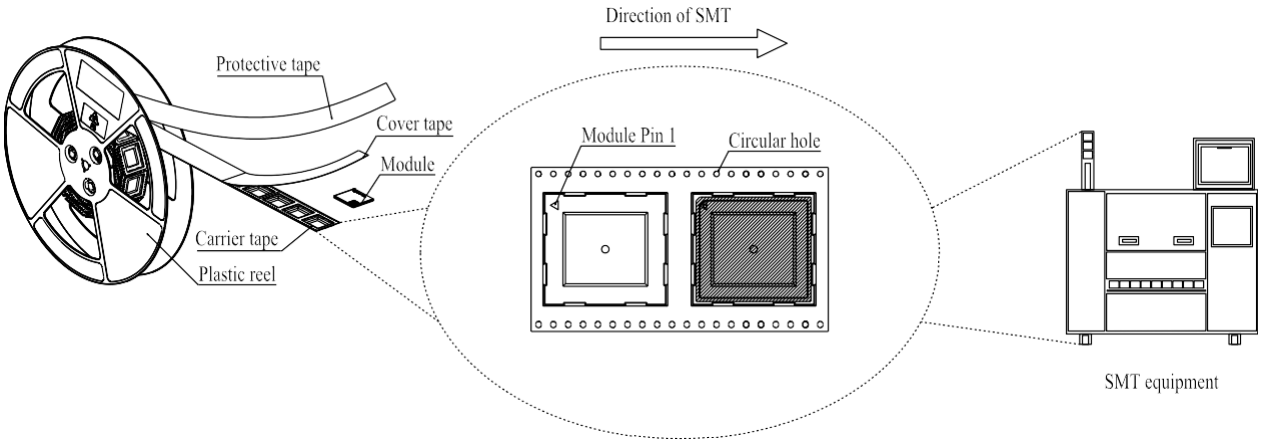
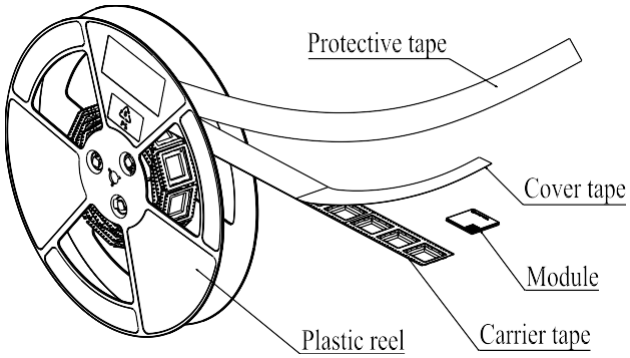


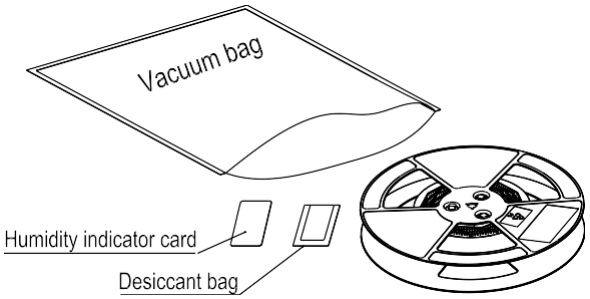
Figure 43: Mounting Direction

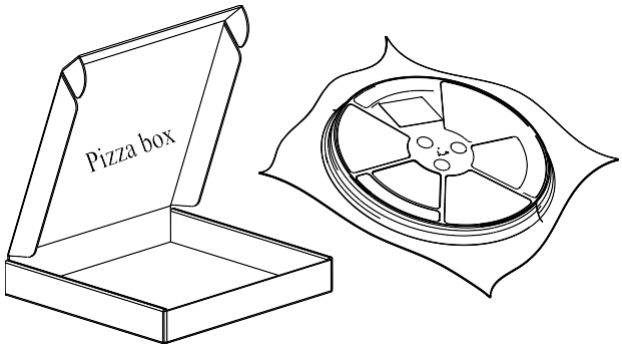
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 cartoon box and seal it. 1 cartoon box can pack 1000 modules.

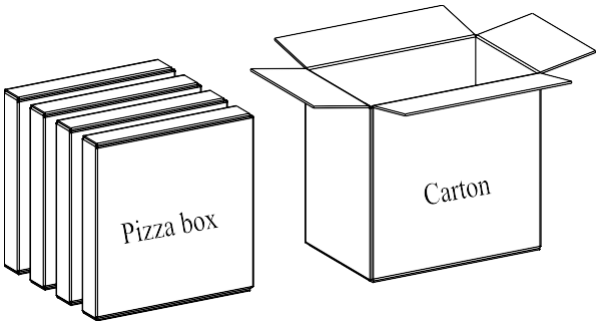


Figure 44: Packaging Process

9 Appendix References

Table 43: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG800Q-EU&EG915Q-NA_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_Application_Note

Table 44: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX
CTS	Clear To Send
DCE	Data Communications Equipment
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
DTR	Data Terminal Ready

ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GRFC	General RF Control
HB	High Band
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I2C	Inter-Integrated Circuit
I/O	Input/Output
IMT-2000	International Mobile Telecommunications 2000
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board

PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RI	Ring Indicator
RF	Radio Frequency
Rx	Receive
SMD	Surface Mount Device
SMS	Short Message Service
SSL	Secure Sockets Layer
SPI	Serial Peripheral Interface
TCP	Transmission Control Protocol
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V_{IH}	High-level input voltage

V_{IL}	Low-level input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio

Product Marketing Name: Quectel EG915Q-NA

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device. And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2023EG915QNA
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	**FCC Max Antenna Gain dBi**
LTE Band 2	**8.00**
LTE Band 4	**5.00**
LTE Band 5	**9.41**
LTE Band 12	**8.70**
LTE Band 13	**9.16**
LTE Band 66	**5.00**

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above).
The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2023EG915QNA" or "Contains FCC ID: XMR2023EG915QNA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN
"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :
(1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF
L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.
The host product shall be properly labeled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:
"Contains IC: 10224A-023EG915QNA" or "where: 10224A-023EG915QNA is the module's certification number".
Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.
L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être

clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:
"Contient IC: 10224A-023EG915QNA " ou "où: 10224A-023EG915QNA est le numéro de certification du module".