RG520N-AT

Hardware Design

5G Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

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1.0.0	2023-06-09	Nate WANG/ Johnson QIAO/ Jhin XIE/	Preliminary

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1 Introduction

This document defines RG520N-AT module and describes its air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

RG520N-AT is 5G NR/LTE wireless communication module, which provides data connectivity on 5G NR SA and NSA, LTE-FDD networks. It also provides GNSS to meet your specific application demands.

RG520N-AT is an industrial-grade module for industrial and commercial applications only.

The following table shows a brief introduction to the module. For CA and EN-DC configurations, see ***document [1]***.

Table 2: Brief Introduction

Categories	
Package	LGA
Pin counts	392
Dimensions	(44.0 ±0.2) mm × (41.0 ±0.2) mm × (2.75 ±0.2) mm
Weight	Approx. 11 g

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	RG520N-AT
5G NR	n2/n5/n12/n14/n29/n30/n66/n77
LTE-FDD	B2/B5/B12/B14/B17/B29/B30/B66
LTE-TDD	-
GNSS	GPS/GLONASS/BDS/Galileo/QZSS

2.2. Key Features

Table 4: Key Features

Feature	Detail
Power Supply	● Supply voltage: 3.3–4.4 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	Supports USIM/SIM card: 1.8/2.95 V
Audio Features	● Supports two digital audio interfaces: PCM and I2S* ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interfaces	● Supports two PCM interfaces, one is only used for Bluetooth audio* and the other is used for SLIC or Codec (multiplexed with I2S*) ● Supports 16-bit linear data format ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes, but must be in master mode for long frame synchronization
SPI	● Provides a duplex, synchronous and serial communication link with the peripheral devices ● One SPI that only supports master mode ● 1.8 V operation voltage with clock frequency up to 50 MHz
I2C Interface	● One I2C interface ● Comply with *I2C Specification, Version 3.0* ● Multi-master mode is not supported
I2S Interface*	● Supports 16-bit linear data format ● I2S is a common 4-wire DAI used in Hi-Fi, STB and portable devices ● The DIN and DOUT traces are used for audio transmission, whilst the bit clock and left/right clock synchronize the link
USB Interface	● Compliant with USB 3.1 and 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB* ● Supports USB serial driver: Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–13.x
SDIO Interface	Compliant with SD 3.0 protocol

UART	**Main UART:** ● Used for AT command communication ● Baud rate: 115200 bps by default **Debug UART:** ● Used for Linux console and log output ● Baud rate: 115200 bps **Bluetooth UART*:** ● Used for Bluetooth communication ● Baud rate: 115200 bps ● Supports RTS and CTS hardware flow control
PCIe Interface	● Complaint with PCIe Gen 3, supports two lanes, 8 Gbps per lane ● Supports RC (Root Complex) mode and EP (End Point) mode ● Used to connect an external Ethernet IC (MAC and PHY) or Wi-Fi IC
eSIM	Optional
Network Indication	NET_MODE and NET_STATUS to indicate network connectivity status
AT Commands	Compliant with *3GPP TS 27.007*, *27.005* and Quectel enhanced AT commands
Rx-diversity	5G NR/LTE
Antenna Interfaces	● Four cellular antenna interfaces (ANT0/ANT1/ANT2/ANT3) ● One GNSS antenna interface (ANT_GNSS) ● 50 Ω impedance
Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● 5G NR: Class 3 (23 dBm ±2 dB) ● 5G NR n77 HPUE: Class 2 (26 dBm +2/-3 dB)
5G NR Features	● Supports 3GPP Rel-16 ● Supports waveforms: - Uplink: CP-OFDM and DFT-s-OFDM - Downlink: CP-OFDM ● Supports modulations: - Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports DL 4 × 4 MIMO: n2/n5/n12/n14/n30/n66/n77 ● Supports UL 2 × 2 MIMO [1]: n77 ● Supports SCS 15 kHz [2] and 30 kHz [2] ● Bandwidth supported: - n2: 5/10/15/20 MHz - n5: 5/10/15/20 MHz - n12: 5/10/15 MHz - n14: 5/10 MHz - n29: 5/10 MHz

[1] UL 2 × 2 MIMO is only supported in 5G SA mode.
[2] 5G NR FDD bands only support 15 kHz SCS, and NR TDD bands only support 30 kHz SCS.

	- n30: 5/10 MHz - n66: 5/10/15/20/25/30/40 MHz - n77: 10/15/20/25/30/40/50/60/70/80/90/100 MHz ● Supports SA and NSA operation modes ● Supports n77 2T4R SRS in SA mode and 1T4R SRS in NSA mode ● Supports Option 3x, 3a, 3 and Option 2 ● Max. transmission data rates [3]: NSA TDD: Max. 3.4 Gbps (DL)/550 Mbps (UL) SA TDD: Max. 2.4 Gbps (DL)/900 Mbps (UL)
LTE Features	● Supports FDD ● Supports CA Categories: - Supports up to UL CA Cat 18 - Supports up to DL CA Cat 19 ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supports UL and DL QPSK, 16QAM, 64QAM and 256QAM modulations ● Supports DL 4 × 4 MIMO: B2/B5/B12/B14/B17/B30/B66 ● Max. transmission data rates [3]: LTE: 1.6 Gbps (DL)/200 Mbps (UL)
Internet Protocol Features	● Supports NITZ, PING and QMI protocols ● Supports PAP and CHAP for PPP connections
GNSS Features	● Supports dual-band GNSS: L1 and L5 ● Supports GPS, GLONASS, BDS, Galileo and QZSS ● Protocol: NMEA 0183 ● Data update rate: 1 Hz by default
Temperature Ranges	● Operating temperature range [4]: -30 to +75 °C ● Extended temperature range [5]: -40 to +85 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB interface or FOTA for firmware upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

[3] The maximum rates are theoretical and the actual values depend on the network configuration.
[4] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
[5] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency
- Peripheral interfaces

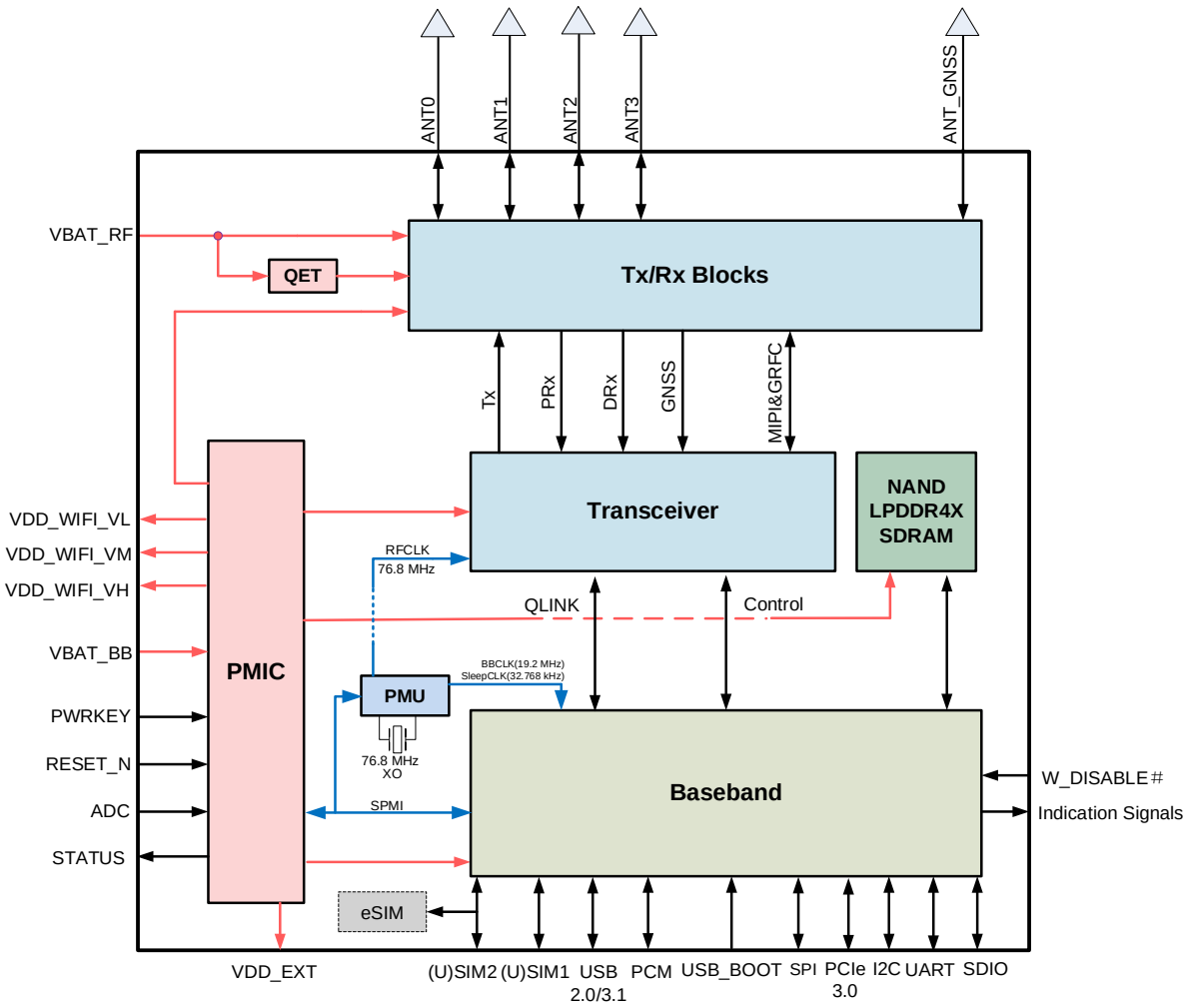


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

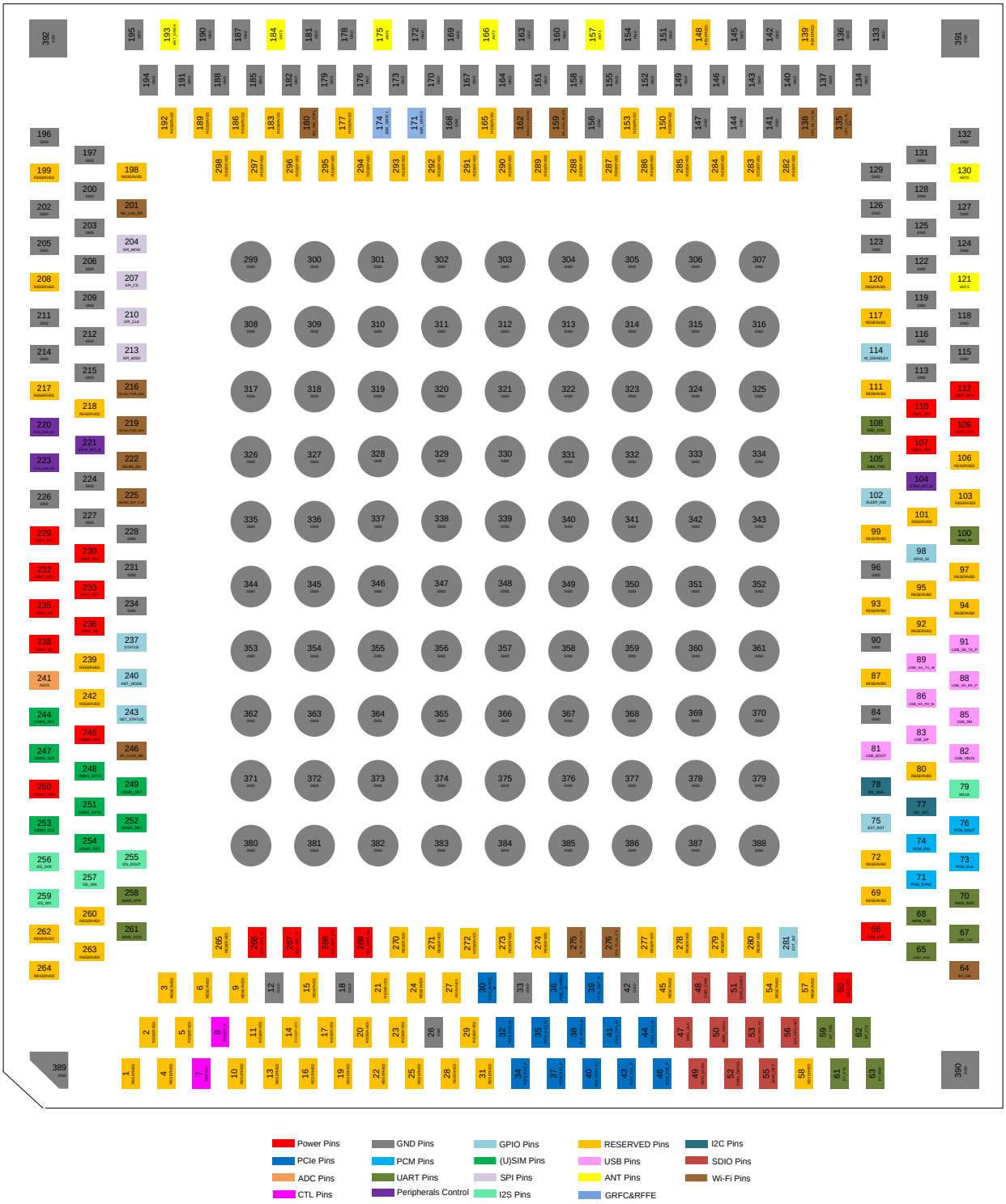


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED or unused pins unconnected.
2. All GND pins should be connected to ground.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	235, 236, 238	PI	Power supply for the module's baseband part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	

VBAT_RF1	229, 230, 232, 233	PI	Power supply for the module's RF part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF2 [6]	107, 109, 110, 112	PI	Power supply for the module's RF part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	
VDD_WIFI_VL	266, 267	PO	Provides 0.95 V for Wi-Fi/Bluetooth modules	Vnom = 0.95 V $I_O$max = 1.7 A	Power supply for Wi-Fi/Bluetooth modules.
VDD_WIFI_VM	268	PO	Provides 1.28 V for Wi-Fi/Bluetooth modules	Vmax = 1.35 V Vnom = 1.28 V $I_O$max = 400 mA	
VDD_WIFI_VH	269	PO	Provides 1.88 V for Wi-Fi/Bluetooth modules	Vnom = 1.88 V $I_O$max = 400 mA	
VDD_EXT	66	PO	Provides 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
GND	12, 18, 26, 33, 42, 84, 90, 96, 113, 115, 116, 118, 119, 122–129, 131–134, 136, 137, 140–147, 149, 151, 152, 154–156, 158, 160, 161, 163, 164, 167–170, 172, 173, 176, 178, 179, 181, 182, 185, 187, 188, 190, 191, 194–197, 200, 202, 203, 205, 206, 209, 211, 212, 214, 215, 224, 226, 227, 228, 231, 234, 299–392				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turns on/off the module	1.8 V high level	Internally pulled up to 1.8 V.
RESET_N	8	DI	Resets the module	1.8 V	Internally pulled up to 1.8 V with a 40 kΩ resistor. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

[6] VBAT_RF2 should be connected to an external VBAT power supply while Power Class 1.5 (optional) is designed; otherwise, it is only used to connect decoupling capacitors.

STATUS	237	DO	Indicates the module's operation status	1.8 V	
NET_MODE	240	DO	Indicates the module's network registration mode		
NET_STATUS	243	DO	Indicates the module's network activity status		
SLEEP_IND	102	DO	Indicates the module's sleep mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	82	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.3 V Vnom = 5.0 V	For USB connection detect only. A test point must be reserved.
USB_DP	83	AIO	USB 2.0 differential data (+)		Requires differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	85	AIO	USB 2.0 differential data (-)		
USB_SS_TX_P	91	AO	USB 3.1 SuperSpeed transmit (+)		Requires differential impedance of 85 Ω. USB 3.1 Gen 2 compliant.
USB_SS_TX_M	89	AO	USB 3.1 SuperSpeed transmit (-)		
USB_SS_RX_P	88	AI	USB 3.1 SuperSpeed receive (+)		
USB_SS_RX_M	86	AI	USB 3.1 SuperSpeed receive (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	245	PO	(U)SIM1 card power supply	1.8/2.95 V	

USIM1_DATA	248	DIO	(U)SIM1 card data	USIM1_VDD 1.8/2.95 V	
USIM1_CLK	247	DO	(U)SIM1 card clock		
USIM1_RST	244	DO	(U)SIM1 card reset		
USIM1_DET	249	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_VDD	250	PO	(U)SIM2 card power supply	1.8/2.95 V	
USIM2_DATA	251	DIO	(U)SIM2 card data	USIM2_VDD 1.8/2.95 V	
USIM2_CLK	253	DO	(U)SIM2 card clock		
USIM2_RST	254	DO	(U)SIM2 card reset		
USIM2_DET	252	DI	(U)SIM2 card hot-plug detect	1.8 V	If unused, keep it open.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_TXD	68	DO	Main UART transmit	1.8 V	
MAIN_RXD	70	DI	Main UART receive		
MAIN_RI	100	DO	Main UART ring indication		
MAIN_DTR	258	DI	Main UART data terminal ready		
MAIN_DCD*	261	DO	Main UART data carrier detect		
Bluetooth UART*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_TXD	59	DO	Bluetooth UART transmit	1.8 V	
BT_RXD	63	DI	Bluetooth UART receive		
BT_RTS	61	DI	Request to send signal to the module		Connect to the peripheral's RTS.

BT_CTS	62	DO	Clear to send signal from the module		Connect to the peripheral's CTS.
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	108	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	105	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	77	OD	I2C serial clock	1.8 V	Pull each of them up to VDD_EXT with an external 4.7 kΩ resistor. If unused, keep them open.
I2C_SDA	78	OD	I2C serial data		
I2S Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_WS	259	DIO	I2S word select	1.8 V	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_SCK	256	DIO	I2S clock		In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_DIN	257	DI	I2S data in		
I2S_DOUT	255	DO	I2S data out		
MCLK	79	DO	Master clock output for codec		If unused, keep it open.
PCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	71	DIO	PCM data frame sync	1.8 V	Only used for Bluetooth audio.

PCM_CLK	73	DIO	PCM clock		If unused, keep them open.
PCM_DIN	74	DI	PCM data input		
PCM_DOUT	76	DO	PCM data output		
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)		In root complex mode, it is an output signal. In endpoint mode, it is an input signal. Requires differential impedance of 85 Ω.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)		
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)		Requires differential impedance of 85 Ω. If unused, keep them open.
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)		
PCIE_TX1_M	41	AO	PCIe transmit 1 (-)		
PCIE_TX1_P	43	AO	PCIe transmit 1 (+)		
PCIE_RX0_M	32	AI	PCIe receive 0 (-)		
PCIE_RX0_P	34	AI	PCIe receive 0 (+)		
PCIE_RX1_M	35	AI	PCIe receive 1 (-)		
PCIE_RX1_P	37	AI	PCIe receive 1 (+)		
PCIE_CLKREQ_N	36	OD	PCIe clock request	1.8 V	In root complex mode, it is an input signal. In endpoint mode, it is an output signal.
PCIE_RST_N	39	DIO	PCIe reset		In root complex mode, it is an output signal. In endpoint mode, it is an input signal.
PCIE_WAKE_N	30	OD	PCIe wake up		In root complex mode, it is an input signal.

					In endpoint mode, it is an output signal.
WWAN/WLAN Application Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
COEX_RXD	65	DI	Coexistence UART receive	1.8 V	Only for Qualcomm platform. Signal interface used for WWAN/WLAN coexistence mechanism. Pin 65 can be multiplexed into SDX2AP_E911 function. Pin 67 can be multiplexed into SDX2AP_STATUS function. For details, contact Quectel Technical Support.
COEX_TXD	67	DO	Coexistence UART transmit		
HST_LAA_TX_EN	135	DO	Notifies LAA/n79 transmission from SDR transceiver to WLAN		This pin is used for the coexistence of n79 and Wi-Fi 5 GHz. If n79 is needed in your future project with Quectel modules, then this pin should be reserved; otherwise, keep it unconnected.
HST_WL_TX_EN	138	DI	Notifies WLAN transmission from WLAN to SDR transceiver		
WLAN_PWR_EN1	216	DO	Controls WLAN PA power		
WLAN_PWR_EN2	219	DO	Controls other power of WLAN		

BT_EN	64	DO	Bluetooth enable control		
WLAN_EN	222	DO	WLAN function enable control		
WL_SW_CTRL	180	DI	76.8 MHz system clock request		
WLAN_SLP_CLK	225	AO	32.768 kHz sleep clock output		
RF_CLK3_WL	246	AO	76.8 MHz system clock output	Vmax = 1.08 V Vnom = 1.05 V Vmin = 1.02 V	
SDX_TO_WL_CTI	276	DO	-		Not used by default. Keep it open.
WLAN_PA_MUTING	162	DO	GPIO from SDX to disable WLAN PA		
WL_LAA_AS_EN	159	DO	GPIO allows SDR to power on monitoring for WCN when WLAN is sleeping or disabled. Additionally, the control logic in WLAN AON domain allows SDR to control 5G WLAN xLNA (LNA in FEMs).	1.8 V	
WL_LAA_RX	201	DO	SoC signal to set 5G xLNA to high gains or high isolation when both chains (LAA and 5G WLAN) are active simultaneously. No individual control for each chain.		
WL_TO_SDX_CTI	275	DI	-		Not used by default. Keep it open.
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC**	**Comment**

				Characteristics	
SDIO_VDD	60	PI	SDIO power supply		1.8/2.95 V configurable input. If unused, connect it to VDD_EXT.
SDIO_DATA0	49	DIO	SDIO data bit 0	The power domain of SDIO pins depends on SDIO_VDD.	If unused, keep them open.
SDIO_DATA1	50	DIO	SDIO data bit 1		
SDIO_DATA2	51	DIO	SDIO data bit 2		
SDIO_DATA3	52	DIO	SDIO data bit 3		
SDIO_CMD	48	DIO	SDIO command		
SDIO_CLK	47	DO	SDIO clock		
SDIO_PWR_EN	53	DO	SDIO power supply enable	1.8 V	
SDIO_PWR_VSET	56	DO	SDIO power domain set		
SDIO_DET	55	DI	SD card detect		Pull it up to VDD_EXT with a 470 kΩ resistor. If unused, keep it open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**		**Comment**
ANT0	130	AIO	**Antenna 0 interface:** - **5G NR**: n77 TRX0 - **LTE**: LMB_TRX0 & HB_DRX - **Refarmed**: LMB_TRX0 & HB_TRX1		50 Ω impedance.
ANT1	157	AIO	**Antenna 1 interface:** - **5G NR**: n77 DRX MIMO - **LTE**: LMB_PRX MIMO & HB_DRX MIMO - **Refarmed**: LMB_PRX MIMO & HB_DRX MIMO		
ANT2	166	AIO	**Antenna 2 interface:** - **5G NR**: n77 PRX MIMO - **LTE**: LMB_DRX MIMO & HB_PRX MIMO		

			- **Refarmed**: LMB_DRX MIMO & HB_PRX MIMO		
ANT3	184	AIO	**Antenna 3 interface:** - **5G NR**: n77 TRX1 - **LTE**: LMB_TRX1 & HB_TRX0 - **Refarmed**: LMB_TRX1 & HB_TRX0		
ANT_GNSS	193	AI	**GNSS antenna interface:** - L1/L5		
Antenna Tuner Control Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDR_GRFC0	171	DO	GRFC interfaces dedicated for external antenna tuner control	1.8 V	If unused, keep them open.
SDR_GRFC1	174	DO			
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	210	DO	SPI clock	1.8 V	Only master mode is supported.
SPI_CS	207	DO	SPI chip select		
SPI_MISO	213	DI	SPI master-in slave-out		
SPI_MOSI	204	DO	SPI master-out slave-in		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	241	AI	General-purpose ADC interface	Voltage range: 0–1.875 V	
Time Service and Repeater Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_32	98	DO	Supports time service and repeater functions; supports 1PPS pulse output and frame	1.8 V	The pin can be multiplexed into AP2SDX_STATUS function. For details, contact Quectel Technical

			synchronization		Support.
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	81	DI	Forces the module into emergency download mode	1.8 V	A test point is recommended to be reserved.
EXT_RST	75	DO	External audio reset		
EXT_INT	281	DI	External audio interrupt		
W_DISABLE#	114	DI	Airplane mode control		
ETH1_PWR_EN	220	DO	Ethernet PHY 1 power enable		These pins are the control pins of PHY chip recommended by the platform.
ETH2_PWR_EN	223	DO	Ethernet PHY 2 power enable		
ETH1_INT_N	221	DI	Interrupts input from Ethernet PHY 1		
ETH2_INT_N	104	DI	Interrupts input from Ethernet PHY 2		
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	1–6, 9, 10, 11, 13, 14, 15, 16, 17, 19, 20, 21, 22, 23, 24, 25, 27, 28, 29, 31, 45, 54, 57, 58, 69, 72, 80, 87, 92–95, 97, 99, 101, 103, 106, 111, 117, 120, 139, 148, 150, 153, 165, 177, 183, 186, 189, 192, 198, 199, 208, 217, 218, 239, 242, 260, 262–265, 270, 271–273, 274, 277–280, 282–298				Keep these pins unconnected.

NOTE

RG520N-AT has 5 antenna interfaces (ANT0/ANT1/ANT2/ANT3 + ANT_GNSS).

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies two evaluation boards (5G EVB and RTA001-EV EVB) with accessories to develop or test the module. For more details, see ***document [2]***.

NOTE

If QPS615 is matched, please choose RTA001-EV EVB for verification.

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or driving W_DISABLE# low can set the module to airplane mode. In this mode, RF function is invalid.	
Sleep Mode	In this mode, current consumption of the module is reduced to the minimal level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.	

NOTE

For more details about AT command, see ***document [3]***.

3.2. Sleep Mode

DRX of the module is able to reduce the current consumption to a minimum value during sleep mode. The diagram below illustrates the relationship between the DRX run time and the current consumption of the module in this mode.

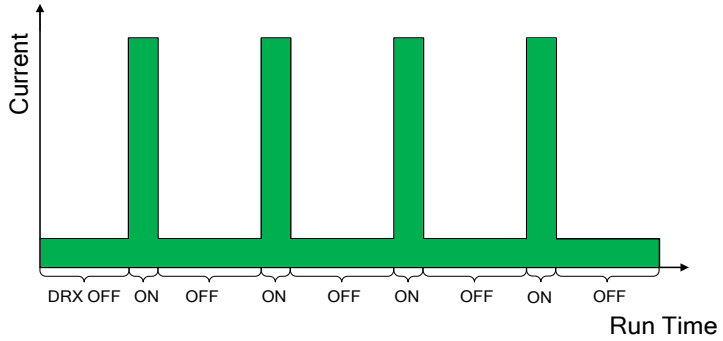


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

3.2.1. UART Application Scenario

If MCU communicates with the module via UART, the following two preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR high.

The figure illustrates the connection between the module and MCU.

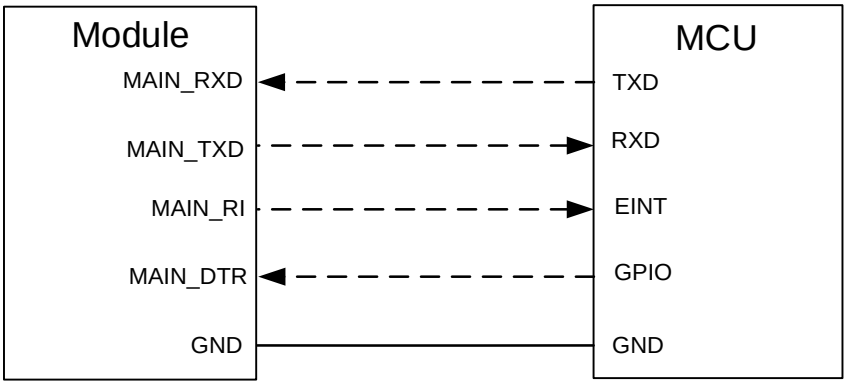


Figure 4: Sleep Mode Application via UART

- Driving MAIN_DTR low with the host will wake up the module.

- When the module has a URC to report, MAIN_RI signal will wake up the host. See ***Chapter 4.14*** for details about RI behavior.

3.2.2. USB Application Scenario

3.2.2.1.USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure illustrates the connection between the module and the host.

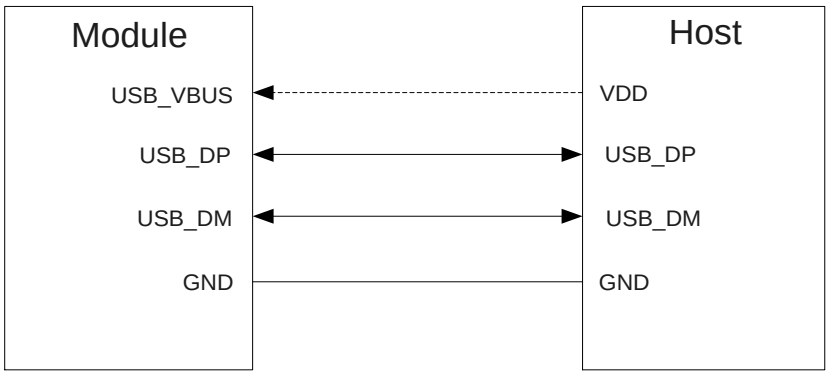


Figure 5: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2.USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

In this case, the following three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure MAIN_DTR is held at a high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure illustrates the connection between the module and the host.

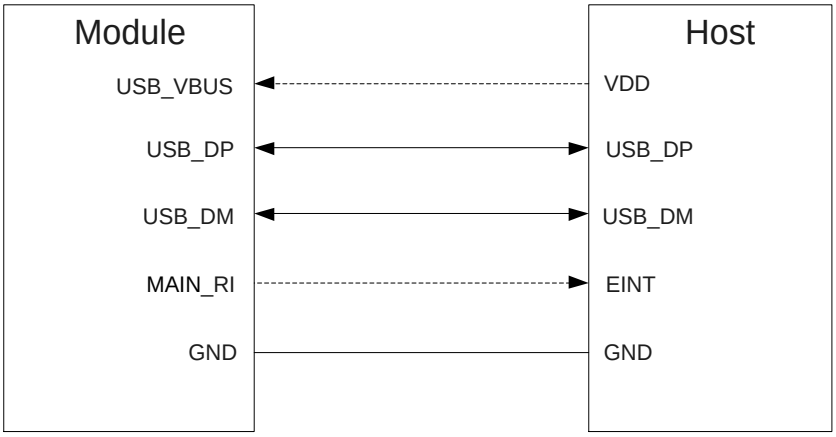


Figure 6: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the MAIN_RI signal will wake up the host.

3.2.2.3.USB Application without USB Suspend Function

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at a high level or keep it open.
- Disconnect USB_VBUS.

The figure illustrates the connection between the module and the host.

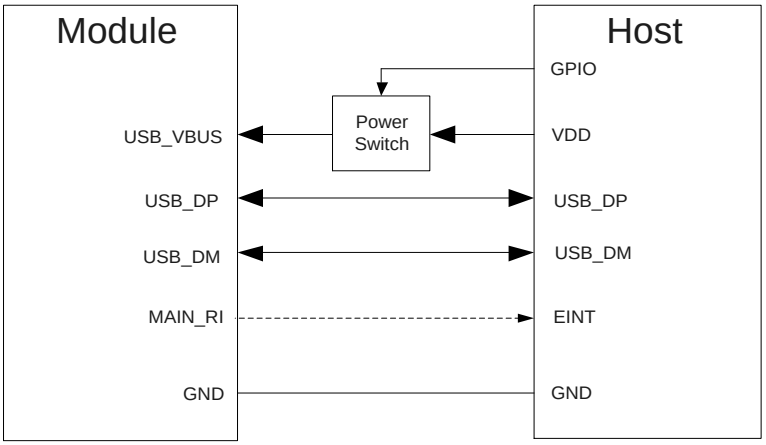


Figure 7: Sleep Mode Application without Suspend Function

Turning on the power switch and supplying power to USB_VBUS will wake up the module.

NOTE

Pay attention to the level match shown in dotted line between the module and the host.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

3.3.1. Hardware

The W_DISABLE# pin is pulled up by default. Driving it low will set the module to airplane mode.

3.3.2. Software

AT+CFUN=<fun> provides choices of the functionality level by setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality. Both RF and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality mode (default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** will not affect GNSS function.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 11 VBAT pins dedicated to the connection with the external power supply. There are 3 separate voltage domains for VBAT.

- 4 VBAT_RF1 pins and 4 VBAT_RF2 pins for RF part.
- 3 VBAT_BB pins for baseband part.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	235, 236, 238	PI	Power supply for the module's baseband part	3.3	3.8	4.4	V
VBAT_RF1	229, 230, 232, 233	PI	Power supply for the module's RF part	3.3	3.8	4.4	V
VBAT_RF2 [7]	107, 109, 110, 112	PI	Power supply for the module's RF part	3.3	3.8	4.4	V

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power supply design. The continuous current of the power supply should be 3 A at least and the peak current should be 4 A at least.

The following figure shows a reference design for +5 V input power source. The designed output of the power supply is about 3.8 V.

[7] VBAT_RF2 should be connected to an external VBAT power supply when Power Class 1.5 (optional) is designed; otherwise, it is only used to connect decoupling capacitors.

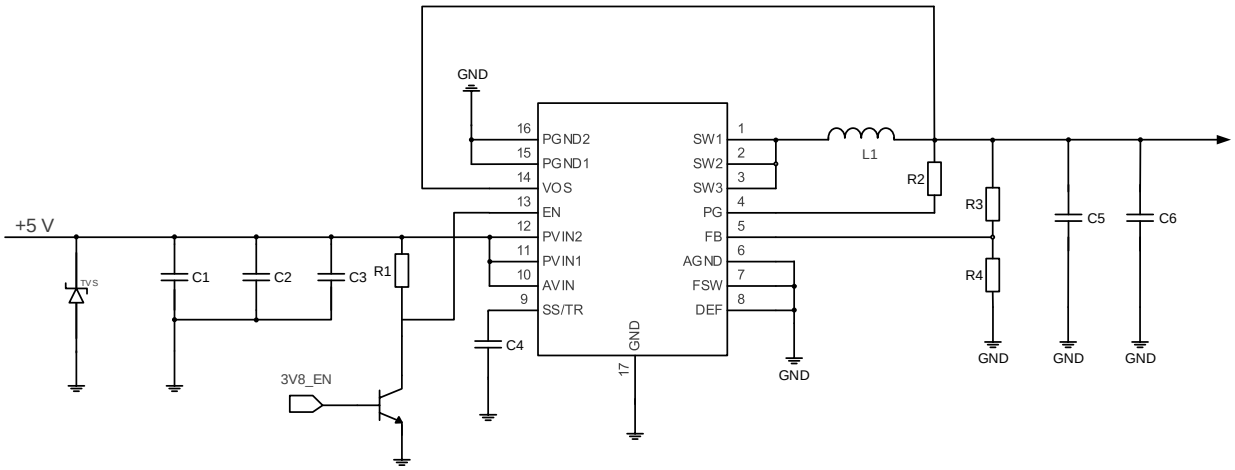


Figure 8: Reference Design of Power Supply

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is turned off with PWRKEY or AT command, the power supply can be cut off.
2. If you turn off the module by cutting off the power supply, do not power on the module until the power drops to 0 V, or there is a risk that the module cannot be turned on.

3.4.3. Power Supply Voltage Monitoring

AT+CBC can monitor the VBAT_BB voltage value.

3.4.4. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.4 V. Please make sure the input voltage will never drop below 3.3 V.

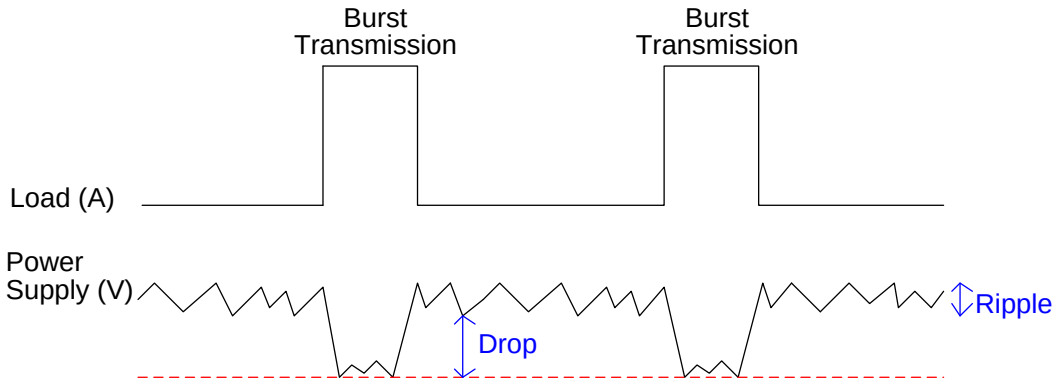


Figure 9: Power Supply Limits during Burst Transmission

To decrease the voltage drop, use a decoupling capacitor of about 100 μF with low ESR and reserve a decoupling capacitor of about 100 μF. In addition, a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use 16 ceramic capacitors for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star structure. The width of VBAT_BB trace should be not less than 2 mm and the width of VBAT_RF1 and VBAT_RF2 trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to ensure the stability of the power supply, it is necessary to add a high-power TVS at the front end of the power supply. Reference circuit is shown as below:

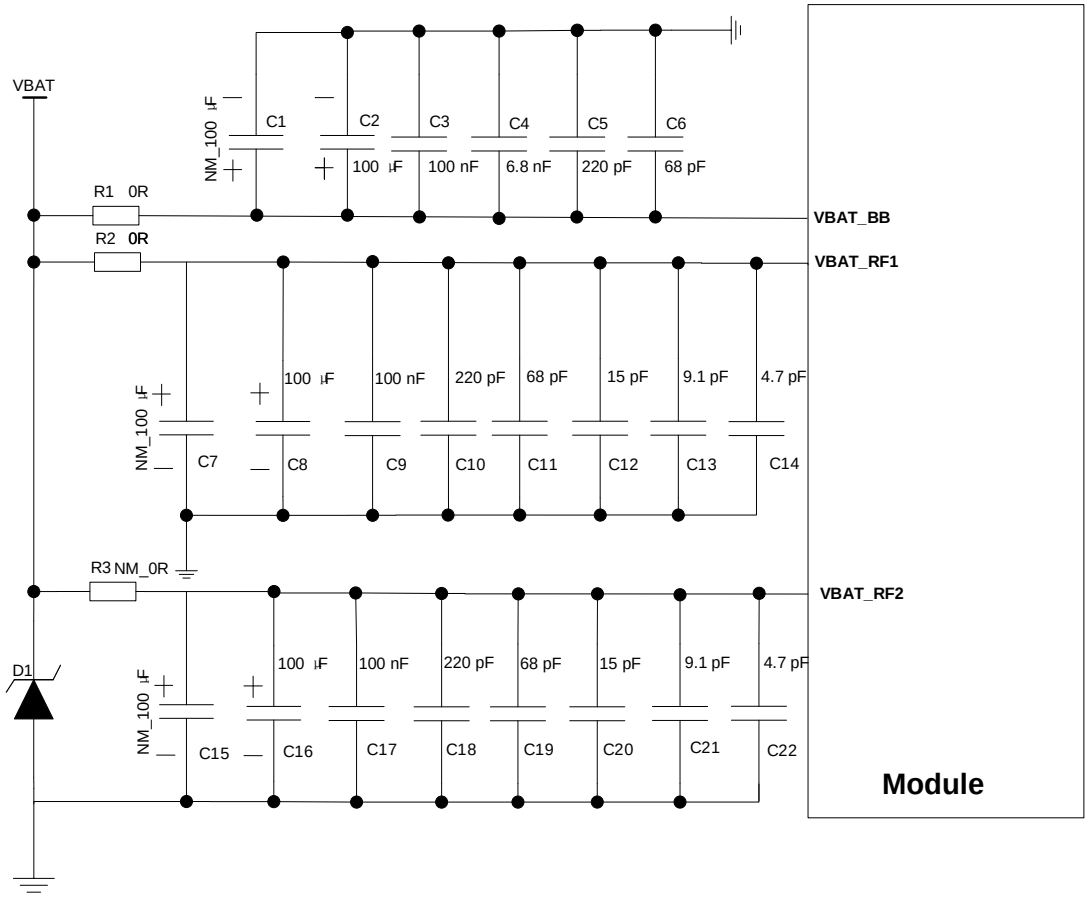


Figure 10: Star Structure of the Power Supply

NOTE

1. Filter capacitors for VBAT_BB include 100 μF, 100 nF, 6.8 nF, 220 pF and 68 pF, and a 100 μF is reserved.
2. Filter capacitors for VBAT_RF1 and VBAT_RF2 respectively include 100 μF, 100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF and 4.7 pF, and a 100 μF is reserved.
3. R3 needs to be reserved since VBAT_RF2 should be connected to an external VBAT power supply when Power Class 1.5 (optional) is designed.

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turns on/off the module	Internally pulled up to 1.8 V.

When the module is in power off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open-drain/open-collector driver to control PWRKEY. After STATUS pin outputs a high level, PWRKEY can be released.

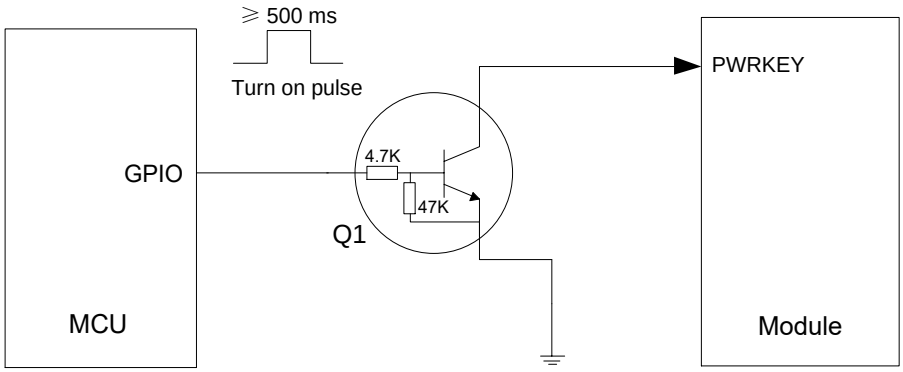


Figure 11: Reference Circuit of Turning on the Module with Driving Circuit

Another way to control PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may generate from finger. Therefore, a TVS component shall be placed near the button for ESD protection.

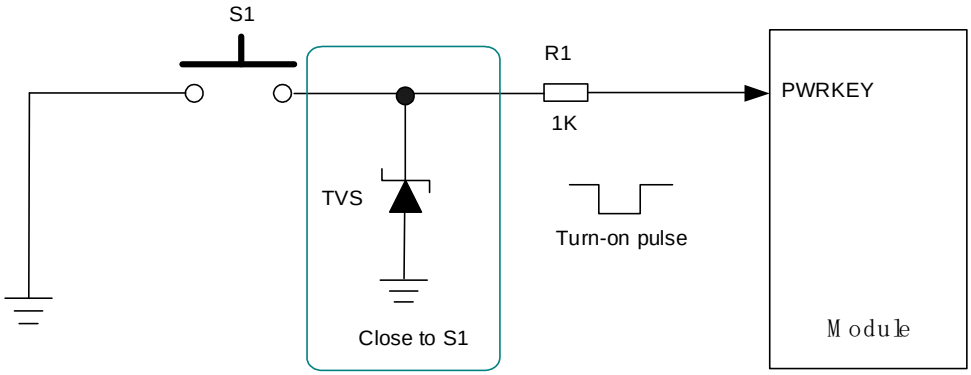


Figure 12: Reference Circuit of Turning on the Module with a Button

The turn-on timing is illustrated in the following figure.

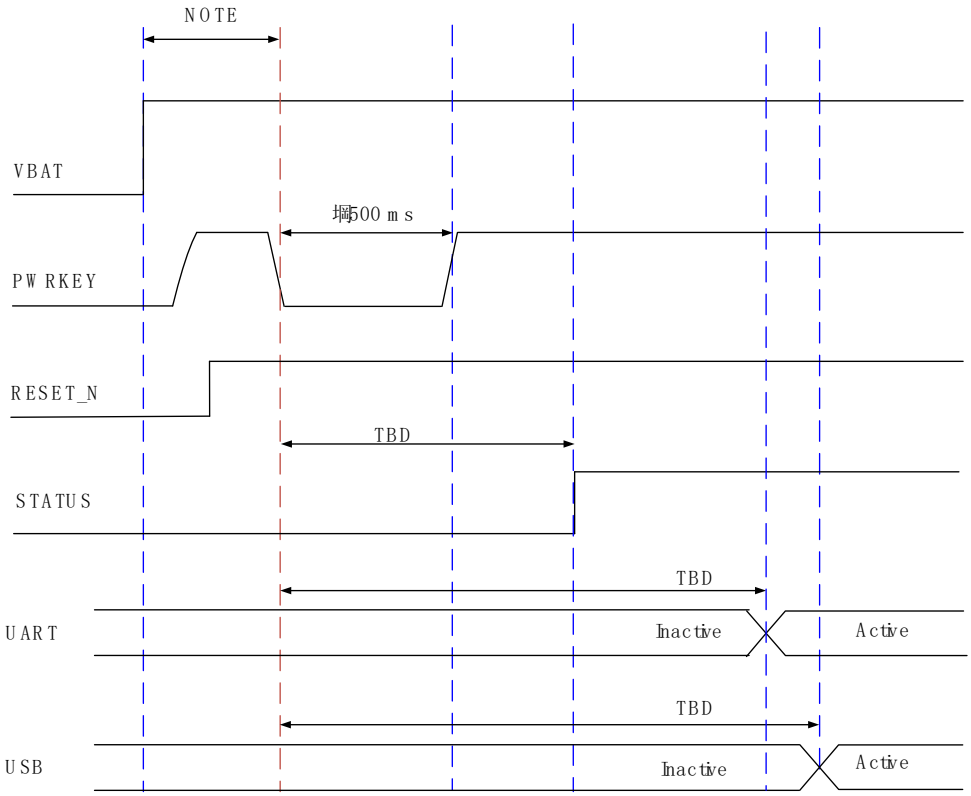


Figure 13: Turn-on Timing

NOTE

Ensure that VBAT is stable for at least 30 ms before pulling down the PWRKEY.

3.6. Turn Off

3.6.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 800 ms, then the module will execute power-down procedure after the PWRKEY is released.

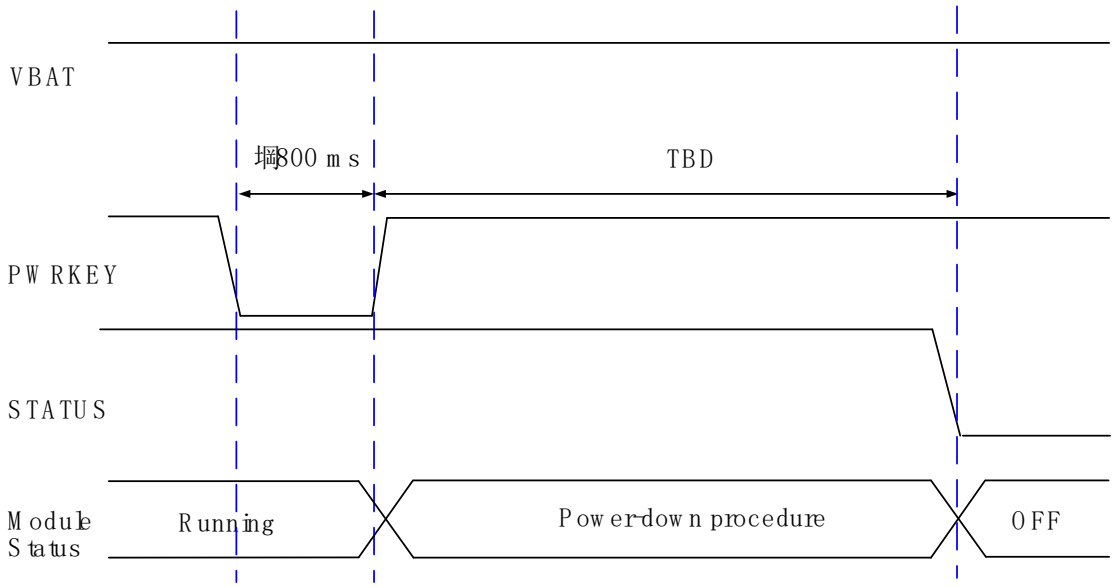


Figure 14: Turn-off Timing

3.6.2. Turn Off with AT Command

It is safe to turn off the module with **AT+QPOWD**, which is similar to turning off the module via PWRKEY.

See ***document [3]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when it works normally. Only after the module is turned off with PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with AT command, please keep PWRKEY at a high level after the execution of turn-off command. Otherwise, the module will be turned on again after being turned off.

3.7. RESET_N

The module can be reset by driving RESET_N low for at least 500 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	8	DI	Resets the module	Internally pulled up to 1.8 V with a 40 kΩ resistor.

The recommended circuit is the same as the PWRKEY control circuit. An open-drain/open-collector driver or button can be used to control the RESET_N.

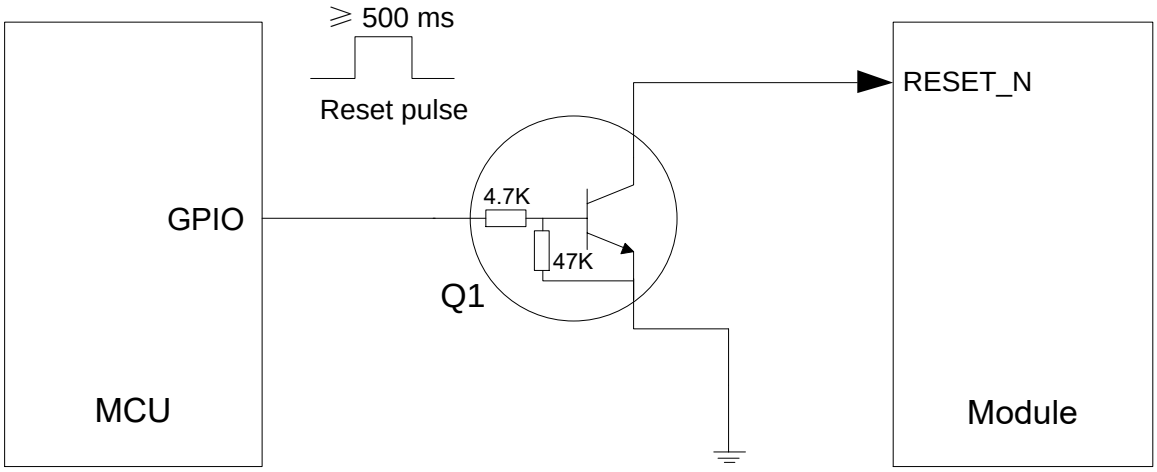


Figure 15: Reference Circuit of RESET_N with Driving Circuit

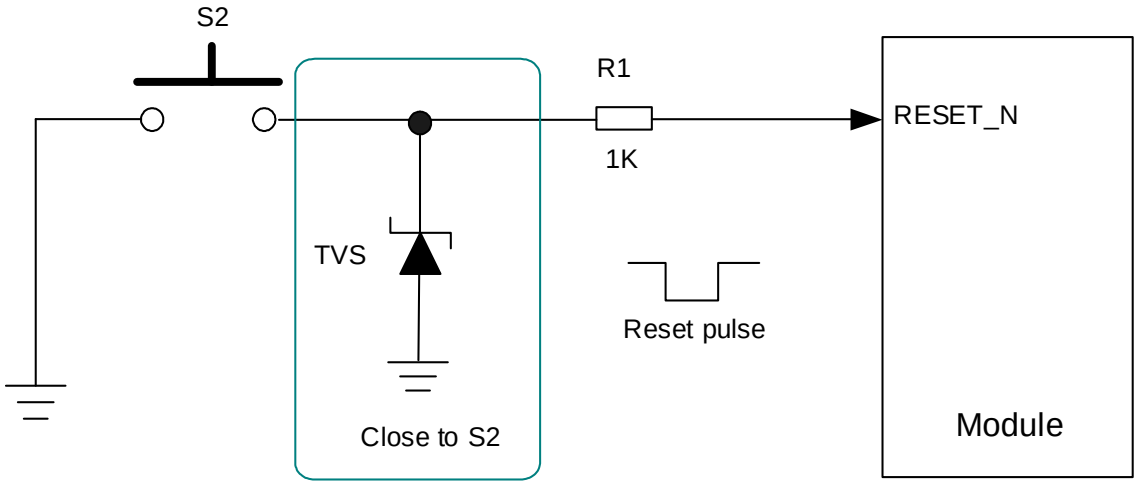


Figure 16: Reference Circuit of RESET_N with a Button

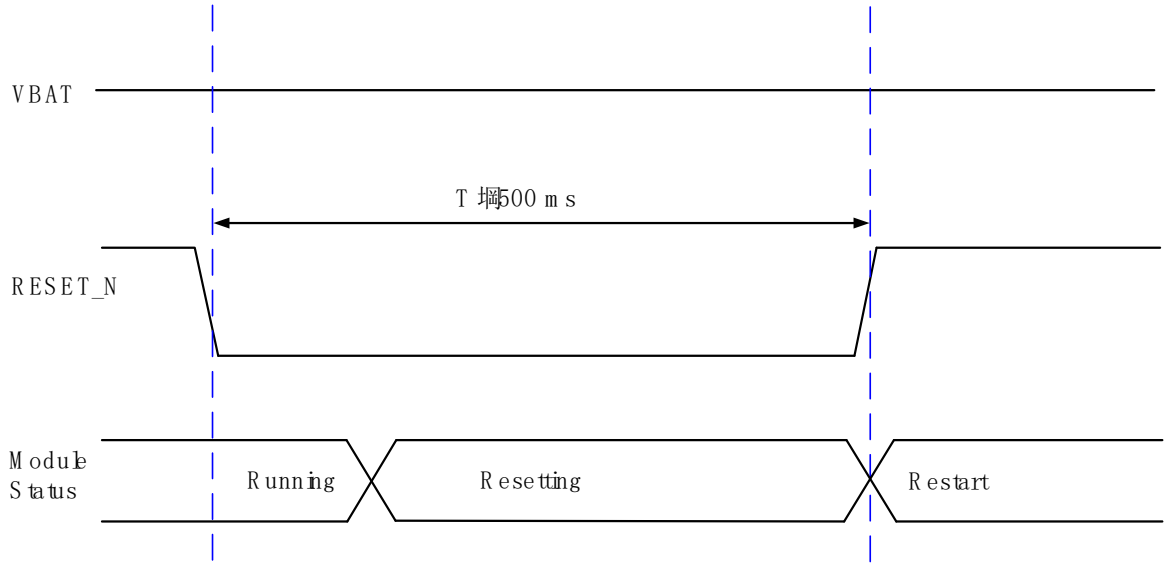


Figure 17: Reset Timing

NOTE

1. Use RESET_N only when you fail to turn off the module with **AT+QPOWD** and PWRKEY.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface. The USB interface complies with the USB 3.1 and USB 2.0 specifications, and supports SuperSpeed (10 Gbps) for USB 3.1 Gen 2, high-speed (480 Mbps) and full-speed (12 Mbps) for USB 2.0.

Table 11: Functions of the USB Interface

Functions	
AT command communication	√
Data transmission	√
GNSS NMEA sentence output	√
Software debugging	√
Firmware upgrade	√
Voice over USB*	√

Pin definition of the USB interface is listed as follows:

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	82	AI	USB connection detect	For USB connection detect only.
USB_DP	83	AIO	USB 2.0 differential data (+)	Requires differential impedance of 90 Ω. USB 2.0 compliant.
USB_DM	85	AIO	USB 2.0 differential data (-)	

USB_SS_TX_P	91	AO	USB 3.1 SuperSpeed transmit (+)	Requires differential impedance of 85 Ω. USB 3.1 Gen 2 compliant.
USB_SS_TX_M	89	AO	USB 3.1 SuperSpeed transmit (-)	
USB_SS_RX_P	88	AI	USB 3.1 SuperSpeed receive (+)	
USB_SS_RX_M	86	AI	USB 3.1 SuperSpeed receive (-)	

Test points must be reserved for debugging and firmware upgrading in your designs. The following figure shows the reference circuit of USB interface.

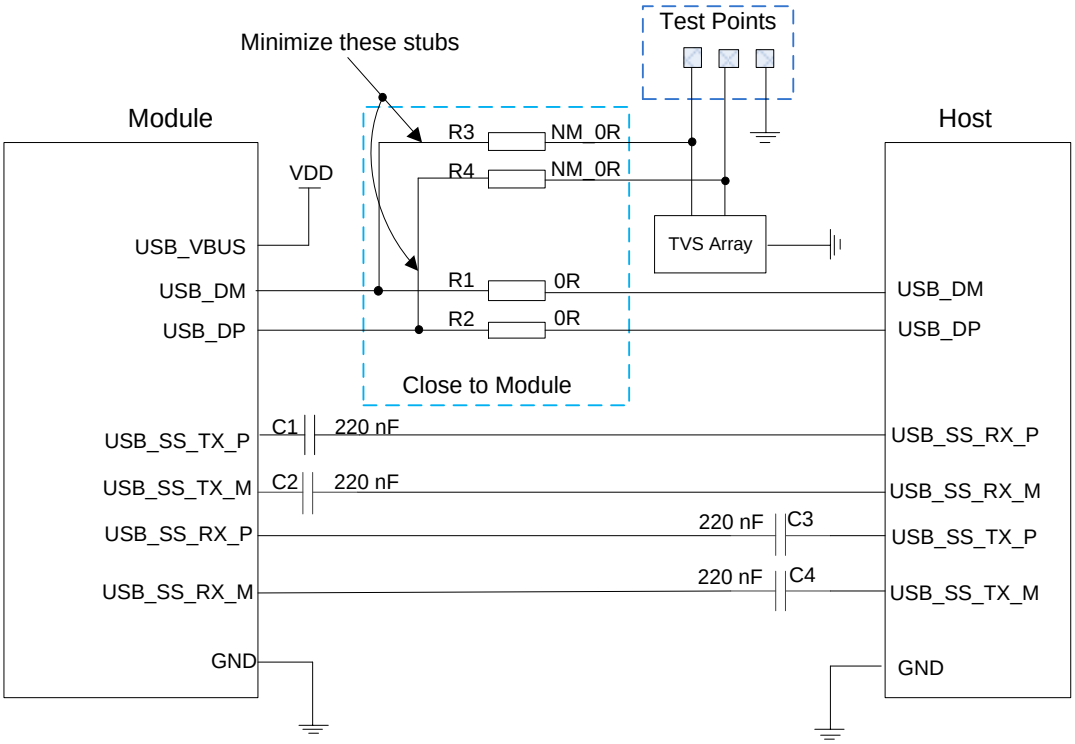


Figure 18: Reference Circuit of USB Application

To ensure the signal integrity of USB data traces, you must place R1, R2, R3, R4, C1 and C2 close to the module, C3 and C4 close to the host, and keep these resistors close to each other. Keep the extra stubs of trace as short as possible.

The following principles should be complied with when designing the USB interface, to meet USB specifications.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB 2.0 differential trace is 90 Ω. The impedance of USB 3.1 differential trace is 85 Ω.

- For USB 2.0 signal traces, the trace length should be less than 250 mm, and the length matching of each differential data pair (DP/DM) should be less than 2 mm (14 ps). For USB 3.1 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.7 mm (5 ps), while the matching between Tx and Rx should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1.
- Keep ESD protection components as close to the USB connector as possible.

For more details about the USB specifications, please visit http://www.usb.org/home.

Table 13: USB Trace Length in the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-M) (mm)
83	USB_DP	31.10	-0.05
85	USB_DM	31.15	
91	USB_SS_TX_P	32.90	-0.12
89	USB_SS_TX_M	33.02	
88	USB_SS_RX_P	30.90	-0.17
86	USB_SS_RX_M	30.73	

NOTE

Both USB 3.1 interface and PCIe interface support data transmission, and USB 3.1 interface is used by default. If you want to use PCIe interface for communication, set it with **AT+QCFG** via USB or main UART. For more details about AT command, see ***document [3]***.

4.2. USB_BOOT

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before turning on the module, thus the module will enter emergency download mode after being turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 14: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description
USB_BOOT	81	DI	Forces the module into emergency download mode

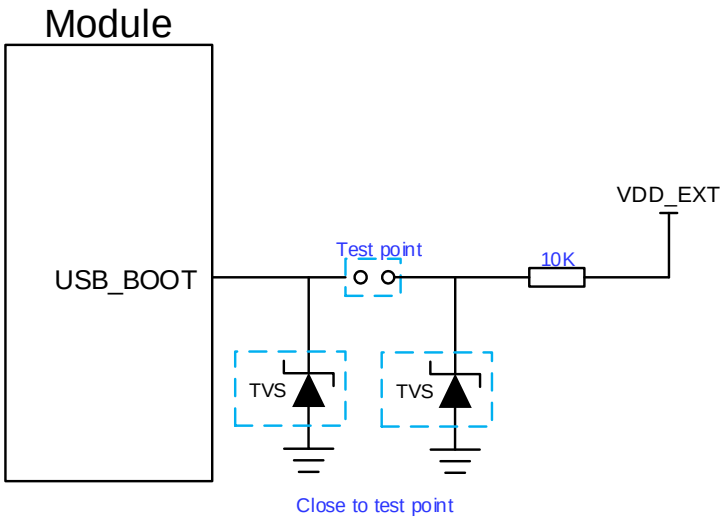


Figure 19: Reference Circuit of USB_BOOT Interface

4.3. (U)SIM Interfaces

(U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both Class B (2.95 V) and Class C (1.8 V) (U)SIM cards are supported, and Dual SIM Single Standby function is supported.

Table 15: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	245	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V is supported and can be identified automatically by the module.
USIM1_DATA	248	DIO	(U)SIM1 card data	
USIM1_CLK	247	DO	(U)SIM1 card clock	
USIM1_RST	244	DO	(U)SIM1 card reset	

USIM1_DET	249	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_VDD	250	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V is supported and can be identified automatically by the module.
USIM2_DATA	251	DIO	(U)SIM2 card data	
USIM2_CLK	253	DO	(U)SIM2 card clock	
USIM2_RST	254	DO	(U)SIM2 card reset	
USIM2_DET	252	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pin, and both high level and low level detection is supported. The function is disabled by default and can be configured via **AT+QSIMDET**. See ***document [3]*** for more details about the command.

The following figure illustrates a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

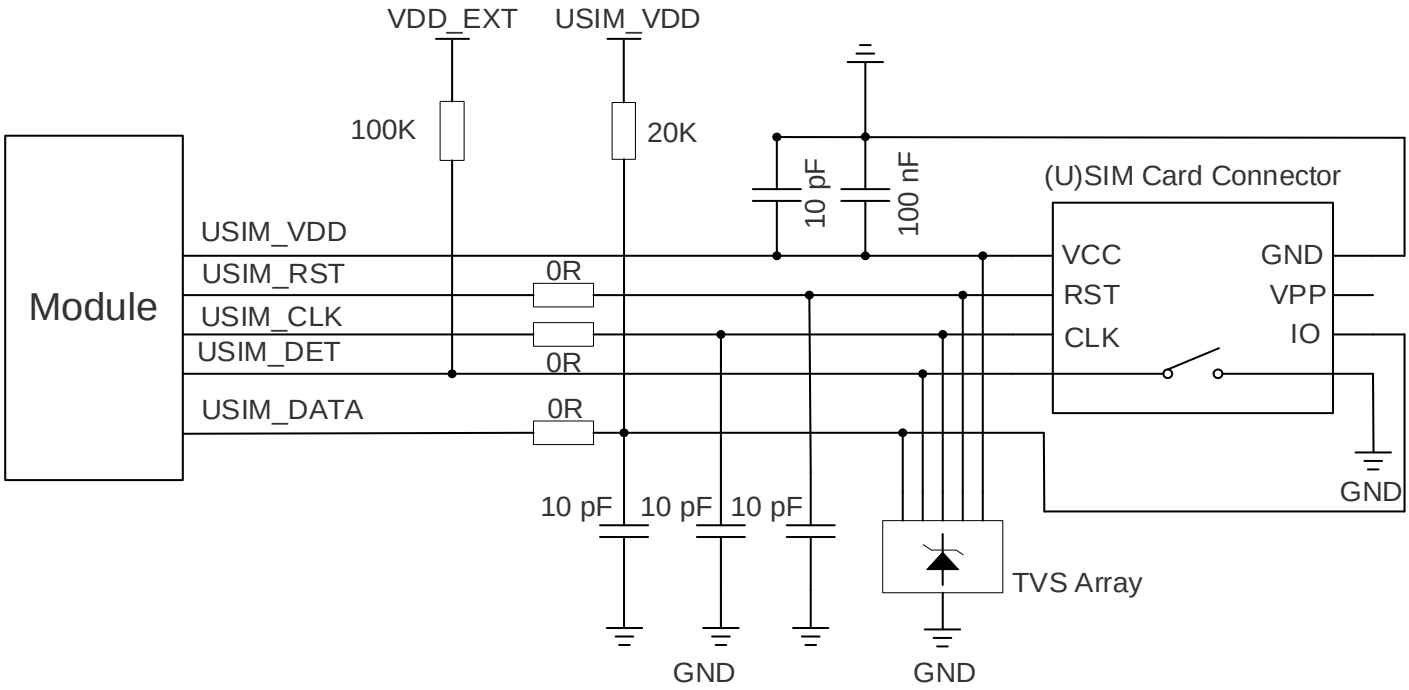


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

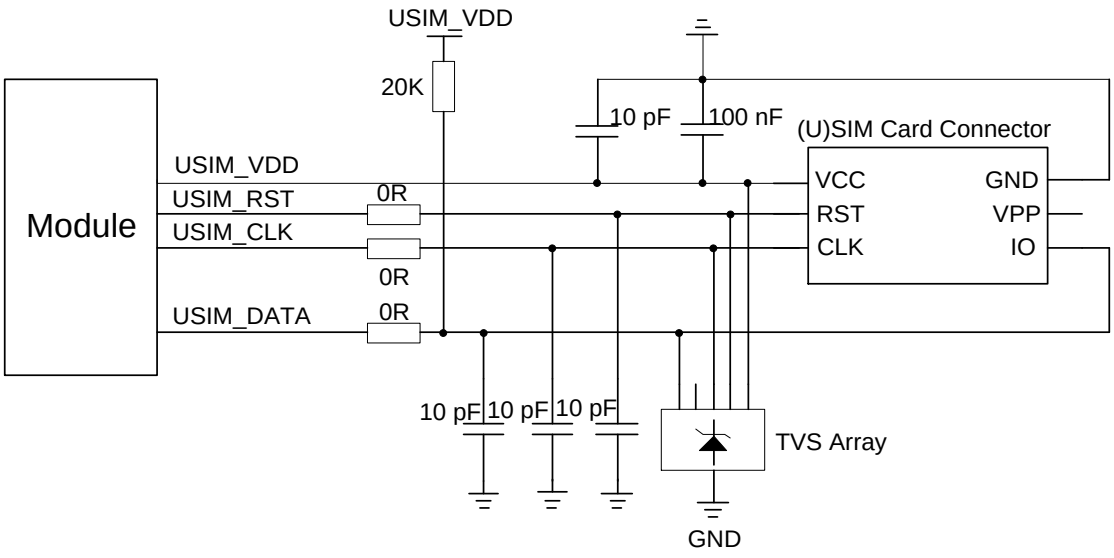


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signal traces away from RF and VBAT traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- To offer better ESD protection, add a TVS array with parasitic capacitance not exceeding 10 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. The 10 pF capacitors are used to filter out RF interference.
- The 20 kΩ pull-up resistor on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.
- A space has been reserved for eSIM inside the module on the (U)SIM2 interface.
- All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

4.4. I2C Interface

The module provides one I2C interface. As an open drain output, it should be pulled up to 1.8 V.

Pin definition is listed as follows:

Table 16: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	77	OD	I2C serial clock	Pull them up to VDD_EXT with an external 4.7 kΩ resistor respectively. If unused, keep them open.
I2C_SDA	78	OD	I2C serial data	

4.5. I2S Interface*

The module provides one I2S interface.

Pin definition is listed as follows:

Table 17: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
I2S_WS	259	DIO	I2S word select	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_SCK	256	DIO	I2S clock	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_DIN	257	DI	I2S data in	
I2S_DOUT	255	DO	I2S data out	
MCLK	79	DO	Master clock output for codec	If unused, keep it open.

The following figure shows a reference design of I2S interface with an external codec IC.

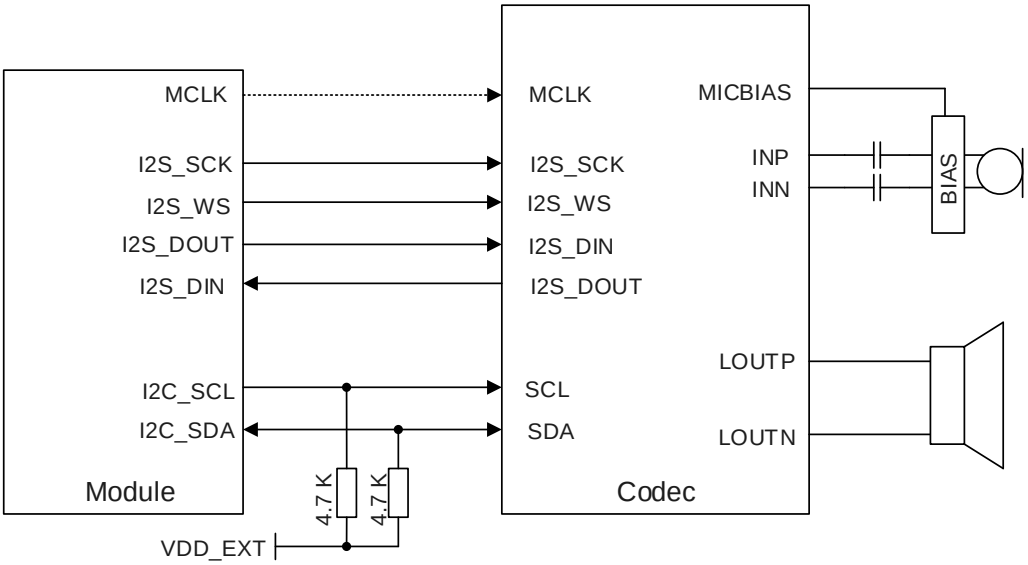


Figure 22: Reference Circuit of I2S Application with Audio Codec

NOTE

The I2S interface can be multiplexed as PCM function and is configured as PCM by default. If you need I2S function, contact Quectel Technical Support.

4.6. PCM Interfaces

The module provides two PCM digital interfaces, one is used for SLIC or Codec (multiplexed with I2S*), the other is only for Bluetooth audio*. PCM interfaces support the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

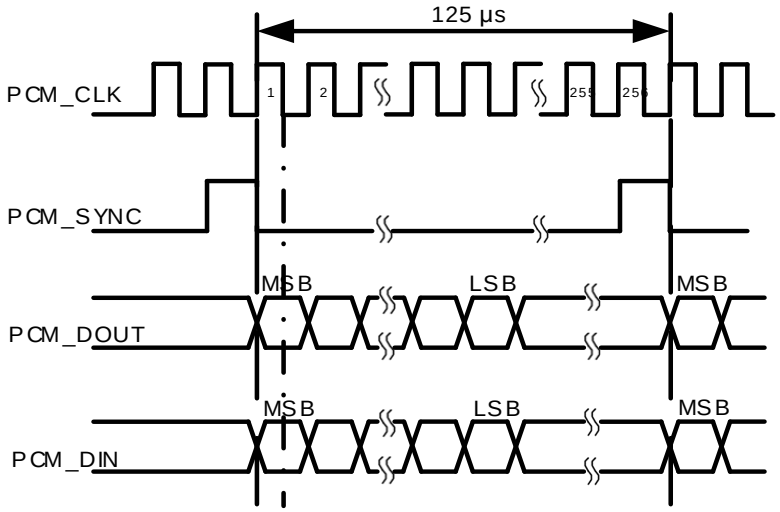


Figure 23: Primary Mode Timing

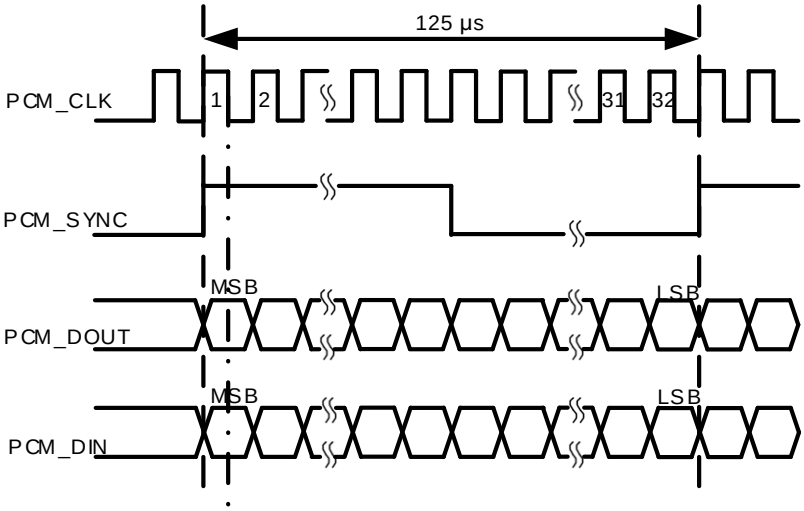


Figure 24: Auxiliary Mode Timing

Clock and mode can be configured via **AT+QDAI**, and the default configuration is master mode using short frame sync format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [3]*** about **AT+QDAI** for details.

4.6.1. PCM for SLIC or Codec

The module provides one PCM interface for SLIC or codec, which is multiplexed with I2S interface. Pin definition of PCM for SLIC or codec is as follows:

Table 18: Pin Definition of PCM Interface for SLIC or Codec

Pin Name	Pin No.	Multiplexed Function	I/O	Description	Comment
I2S_WS	259	PCM_SYNC	DIO	PCM data frame sync	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_SCK	256	PCM_CLK	DIO	PCM clock	In master mode, it is an output signal. In slave mode, it is an input signal.
I2S_DIN	257	PCM_DIN	DI	PCM data input	
I2S_DOUT	255	PCM_DOUT	DO	PCM data output	

The reference design is illustrated as follows:

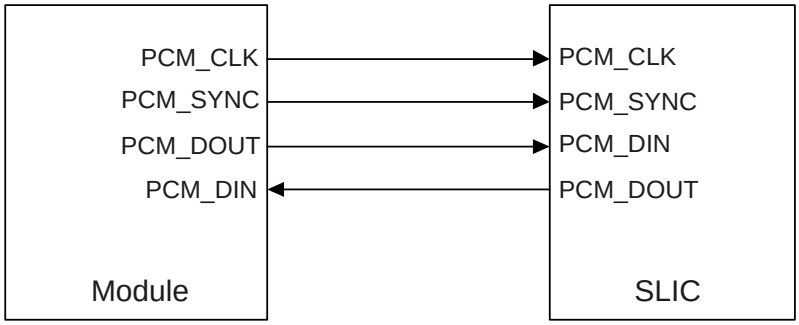


Figure 25: Reference Circuit of SLIC PCM Interface

4.6.2. PCM for Bluetooth Audio*

The module provides one PCM interface only for Bluetooth audio. Pin definition of PCM for Bluetooth audio is as follows:

Table 19: Pin Definition of Bluetooth PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	71	DIO	PCM data frame sync	If unused, keep them open.
PCM_CLK	73	DIO	PCM clock	
PCM_DIN	74	DI	PCM data input	
PCM_DOUT	76	DO	PCM data output	

The reference design is illustrated as follows:

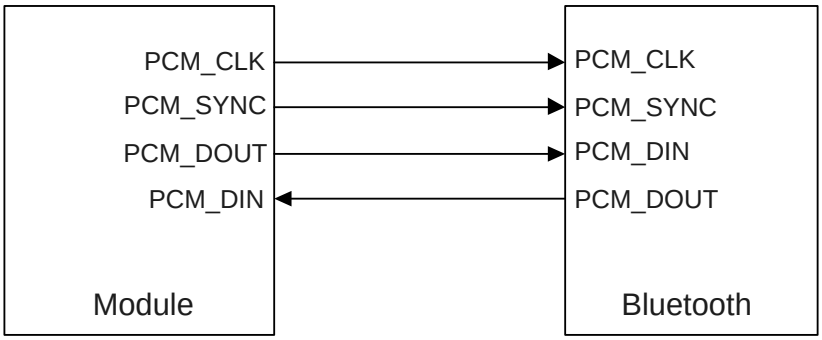


Figure 26: Reference Circuit of Bluetooth PCM Interface

4.7. UART

It provides three UART: main UART, debug UART, Bluetooth UART*. The following shows their features:

- Main UART supports 115200 bps baud rate by default. It is used for AT command communication.
- Debug UART supports 115200 bps baud rate. It is used for Linux console and log output.
- Bluetooth UART supports 115200 bps baud rate. It is used for Bluetooth communication. It supports RTS and CTS hardware flow control.

Pin definition of UART is listed as follows:

Table 20: Pin Definition of UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_TXD	68	DO	Main UART transmit	1.8 V power domain.

MAIN_RXD	70	DI	Main UART receive	
MAIN_RI	100	DO	Main UART ring indication	
MAIN_DTR	258	DI	Main UART data terminal ready	
MAIN_DCD*	261	DO	Main UART data carrier detect	
BT_TXD*	59	DO	Bluetooth UART transmit	
BT_RXD*	63	DI	Bluetooth UART receive	
BT_RTS*	61	DI	Request to send signal to the module	Connect to the peripheral's RTS. 1.8 V power domain.
BT_CTS*	62	DO	Clear to send signal from the module	Connect to the peripheral's CTS. 1.8 V power domain.
DBG_RXD	108	DI	Debug UART receive	1.8 V power domain.
DBG_TXD	105	DO	Debug UART transmit	

The following figure illustrates the reference design for Bluetooth UART.

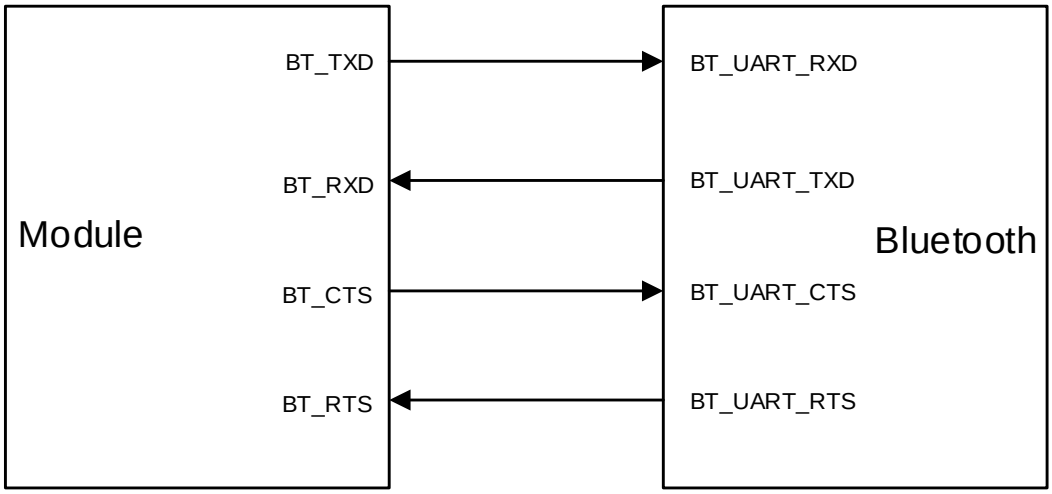


Figure 27: UART Connection

The module provides 1.8 V UART. A voltage-level translator should be used if the application is equipped with a 3.3 V UART.

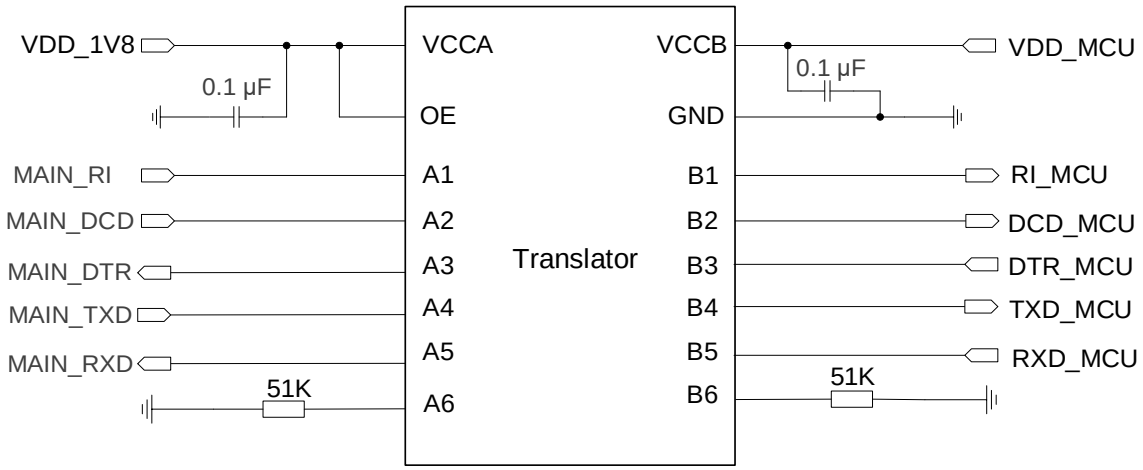


Figure 28: Reference Circuit with a Voltage-level Translator

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

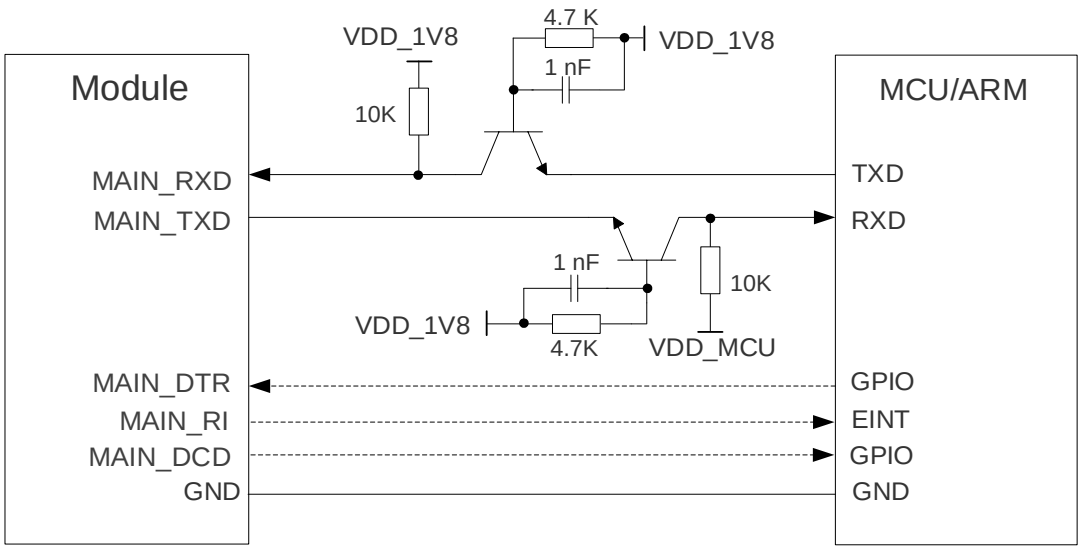


Figure 29: Reference Circuit with Transistor Circuit

NOTE

1. Transistor solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Other baud rates of the main UART are under development.
3. Please note that the module's BT_CTS is connected to the peripheral's CTS, and the module's BT_RTS is connected to the peripheral's RTS.

4.8. SDIO Interface

The module provides one SDIO interface which supports SD 3.0 protocol for SD card connection.

Table 21: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_VDD	60	PI	SDIO power supply	1.8/2.95 V configurable input. If unused, connect it to VDD_EXT.
SDIO_DATA0	49	DIO	SDIO data bit 0	If unused, keep them open.
SDIO_DATA1	50	DIO	SDIO data bit 1	
SDIO_DATA2	51	DIO	SDIO data bit 2	
SDIO_DATA3	52	DIO	SDIO data bit 3	
SDIO_CMD	48	DIO	SDIO command	
SDIO_CLK	47	DO	SDIO clock	
SDIO_PWR_EN	53	DO	SDIO power supply enable	
SDIO_PWR_VSET	56	DO	SDIO power domain set	
SDIO_DET	55	DI	SD card detect	Pull it up to VDD_EXT with a 470 kΩ resistor. If unused, keep it open.

The following figure illustrates a reference design of SDIO interface.

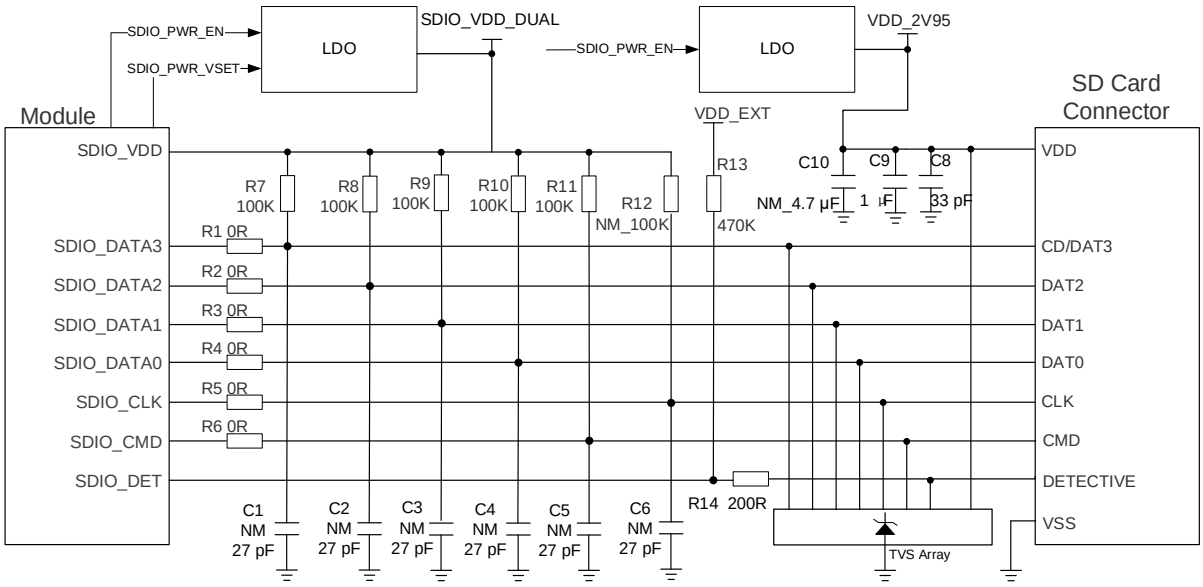


Figure 30: Reference Circuit of SDIO Interface

In SDIO interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD power supply VDD_2V95 is 2.7–3.6 V and a sufficient current of up to 0.8 A should be provided. SDIO_VDD_DUAL is an SDIO bus power domain, which can be used for SD card I/O signals pull-up. Note that SDIO_VDD is an input pin of the module.
- To avoid jitter of bus, pull up SDIO_CMD and SDIO_DATA[0:3] to SDIO_VDD_DUAL with resistors R7 to R11. The resistance can be 10–100 kΩ and 100 kΩ is recommended.
- To improve signal quality, add 0 Ω resistors R1 to R6 in series between the module and the SD card connector. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the SD card connector.
- For good ESD protection, add ESD protection components with capacitance value less than 1.2 pF on each SD card pin.
- Route the SDIO signal traces at inner layer with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noise signals such as clock signals and DC-DC signals.
- Keep the trace length difference between SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD less than 2 mm and the total routing length less than 50 mm for SDR104 mode. For other speed modes, the trace length difference between SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD should be less than 6 mm and the total trace routing length less than 150 mm.
- Make sure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 5.0 pF.
- The DETECTIVE pin of SD card connector must be connected to the module when the SD card function is being used.

Table 22: SDIO Trace Length in the Module

Pin No.	Pin Name	Length (mm)
49	SDIO_DATA0	33.46
50	SDIO_DATA1	33.50
51	SDIO_DATA2	33.15
52	SDIO_DATA3	33.51
48	SDIO_CMD	34.38
47	SDIO_CLK	33.57

4.9. ADC Interface

The module provides one Analog-to-Digital Converter (ADC) interface. In order to improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

Table 23: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description
ADC0	241	AI	General-purpose ADC interface

The voltage value on ADC pin can be read via **AT+QADC=<port>**:

- **AT+QADC=0:** read the voltage value on ADC0

For more details about the AT command, see ***document [3]***.

The following table describes the characteristic of the ADC interface.

Table 24: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	1.875	V

ADC Input Resistance	10	-	-	MΩ
ADC Resolution	-	64.879	-	μV
ADC Sample Clock	-	4.8	-	MHz

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

4.10. SPI

The module provides one SPI which only supports master mode with a maximum clock frequency of up to 50 MHz.

Table 25: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	210	DO	SPI clock	1.8 V power domain. Only master mode is supported.
SPI_CS	207	DO	SPI chip select	
SPI_MISO	213	DI	SPI master-in slave-out	
SPI_MOSI	204	DO	SPI master-out slave-in	

The module provides a 1.8 V SPI. Use a voltage-level translator between the module and the peripheral device if the peripheral device is 3.3 V power domain. The following figure shows the reference design.

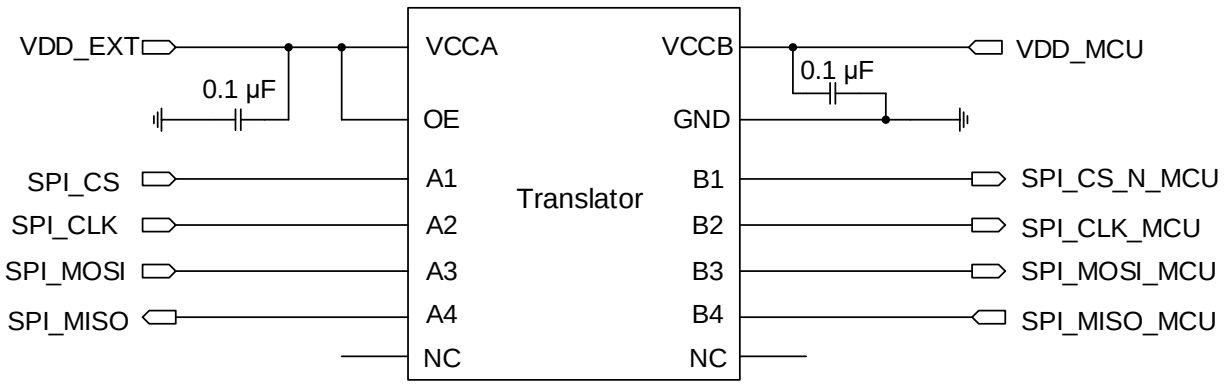


Figure 31: Reference Circuit of SPI with a Voltage-level Translator

4.11. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface. The key features of the PCIe interface are mentioned below:

- *PCI Express Specification Revision 3.0* compliance.
- Data rate at 8 Gbps per lane for PCIe 3.0.
- Used to connect to an external Ethernet IC (MAC and PHY) or Wi-Fi IC.

Table 26: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)	In root complex mode, it is an output signal. In endpoint mode, it is an input signal. Requires differential impedance of 85 Ω.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)	
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)	Requires differential impedance of 85 Ω. If unused, keep them open.
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)	
PCIE_TX1_M	41	AO	PCIe transmit 1 (-)	
PCIE_TX1_P	43	AO	PCIe transmit 1 (+)	
PCIE_RX0_M	32	AI	PCIe receive 0 (-)	

PCIE_RX0_P	34	AI	PCIe receive 0 (+)	
PCIE_RX1_M	35	AI	PCIe receive 1 (-)	
PCIE_RX1_P	37	AI	PCIe receive 1 (+)	
PCIE_CLKREQ_N	36	OD	PCIe clock request	1.8 V power domain. In root complex mode, it is an input signal. In endpoint mode, it is an output signal.
PCIE_RST_N	39	DIO	PCIe reset	1.8 V power domain. In root complex mode, it is an output signal. In endpoint mode, it is an input signal.
PCIE_WAKE_N	30	OD	PCIe wake up	1.8 V power domain. In root complex mode, it is an input signal. In endpoint mode, it is an output signal.

The following figure illustrates the PCIe interface connection.

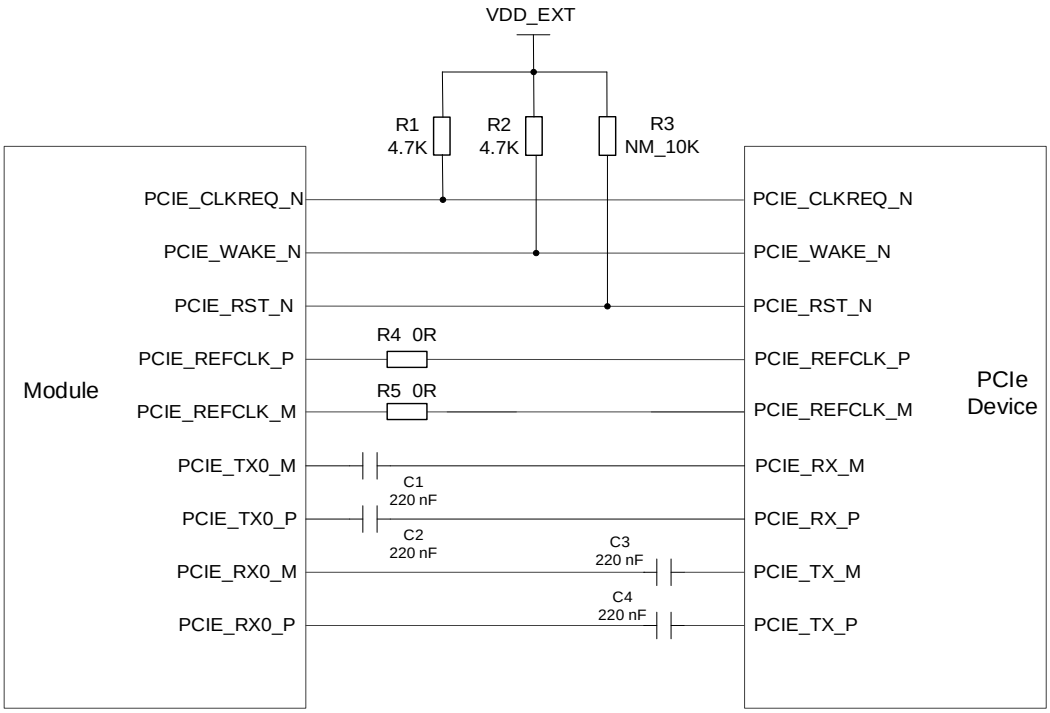


Figure 32: PCIe Interface Connection

The following principles of PCIe interface design should be complied with to meet PCIe specifications.

- Route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 72.5–97.5 Ω and 85 Ω is recommended.
- PCIe signals must be protected from noise signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, intra-lane length match should be less than 0.7 mm. The total bus length should be less than 300 mm for PCIe 3.0.
- Inter-lane length match, i.e., the trace length matching between the reference clock (Tx and Rx pairs) is not required.
- The space between Tx and Rx, and the space between PCIe lanes and all other signals, should be larger than 4 times of the trace width.
- PCIe Tx AC coupling capacitors can be placed anywhere along the trace, but better to be placed close to source or connector side to keep good signal integrity of main route on PCB. PCIe Tx AC coupling capacitors should be 220 nF for Gen 3 and 100 nF for Gen 2/Gen 1.
- Ensure not to stagger the capacitors since this will affect the differential integrity of the design and create EMI.
- In the case of trace serpentines, one line of a differential pair must be routed to make up a length delta, then it must be routed at the source (breakout) – this ensures that traces stay differential thereafter.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions on the main route (in other words, apply layer transitions only at module breakouts and connectors to ensure minimum layer transitions on the main route).

Table 27: PCIe Trace Length in the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-M) (mm)
40	PCIE_REFCLK_P	7.52	-0.06
38	PCIE_REFCLK_M	7.58	
46	PCIE_TX0_P	12.87	-0.03
44	PCIE_TX0_M	12.90	
43	PCIE_TX1_P	10.36	-0.01
41	PCIE_TX1_M	10.37	
34	PCIE_RX0_P	3.92	-0.17
32	PCIE_RX0_M	4.09	
37	PCIE_RX1_P	4.88	0.03

35	PCIE_RX1_M	4.85

4.12. Control Signal

Pin definition of control signal is listed as follows:

Table 28: Pin Definition of Control Signal

Pin Name	Pin No.	I/O	Description
W_DISABLE#	114	DI	Airplane mode control

4.12.1. W_DISABLE#

The module provides a W_DISABLE# pin to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode.

The RF function can also be enabled or disabled through software AT commands.

Table 29: RF Function Status

Logic Level	AT Command	RF Function	Operating Mode
High Level	**AT+CFUN=1**	Enabled	Full functionality mode
	AT+CFUN=0	Disabled	Minimum functionality mode
	AT+CFUN=4	Disabled	Airplane mode
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled	Airplane mode

4.13. Indication Signals

Pin definition of indication signals is as follows:

Table 30: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	240	DO	Indicates the module's network registration mode	1.8 V power domain.
STATUS	237	DO	Indicates the module's operation status	
NET_STATUS	243	DO	Indicates the module's network activity status	
SLEEP_IND	102	DO	Indicates the module's sleep mode	

4.13.1. Network Status Indication

These network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET_MODE and NET_STATUS. The following table describes logic level changes in different network status.

Table 31: Working State of the Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling
	Always Low	Minimum functionality mode

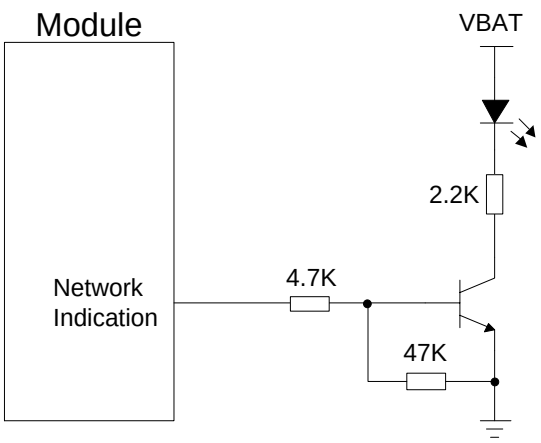


Figure 33: Reference Circuit of the Network Status Indication

4.13.2. STATUS

The STATUS pin indicates the module's operation status. It will output high level when the module is powered on successfully.

A reference circuit is shown as below.

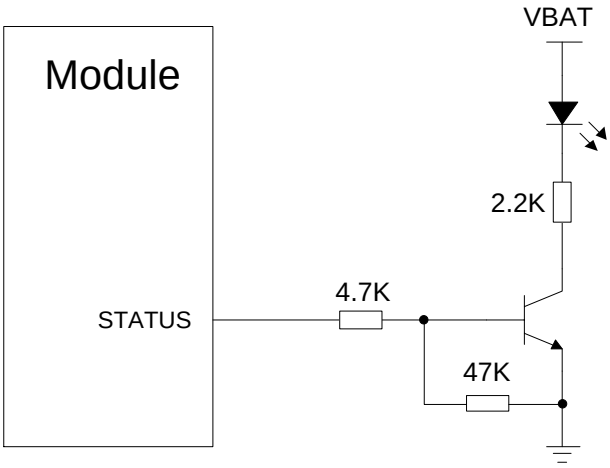


Figure 34: Reference Circuit of STATUS

4.13.3. IPQ Status and Err Fatal Interface

The module provides one IPQ status interface and one err fatal interface for connection between the module and IPQ. Pin definition of IPQ status and err fatal interfaces is as follows:

Table 32: Pin Definition of IPQ Status and Err Fatal Interface

Pin Name	Pin No.	Multiplexed Function	I/O	Description
COEX_RXD	65	SDX2AP_E911	DO	Module to AP err fatal
COEX_TXD	67	SDX2AP_STATUS	DO	Module to AP status
GPIO_32	98	AP2SDX_STATUS	DI	AP to module status

The following figure shows a reference design of the module with IPQ GPIOs.

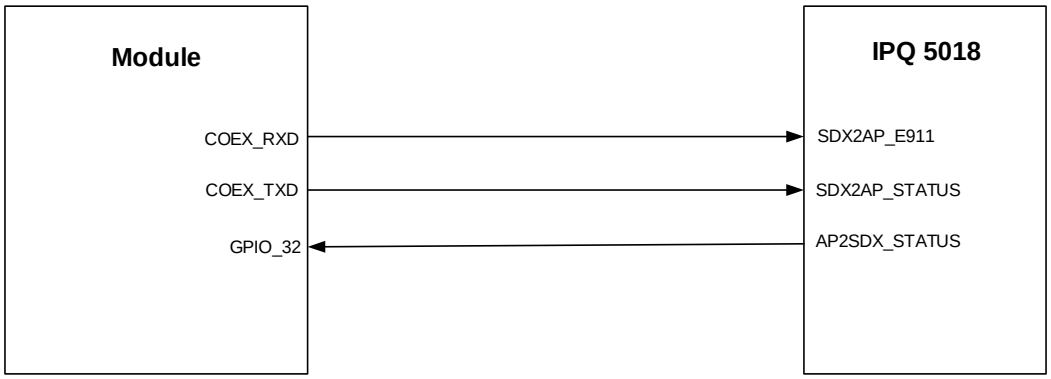


Figure 35: Module with IPQ GPIO Application

NOTE

1. IPQ indicates an application processor, and IPQ5018 is used by default here.
2. For details, contact Quectel Technical Support.

4.14. MAIN_RI

AT+QCFG= "risignaltype", "physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI pin.

NOTE

The URC can be outputted via UART, USB AT port and USB modem port, which can be set via **AT+QURCCFG**. The default port is USB AT port.

In addition, MAIN_RI behaviors can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 33: Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"**.

4.15. Time Service and Repeater Interface

Time service provides time information for other devices or systems through standard or customized interfaces and protocols. Its basic channels are shortwave, TV signals, cables, networks, satellites, base stations, etc.

Repeater is a kind of wireless signal relay device, which amplifies the base station signal and then transmits it to areas with weak signal coverage, expanding the network coverage.

With GNSS time service and repeater functions, the module can provide 1PPS pulse output, and can execute time service through AT commands based on baseline SIB9 system messages.

Table 34: Pin Definition of Time Service and Repeater Function

Pin Name	Pin No.	I/O	Description	Comment
GPIO_32	98	DO	Supports time service and repeater functions; supports 1PPS pulse output and frame synchronization	1.8 V power domain. The pin can be multiplexed into AP2SDX_STATUS function. For details, contact Quectel Technical Support.

NOTE

If GPIO_32 is needed for other purposes, its default function should be disabled in the relevant software configuration.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

Table 35: Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - **5G NR**: n77 TRX0 - **LTE**: LMB_TRX0 & HB_DRX - **Refarmed**: LMB_TRX0 & HB_TRX1	50 Ω impedance.
ANT1	157	AIO	**Antenna 1 interface:** - **5G NR**: n77 DRX MIMO - **LTE**: LMB_PRX MIMO & HB_DRX MIMO - **Refarmed**: LMB_PRX MIMO & HB_DRX MIMO	
ANT2	166	AIO	**Antenna 2 interface:** - **5G NR**: n77 PRX MIMO - **LTE**: LMB_DRX MIMO & HB_PRX MIMO - **Refarmed**: LMB_DRX MIMO & HB_PRX MIMO	
ANT3	184	AIO	**Antenna 3 interface:** - **5G NR**: n77 TRX1 - **LTE**: LMB_TRX1 & HB_TRX0 - **Refarmed**: LMB_TRX1 & HB_TRX0	

Table 36: Cellular Network Antenna Mapping

Antenna	LTE	5G NR		LB (MHz)	MHB (MHz)	n77 (MHz)
		Refarmed	n77			
ANT0	LMB_TRX0, HB_DRX	LMB_TRX0, HB_TRX1	TRX0	617–894	1710–2690	3300–4200
ANT1	LMB_PRX MIMO, HB_DRX MIMO,	LMB_PRX MIMO, HB_DRX MIMO	DRX MIMO	617–894	1710–2690	3300–4200
ANT2	LMB_DRX MIMO, HB_PRX MIMO,	LMB_DRX MIMO, HB_PRX MIMO	PRX MIMO	617–894	1710–2690	3300–4200
ANT3	LMB_TRX1, HB_TRX0	LMB_TRX1, HB_TRX0	TRX1	617–894	1710–2690	3300–4200

NOTE

1. LTE LMB_TRX1 is activated when 5G NR FDD low/middle bands are supported in NSA mode.
2. TRX0/1 = TX0/1 + PRX/DRX.

5.1.2. Antenna Tuner Control Interfaces*

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 37: Pin Definition of Antenna Tuner Control Interfaces

Pin Name	Pin No.	I/O	Default Status	Description	Comment
SDR_GRFC0	171	DO	PD	GRFC interfaces dedicated for external antenna tuner control	If unused, keep them open.
SDR_GRFC1	174	DO	PD		

Table 38: Logic Levels of Antenna Tuner Control Interfaces

Parameter	Min.	Max.	Unit
V_{OL}	-	0.45	V
V_{OH}	1.35	-	V

Table 39: Truth Table of Antenna Tuner Control Interfaces

GRFC0 Level	GRFC1 Level	Frequency Range (MHz)	Band
Low	Low	TBD	TBD
Low	High	TBD	TBD
High	Low	TBD	TBD
High	High	TBD	TBD

5.1.3. Tx Power

The following table shows the RF output power of the module.

Table 40: Tx Power

Mode	Frequency Bands	Max. Tx Power	Min. Tx Power
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	5G NR HPUE band (n77)	26 dBm +2/-3 dB (Class 2)	< -40 dBm

NOTE

For 5G NR bands, they have different standards for different channel bandwidth, see the specifications as described in ***Clause 6.3.1*** of *TS 38.101-1 [2]*.

5.1.4. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 41: Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [8]	
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B14 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B17 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B29 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B30 (10 MHz)	TBD	TBD	TBD	-95.3
LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	-95.8
5G NR FDD n2 (20 MHz)	TBD	TBD	TBD	-94.5
5G NR FDD n5 (20 MHz)	TBD	TBD	TBD	-90.8
5G NR FDD n12 (10 MHz)	TBD	TBD	TBD	-93.8
5G NR FDD n14 (10 MHz)	TBD	TBD	TBD	-93.8
5G NR FDD n29 (10 MHz)	TBD	TBD	TBD	TBD
5G NR FDD n30 (10 MHz)	TBD	TBD	TBD	-95.8
5G NR FDD n66 (40 MHz)	TBD	TBD	TBD	-93
5G NR TDD n77 (100 MHz)	TBD	TBD	TBD	-87.3

[8] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas, and 5G n2/n30/n66/n77 bands are tested with 4 Rx antennas and 5G n5/n12/n14/n29 bands are tested with 2 Rx antennas.

5.1.5. Reference Design

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (like C1, R1, and C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

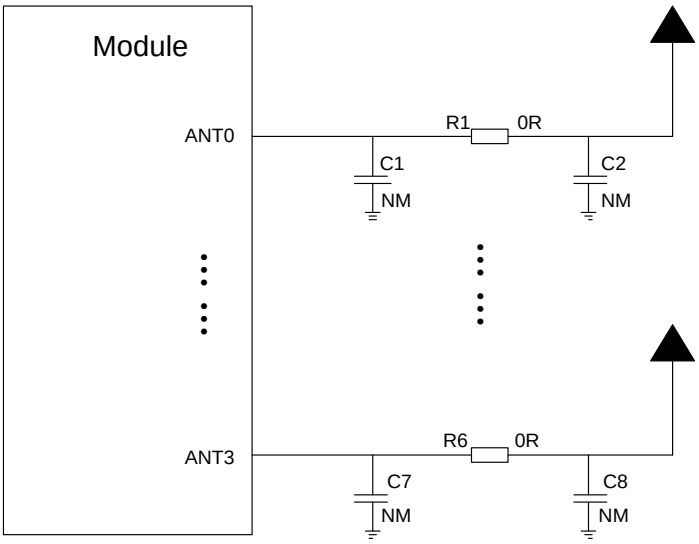


Figure 36: Reference Circuit for Cellular Antenna Interfaces

NOTE

1. Use a π-type circuit for all the antenna circuits to facilitate future debugging.
2. Keep the impedance of the cellular antennas (ANT0–ANT3) traces as 50 Ω when routing.
3. Keep at least 15 dB isolation between cellular antennas to improve the receiving sensitivity, and at least 20 dB isolation between 5G NR UL MIMO antennas.
4. The isolation between each antenna trace on PCB is recommended to be more than 75 dB.
5. Keep digital circuits such as switch mode power supply, (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.

5.2. GNSS

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences via USB interface (data update rate: 1–10 Hz, 1 Hz by default).

By default, the module's GNSS function is disabled. It must be enabled via **AT+QGPS=1**. For more details about GNSS function's technology and configurations, see ***document [4].***

5.2.1. Antenna Interface & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 42: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	193	AI	GNSS antenna interface	50 Ω impedance.

Table 43: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023 (GPS L1) 1176.45 ±10.23 (GPS L5)	MHz
GLONASS	1597.5–1605.8	
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)	
BDS	1561.098 ±2.046	
QZSS	1575.42 (L1) 1176.45 (L5)	

5.2.2. GNSS Performance

Table 44: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Acquisition	Autonomous	TBD	dBm
	Reacquisition		TBD	
	Tracking		TBD	
TTFF (GNSS)	Cold start		TBD	s
	@ open sky	XTRA enabled	TBD	

	Warm start	Autonomous	TBD	
	@ open sky	XTRA enabled	TBD	
	Hot start	Autonomous	TBD	
	@ open sky	XTRA enabled	TBD	
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

The following is the reference circuit of GNSS antenna.

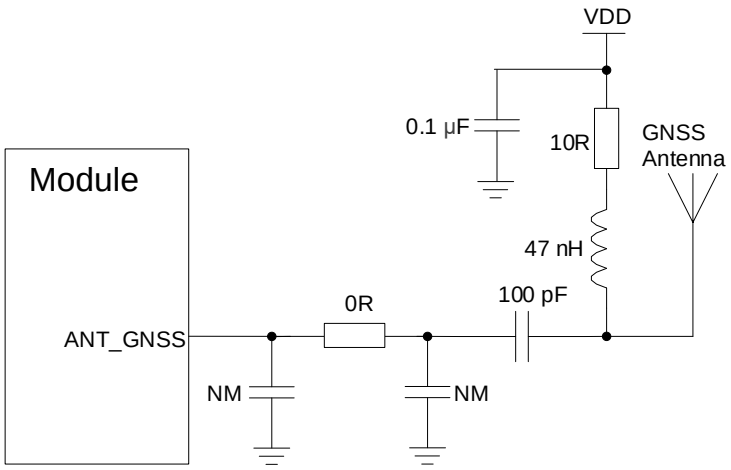


Figure 37: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected when supplying power according to the active antenna

requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.
3. Keep the characteristic impedance for ANT_GNSS trace as 50 Ω.
4. Place the π-type matching components as close to the antenna as possible.
5. Keep digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.
6. The isolation between each antenna trace on PCB is recommended to be more than 75 dB.
7. Keep at least 15 dB isolation between GNSS and cellular antennas to improve the receiving sensitivity.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

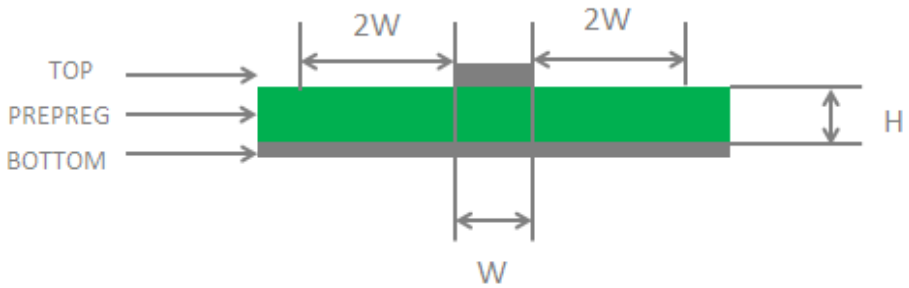


Figure 38: Microstrip Design on a 2-layer PCB

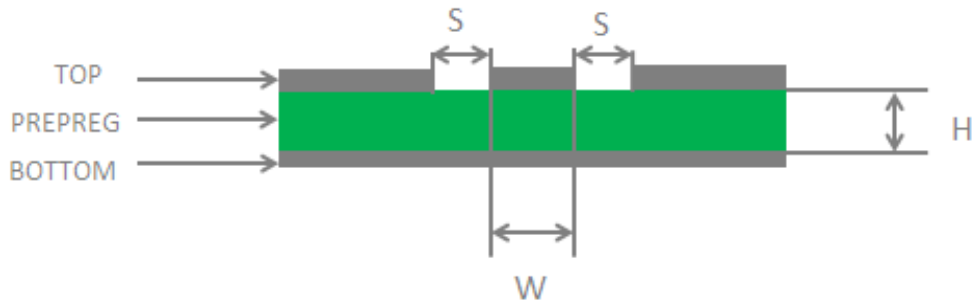


Figure 39: Coplanar Waveguide Design on a 2-layer PCB

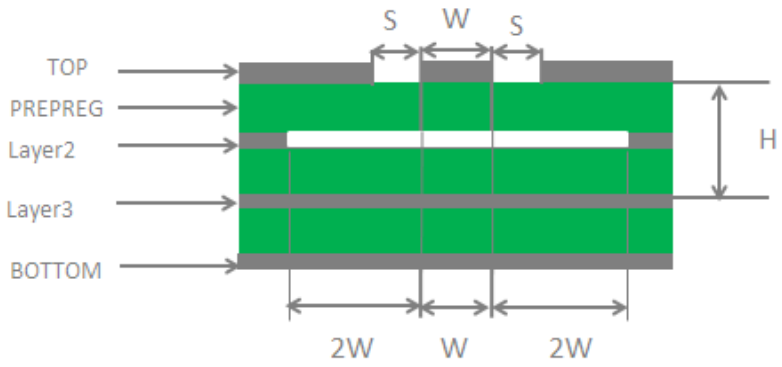


Figure 40: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

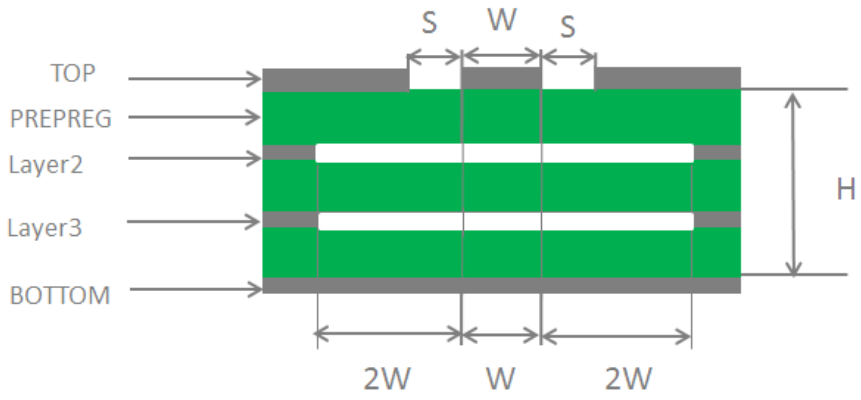


Figure 41: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

5.4. Antenna Design Requirements

Table 45: Antenna Design Requirements

Antenna Type	Requirements
GNSS	● Frequency range: L1: 1559–1609 MHz L5: 1166–1187 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.) ● Passive antenna gain: > 0 dBi
5G NR/LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max input power: 50 W ● Input impedance: 50 Ω ● Polarization: Vertical ● Cable insertion loss: - **< 1 dB:** LB (< 1 GHz) - **< 1.5 dB:** MB (1–2.3 GHz) - **< 2 dB:** HB (> 2.3 GHz)

NOTE

It is recommended to use a passive GNSS antenna when LTE B14 is supported, as the use of active

antenna may generate harmonics which will affect the GNSS performance.

5.5. RF Connector Recommendation

The receptacle dimensions are illustrated as below.

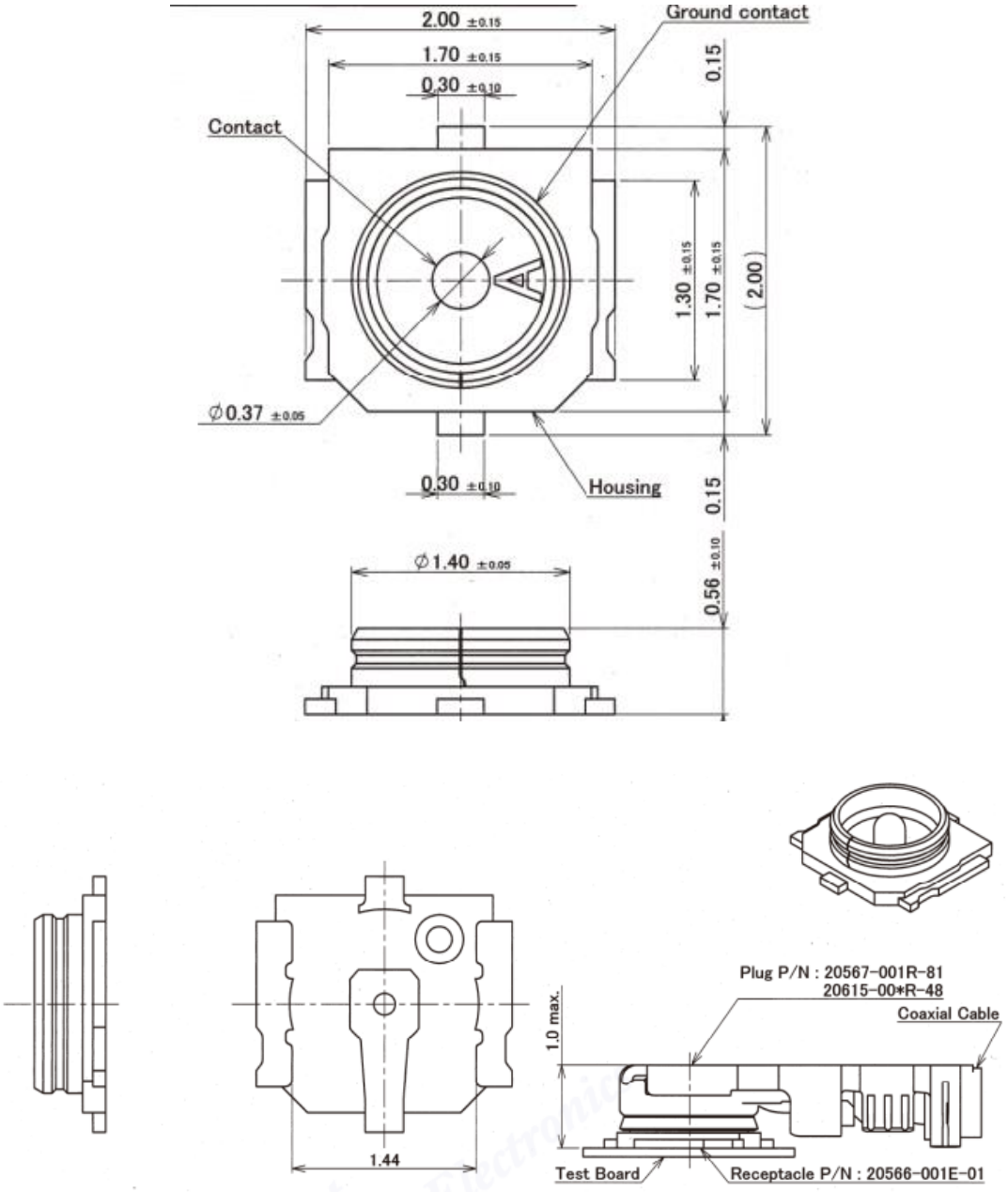


Figure 42: Dimensions of the Receptacles (Unit: mm)

The following figure shows the dimensions of mated plugs using Ø0.81 mm coaxial cables.

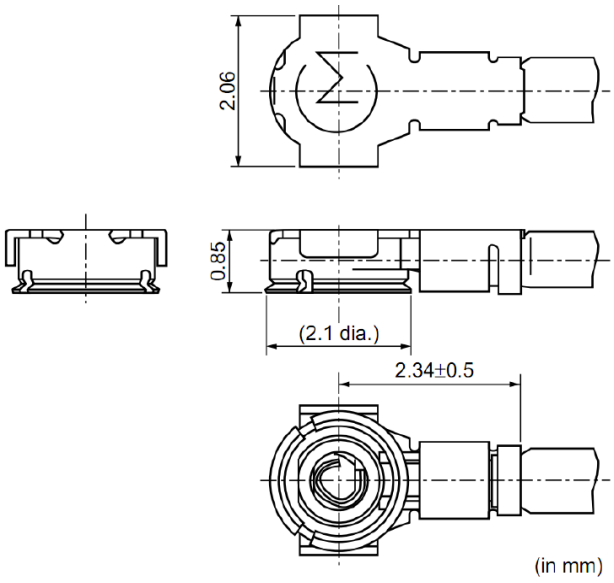


Figure 43: Dimensions of Mated Plugs Using Ø0.81 mm Coaxial Cables (Unit: mm)

5.5.1. Recommended RF Connector for Installation

5.5.1.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

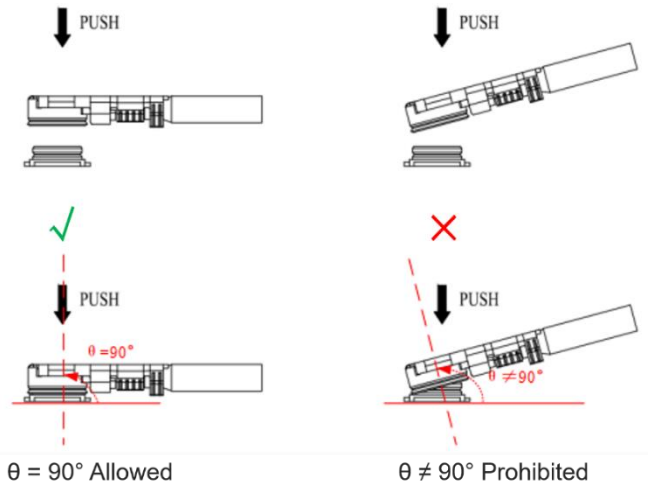


Figure 44: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

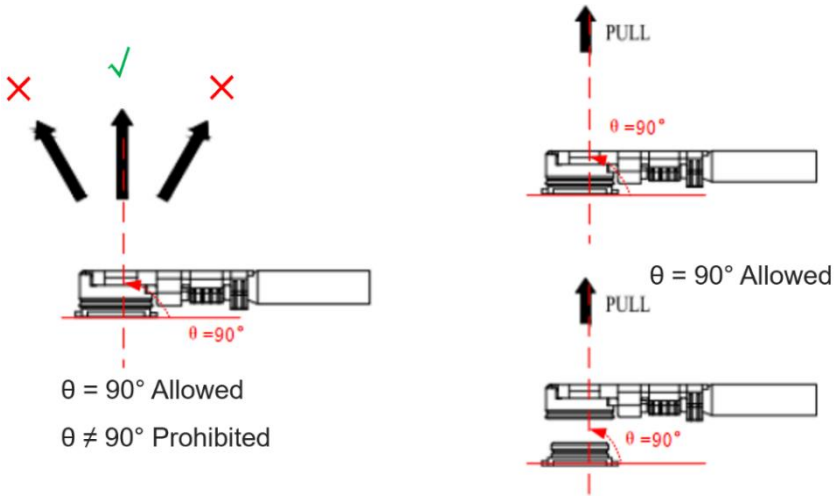


Figure 45: Pull out a Coaxial Cable Plug

5.5.1.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

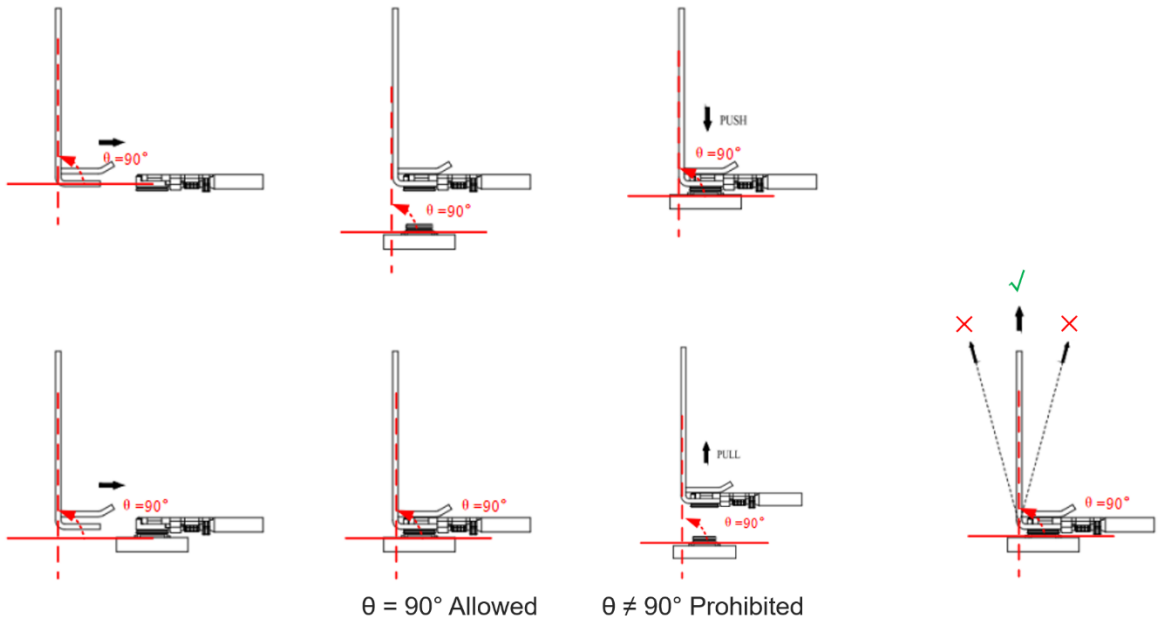


Figure 46: Install the Coaxial Cable Plug with Jig

5.5.2. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 46: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.5	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.32	A
Peak Current of VBAT_RF	-	3.2	A
Voltage at Digital Pins	-0.5	2.2	V
Voltage at ADC0	-0.5	2.2	V

6.2. Power Supply Ratings

Table 47: Module Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum	3.3	3.8	4.4	V

		values.				
USB_VBUS	USB connection detect		3.3	5.0	5.25	V

6.3. Power Consumption

Table 48: Power Consumption

Mode	Conditions	Band/Combinations	Current	Unit
Power-off	Power off	-	150	μA
RF Disabled	**AT+CFUN=0** (USB 3.0 suspend)	-	4	mA
	AT+CFUN=4 (USB 3.0 suspend)	-	4.1	mA
Sleep State	SA FDD PF = 64 (USB 3.0 suspend)	-	9.3	mA
	SA TDD PF = 64 (USB 3.0 suspend)	-	9.3	mA
Idle State	SA PF = 64 (USB 2.0 active)	-	40	mA
	SA PF = 64 (USB 3.0 active)	-	60	mA
LTE	LTE LB @ 23 dBm	B5	TBD	mA
	LTE MB @ 23 dBm	B2	TBD	mA
	LTE HB @ 23 dBm	B30	TBD	mA
LTE CA	DL 3CA, 256QAM	CA_2A-5A-66A	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA (1 Tx)	5G NR LB @ 23 dBm	n12	TBD	mA
	5G NR MB @ 23 dBm	n66	TBD	mA
	5G NR HB @ 23 dBm	n30	TBD	mA
	5G NR UHB @ 26 dBm	n77	TBD	mA
5G SA (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n77	TBD	mA

5G SA CA	DL 2CA, 256QAM	CA_n77C	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 26 dBm			
LTE + 5G EN-DC	LTE DL, 256QAM	DC_2A-n77	TBD	mA
	LTE UL QPSK			
	NR DL, 256QAM			
	NR UL QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

6.4. Digital I/O Characteristics

Table 49: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.26	2.1	V
V_{IL}	Input low voltage	-0.3	0.54	V
V_{OH}	Output high voltage	1.35	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 50: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	Input high voltage	1.26	2.1	V
V_{IL}	Input low voltage	-0.3	0.36	V
V_{OH}	Output high voltage	1.44	-	V

V_{OL}	Output low voltage	-	0.4	V

Table 51: (U)SIM 2.95 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	2.06	3.25	V
V_{IL}	Input low voltage	-0.3	0.59	V
V_{OH}	Output high voltage	2.36	-	V
V_{OL}	Output low voltage	-	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 52: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 53: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [9]	-30	+25	+75	°C
Extended Temperature Range [10]	-40	-	+85	°C
Storage temperature range	-40	-	+90	°C

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation;
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

[9] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
[10] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

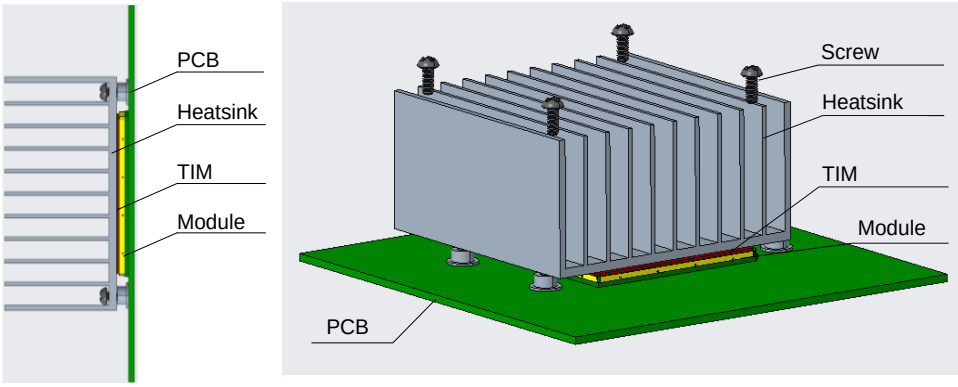


Figure 47: Placement and Fixing of the Heatsink

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

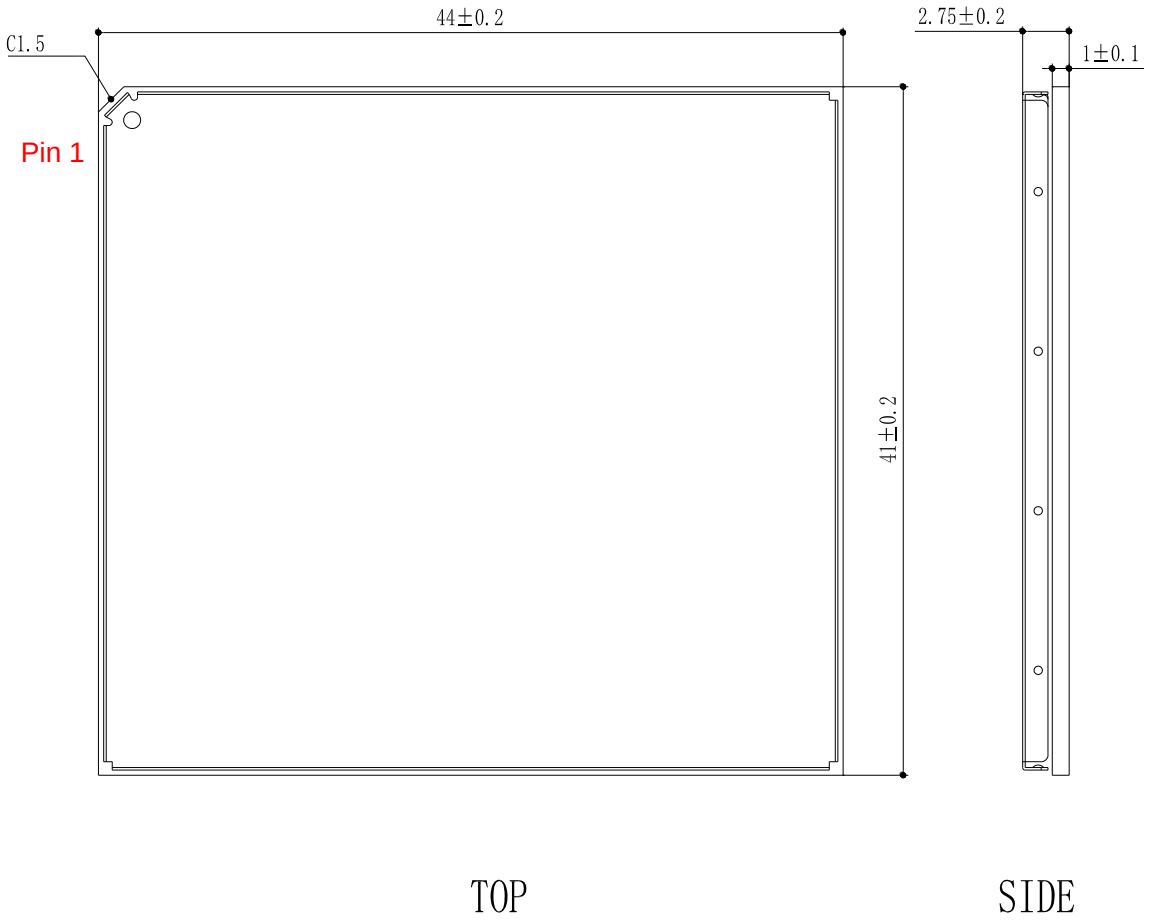


Figure 48: Module Top and Side Dimensions

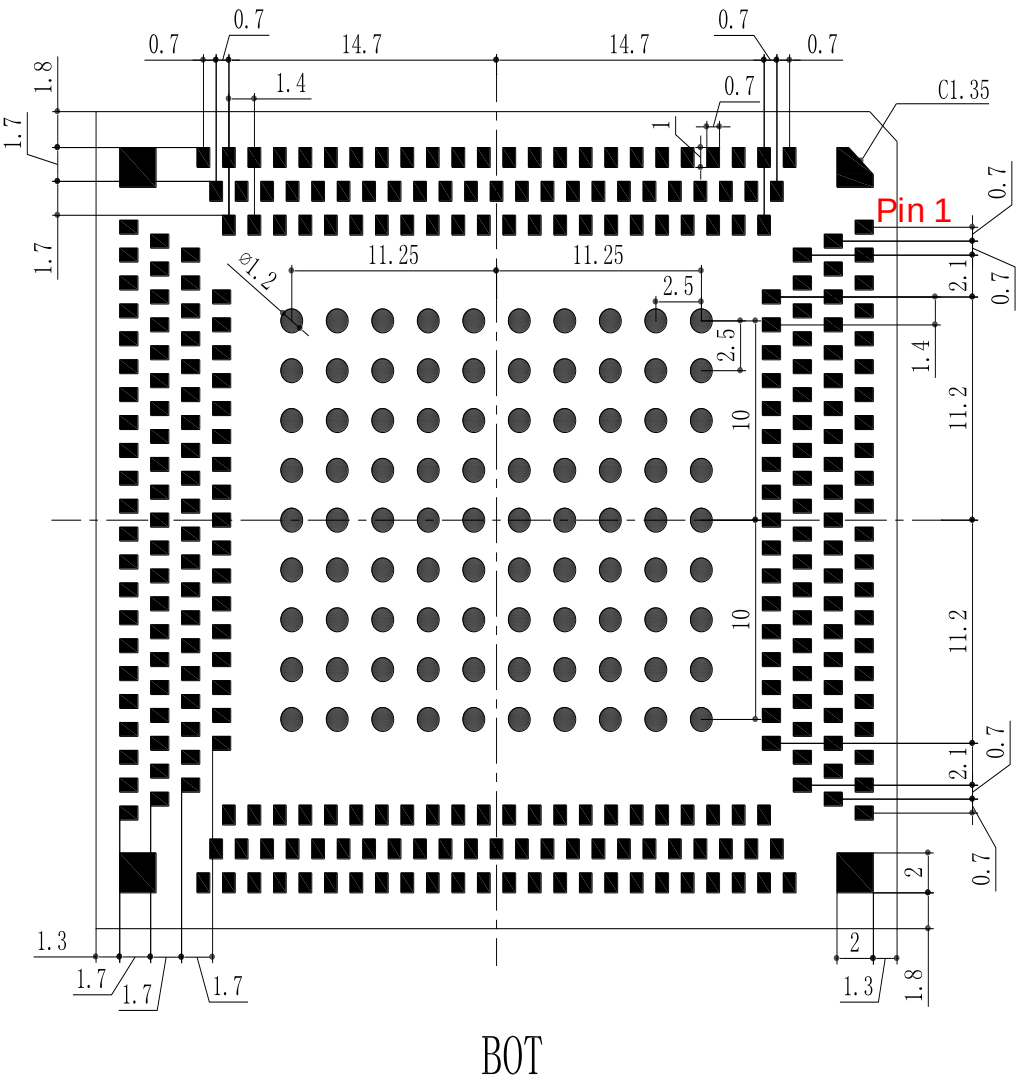


Figure 49: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

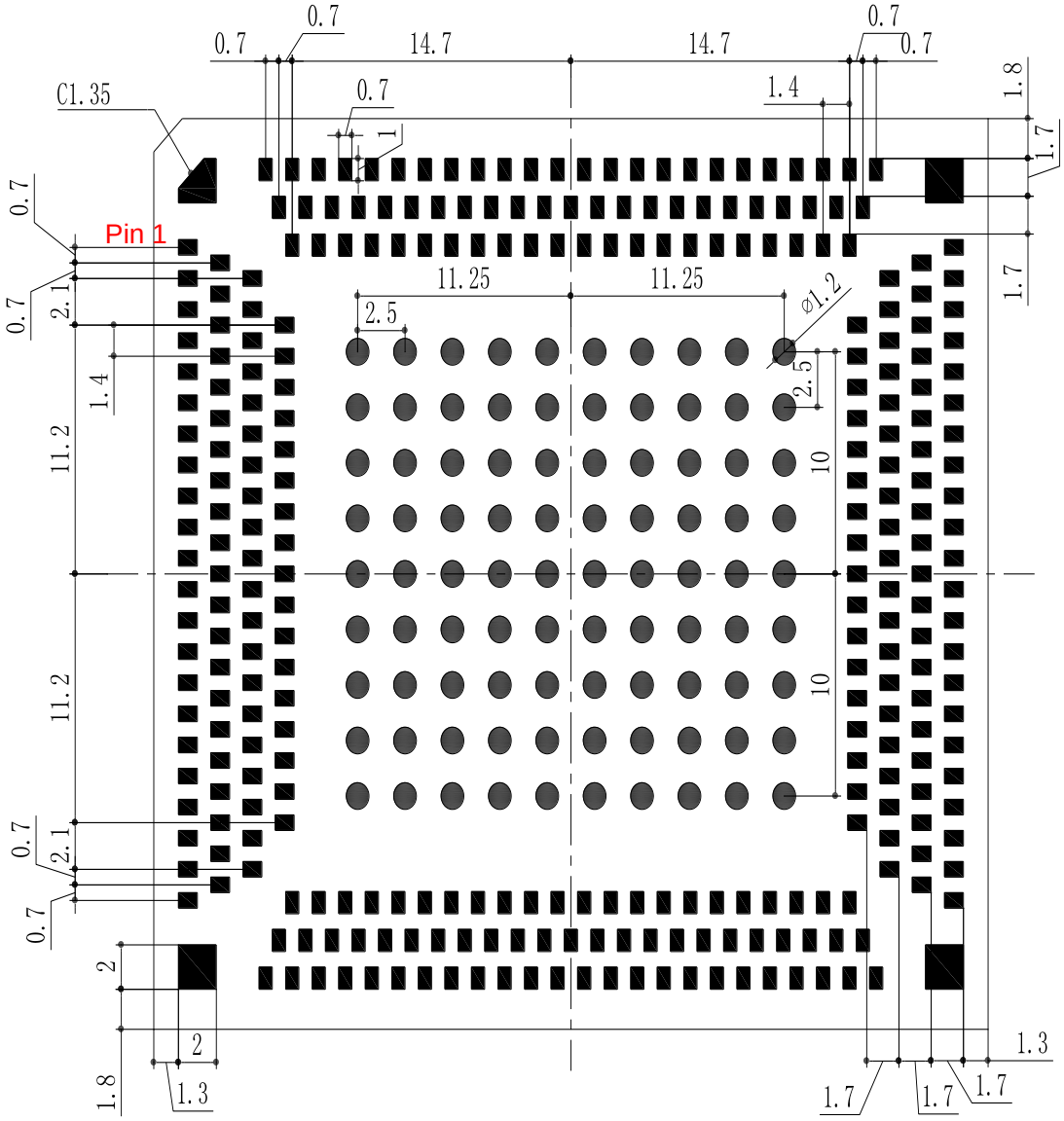


Figure 50: Recommended Footprint

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

7.3. Top and Bottom Views

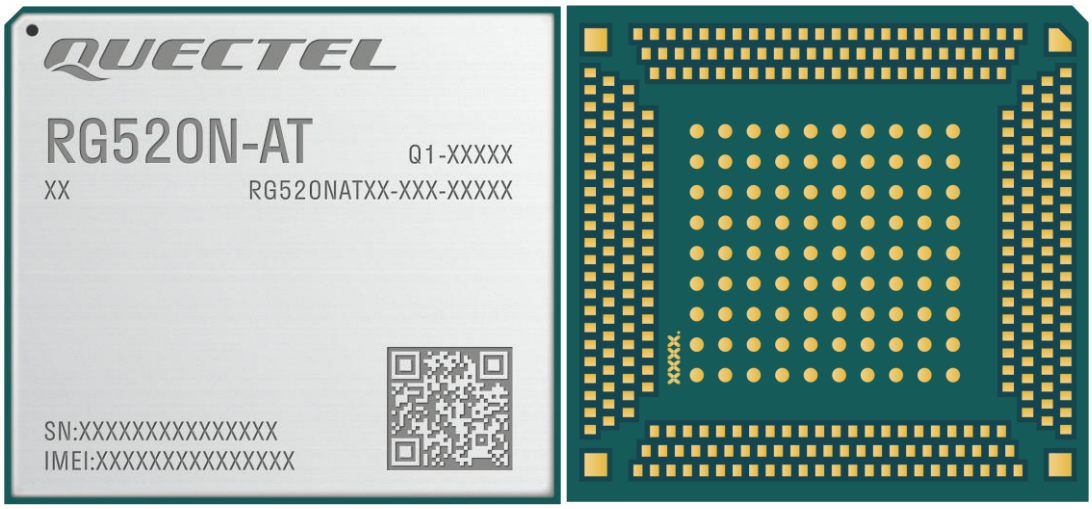


Figure 51: Top & Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided in vacuum-sealed packaging. MSL of the module is rated at 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [11] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[11] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the module.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [6]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

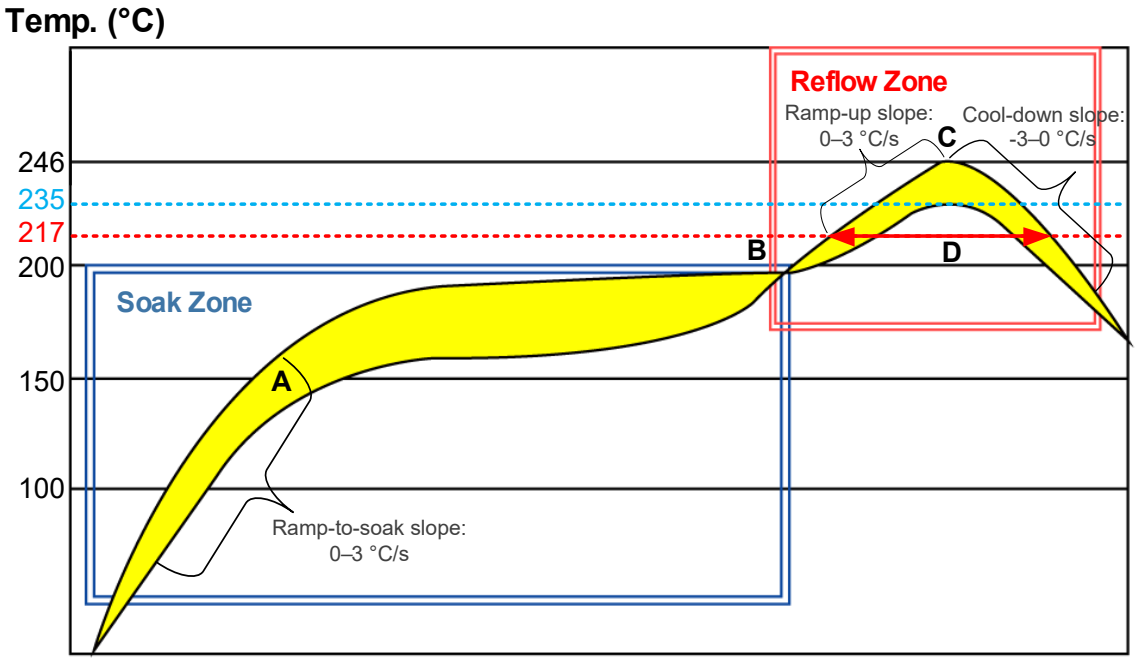


Figure 52: Recommended Reflow Soldering Thermal Profile

Table 54: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

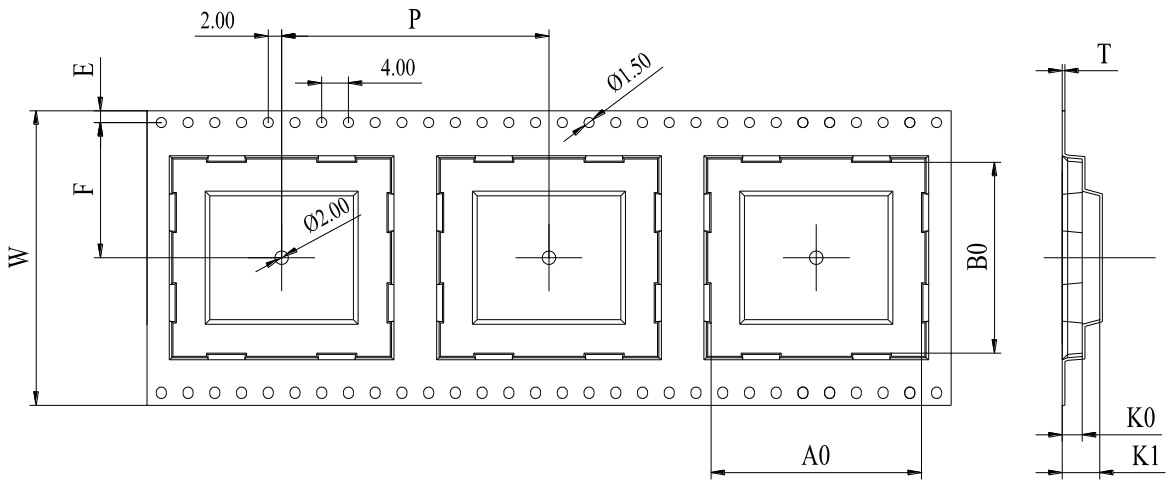


Figure 53: Carrier Tape Dimension Drawing

Table 55: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	44.7	41.7	4.2	5.2	34.2	1.75

8.3.2. Plastic Reel

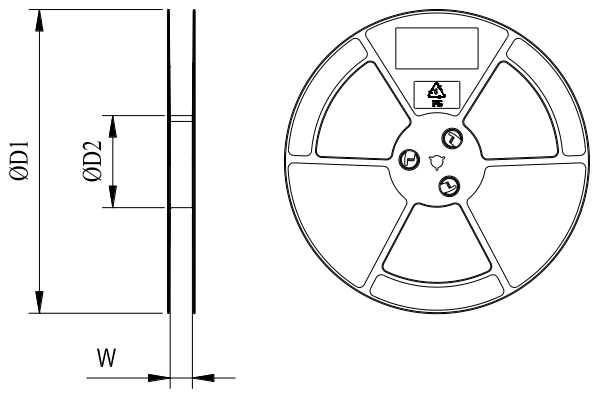


Figure 54: Plastic Reel Dimension Drawing

Table 56: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

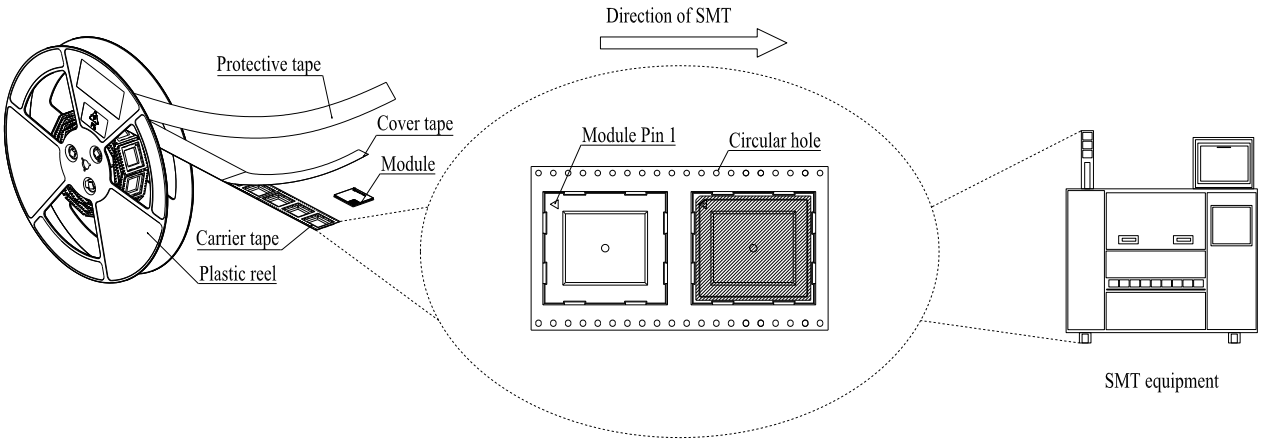
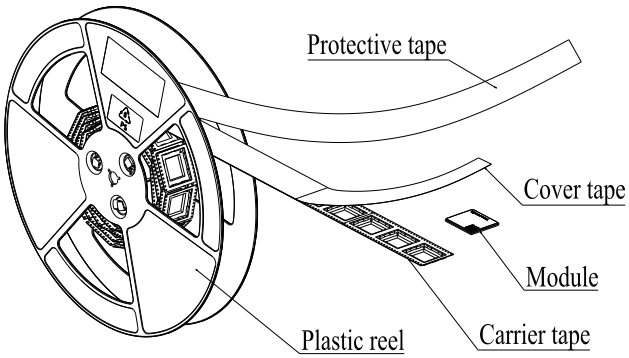


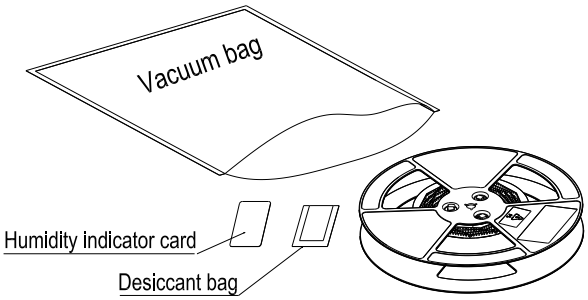
Figure 55: Mounting Direction

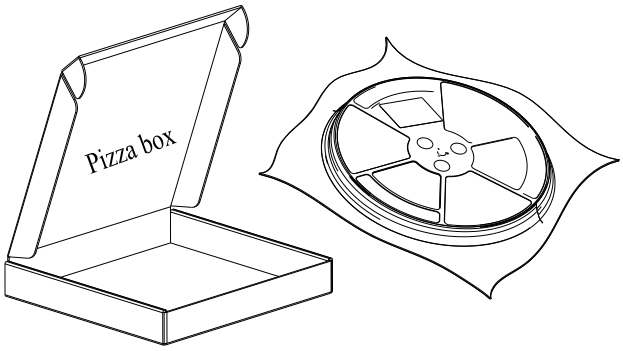
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 200 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 800 modules.

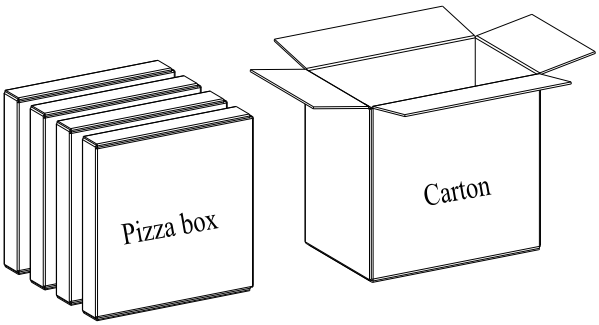


Figure 56: Packaging Process

9 Appendix A References

Table 57: Related Documents

Document Name	
[1]	Quectel_RG520N-AT_CA&EN-DC_Features
[2]	Quectel_RTA001-EV_EVB_User_Guide
[3]	Quectel_RG520N&RG52xF&RG530F&RM520N&RM530N_Series_AT_Commands_Manual
[4]	Quectel_RG520N&RG52xF&RG530F&RM520N&RM530N_Series_GNSS_Application_Note
[5]	Quectel_RF_Layout_Application_Note
[6]	Quectel_Module_SMT_Application_Note

Table 58: Terms and Abbreviations

Abbreviation	Description
1PPS	1 Pulse Per Second
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Application Processor
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
CA	Carrier Aggregation

CTS	Clear To Send
CP-OFDM	Cyclic Prefix-Orthogonal Frequency Division Multiplexing
DAI	Digital Audio Interface
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DFT-s-OFDM	Discrete Fourier Transform-Spread-Orthogonal Frequency Division Multiplexing
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
EN-DC	E-UTRA New Radio Dual Connectivity
ESD	Electrostatic Discharge
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
FEM	Front-End Module
FOTA	Firmware Over-The-Air
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit

I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MT	Mobile Terminated
NR	New Radio
NSA	Non-Stand Alone
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PHY	Physical Layer

PRX	Primary Receive
ps	Picosecond
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIB	System Information Block
SIMO	Single Input Multiple Output
SMS	Short Message Service
SoC	System on a Chip
SPI	Serial Peripheral Interface
SRS	Sounding Reference Signal
STB	Set Top Box
TDD	Time Division Duplexing
TRX	Transmit & Receive
TTFF	Time to First Fix
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink

URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

10 Appendix B Operating Frequencies

Table 59: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Frequency	Downlink Operating Frequency	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz

n39	TDD	1880–1920	1880–1920	MHz
n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz
n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz

n86	SUL	1710–1780	-	MHz
n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz
n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz
n257	-	26.50–29.50	26.50–29.50	GHz
n258	-	24.25–27.50	24.25–27.50	GHz
n260	-	37.00–40.00	37.00–40.00	GHz
n261	-	27.50–28.35	27.50–28.35	GHz

Table 60: Operating Frequencies (2G + 3G + 4G)

2G	3G	4G	Duplex Mode	Uplink Operating Frequency	Downlink Operating Frequency	Unit
-	B1	B1	FDD	1920–1980	2110–2170	MHz
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990	MHz
DCS1800	B3	B3	FDD	1710–1785	1805–1880	MHz
-	B4	B4	FDD	1710–1755	2110–2155	MHz
GSM850	B5/BC0	B5	FDD	824–849	869–894	MHz
-	B6	-	FDD	830–840	875–885	MHz

-	B7	B7	FDD	2500–2570	2620–2690	MHz
EGSM900	B8	B8	FDD	880–915	925–960	MHz
-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9	MHz
-	B10	B10	FDD	1710–1770	2110–2170	MHz
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9	MHz
-	B12	B12	FDD	699–716	729–746	MHz
-	B13	B13	FDD	777–787	746–756	MHz
-	B14	B14	FDD	788–798	758–768	MHz
-	-	B17	FDD	704–716	734–746	MHz
-	-	B18	FDD	815–830	860–875	MHz
-	B19	B19	FDD	830–845	875–890	MHz
-	B20	B20	FDD	832–862	791–821	MHz
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9	MHz
-	B22	B22	FDD	3410–3490	3510–3590	MHz
-	-	B24	FDD	1626.5–1660.5	1525–1559	MHz
-	B25	B25	FDD	1850–1915	1930–1995	MHz
-	B26	B26	FDD	814–849	859–894	MHz
-	-	B27	FDD	807–824	852–869	MHz
-	-	B28	FDD	703–748	758–803	MHz
-	-	B29	FDD [12]	-	717–728	MHz
-	-	B30	FDD	2305–2315	2350–2360	MHz
-	-	B31	FDD	452.5–457.5	462.5–467.5	MHz
-	-	B32	FDD	-	1452–1496	MHz
-	B33	B33	TDD	1900–1920	1900–1920	MHz
-	B34	B34	TDD	2010–2025	2010–2025	MHz

[12] Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	B35	B35	TDD	1850–1910	1850–1910	MHz
-	B36	B36	TDD	1930–1990	1930–1990	MHz
	B37	B37	TDD	1910–1930	1910–1930	MHz
-	B38	B38	TDD	2570–2620	2570–2620	MHz
-	B39	B39	TDD	1880–1920	1880–1920	MHz
-	B40	B40	TDD	2300–2400	2300–2400	MHz
-	-	B41	TDD	2496–2690	2496–2690	MHz
-	-	B42	TDD	3400–3600	3400–3600	MHz
-	-	B43	TDD	3600–3800	3600–3800	MHz
-	-	B44	TDD	703–803	703–803	MHz
-	-	B45	TDD	1447–1467	1447–1467	MHz
-	-	B46	TDD	5150–5925	5150–5925	MHz
-	-	B47	TDD	5855–5925	5855–5925	MHz
-	-	B48	TDD	3550–3700	3550–3700	MHz
-	-	B50	TDD	1432–1517	1432–1517	MHz
-	-	B51	TDD	1427–1432	1427–1432	MHz
-	-	B52	TDD	3300–3400	3300–3400	MHz
-	-	B65	FDD	1920–2010	2110–2200	MHz
-	-	B66	FDD [13]	1710–1780	2110–2200	MHz
-	-	B67	FDD	-	738–758	MHz
-	-	B68	FDD	698–728	753–783	MHz
-	-	B69	FDD	-	2570–2620	MHz
-	-	B70	FDD [14]	1695–1710	1995–2020	MHz
-	-	B71	FDD	663–698	617–652	MHz

[13] The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.
[14] The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 295 MHz.

-	-	B72	FDD	451–456	461–466	MHz
-	-	B73	FDD	450–455	460–465	MHz
-	-	B74	FDD	1427–1470	1475–1518	MHz
-	-	B75	FDD	-	1432–1517	MHz
-	-	B76	FDD	-	1427–1432	MHz
-	-	B85	FDD	698–716	728–746	MHz
-	-	B87	FDD	410–415	420–425	MHz
-	-	B88	FDD	412–417	422–427	MHz

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2023RG520NAT” The FCC ID can be used only when all FCC compliance requirements are met.

Antenna

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.