AG598E-ROWA QuecOpen Hardware Design

Automotive Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

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Contents

Safety Information **3**

About the Document **4**

Contents **5**

Table Index **8**

Figure Index **9**

1 Introduction **11**
1.1. Special Marks 12

2 Product Overview **13**
2.1. Frequency Bands and Functions 13
2.2. Key Features 14
2.3. Pin Assignment 18
2.4. Pin Description 19
2.4.1. Pin Definition 19
2.4.2. Pin Multiplexing 33
2.5. EVB Kit 34

3 Operating Characteristics **35**
3.1. Operating Modes 35
3.2. Power Saving 36
3.2.1. Low Power Mode (LPM) 36
3.2.1.1. LPM and Wakeup Functions 36
3.2.1.2. LPM and Wakeup Timing 37
3.2.2. Airplane Mode 38
3.3. Power Supply 39
3.3.1. Power Supply Pins 39
3.3.2. Reference Design for Power Supply 39
3.3.3. Voltage Stability Requirements 40
3.4. Turn-on 42
3.4.1. Turn-on with PWRKEY 42
3.4.2. Turn-on with CBL_PWR_N 44
3.5. Turn-off 45
3.5.1. Turn-off with PWRKEY 45
3.5.2. Turn-off with Linux Commands/API Function 46
3.6. RESET_N 47

4 Application Interfaces **49**
4.1. (U)SIM Interfaces 49
4.2. USB Interface 51
4.3. UART Interfaces 53

4.4. I2S and I2C Interfaces 56
4.5. PCM Interface 58
4.6. SDIO Interfaces 59
4.6.1. Reference Design for eMMC Application 61
4.7. PCIe Interfaces 62
4.8. WLAN and Bluetooth Application Interfaces 65
4.9. SPIs 68
4.10. RGMII Interface 69
4.11. SGMII Interface 72
4.12. GPIO Interfaces 75
4.13. ADC Interfaces 76
4.14. USB_BOOT Interface 77
4.15. RTC 79
4.16. DR_SYNC 79
4.17. IMU Interrupt Interface 80
4.18. SEL_BOOT_PARTION* 81

5 RF Specifications 83
5.1. Cellular Antenna Interfaces 84
5.1.1. Pin Definition 84
5.1.2. Operating Frequencies 85
5.1.3. Transmitting Power 87
5.1.4. Receiver Sensitivity 88
5.1.5. Reference Design 90
5.2. GNSS Antenna Interface (Optional) 91
5.2.1. Pin Definition 92
5.2.2. Operating Frequency 92
5.2.3. GNSS Performance 92
5.2.4. Reference Design 93
5.3. RF Routing Guidelines 94
5.4. Antenna Design Requirements 96
5.5. RF Connector Recommendation 97

6 Electrical Characteristics and Reliability 99
6.1. Absolute Maximum Ratings 99
6.2. Power Supply Ratings 99
6.3. Power Consumption 100
6.4. Digital I/O Characteristics 109
6.5. ESD Protection 109
6.6. Operating and Storage Temperatures 110
6.7. Thermal Dissipation 110

7 Mechanical Information 113
7.1. Mechanical Dimensions 113
7.2. Recommended Footprint 115
7.3. Top and Bottom Views 116

8 Storage, Manufacturing and Packaging 117
8.1. Storage Conditions 117
8.2. Manufacturing and Soldering 118
8.3. Packaging Specification 120
8.3.1. Carrier Tape 120
8.3.2. Plastic Reel 120
8.3.3. Mounting Direction 121
8.3.4. Packaging Process 122

9 Appendix References 123

FCC Statement 130

IC Statement 132

Table Index

Table 1: Special Marks 12
Table 2: Basic Information 13
Table 3: Frequency Bands and Functions 13
Table 4: Key Features 14
Table 5: I/O Parameters Definition 19
Table 6: Pin Description 20
Table 7: Overview of Operating Modes 35
Table 8: GPIO Configuration Related to LPM/Wakeup Function 37
Table 9: VBAT and GND Pins 39
Table 10: Pin Description of PWRKEY 42
Table 11: Pin Description of CBL_PWR_N 44
Table 12: Pin Description of RESET_N 47
Table 13: Pin Description of (U)SIM Interfaces 49
Table 14: Pin Description of USB Interface 51
Table 15: Basic Information of UART Interfaces 54
Table 16: Pin Description of UART Interfaces 54
Table 17: Pin Description of I2S Interfaces 57
Table 18: Pin Description of I2C Interfaces 57
Table 19: Pin Definition of PCM Interface 58
Table 20: Pin Description of SDIO Interface 59
Table 21: Pin Description of PCIe Interface 62
Table 22: Pin Description of WLAN and Bluetooth Application Interfaces 65
Table 23: Pin Description of SPIs 68
Table 24: Parameters of SPI Timing 69
Table 25: Pin Description of Ethernet Management and Control Interfaces 70
Table 26: Pin Description of RGMII Interface 70
Table 27: Pin Description of SGMII Interface 73
Table 28: Pin Description of GPIO Interfaces 75
Table 29: Pin Description of ADC Interfaces 76
Table 30: Characteristic of ADC Interface 77
Table 31: Pin Description of USB_BOOT Interface 77
Table 32: Pin Description of DR_SYNC 79
Table 33: Pin Description of IMU Interrupt Interface 80
Table 34: Pin Description of SEL_BOOT_PARTION 81

Figure Index

Figure 2: Pin Assignment (Top View) 19
Figure 3: Module Power Consumption in Low Power Mode 36
Figure 4: LPM/Wakeup Function Implementation Schematic Diagram 37
Figure 5: LPM Wakeup Timing 38
Figure 6: Reference Design of Power Supply 40
Figure 7: Power Supply Limits During Burst Transmission 41
Figure 8: Power Supply Design 41
Figure 9: Turn On the Module Using Driving Circuit 42
Figure 10: Turn On the Module Using a Button 43
Figure 11: Power-up Timing 43
Figure 12: Turn On the Module Using CBL_PWR_N 45
Figure 13: Power-down Timing 46
Figure 14: Reference Circuit of RESET_N by Using Driving Circuit 47
Figure 15: Reference Circuit of RESET_N by Using Button 48
Figure 16: Reset Timing 48
Figure 17: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector 50
Figure 18: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector 50
Figure 19: Reference Design of USB 2.0 Application 52
Figure 20: Reference Design of USB 3.1 Application 52
Figure 21: Reference Design of UART Interface with Translator Chip (UART1) 55
Figure 22: Reference Circuit with Transistor Circuit (UART1) 56
Figure 23: Reference Design of I2S1 and I2C1 Interfaces with External Audio Codec 58
Figure 24: PCM Timing (Short Frame Sync) 59
Figure 25: Reference Design for eMMC Application 61
Figure 26: Reference Design of PCIe Interface 63
Figure 27: Curved Trace of Differential Pair 64
Figure 28: PCIe Trace Requirements 65
Figure 29: Reference Design of WLAN & Bluetooth Application Interfaces (AF67E) 67
Figure 30: SPI Timing 68
Figure 31: Simplified Block Diagram for Automotive Ethernet Application 71
Figure 32: Reference Circuit of RGMII Interface with PHY Application 71
Figure 33: Simplified Block Diagram for Automotive Ethernet Application 73
Figure 34: Reference Circuit of SGMII Interface with PHY Application 74
Figure 35: Reference Design of USB_BOOT Interface 78
Figure 36: Forced Download Mode Timing 78
Figure 37: Reference Design of DR_SYNC for Clock Synchronization Application 79
Figure 38: IMU Reference Design Circuit 80
Figure 39: Reference Design of SEL_BOOT_PARTION 81
Figure 40: Timing of Switching A/B System 82
Figure 41: Reference Design of Main and Diversity Antenna Interfaces 91
Figure 42: Reference Circuit of GNSS Antenna 94

Figure 43: Microstrip Design on a 2-layer PCB 95
Figure 44: Coplanar Waveguide Design on a 2-layer PCB 95
Figure 45: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground) 95
Figure 46: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground) 96
Figure 47: Feature of the HFM Connector 98
Figure 48: Heatsink Design Example 112
Figure 49: Module Top and Side Dimensions 113
Figure 50: Module Bottom Dimensions (Unit: mm) 114
Figure 51: Recommended Footprint (Unit: mm) 115
Figure 52: Top and Bottom Views of the Module 116
Figure 53: Recommended Reflow Soldering Thermal Profile 118
Figure 54: Carrier Tape Dimension Drawing (Unit: mm) 120
Figure 55: Plastic Reel Dimension Drawing 121
Figure 56: Mounting Direction 121
Figure 57: Packaging Process 122

1 Introduction

AG598E-ROWA QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and cost-effectiveness

AG598E-ROWA QuecOpen® module is a baseband processor platform based on Quad-Core Cortex-A55. The maximum dominant frequency is up to 2.0 GHz. You can use AG598E-ROWA module as the basis for development of QuecOpen® applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

Hereby, Quectel Wireless Solutions Co., Ltd.declares that the radio equipment type AG598E-ROWA is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet: http://www.quectel.com/support/technical.htm

The device could be used with a separation distance of 20cm to the human body.

NOTE

This document is also applicable to the TelSDK and TelAF solutions.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

2.1. Frequency Bands and Functions

AG598E-ROWA is automotive-grade 5G NR Sub-6 GHz wireless communication module.

Table 2: Basic Information

AG598E-ROWA	
Pin number and package	452 LGA pins
Dimensions	(45.0 ±0.2) mm × (45.0 ±0.2) mm × (3.45 ±0.2) mm
Weight	Approx.17 g
Wireless technologies	● 5G NR, LTE, WCDMA, GSM ● GNSS

Table 3: Frequency Bands and Functions

Network Type/ Function		AG598E-ROWA
5G NR	5G SA	n1/n2/n3/n5/n7/n8/n12/n18/n20/n25/n26/n28/ n38/n40/n41/n66/n71/n77/n78/n79
	5G NSA	n1/n2/n3/n5/n7/n8/n12/n20/n25/n26/n28/ n38/n40/n41/n66/n71/n77/n78/n79
LTE	LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B18/B19/B20/B25/B26/B28/B32 [1]/B66/B71
	LTE-TDD	B34/B38/B39/B40/B41/B42
WCDMA		B1/B2/B4/B5/B8/B19
GSM		GSM850/EGSM900/DCS1800/PCS1900

[1] B32 support Rx only.

Dual SIM Feature	DSDS
GNSS (optional)	● Dual-band GNSS: L1 + L5 (default); L1 + L2* (optional) ● Constellation: GPS, GLONASS, BDS, Galileo, NavIC, QZSS

2.2. Key Features

The following table describes the detailed features of the module.

Table 4: Key Features

Feature	Details
Power Supply	VBAT_BB/VBAT_RF: Supply voltage range: 3.3–4.3 V Typical supply voltage: 3.8 V
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast
(U)SIM Interfaces	● Support dual (U)SIM cards, DSDS (Dual SIM Dual Standby) ● (U)SIM1: 1.8/3.0 V ● (U)SIM2: 1.8 V (by default); 3.0 V (optional)
USB Interface	● Compliant with USB 3.1 Gen 2 and USB 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● USB 2.0 and USB 3.1 are used for firmware upgrade, AT command communication, data transmission, GNSS NMEA sentences output and software debugging. ● When USB 2.0 and USB 3.1 are connected to the same host, USB 2.0 and USB 3.1 cannot be used simultaneously, USB 3.1 takes effect by default. ● Support USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7
UART Interfaces	**UART1 & UART2:** ● Used for data transmission, UART2 is used for Bluetooth connection by default ● Baud rate reach up to 921600 bps ● Default baud rate is 9600 bps ● Supports RTS and CTS hardware flow control **UART3 & UART4:** ● Used for data transmission ● Baud rate reach up to 921600 bps

	● Default baud rate is 9600 bps **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate by default
I2S Interfaces	● Support two I2S interfaces ● I2S1 is used for external codec by default ● I2S2 can be used according to your application. ● Support master and slave modes
I2C Interfaces	● Support two I2C interfaces ● I2C1 is used for external audio codec configuration by default ● I2C2 is used for IMU by default ● Compliant with *I2C-bus Specification Version 3.0* ● HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
PCM Interface	● Used for Bluetooth audio data transmission by default ● Supports 16-bit linear data format ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes
SDIO Interfaces	**SDIO1:** Compliant with eMMC 5.1 4-bit by default, max. up to 8-bit, supports 1.8 V only SDIO1 can be used for eMMC function **SDIO2:** Compliant with SD 3.0 4-bit by default, supports 1.8 V only SDIO2 can be used to connect to external DSRC module if required
PCIe Interfaces	**PCIe1:** ● Compliant with *PCI Express Base Specification Revision 3.0* ● Support 2 lanes, with maximum rate of 8 GT/s × 1 lane ● Support RC and EP modes, works in RC mode by default ● Used for WLAN function by default **PCIe2:** ● Compliant with *PCI Express Base Specification Revision 3.0* ● Support 1 lane, with maximum rate of 8 GT/s × 1 lane ● Support RC configuration only
WLAN and Bluetooth Application Interfaces	● Support PCIe1 (Gen 3) interface for WLAN ● Support Bluetooth UART and PCM interfaces for Bluetooth
SPIs	● Support 2 SPIs by default ● Support master mode and slave mode ● Maximum clock frequency rate: 50 MHz

RGMII Interface	● Supports 10/100/1000 Mbps Ethernet connection [2]
SGMII Interface	● Supports 1000/2500 Mbps Ethernet connection
Antenna Interfaces [3]	● One main antenna interface (ANT_MAIN) ● One diversity antenna interface (ANT_DIV) ● Two MIMO antenna interfaces (ANT_MIMO3, ANT_MIMO4) ● One GNSS antenna interface (ANT_GNSS)
Temperature Range	● Operating temperature range [4]: -35 to +75 °C ● Extended temperature range [5]: -40 to +85 °C ● eCall temperature range [6]: -40 to +95 °C ● Storage temperature range: -40 to +95 °C
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Audio Features	● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE/5G: AMR/AMR-WB/EVS ● Support VoLTE (Voice over LTE) ● Support echo cancellation and noise suppression
Transmitting Power	● 5G NR TDD HPUE bands (n41/n79): Class 2 (26 dBm ±2 dB) 5G NR TDD HPUE bands (n77/n78): Class 2 (26 dBm +1/-2 dB) ● 5G NR FDD bands and 5G NR TDD n38/n40: Class 3 (23 dBm ±2 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE TDD HPUE bands (B40/B41): Class 2 (26 dBm ±2 dB) ● WCDMA bands: Class 3 (23 dBm ±2 dB) ● GSM850: Class 4 (33 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● PCS1900: Class 1 (30 dBm ±2 dB) ● GSM850 8-PSK: Class E2 (27 dBm ±3 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) ● PCS1900 8-PSK: Class E2 (26 dBm ±3 dB)
5G NR Features	● Support 3GPP Rel-16 ● Support 5G NR DL CA up to 2 FR1

[2] The module's RGMII/SGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.
[3] 5 antennas (ANT_MAIN & ANT_DIV & ANT_MIMO3 & ANT_MIMO4 & ANT_GNSS) are supported by default.
[4] Within the operating temperature range, the module meets 3GPP specifications.
[5] Within the extended temperature range, the module remains fully functional and the ability to establish and maintain functions such as voice, SMS, data transmission, eCall, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[6] Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of eCall.

	● Supported modulations: Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Support 4 × 4 MIMO [7] for MB, HB and UHB bands [8] in DL direction ● Support SCS 15 kHz (FDD) and 30 kHz (TDD) ● Support option 3x, 3a and option 2 ● Support SRS antenna rotation function: NSA: 1T4R (n77, n78 and n79) SA: 1T4R (n77, n78 and n79) ● Support SA and NSA ● Max. transmission data rates: NSA: 2.5 Gbps (DL)/625 Mbps (UL) SA: 2.1 Gbps (DL)/525 Mbps (UL)

LTE Features	● Support LTE-FDD and TDD, up to DL 5CA Cat 19 and UL 2CA Cat 18
	● Support 1.4/3/5/10/15/20 MHz RF bandwidth
	● Support 4 × 4 MIMO [9] for MB, HB and UHB bands [8] in DL direction
	● Support modulations:
	  ● Uplink: QPSK, 16QAM, 64QAM, 256QAM
	  ● Downlink: QPSK, 16QAM, 64QAM, 256QAM
	● LTE-FDD: Max. 1.6 Gbps (DL)/200 Mbps (UL)
	● LTE-TDD: Max. 1.0 Gbps (DL)/120 Mbps (UL)

UMTS Features	● Support 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA ● Support QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** ● Support GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Support EDGE multi-slot class 33 (33 by default) ● Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 296 kbps (DL)/236.8 kbps (UL)
Rx-diversity	Support 5G, LTE and WCDMA Rx-diversity
GNSS (Optional)	● Constellation: GPS, GLONASS, BDS, Galileo, NavIC, QZSS ● Augmentation system: SBAS

[7] 5G NR n2/n5/n8/n12/n18/n20/n25/n26/n28/n71 do not support DL 4 × 4 MIMO, support DL 2 × 2 MIMO only.
[8] MB: 1–2.3 GHz, HB: 2.3–2.7 GHz, UHB: 3.3–6.0 GHz.
[9] LTE B2/B5/B8/B12/B18/B19/B20/B25/B26/B28/B32/B34/B39/B71 do not support DL 4 × 4 MIMO, support DL 2 × 2 MIMO only.

	● Dual-band GNSS: L1 + L5 (default); L1 + L2* (optional) ● Protocol: NMEA 0183 ● Update rate: 1 Hz by default, max. up to 10 Hz
Firmware Upgrade	● USB 2.0 or USB 3.1 interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Pin Assignment

The following figure shows the pin assignment of the module.

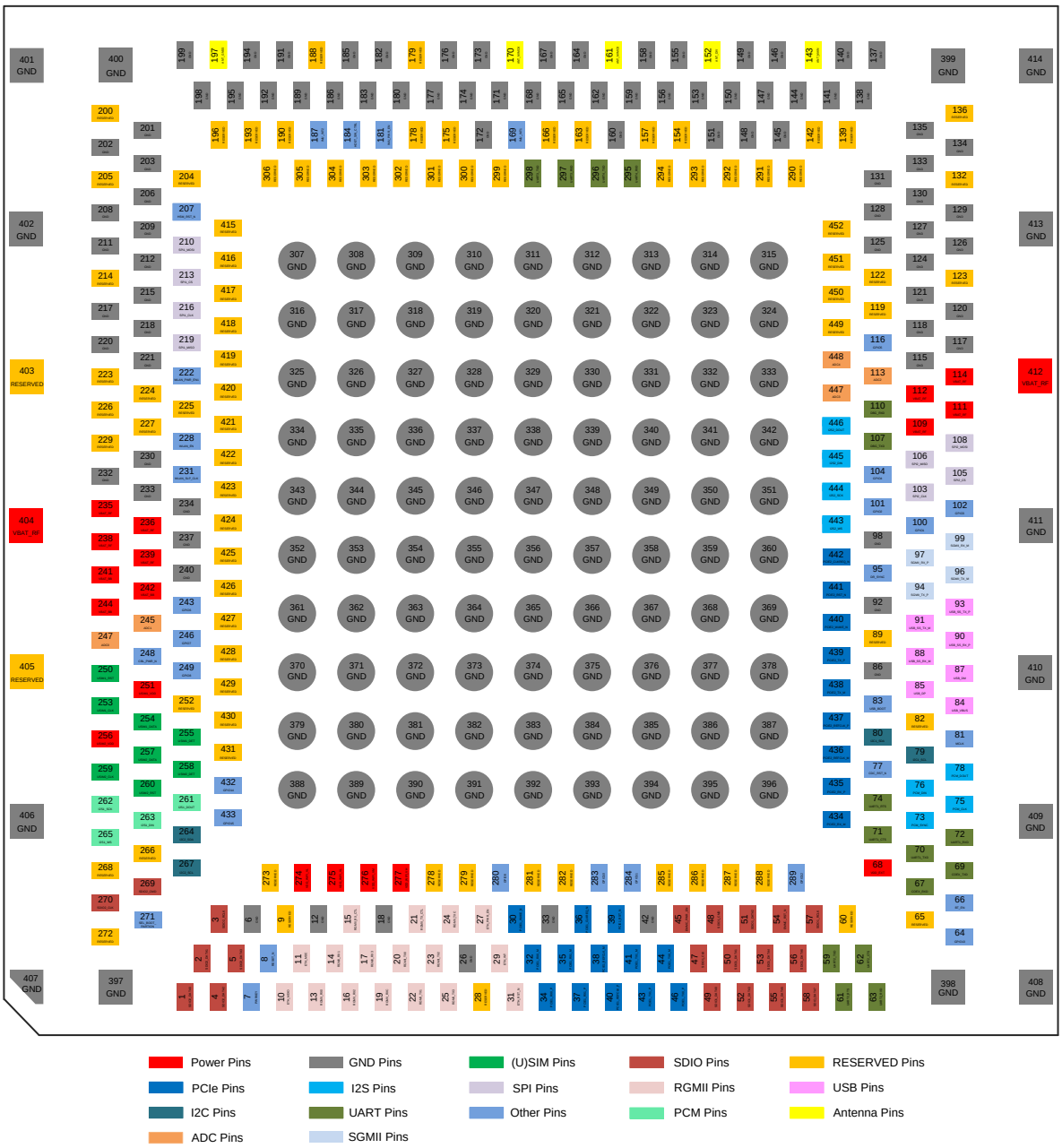


Figure 1: Pin Assignment (Top View)

NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.
3. Ensure that there is no current sink on the module's pins before the module turns on.

2.4. Pin Description

2.4.1. Pin Definition

The following tables show the pin definition of the module.

Table 5: I/O Parameters Definition

Symbol	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	241, 242, 244	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF	109, 111, 112, 114, 235, 236, 238, 239, 404, 412	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	
VDD_EXT	68	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V Max. current in full functionality mode: Iomax = 50 mA Max. current in low power mode: Iomax = 10 mA	This pin can be used to connect with VDD_IO of Quectel Wi-Fi & Bluetooth module, it also can be used as power supply for external pull up circuits. A test point is recommended to be reserved.
VDD_WIFI_VL	274, 275	PO	Low-voltage power supply for Wi-Fi & Bluetooth modules	Vnom = 0.976 V $I_O$max = 1.7 A	After the Wi-Fi driver is loaded, the output voltage of these pins will be adjusted automatically to adapt to Wi-Fi & Bluetooth module.
VDD_WIFI_VM	276	PO	Medium-voltage power supply for Wi-Fi & Bluetooth modules	Vnom = 1.28 V $I_O$max = 0.45 A	
VDD_WIFI_VH	277	PO	High-voltage power supply for Wi-Fi & Bluetooth modules	Vnom = 1.88 V $I_O$max = 0.45 A	
GND	6, 12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172,				

	173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 406, 407, 408, 409, 410, 411, 413, 414				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.42 V	Pulled up internally. Active low. Due to the voltage drop inside the chip, the pin has around 0.75 V level after the module is powered up.
RESET_N	8	DI	Reset the module	V_{IH}max = 1.5 V V_{IH}min = 0.78 V V_{IL}max = 0.42 V	Pulled up internally. Active low. A test point is recommended to be reserved if unused.
CBL_PWR_N	248	DI	Cable power-on; initiates power on when grounded	V_{IH}max = 2.1 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	Pulled up internally. Active low. Pulling it low for an extended period will not trigger hardware reset.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Configurable Function**	**DC Characteristics**	**Comment**
GPIO1	100	DI	WAKEUP_IN	1.8 V	Used as WAKEUP_IN by default. If the default function is not used, it can be configured to GPIO.

					Support wake-up interrupt.
		DIO	GPIO		General-purpose input/output. Support wake-up interrupt.
GPIO2	101	DIO	GPIO		Support wake-up interrupt.
GPIO3	102	DIO	GPIO		General-purpose input/output. **Not** support wake-up interrupt.
GPIO4	104	DO	SLEEP_SYS_IND		Used as SLEEP_SYS_IND by default. If the default function is not used, it can be configured to GPIO. Support wake-up interrupt.
		DIO	GPIO		General-purpose input/output. Support wake-up interrupt.
GPIO5	116	DIO	GPIO		General-purpose input/output. Support wake-up interrupt.
GPIO6	243	DO	STATUS		Used as STATUS by default. If the default function is not used, it can be configured to GPIO. **Not** support wake-up interrupt.
		DIO	GPIO		General-purpose input/output. **Not** support wake-up interrupt.
GPIO7	246	DIO	GPIO		General-purpose

GPIO8	249	DIO	GPIO		input/output. Support wake-up interrupt.
GPIO9	280	DIO	GPIO		
GPIO10	283	DIO	GPIO		
GPIO11	284	DIO	GPIO		
GPIO12	289	DIO	GPIO		
GPIO13	64	DIO	GPIO		
GPIO14	432	DIO	GPIO		
GPIO15	433	DIO	GPIO		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	84	DI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Maximum current: 0.1 mA. A 47 kΩ resistor is connected in series inside the module. If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved.
USB_DP	85	AIO	USB 2.0 differential data (+)		Compliant with USB 2.0 standard specifications. Require differential impedance of 90 Ω. If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved.
USB_DM	87	AIO	USB 2.0 differential data (-)		

USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)		Compliant with USB 3.1 standard specifications. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)		
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)		
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	251	PO	(U)SIM1 card power supply	**High-voltage:** Vmin = 2.7 V Vnom = 2.95 V Vmax = 3.05 V **Low-voltage:** Vmin = 1.65 V Vnom = 1.8 V Vmax = 1.95 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	254	DIO	(U)SIM1 card data	USIM1_VDD	
USIM1_RST	250	DO	(U)SIM1 card reset		
USIM1_CLK	253	DO	(U)SIM1 card clock		
USIM2_VDD	256	PO	(U)SIM2 card power supply	**Low-voltage:** Vmin = 1.65 V Vnom = 1.8 V Vmax = 1.95 V	Only 1.8 V is supported by default. 3.0 V is optional.
USIM2_DATA	257	DIO	(U)SIM2 card data	USIM2_VDD	
USIM2_RST	260	DO	(U)SIM2 card reset		
USIM2_CLK	259	DO	(U)SIM2 card clock		
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep them open.
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect		

UART1, UART3 and UART4 Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_CTS	71	DO	Clear to send signal from the module	1.8 V	If unused, keep it open. Connect to the MCU's CTS.
UART1_RTS	74	DI	Request to send signal to the module		If unused, keep it open. Connect to the MCU's RTS.
UART1_TXD	70	DO	UART1 transmit		If unused, keep these pins open.
UART1_RXD	72	DI	UART1 receive		
UART3_TXD	298	DO	UART3 transmit		
UART3_RXD	297	DI	UART3 receive		
UART4_TXD	296	DO	UART4 transmit		
UART4_RXD	295	DI	UART4 receive		

UART2 (Bluetooth UART) Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_TXD	59	DO	Bluetooth UART transmit	1.8 V	If unused, keep them open.
UART2_RXD	63	DI	Bluetooth UART receive		
UART2_RTS	61	DI	Request to send signal to the module		If unused, keep it open. Connect to the Wi-Fi & Bluetooth module's RTS.
UART2_CTS	62	DO	Clear to send signal from the module		If unused, keep it open. Connect to the Wi-Fi & Bluetooth module's CTS.

Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

DBG_RXD	110	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	107	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	79	OD	I2C1 serial clock	1.8 V	External pull-up resistors are required. If unused, keep them open.
I2C1_SDA	80	OD	I2C1 serial data		
I2C2_SCL	267	OD	I2C2 serial clock		
I2C2_SDA	264	OD	I2C2 serial data		
I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CDC_RST_N	77	DO	External codec reset	1.8 V	
MCLK	81	DO	Clock output for codec	1.8 V	12.288 MHz clock output
I2S1_WS	265	DIO	I2S1 word select		Serve as output signals in master mode. Serve as input signals in slave mode.
I2S1_SCK	262	DIO	I2S1 clock		
I2S1_DIN	263	DI	I2S1 data in		
I2S1_DOUT	261	DO	I2S1 data out		
I2S2_WS	443	DIO	I2S2 word select	1.8 V	Serve as output signals in master mode. Serve as input signals in slave mode.
I2S2_SCK	444	DIO	I2S2 clock		
I2S2_DIN	445	DI	I2S2 data in		
I2S2_DOUT	446	DO	I2S2 data out		
PCM Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_SYNC	73	DIO	PCM data frame sync	1.8 V	Serve as output signals in master mode. Serve as input signals in slave mode.
PCM_CLK	75	DIO	PCM clock		
PCM_DIN	76	DI	PCM data input		
PCM_DOUT	78	DO	PCM data output		
PCIe1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE1_REFCLK_P	40	AIO	PCIe1 reference clock (+)		Serve as output signals in RC mode. Serve as input signals in EP mode. The differential impedance should be the same as that for PCIE_TX/RX.
PCIE1_REFCLK_M	38	AIO	PCIe1 reference clock (-)		
PCIE1_TX0_P	46	AO	PCIe1 transmit 0 (+)		If PCIE1_TX and PCIE1_RX are unused, keep these pins unconnected. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE1_TX0_M	44	AO	PCIe1 transmit 0 (-)		
PCIE1_RX0_P	34	AI	PCIe1 receive 0 (+)		
PCIE1_RX0_M	32	AI	PCIe1 receive 0 (-)		
PCIE1_TX1_P	43	AO	PCIe1 transmit 1 (+)		
PCIE1_TX1_M	41	AO	PCIe1 transmit 1 (-)		
PCIE1_RX1_P	37	AI	PCIe1 receive 1 (+)		
PCIE1_RX1_M	35	AI	PCIe1 receive 1 (-)		
PCIE1_CLKREQ_N	36	DIO	PCIe1 clock request	1.8 V	Serve as input signals in RC mode. Serve as output
PCIE1_WAKE_N	30	DIO	PCIe1 wake up		

					signals in EP mode.
PCIE1_RST_N	39	DIO	PCIe1 reset		Serve as an output signal in RC mode. Serve as an input signal in EP mode.
PCIe2 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE2_REFCLK_P	437	AO	PCIe2 reference clock (+)		Only used in RC mode. The differential impedance should be the same as that for PCIE_TX/RX.
PCIE2_REFCLK_M	436	AO	PCIe2 reference clock (-)		
PCIE2_TX_P	439	AO	PCIe2 transmit (+)		If PCIE2_TX and PCIE2_RX are unused, keep these pins unconnected. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE2_TX_M	438	AO	PCIe2 transmit (-)		
PCIE2_RX_P	435	AI	PCIe2 receive (+)		
PCIE2_RX_M	434	AI	PCIe2 receive (-)		
PCIE2_CLKREQ_N	442	DI	PCIe2 clock request	1.8 V	Only used in RC mode.
PCIE2_WAKE_N	440	DI	PCIe2 wake up		
PCIE2_RST_N	441	DO	PCIe2 reset		Only used in RC mode.
WLAN and Bluetooth Application Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	1.8 V	Used for Quectel Wi-Fi & Bluetooth module power control.
BT_EN	66	DO	Bluetooth enable control		
WLAN_SLP_CLK	231	DO	WLAN 32 kHz sleep clock	1.8 V	If unused, keep it open.

WLAN_EN	228	DO	WLAN function enable control		
HOST_SW_CTRL	184	DI	Switch control	1.8 V	Output signal from Quectel Wi-Fi & Bluetooth module.
COEX_RXD	67	DI	LTE & WLAN & Bluetooth coexistence receive		
COEX_TXD	69	DO	LTE & WLAN & Bluetooth coexistence transmit		
Ethernet Management and Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ETH_MDIO	10	DIO	Ethernet management data	1.8 V	Add a pull-up resistor to this pin, and place the resistor close to the external PHY.
ETH_MDC	11	DO	Ethernet management clock		Do not add any pull-up resistor to this pin, otherwise it may cause higher power consumption during low power mode.
ETH_PWR_EN	27	DO	Enable external power supply to power Ethernet PHY	1.8 V	
ETH_INT	29	DI	Ethernet PHY interrupt		
ETH_RST_N	31	DO	Ethernet PHY reset		
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SGMII_TX_P	94	AO	SGMII transmit (+)		Require differential impedance of 90–110 Ω, and 100 Ω is recommended. 100 nF AC coupling
SGMII_TX_M	96	AO	SGMII transmit (-)		
SGMII_RX_P	97	AI	SGMII receive (+)		

SGMII_RX_M	99	AI	SGMII receive (-)		capacitor is required.
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_RXC	19	DI	RGMII receive clock	1.8 V	The single-ended impedance requires 50 Ω.
RGMII_RX_CTL	15	DI	RGMII receive control		
RGMII_RX0	13	DI	RGMII receive data bit 0		
RGMII_RX1	14	DI	RGMII receive data bit 1		
RGMII_RX2	16	DI	RGMII receive data bit 2		
RGMII_RX3	17	DI	RGMII receive data bit 3		
RGMII_TXC	24	DO	RGMII transmit clock		
RGMII_TX_CTL	21	DO	RGMII transmit control		
RGMII_TX0	20	DO	RGMII transmit data bit 0		
RGMII_TX1	22	DO	RGMII transmit data bit 1		
RGMII_TX2	23	DO	RGMII transmit data bit 2		
RGMII_TX3	25	DO	RGMII transmit data bit 3		
SDIO1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO1_DATA0	49	DIO	SDIO1 data bit 0	1.8 V	
SDIO1_DATA1	50	DIO	SDIO1 data bit 1		
SDIO1_DATA2	51	DIO	SDIO1 data bit 2		
SDIO1_DATA3	52	DIO	SDIO1 data bit 3		
SDIO1_CMD	48	DIO	SDIO1 command		

SDIO1_CLK	47	DO	SDIO1 clock		
SDIO1_RCLK	57	DI	SDIO1 return clock		
SDIO1_DATA4	53	DIO	SDIO1 data bit 4		
SDIO1_DATA5	55	DIO	SDIO1 data bit 5		
SDIO1_DATA6	56	DIO	SDIO1 data bit 6		
SDIO1_DATA7	58	DIO	SDIO1 data bit 7		
EMMC_RST_N	54	DO	eMMC reset	1.8 V	This pin is not supported.
EMMC_PWR_EN	45	DO	eMMC power supply enable control		
SDIO2 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO2_DATA0	1	DIO	SDIO2 data bit 0		
SDIO2_DATA1	2	DIO	SDIO2 data bit 1		
SDIO2_DATA2	4	DIO	SDIO2 data bit 2		
SDIO2_DATA3	5	DIO	SDIO2 data bit 3	1.8 V	
SDIO2_CMD	269	DIO	SDIO2 command		
SDIO2_CLK	270	DO	SDIO2 clock		
SDIO2_RCLK	3	DI	SDIO2 return clock		
Antenna Interfaces [10]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	143	AIO	Main antenna interface		50 Ω impedance
ANT_DIV	152	AIO	Diversity antenna interface		
ANT_MIMO3	161	AIO	MIMO3 antenna interface		
ANT_MIMO4	170	AIO	MIMO4 antenna interface		

[10] 5 antennas (ANT_MAIN & ANT_DIV & ANT_MIMO3 & ANT_MIMO4 & ANT_GNSS) are supported by default.

ANT_GNSS	197	AI	GNSS antenna interface		
SPIs					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CLK	216	DO	SPI1 clock	1.8 V	SPI supports master mode by default. Contact Quectel Technical Support if slave mode needs to be supported.
SPI1_CS	213	DO	SPI1 chip select		
SPI1_MISO	219	DI	SPI1 master-in slave-out		
SPI1_MOSI	210	DO	SPI1 master-out slave-in		
SPI2_CLK	103	DO	SPI2 clock		
SPI2_CS	105	DO	SPI2 chip select		
SPI2_MISO	106	DI	SPI2 master-in slave-out		
SPI2_MOSI	108	DO	SPI2 master-out slave-in		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	247	AI	General-purpose ADC interface	Input voltage range: 0–1.875 V	
ADC1	245	AI	General-purpose ADC interface		
ADC2	113	AI	General-purpose ADC interface		
ADC3	447	AI	General-purpose ADC interface		
ADC4	448	AI	General-purpose ADC interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	83	DI	Force the module into download mode	1.8 V	Active high. It is recommended to reserve test points.

SEL_BOOT_PARTION*	271	DI	Select to boot from A or B partition address		By default, the module boots from A partition address. When this pin is pulled high, the module will boot from B partition address when it restarts. If unused, keep it open.
DR_SYNC	95	DO	Dead reckoning sync		
IMU_PWR_EN	181	DO	IMU power enable control		If unused, keep these pins open.
IMU_INT1	169	DI	IMU interrupt 1		
IMU_INT2	187	DI	IMU interrupt 2		
HSM_RST_N	207	DO	External HSM reset		

RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	9, 28, 60, 65, 82, 89, 119, 122, 123, 132, 136, 139, 142, 154, 157, 163, 166, 175, 178, 179, 188, 190, 193, 196, 200, 204, 205, 214, 223, 224, 225, 226, 227, 229, 252, 266, 268, 272, 273, 278, 279, 281, 282, 285, 286, 287, 288, 290, 291, 292, 293, 294, 299, 300, 301, 302, 303, 304, 305, 306, 403, 405, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 449, 450, 451, 452	Keep these pins open.

NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.

2.4.2. Pin Multiplexing

See ***document [1]*** for details about pin multiplexing of the module.

2.5. EVB Kit

Quectel supplies an evaluation board (V2X&5G EVB) with accessories to develop or test the module. For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Voice/Data	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** or device management related API function can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or device management related API function can set the module into airplane mode where the RF function is invalid.	
Low Power Mode	The module remains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the power consumption of the module is reduced to a very low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

1. See ***document [3]*** for details of device management API functions.
2. For more details about **AT+CFUN**, please contact Quectel Technical Support.

3.2. Power Saving

3.2.1. Low Power Mode (LPM)

The module is able to reduce its power consumption to a ultra-low level during the low power mode. This chapter mainly introduces methods to enter or exit LPM. The diagram below illustrates the power consumption of the module during LPM. See ***document [5]*** for details about LPM of the module.

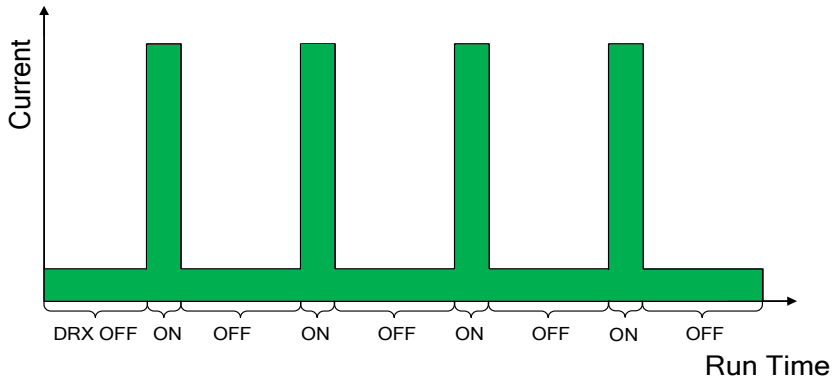


Figure 2: Module Power Consumption in Low Power Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1.1. LPM and Wakeup Functions

The module provides some specific GPIOs to implement the LPM/wakeup function between the module and the MCU.

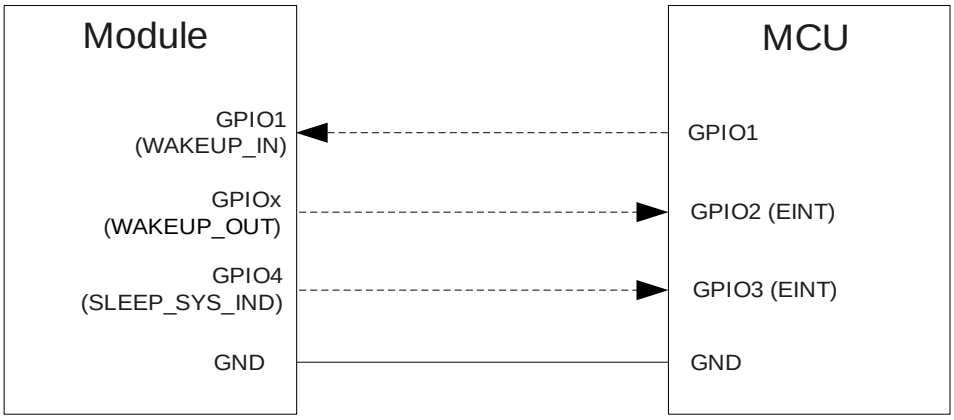


Figure 3: LPM/Wakeup Function Implementation Schematic Diagram

Table 8: GPIO Configuration Related to LPM/Wakeup Function

Pin Name	Pin No.	Default Function	Status Indication
GPIO1	100	WAKEUP_IN	● Falling edge: MCU controls the module to enter LPM ● Rising edge: MCU wakes up from LPM
GPIO4	104	SLEEP_SYS_IND	● Low level: the module enters LPM by default ● High level: the module exits LPM by default
GPIOx	User Specified	WAKEUP_OUT	Recommended design: ● Low level: the user application enters LPM ● High level: the user application exits LPM

See ***document [5]*** for details.

NOTE

1. Pay attention to the voltage-level matching of the circuit in dotted line, when the MCU interface is not 1.8 V power domain.
2. GPIO1 of the module is used as WAKEUP_IN (input signal) by default, through which the MCU informs the module to enter/exit LPM.
3. GPIOx can be any GPIO of the module, i.e., you can define any GPIO into WAKEUP_OUT (output signal).

3.2.1.2. LPM and Wakeup Timing

The following figure shows the LPM and wakeup timing of the module.

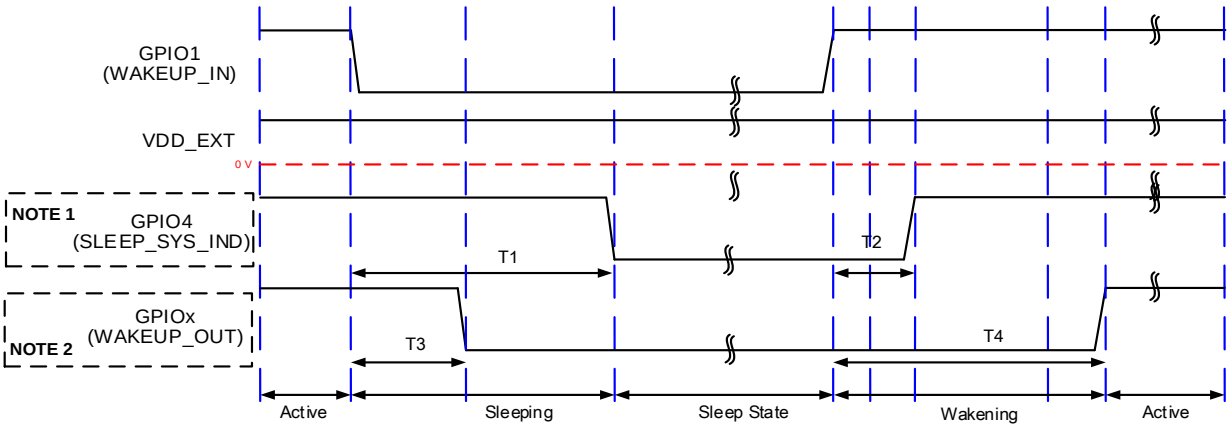


Figure 4: LPM Wakeup Timing

NOTE

1. The time (T1) between the falling edges of WAKEUP_IN and SLEEP_SYS_IND depends on the real application scenario. If the module needs to process any task during the period, the time will be longer.
2. T3 and T4 depends on the application.

3.2.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, all AT commands and API functions correlative with RF function will be inaccessible.

AT command:

The mode can be set via **AT+CFUN=<fun>**. The parameter **<fun>** of **AT+CFUN** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

API functions:

The mode can be set via device management related API functions. For more information about device management API functions, see ***document [3].***

NOTE

The execution of **AT+CFUN** or related API functions will not affect GNSS function.

3.3. Power Supply

3.3.1. Power Supply Pins

The module provides VBAT pin for connection with external power supplies. VBAT pins are separately used to supply power for three parts of the module.

- 10 VBAT_RF pins for module's RF part, distributed on two sides of the module.
- 3 VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 9: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	109, 111, 112, 114, 235, 236, 238, 239, 404, 412	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	241, 242, 244	Power supply for the module's baseband part	3.3	3.8	4.3	V
GND	6, 12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 406, 407, 408, 409, 410, 411, 413, 414				

3.3.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. If the voltage drop between the

input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +12/+24 V input power source when applying the module to 5G solution. The designed output is 3.8 V, and the maximum rated current of the DC-DC converter is 5 A.

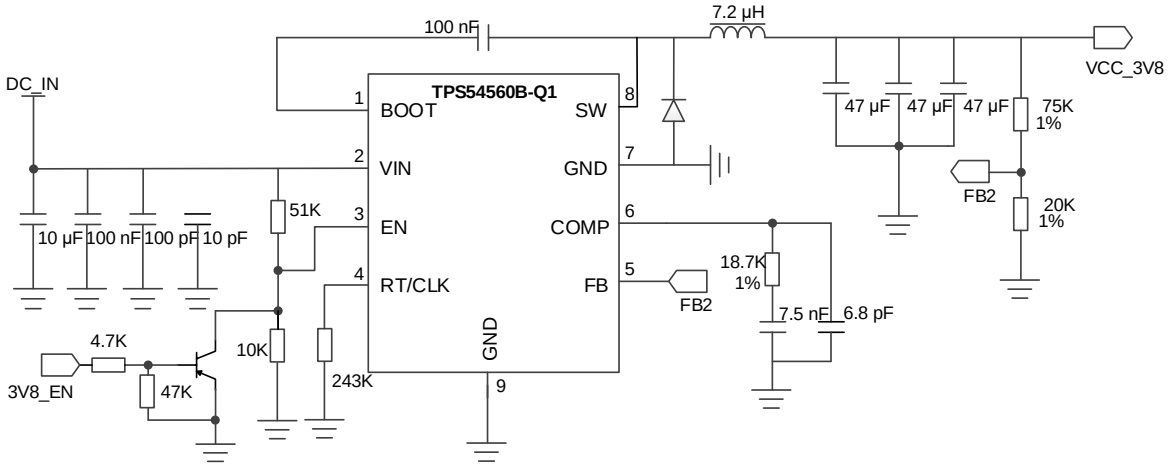


Figure 5: Reference Design of Power Supply

NOTE

1. To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or Linux power off commands or API functions can you cut off the power supply.
2. It is recommended to use the MCU's GPIO (3V8_EN) with the default type of pull down to control the power supply of the module, otherwise the module will shutdown abnormally when MCU updates the firmware and reboots. The GPIO of MCU can control the module to power off, only if the module crashes.

3.3.3. Voltage Stability Requirements

The power supply range of VBAT_BB and VBAT_RF is 3.3–4.3 V. Ensure that the input voltage of VBAT_BB and VBAT_RF never drops below 3.3 V. The following figure shows the voltage drop during high load (e.g. burst transmission in GSM and 5G NSA networks). The voltage drop will be less in 3G, 4G and 5G SA networks.

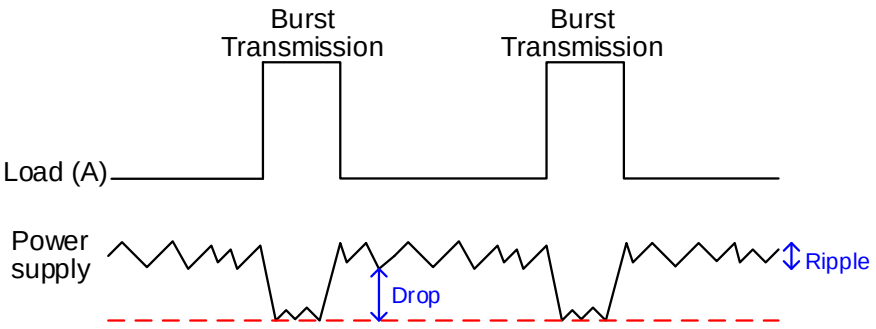


Figure 6: Power Supply Limits During Burst Transmission

To decrease voltage-drop, use bypass capacitors of at least 100 µF + 47 uF with low ESR for each group of VBAT_RF and VBAT_BB, and reserve multi-layer ceramic chip capacitor (MLCC) arrays due to their low ESR. It is recommended to use at least three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. While connecting the module to an external 3.8 V power supply, route VBAT_BB and VBAT_RF traces in star structure. The width of VBAT_BB trace should be not less than 1.5 mm. The width of VBAT_RF trace should be not less than 3 mm for the main power trace and 2 mm for the branch power trace. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use TVS diodes to prevent EOS, and place them as close to the VBAT pins as possible. The recommended power supply structure is presented in the figure below.

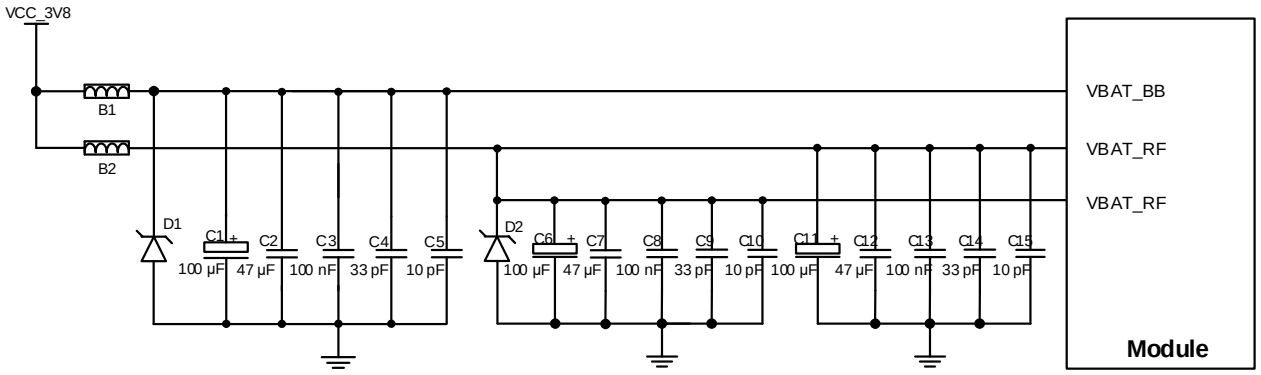


Figure 7: Power Supply Design

3.4. Turn-on

3.4.1. Turn-on with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Pull-up internally. Active low. Due to the voltage drop inside the chip, the pin has around 0.75 V level after the module is powered up.

When the module is in power down mode, it can be turned on by driving the PWRKEY pin low for at least 500 ms and releasing it. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

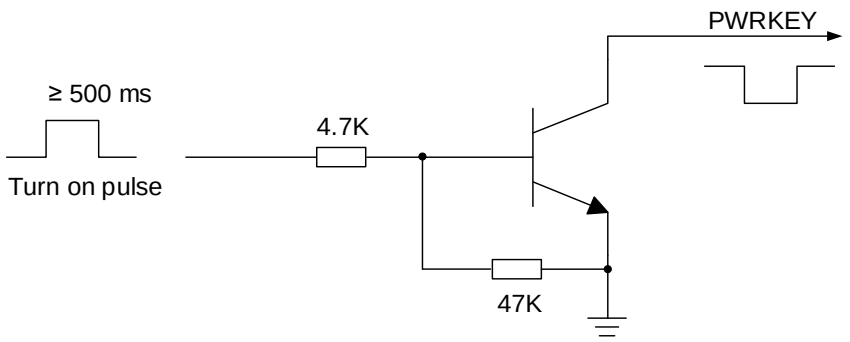


Figure 8: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

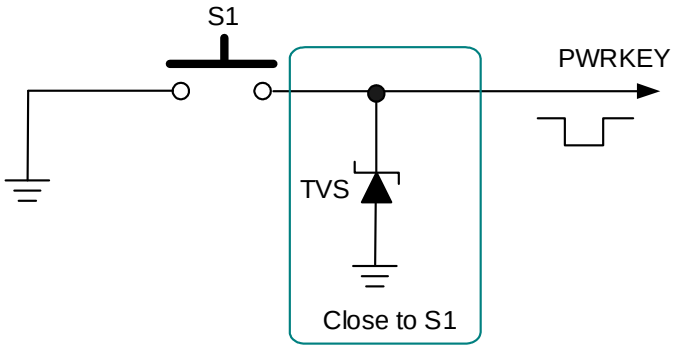


Figure 9: Turn On the Module Using a Button

The power-up timing is illustrated in the following figure.

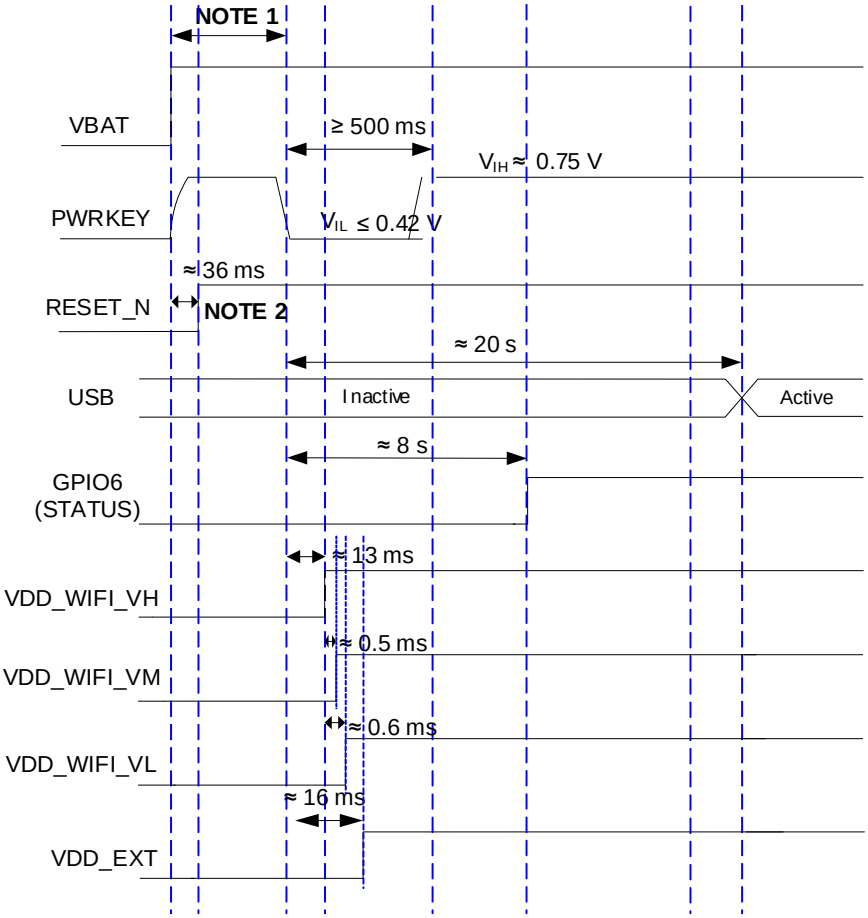


Figure 10: Power-up Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 50 ms.
2. RESET_N will be pulled high automatically when the voltage of VBAT is stable, therefore, MCU does not need to control RESET_N in the power-up timing.
3. The durations listed in the power-up timing above are for reference only. Note that there may be a few milliseconds of difference in the actual testing process, and Quectel only promises that power-on sequence is fixed.
4. The timing of GPIO6 is based on the test data of the factory version and will change accordingly when configured by application program.
5. Do not connect PWRKEY to GND. Pulling PWRKEY low for an extended period will trigger mandatory hardware reset.
6. Ensure that there is no capacitance larger than 10 nF on the PWRKEY pin.

3.4.2. Turn-on with CBL_PWR_N

The following table shows the pin definition of CBL_PWR_N.

Table 11: Pin Description of CBL_PWR_N

Pin Name	Pin No.	I/O	Description	Comment
CBL_PWR_N	248	DI	Cable power-on; initiates power on when grounded	Pulled up internally. Active low. Pulling it low for an extended period will not trigger hardware reset.

When the module is in power down mode, the module can be turned on by driving CBL_PWR_N low to GND. This action only triggers the module to turn on, it does not initiate power-off. After the module is turned on, the pin status of CBL_PWR_N can be disregard.

A simple reference circuit is illustrated in the following figure.

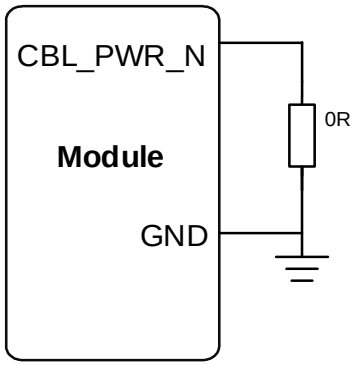


Figure 11: Turn On the Module Using CBL_PWR_N

NOTE

If the CBL_PWR_N pin remains low without being released, the module will turn on again after executing the module shutdown.

3.5. Turn-off

Any of the following methods can be used to turn off the module normally:

- Turn off the module using the PWRKEY pin.
- Turn off the module using Linux commands.
- Turn off the module using API function.

3.5.1. Turn-off with PWRKEY

It is recommended that driving PWRKEY low for at least 2 s and then releasing it will enable the module to execute turn-off procedure. The power-down scenario is illustrated in the following figure.

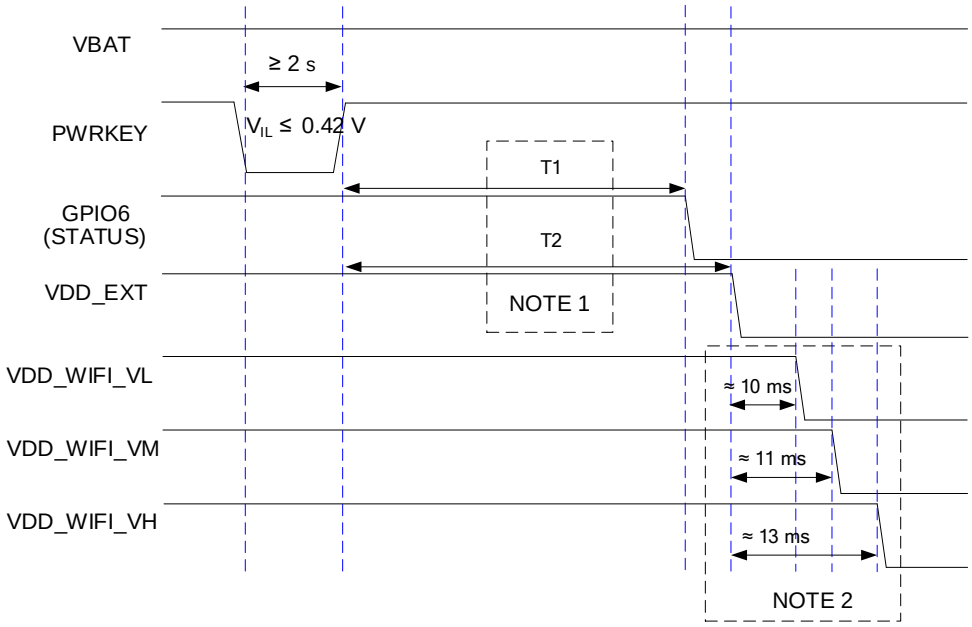


Figure 12: Power-down Timing

NOTE

1. The releasing time of GPIO6 and the power-down time of the power supply (e.g VDD_EXT) depend on the actual running business, and if the module has tasks to deal with during shutdown, the time may be longer.
2. The durations listed in power-down timing above are for reference only. Note that there may be a few milliseconds of difference in the actual testing process, and Quectel only promises that the power-down sequence is fixed.
3. Driving PWRKEY low for 1.5–2 s may result in an unexpected power-down.

3.5.2. Turn-off with Linux Commands/API Function

It is also a safe way to use API functions or Linux commands, such as **shutdown** and **poweroff**, to turn off the module, which is similar to turning off the module via PWRKEY pin.

For more information about the API function for powering off the module, see ***document [3].***

NOTE

1. To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or Linux power off commands or API function can you cut off the power supply.

2. When you turn off module with Linux commands or API function, keep PWRKEY at high level after the execution of Linux commands or API function. Otherwise, the module will be turned on again after successful turn-off.

3.6. RESET_N

The module can be reset by driving RESET_N low for 250–550 ms and then releasing it. As the RESET_N pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground surrounded.

Table 12: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	8	DI	Reset the module	Pulled up internally. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

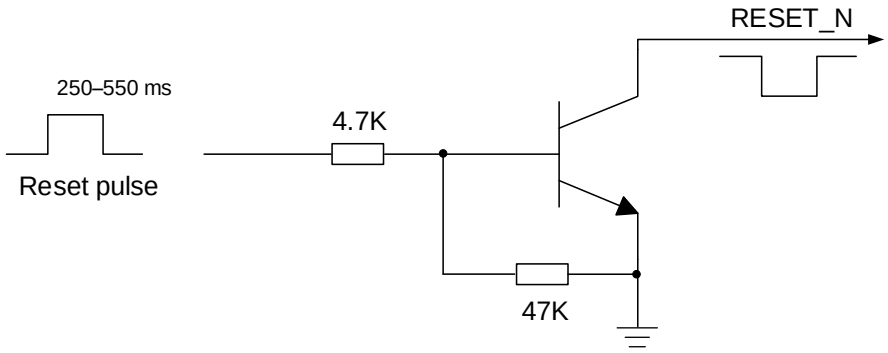


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

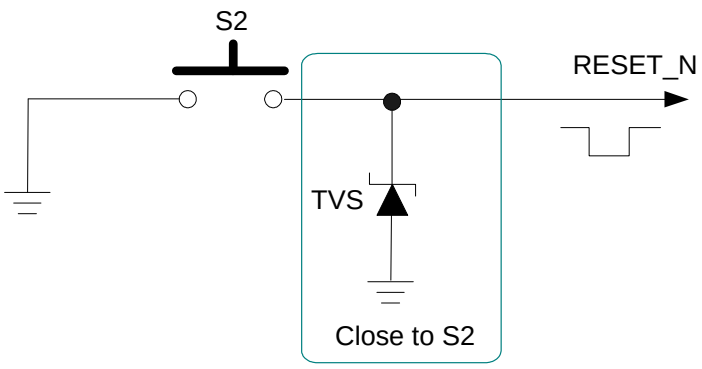


Figure 14: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

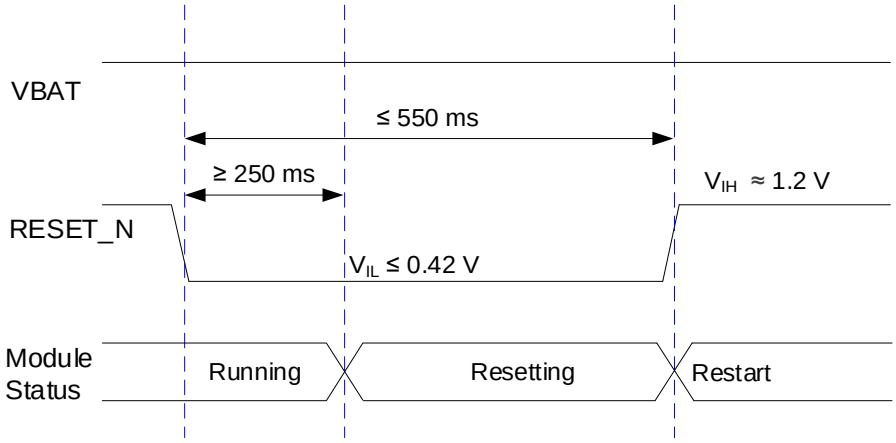


Figure 15: Reset Timing

NOTE

1. RESET_N should only be used when turning off the module by PWRKEY or Linux commands or API function all failed.
2. Ensure that there is no capacitance larger than 10 nF on RESET_N pin.
3. Do not connect RESET_N to GND. Pulling RESET_N low for an extended period (≥ 16 s) will trigger mandatory hardware shutdown.

4 Application Interfaces

4.1. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. The (U)SIM1 interface supports 1.8/3.0 V (U)SIM card. The (U)SIM2 interface supports 1.8 V (U)SIM card by default, 3.0 V is optional.

The module supports dual (U)SIM cards, and (U)SIM1 is the primary interface.

Table 13: Pin Description of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	251	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_CLK	253	DO	(U)SIM1 card clock	
USIM1_RST	250	DO	(U)SIM1 card reset	
USIM1_DATA	254	DIO	(U)SIM1 card data	
USIM2_VDD	256	PO	(U)SIM2 card power supply	Only 1.8 V is supported by default. 3.0 V is optional.
USIM2_CLK	259	DO	(U)SIM2 card clock	
USIM2_RST	260	DO	(U)SIM2 card reset	
USIM2_DATA	257	DIO	(U)SIM2 card data	
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep them open.
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect	

The module supports (U)SIM card hot-plug via USIM_DET pins, and either low-level or high-level detection is supported. The function is disabled by default, and can be enabled by related software command.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

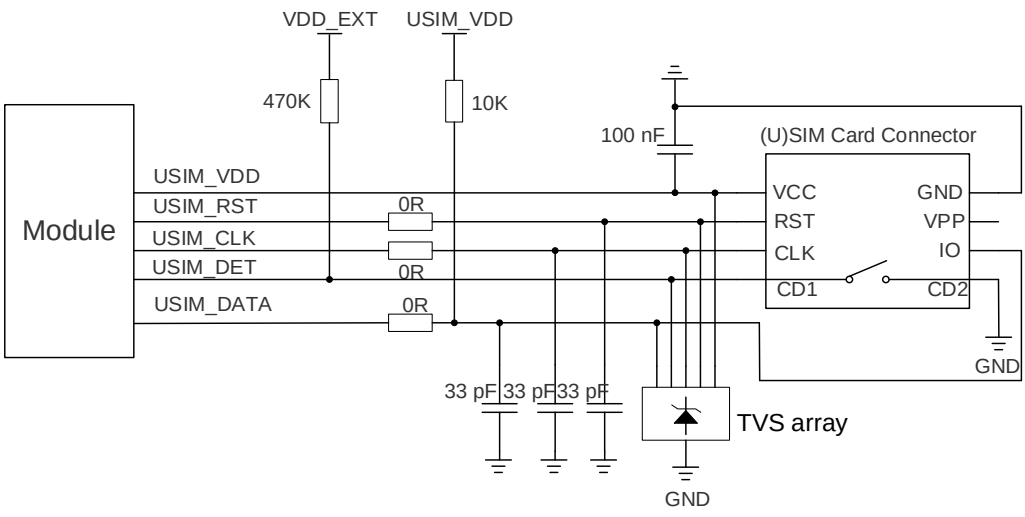


Figure 16: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference design of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

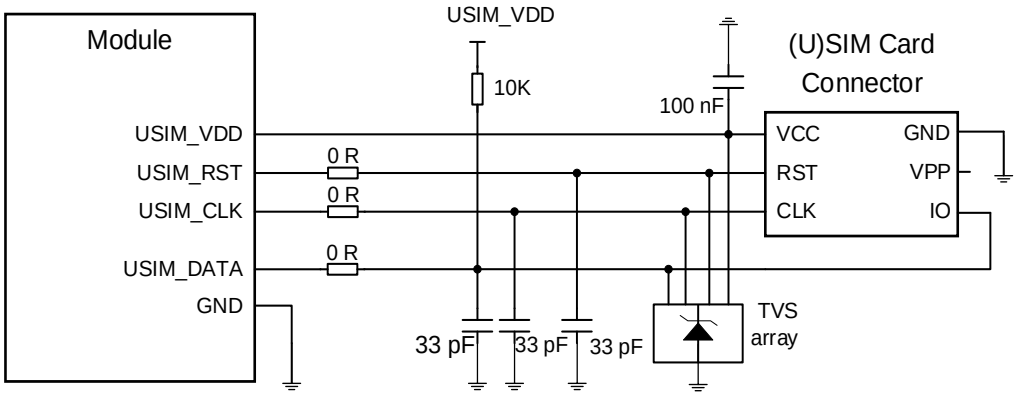


Figure 17: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Ensure the tracing between the ground of (U)SIM card connector and the module is short and wide. To maintain the same electrical potential, the trace width for USIM_VDD must be at least 0.5 mm.
- To avoid cross talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 10 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector

to suppress EMI and enhance ESD protection. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.

- USIM_DATA must be connected to USIM_VDD with a 10 kΩ pull-up resistor. The pull-up resistor can improve anti-jamming capability and should be placed close to the (U)SIM card connector.

4.2. USB Interface

The module provides one USB interface. The USB interface complies with the USB 3.1 Gen 2 and USB 2.0 specifications, and supports SuperSpeed (10 Gbps) on USB 3.1, high-speed (480 Mbps) and full-speed (12 Mbps) on USB 2.0.

Both USB 2.0 interface and USB 3.1 interface can be used for firmware upgrade, AT command communication, data transmission, GNSS NMEA sentences output and software debugging.

The following table shows the pin definition of USB interface.

Table 14: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	84	DI	USB connection detect	Maximum current: 0.1 mA Typical 5.0 V. A 47 kΩ resistor is connected in series inside the module. If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved.
USB_DP	85	AIO	USB 2.0 differential data (+)	Compliant with USB 2.0 standard specifications. Require differential impedance of 90 Ω. If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved.
USB_DM	87	AIO	USB 2.0 differential data (-)	
USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)	Compliant with USB 3.1 standard specifications. Require differential
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)	

USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)	impedance range of 70–100 Ω and 85 Ω is recommended.
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)	

It is recommended to use USB 2.0 for firmware upgrading in application designs. USB 2.0 interface reference circuit is presented below.

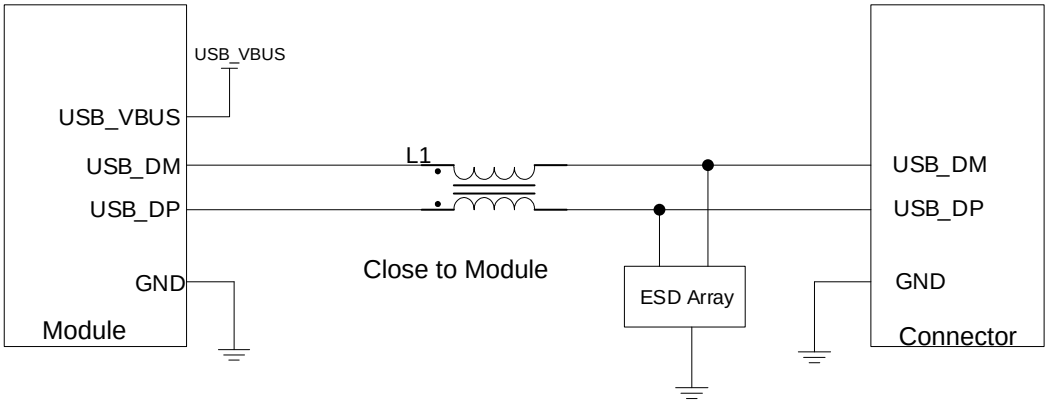


Figure 18: Reference Design of USB 2.0 Application

In USB 2.0 applications, it is recommended to add a common mode choke L1 in series between the module and the connector to suppress EMI.

USB 3.1 interface reference circuit is presented below.

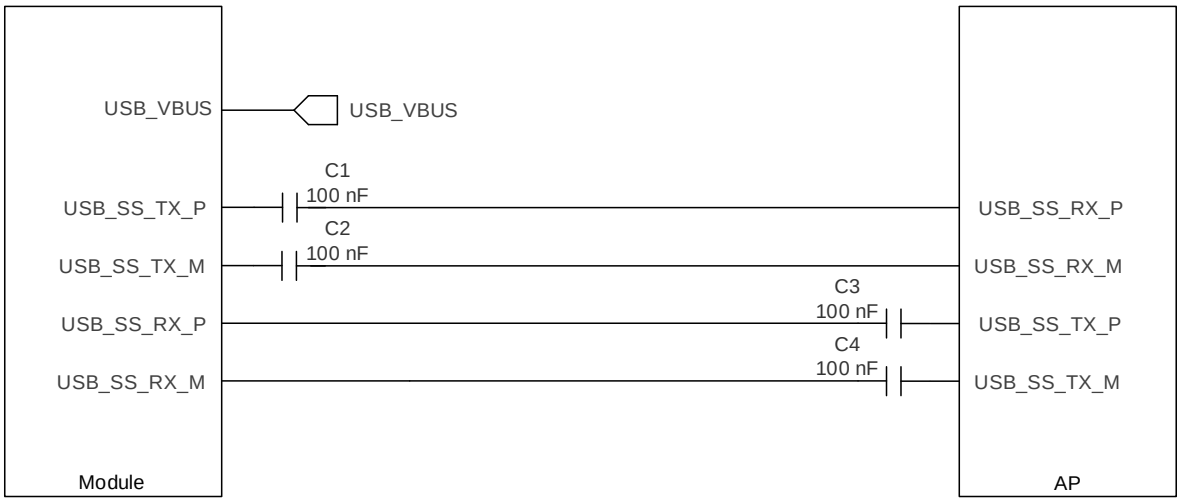


Figure 19: Reference Design of USB 3.1 Application

In USB 3.1 applications, place C1 and C2 near the module, and place C3 and C4 near the AP. The extra stubs of trace must be as short as possible.

To meet USB 2.0 and USB 3.1 specifications, the following principles of USB interface should be complied with.

- It is important to route the USB 2.0 and 3.1 signal traces as differential pairs with total grounding. The recommended differential impedance is 90 Ω for USB 2.0 and 85 Ω for USB 3.1.
- The intra-lane length match should be less than 2.0 mm for USB 2.0 and 0.7 mm for USB 3.1.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. Route the RF signals operating at a 2.4 GHz frequency with the highest isolation possible from the USB_SS_TX/RX traces.
- If a USB connector is used, keep the ESD protection components as close to the USB connector as possible. Junction capacitance of the ESD protection device might cause influences on USB data traces, so pay attention to the selection of the device. Typically, the parasitic capacitance should be less than 2.0 pF for USB 2.0 and less than 0.3 pF for USB 3.1.
- Keep isolation between the USB_SS_TX pair, USB_SS_RX pair, and USB_DP/USB_DM to avoid crosstalk.
- USB_SS_TX AC coupling capacitors can be anywhere along the trace, but it is better to place them close to the source or the ESD/connector side to keep good signal integrity of the main route on the PCB.

For more details about the USB 2.0 and USB 3.1 specifications, visit http://www.usb.org/home.

NOTE

1. The module supports master mode, but works in slave mode by default.
2. The high-speed PHY and SuperSpeed PHY share the same USB 3.1 Gen 2 controller inside baseband chipset, so USB 2.0 and USB 3.1 cannot be used simultaneously. When USB 2.0 and USB 3.1 are connected to the same host, USB 3.1 takes effect by default.
3. As for the AC coupling capacitors C1–C4, the recommended value is 220 nF for USB 3.1 Gen 2 and 100 nF for USB 3.1 Gen 1.

4.3. UART Interfaces

The module provides five UART interfaces: UART1, UART2, UART3, UART4 and debug UART. The following are the features of these UART interfaces.

Table 15: Basic Information of UART Interfaces

UART Type	Supported Baud Rate (bps)	Default Baud Rate (bps)	Description
UART1	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	9600	● Data transmission ● Support RTS and CTS hardware flow control
UART2 [11] (Bluetooth UART)		9600	
UART3		9600	Data transmission
UART4		9600	
Debug UART [12]	115200	115200	Used for Linux console and log output

For more details about baud rate and hardware flow control, see ***document [6].*** The following tables show the pin definition of the UART interfaces.

Table 16: Pin Description of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART1_TXD	70	DO	UART1 transmit	1.8 V power domain. If unused, keep these pins open.
UART1_RXD	72	DI	UART1 receive	
UART1_CTS	71	DO	Clear to send signal from the module	Connect to the MCU's CTS. 1.8 V power domain. If unused, keep the pin open.
UART1_RTS	74	DI	Request to send signal to the module	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep the pin open.
UART2_TXD	59	DO	UART2 transmit	1.8 V power domain. If unused, keep these pins open.
UART2_RXD	63	DI	UART2 receive	
UART2_CTS	62	DO	Clear to send signal from the module	If unused, keep it open. Connect to the Wi-Fi & Bluetooth module's CTS.
UART2_RTS	61	DI	Request to send signal to the module	If unused, keep it open. Connect to the Wi-Fi & Bluetooth module's RTS.

[11] UART2 is used for Bluetooth application by default, but also can be connected to other peripherals. For more details about Bluetooth application, see ***Chapter 4.8.***
[12] The debug UART pins are dedicated ones and cannot be multiplexed into other functions.

UART3_TXD	298	DO	UART3 transmit	1.8 V power domain. If unused, keep these pins open.
UART3_RXD	297	DI	UART3 receive	
UART4_TXD	296	DO	UART4 transmit	
UART4_RXD	295	DI	UART4 receive	
DBG_TXD	107	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved for debug UART.
DBG_RXD	110	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. Use a voltage-level translator if your application is equipped with a 3.3 V UART interface. It is recommended that the enable pin of the voltage-level translator is controlled by VDD_EXT to eliminate the possible influence of current sinking from its internal circuits (e.g. pull-ups) into the module.

The following figure shows a reference design.

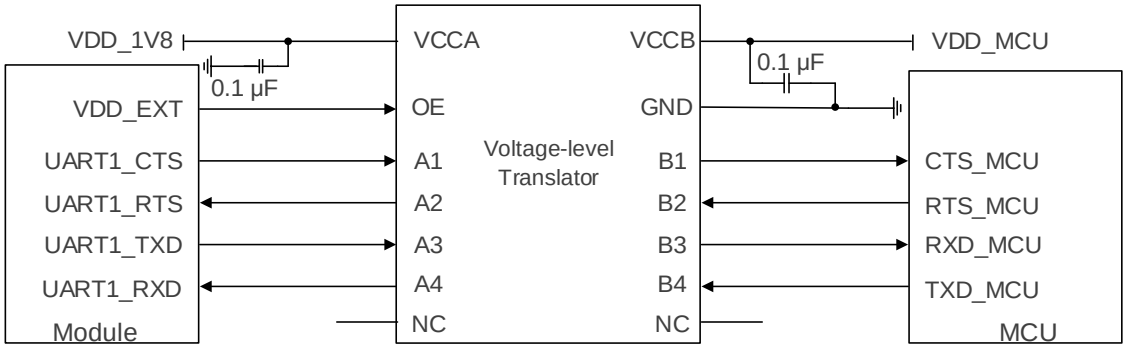


Figure 20: Reference Design of UART Interface with Translator Chip (UART1)

Another example with transistor translation circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

Ensure the VDD_1V8 are not powered on before VDD_EXT, otherwise its pull-up may affect the normal startup of the module.

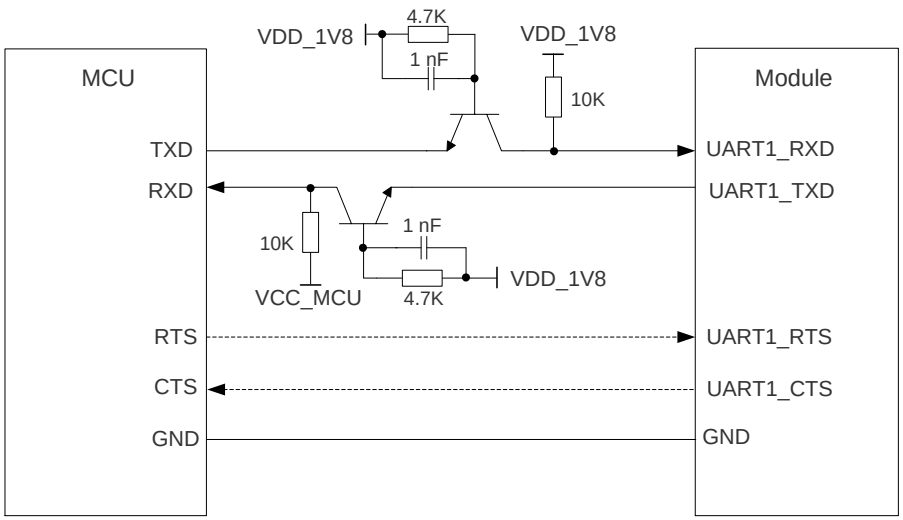


Figure 21: Reference Circuit with Transistor Circuit (UART1)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. To increase the stability of UART communication, it is recommended to add UART hardware flow control design. If hardware flow control is intended to be used, then CTS and RTS should also be designed with the level shifting circuit.
3. Please note that the module' s CTS is connected to the MCU/Wi-Fi & Bluetooth module' s CTS, and the module' s RTS is connected to the MCU/Wi-Fi & Bluetooth module' s RTS.
4. When the module enters LPM, it is recommended to switch off the power supply for VDD_1V8 to reduce power consumption.
5. The level-shifting circuits (***Figure 20*** & ***Figure 21***) are illustrated using UART1 as an example. The circuits of the debug UART and the UART2/UART3/UART4 are connected in the same way as the UART1.

4.4. I2S and I2C Interfaces

The module provides two I2S interfaces and two I2C interfaces.

I2S:

- I2S1 is used for external audio codec by default.
- I2S2 can be used according to your application.

I2C:

- I2C1 is used for external audio codec by default.
- I2C2 is used for IMU (inertial measurement unit) by default.

The following table shows the pin definition of I2S and I2C interfaces.

Table 17: Pin Description of I2S Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MCLK	81	DO	Clock output for codec	12.288 MHz clock output
I2S1_WS	265	DIO	I2S1 word select	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
I2S1_SCK	262	DIO	I2S1 clock	
I2S1_DIN	263	DI	I2S1 data in	1.8 V power domain.
I2S1_DOUT	261	DO	I2S1 data out	
CDC_RST_N	77	DO	External codec reset	
I2S2_WS	443	DIO	I2S2 word select	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
I2S2_SCK	444	DIO	I2S2 clock	
I2S2_DIN	445	DI	I2S2 data in	1.8 V power domain.
I2S2_DOUT	446	DO	I2S2 data out	

Table 18: Pin Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	80	OD	I2C1 serial data	Require external pull-up to 1.8 V. If unused, keep these pins open.
I2C1_SCL	79	OD	I2C1 serial clock	
I2C2_SDA	264	OD	I2C2 serial data	
I2C2_SCL	267	OD	I2C2 serial clock	

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.

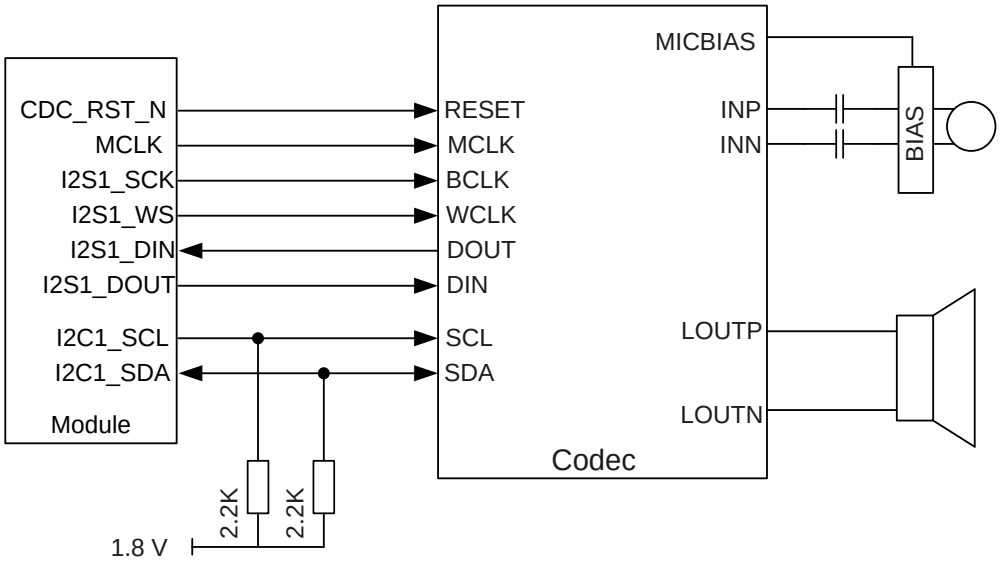


Figure 22: Reference Design of I2S1 and I2C1 Interfaces with External Audio Codec

NOTE

1. It is recommended to reserve an RC circuit on the I2S1 signal traces, especially for I2S1_SCK and MCLK.
2. The module works as a master device in I2C applications.

4.5. PCM Interface

The module provides one PCM interface for Bluetooth audio transmission by default. See ***Chapter 4.8*** for details. The PCM interface supports primary (short frame sync) and auxiliary (long frame sync) modes.

Table 19: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	73	DIO	PCM data frame sync	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
PCM_CLK	75	DIO	PCM clock	
PCM_DIN	76	DI	PCM data input	1.8 V power domain.
PCM_DOUT	78	DO	PCM data output	

The module supports 16-bit linear data format. Clock and mode can be configured, and the default

configuration is primary mode using short frame sync format with 1536 kHz PCM_CLK and 48 kHz PCM_SYNC. For more details, see ***document [7]***.

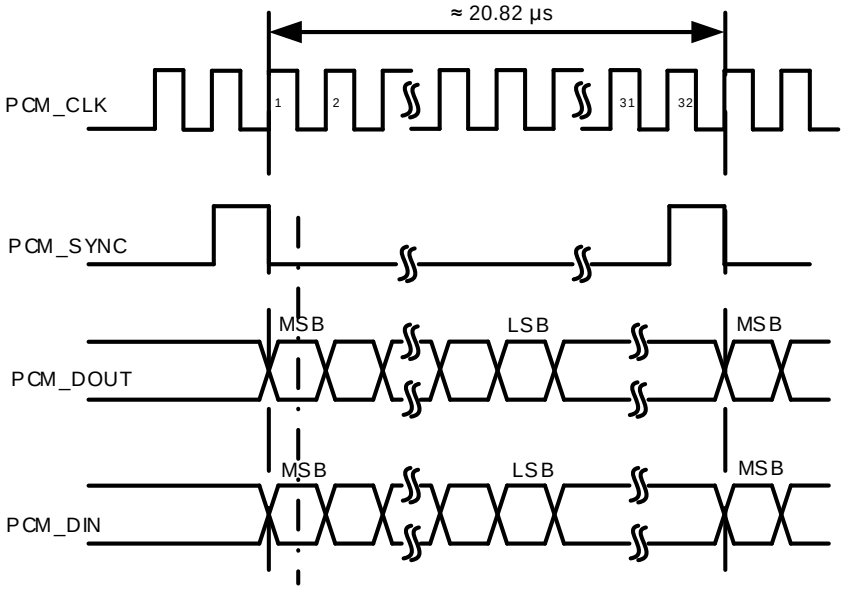


Figure 23: PCM Timing (Short Frame Sync)

NOTE

When using Bluetooth function, PCM_SYNC and PCM_CLK can only be used as output signals.

4.6. SDIO Interfaces

The module provides two SDIO interface:

- SDIO1 can be used for eMMC function. 4-bit by default, max. up to 8-bit, supports 1.8 V only.
- SDIO2 can be used to connect to external DSRC module if required. 4-bit by default, supports 1.8 V only.

The following tables show the pin definition of SDIO interface.

Table 20: Pin Description of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment

SDIO1_DATA0	49	DIO	SDIO1 data bit 0	1.8 V power domain.
SDIO1_DATA1	50	DIO	SDIO1 data bit 1	
SDIO1_DATA2	51	DIO	SDIO1 data bit 2	
SDIO1_DATA3	52	DIO	SDIO1 data bit 3	
SDIO1_CMD	48	DIO	SDIO1 command	
SDIO1_CLK	47	DO	SDIO1 clock	
SDIO1_RCLK	57	DI	SDIO1 return clock	
SDIO1_DATA4	53	DIO	SDIO1 data bit 4	
SDIO1_DATA5	55	DIO	SDIO1 data bit 5	
SDIO1_DATA6	56	DIO	SDIO1 data bit 6	
SDIO1_DATA7	58	DIO	SDIO1 data bit 7	
EMMC_RST_N	54	DO	eMMC reset	1.8 V power domain. The pin function is not supported.
EMMC_PWR_EN	45	DO	eMMC power supply enable control	1.8 V power domain.
SDIO2_DATA0	1	DIO	SDIO2 data bit 0	1.8 V power domain.
SDIO2_DATA1	2	DIO	SDIO2 data bit 1	
SDIO2_DATA2	4	DIO	SDIO2 data bit 2	
SDIO2_DATA3	5	DIO	SDIO2 data bit 3	
SDIO2_CMD	269	DIO	SDIO2 command	
SDIO2_CLK	270	DO	SDIO2 clock	
SDIO2_RCLK	3	DI	SDIO2 return clock	

4.6.1. Reference Design for eMMC Application

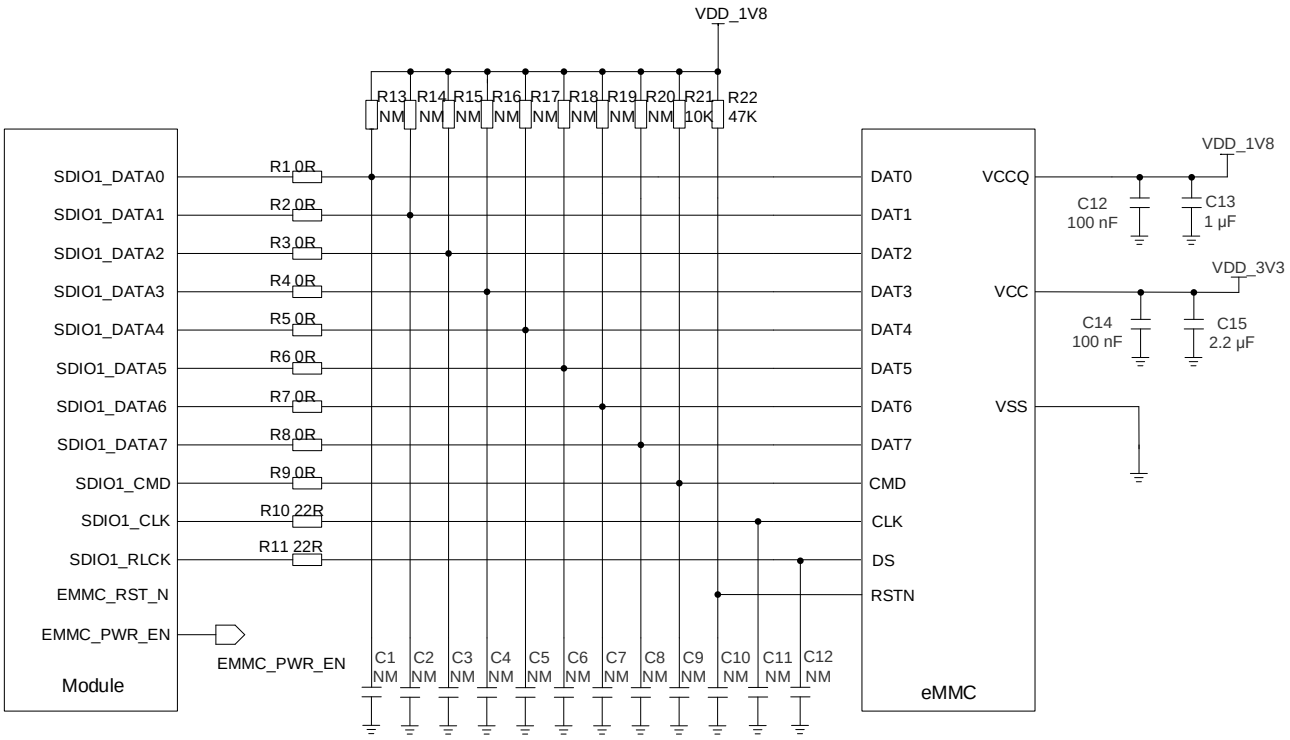


Figure 24: Reference Design for eMMC Application

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve R13–R20 (10–100 kΩ) to pull up SDIO signals to an external 1.8 V VDD. The resistors are not mounted by default, and the recommended value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R1–R11 in series between the module and eMMC. Resistor R10, R11 should be 20–30 Ω and the other resistors are 0 Ω by default. The bypass capacitors C1–C12 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA[0:7]/SDIO_CMD/SDIO_RCLK less than 1 mm and the total routing length less than 60 mm. The total trace length for SDIO1 inside the module is 38 mm, so the exterior total trace length should be less than 22 mm. For SDIO2, the total trace length inside the module is 14 mm, so the exterior total length can be 46 mm.
- Keep the spacing between SDIO and other signal traces at least 2.5 times the trace width.

4.7. PCIe Interfaces

The module provides two PCIe 3.0 interface.

- PCIe1:
  - Supports RC and EP modes, and works in RC mode by default.
  - Supports 2 lanes.
  - Can be used to connect to an external WLAN chip or application processor.
- PCIe2:
  - Supports RC mode only.
  - Supports 1 lane
- Compliant with *PCI Express Base Specification Revision 3.0*
- Maximum rate: 8 GT/s × 1 lane
- Backward compatible

Table 21: Pin Description of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE1_REFCLK_P	40	AIO	PCIe1 reference clock (+)	Serve as output signals in RC mode. Serve as input signals in EP mode. The differential impedance should be the same as that for PCIE_TX/RX.
PCIE1_REFCLK_M	38	AIO	PCIe1 reference clock (-)	
PCIE1_TX0_M	44	AO	PCIe1 transmit 0 (-)	If PCIE1_TX and PCIE1_RX are unused, keep these pins unconnected. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE1_TX0_P	46	AO	PCIe1 transmit 0 (+)	
PCIE1_TX1_M	41	AO	PCIe1 transmit 1 (-)	
PCIE1_TX1_P	43	AO	PCIe1 transmit 1 (+)	
PCIE1_RX0_M	32	AI	PCIe1 receive 0 (-)	
PCIE1_RX0_P	34	AI	PCIe1 receive 0 (+)	
PCIE1_RX1_M	35	AI	PCIe1 receive 1 (-)	
PCIE1_RX1_P	37	AI	PCIe1 receive 1 (+)	
PCIE1_CLKREQ_N	36	DIO	PCIe1 clock request	Serve as input signals in RC mode. Serve as output signals in EP mode.
PCIE1_WAKE_N	30	DIO	PCIe1 wake up	

				1.8 V power domain.
PCIE1_RST_N	39	DIO	PCIe1 reset	Serves as an output signal in RC mode. Serves as an input signal in EP mode. 1.8 V power domain.
PCIE2_REFCLK_P	437	AO	PCIe2 reference clock (+)	Only supports RC mode. The differential impedance should be the same as that for PCIE_TX/RX.
PCIE2_REFCLK_M	436	AO	PCIe2 reference clock (-)	
PCIE2_TX_P	439	AO	PCIe2 transmit (+)	If PCIE2_TX and PCIE2_RX are unused, keep these pins unconnected. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE2_TX_M	438	AO	PCIe2 transmit (-)	
PCIE2_RX_P	435	AI	PCIe2 receive (+)	
PCIE2_RX_M	434	AI	PCIe2 receive (-)	
PCIE2_CLKREQ_N	442	DI	PCIe2 clock request	Only supports RC mode.
PCIE2_WAKE_N	440	DI	PCIe2 wakeup	
PCIE2_RST_N	441	DO	PCIe2 reset	Only supports RC mode.

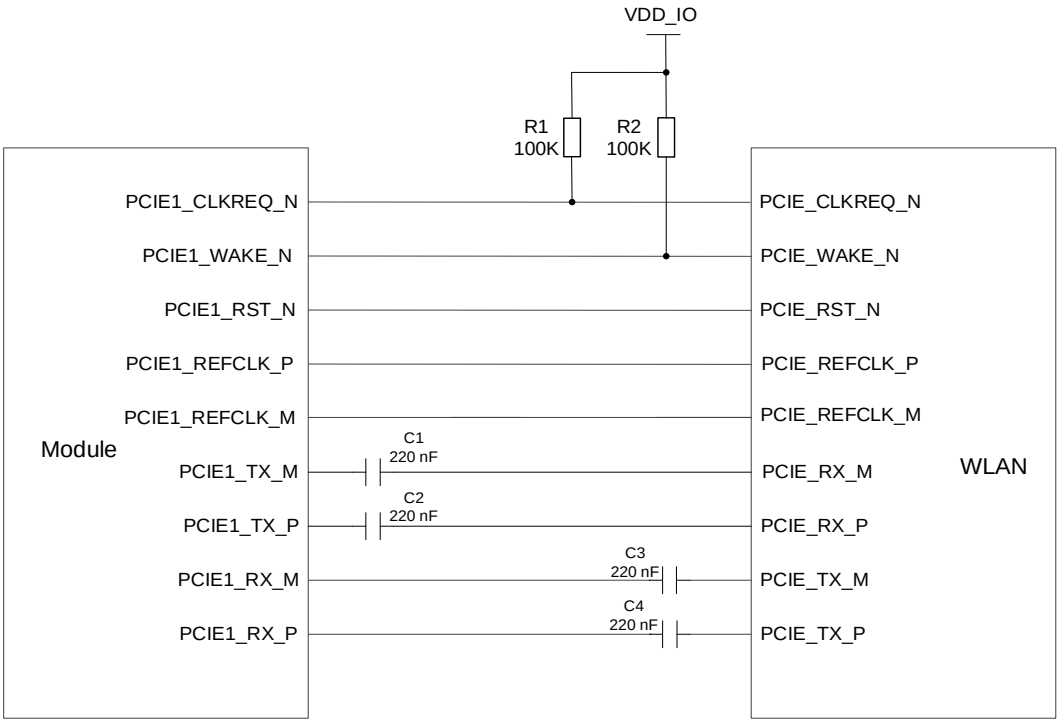


Figure 25: Reference Design of PCIe Interface

To meet PCIe specifications and enhance the reliability of applications, follow the criteria below in the PCIe interface circuit design:

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 70–100 Ω and 85 Ω is recommended for PCIe Tx/Rx/REFCLK traces.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required.
- Do not stagger the capacitors, as this can affect the differential integrity of the design and can create EMI.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions for the main route on the PCB (that is, apply layer transitions only at break in and break out regions). When the differential signal traces changes layers, create ground vias near signal vias, and create at least 1–3 ground vias for each differential pair.
- Avoid bending of the traces to avoid common mode noise to the system. When bending is required, maintain a bend angle greater than 135° as shown in the figure below, and the shortest trace caused by bending should be at least 1.5 times the trace width (1.5W). The spacing between Tx and Rx pairs, and the spacing between PCIe lanes and all other signals, should exceed 4 times the trace width (4W).

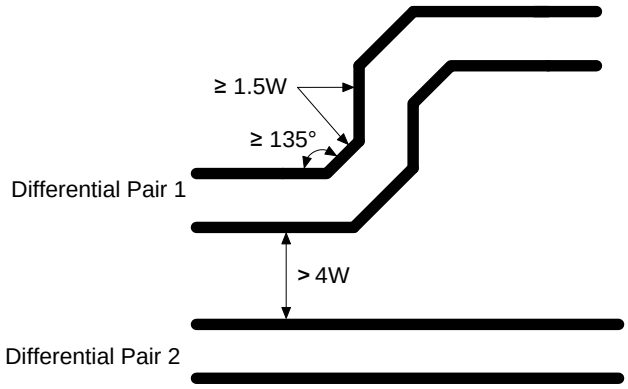


Figure 26: Curved Trace of Differential Pair

- PCIe Tx AC coupling capacitors can be anywhere along the line, but better to be placed close to the source or the receiver side to keep good signal integrity of main route on PCB. Use a serpentine to keep the difference pairs equal in the break out region as much as possible, to ensure that the traces stay differential thereafter. The length of each serpentine section should be at least 3 times the trace width (≥ 3W), and the maximum spacing between the serpentine section and the other differential trace should be less than twice of the normal differential trace spacing (S1 < 2S).

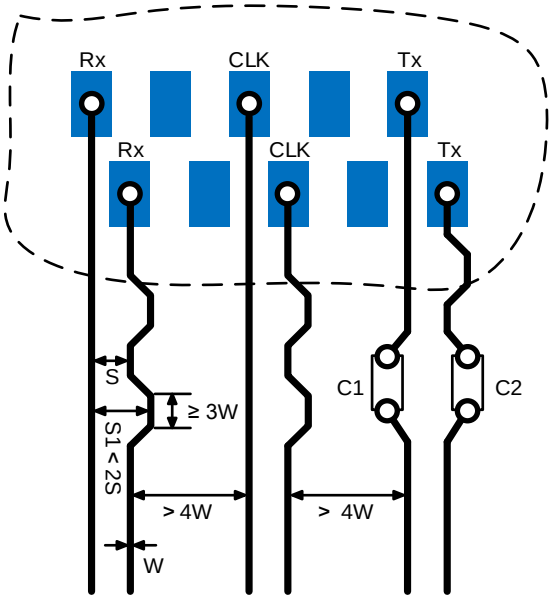


Figure 27: PCIe Trace Requirements

- PCIe Tx AC coupling capacitors should be 220 nF for PCIe Gen 3 applications, and 100 nF for PCIe Gen 2 applications.
- The maximum trace length of each differential pair for PCIe Gen 3 applications should be less than 300 mm, and that for PCIe Gen 2 applications less than 250 mm.

4.8. WLAN and Bluetooth Application Interfaces

The module provides one PCIe1 interface for WLAN function (see ***Chapter 4.7*** for more details), Bluetooth UART and PCM interfaces for Bluetooth function (see ***Chapter 4.3*** and ***Chapter 4.5*** for more details), as well as 4 power supply pins, a coexistence interface and other interfaces for Wi-Fi & Bluetooth.

The following table shows the pin definition of WLAN and Bluetooth application interfaces.

Table 22: Pin Description of WLAN and Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	Comment
Power Supply Interface				
VDD_EXT	68	PO	Provide 1.8 V for external circuits	This pin can be used to connect with VDD_IO of Quectel Wi-Fi & Bluetooth

				module, it also can be used as power supply for external pull up circuits. A test point is recommended to be reserved.
VDD_WIFI_VL	274, 275	PO	Low-voltage power supply for Wi-Fi & Bluetooth modules	After the Wi-Fi driver is loaded, the output voltage of these pins will be adjusted automatically to adapt to Wi-Fi & Bluetooth module.
VDD_WIFI_VM	276	PO	Medium-voltage power supply for Wi-Fi & Bluetooth modules	
VDD_WIFI_VH	277	PO	High-voltage power supply for Wi-Fi & Bluetooth modules	
Coexistence Control Interface				
COEX_TXD	69	DO	LTE & WLAN & Bluetooth coexistence transmit	1.8 V power domain.
COEX_RXD	67	DI	LTE & WLAN & Bluetooth coexistence receive	
Others Interfaces				
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	Used for Quectel Wi-Fi & Bluetooth module power control.
WLAN_EN	228	DO	WLAN function enable control	
BT_EN	66	DO	Bluetooth enable control	
HOST_SW_CTRL	184	DI	Switch control	Output signal from Quectel Wi-Fi & Bluetooth module.
WLAN_SLP_CLK	231	DO	WLAN 32 kHz sleep clock	If unused, keep it open.

NOTE

When WLAN or Bluetooth function is intended to be used, the coexistence interface must be used simultaneously. The coexistence interface cannot be used as general-purpose UART interface.

The module supports use in conjunction with Quectel Wi-Fi 5/6/6E modules, such as AF31G (PCIe), AF65E, AF67E and AF68E. For more details, please contact Quectel Technical Support. The following figure shows the application of the module with Quectel Wi-Fi & Bluetooth module using AF67E as an example. For more details, see ***document [7]***.

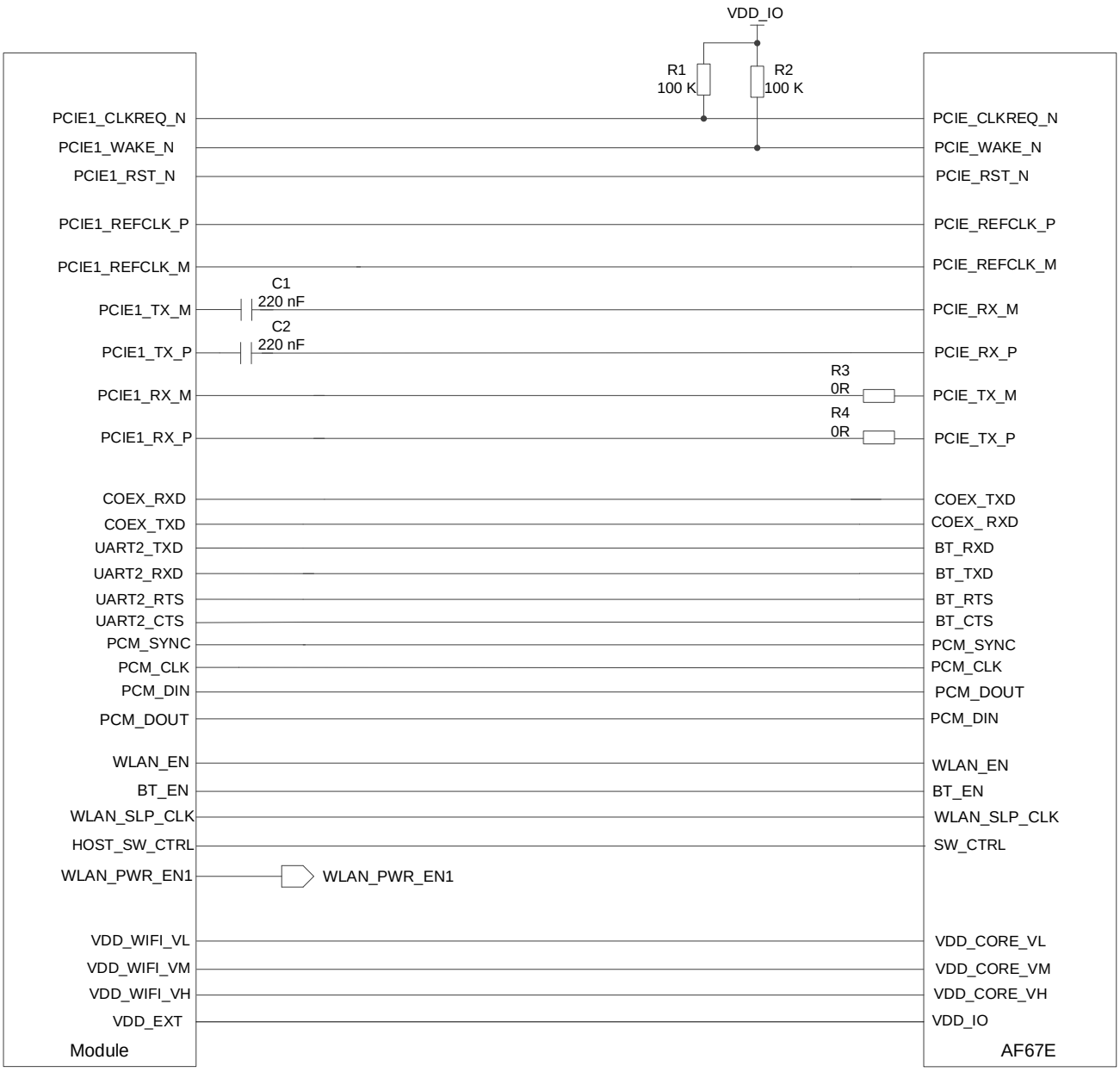


Figure 28: Reference Design of WLAN & Bluetooth Application Interfaces (AF67E)

NOTE

1. For the AF67E module, 220 nF coupling capacitors has been built-in on PCIe Tx signal traces, 0 Ω resistors can be placed externally.
2. When using Bluetooth function, PCM_SYNC and PCM_CLK can only be used as output signals.

4.9. SPIs

The module provides two SPIs by default, which support master and slave* modes. The maximum clock frequency rate is up to 50 MHz. The following tables show the pin definition of SPIs.

Table 23: Pin Description of SPIs

Pin Name	Pin No.	I/O	Description	Comment
SPI1_CLK	216	DO	SPI1 clock	1.8 V power domain. SPI1 supports master mode by default. Contact Quectel Technical Support if slave mode needs to be supported.
SPI1_CS	213	DO	SPI1 chip select	
SPI1_MISO	219	DI	SPI1 master-in slave-out	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	
SPI2_CLK	103	DO	SPI2 clock	1.8 V power domain. SPI2 supports master mode by default. Contact Quectel Technical Support if slave mode needs to be supported.
SPI2_CS	105	DO	SPI2 chip select	
SPI2_MISO	106	DI	SPI2 master-in slave-out	
SPI2_MOSI	108	DO	SPI2 master-out slave-in	

The following figure shows the timing relationship of SPIs.

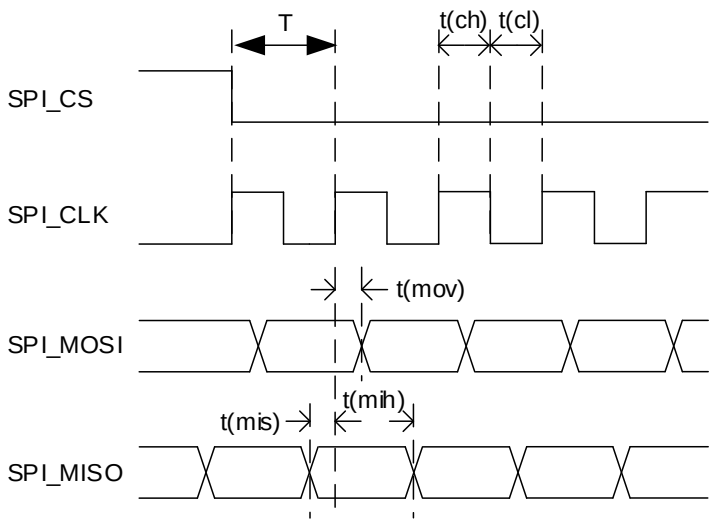


Figure 29: SPI Timing

The related parameters of SPI timing are shown in the table below.

Table 24: Parameters of SPI Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high-level time	8.0	-	-	ns
t(cl)	SPI clock low-level time	8.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8 V SPIs. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface.

4.10. RGMII Interface

The module includes an integrated Ethernet MAC with a RGMII interface which also supports EAVB. Key features of the RGMII interface are shown below:

- IEEE 802.3 compliant
- Supports 10/100/1000 Mbps operation [13]
- Supports protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connecting to an external Ethernet PHY or switch
- Support 1.8 I/O standards

The following table shows the pin definition of RGMII interface.

[13] The module's RGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

Table 25: Pin Description of Ethernet Management and Control Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ETH_MDIO	10	DIO	Ethernet management data	Add a pull-up resistor to this pin, and place the resistor close to the external PHY.
ETH_MDC	11	DO	Ethernet management clock	Do not add any pull-up resistor to this pin, otherwise it may cause higher power consumption during low power mode.
ETH_PWR_EN	27	DO	Enable external power supply to power Ethernet PHY	1.8 V power domain.
ETH_INT	29	DI	Ethernet PHY interrupt	
ETH_RST_N	31	DO	Ethernet PHY reset	

Table 26: Pin Description of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_RXC	19	DI	RGMII receive clock	The single-ended impedance requires 50 Ω.
RGMII_RX_CTL	15	DI	RGMII receive control	
RGMII_RX0	13	DI	RGMII receive data bit 0	
RGMII_RX1	14	DI	RGMII receive data bit 1	
RGMII_RX2	16	DI	RGMII receive data bit 2	
RGMII_RX3	17	DI	RGMII receive data bit 3	
RGMII_TXC	24	DO	RGMII transmit clock	
RGMII_TX_CTL	21	DO	RGMII transmit control	
RGMII_TX0	20	DO	RGMII transmit data bit 0	
RGMII_TX1	22	DO	RGMII transmit data bit 1	
RGMII_TX2	23	DO	RGMII transmit data bit 2	
RGMII_TX3	25	DO	RGMII transmit data bit 3	

The following figure shows the simplified block diagram for Ethernet application.

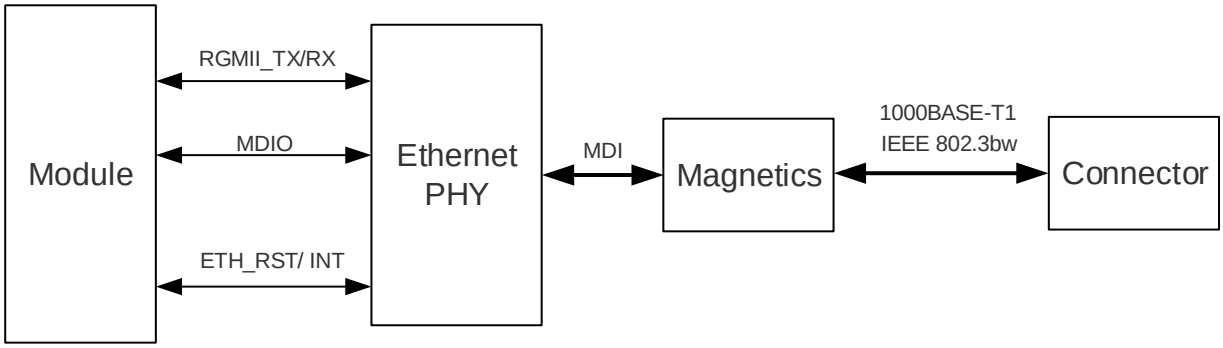


Figure 30: Simplified Block Diagram for Automotive Ethernet Application

The following figure shows a reference design of RGMII interface with PHY application. For more details, see ***document [8]***.

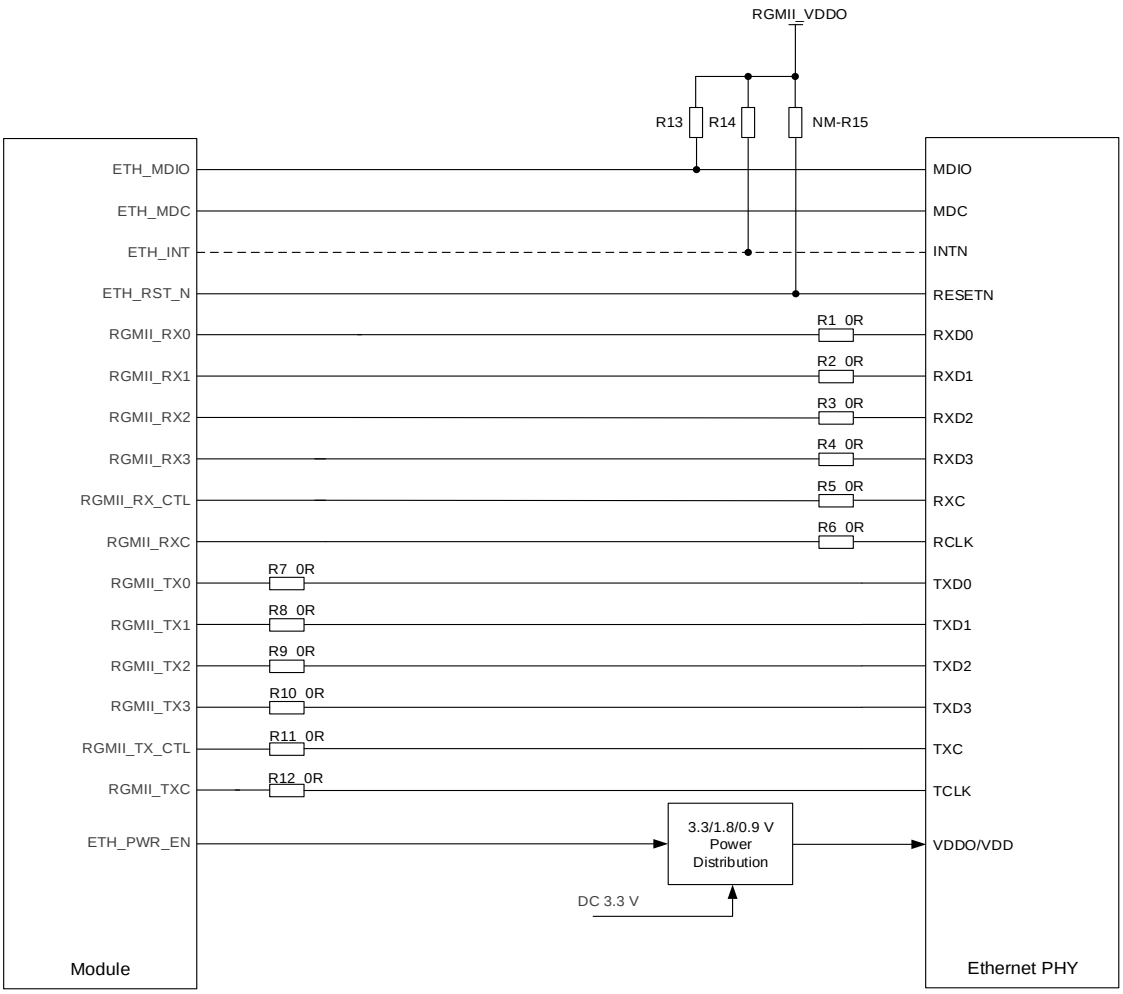


Figure 31: Reference Circuit of RGMII Interface with PHY Application

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- Keep RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- The single-ended impedance of RGMII data traces is 50 Ω ±20 %.
- The length matching between Tx signals (RGMII_TXC, RGMII_TX_CTL and RGMII_TX[0:3]) or Rx signals (RGMII_RXC, RGMII_RX_CTL and RGMII_RX[0:3]) is less than 2 mm.
- Keep the spacing between Tx bus traces (RGMII_TXC to RGMII_TX[0:3]/RGMII_TX_CTL) or that between Rx bus traces (RGMII_RXC to RGMII_RX[0:3]/RGMII_RX_CTL) at least 2 times the trace width.
- Keep the spacing between Tx bus and Rx bus traces at least 2.5 times trace width. Keep the spacing between RGMII and other signal traces at least 3 times trace width. If the PCB space is enough, it is recommended to shield with ground for each signal trace.
- Resistors R7–R12 should be placed near the module. Resistors R1–R6 should be placed near the Ethernet PHY. The value of R1–R15 varies with the selection of PHY.
- ETH_INT and ETH_RST_N are always 1.8 V power domain. A voltage-level translator should be used when the module I/O level does not match with PHY.

NOTE

RGMII and SGMII interfaces cannot be used simultaneously. RGMII is supported by default.

4.11. SGMII Interface

The module includes an integrated Ethernet MAC with a SGMII interface, which supports EAVB. Key features of the SGMII interface are shown below:

- Supports 1000/2500 Mbps operation [14]
- Supports protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connecting to an external Ethernet PHY or switch

For the information about the pin definition of Ethernet management and control interfaces, see ***Table 25***.

[14] The module's SGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

Table 27: Pin Description of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
SGMII_TX_P	94	AO	SGMII transmit (+)	Require differential impedance of 90–110 Ω, and100 Ω is recommended. 100 nF AC coupling capacitor is required.
SGMII_TX_M	96	AO	SGMII transmit (-)	
SGMII_RX_P	97	AI	SGMII receive (+)	
SGMII_RX_M	99	AI	SGMII receive (-)	

The following figure shows the simplified block diagram for Ethernet application.

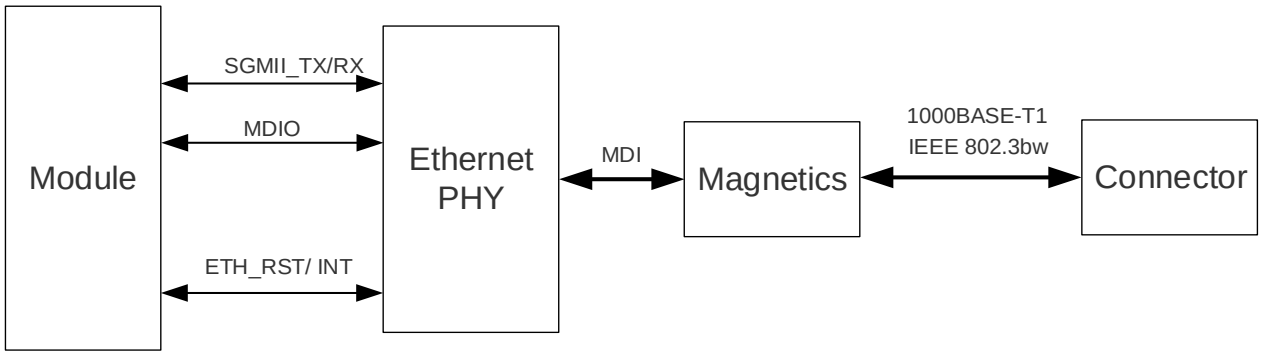


Figure 32: Simplified Block Diagram for Automotive Ethernet Application

The following figure shows a reference design of SGMII interface with PHY application. For more details, see ***document [8].***

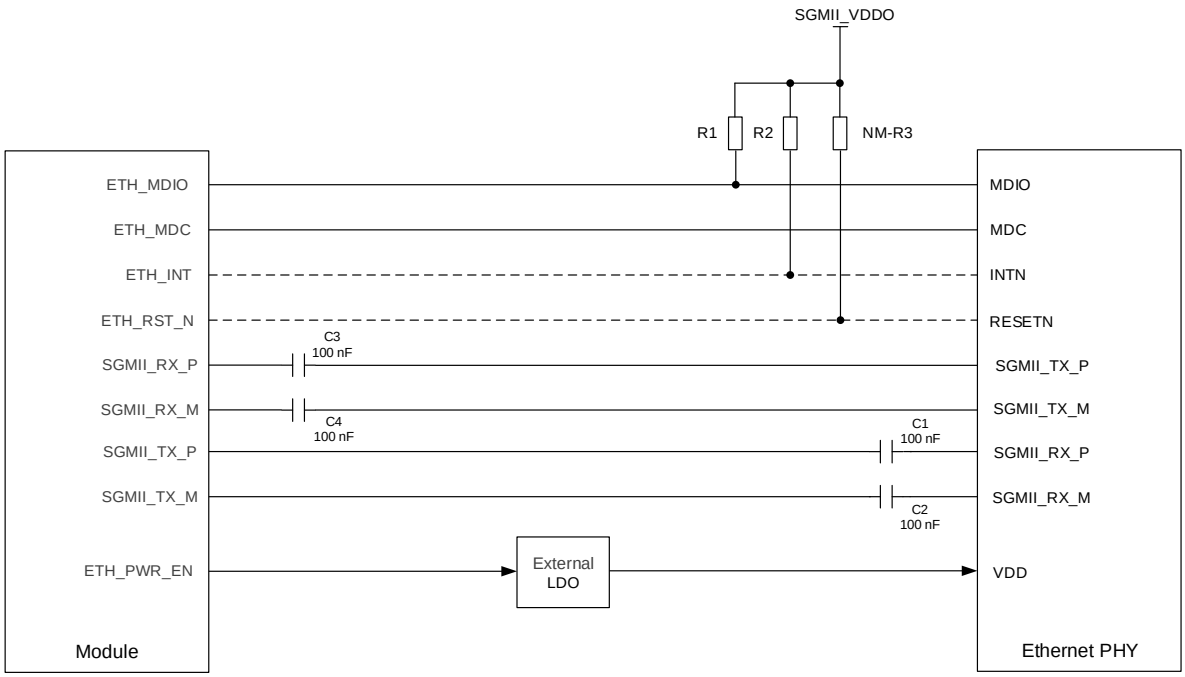


Figure 33: Reference Circuit of SGMII Interface with PHY Application

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- It is important to route the SGMII signal traces as differential pairs with ground surrounded. The differential impedance is 90–110 Ω and 100 Ω is recommended for SGMII Tx/Rx traces.
- SGMII signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from SGMII traces.
- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required.
- The spacing between Tx and Rx pairs, and the spacing between SGMII lanes and all other signals, should exceed 4 times the trace width (4W).
- ETH_INT and ETH_RST_N are always 1.8 V power domain. A voltage-level translator should be used when module I/O level does not match with PHY.

NOTE

RGMII and SGMII interfaces cannot be used simultaneously. RGMII is supported by default.

4.12. GPIO Interfaces

The module provides 15 GPIOs for application designs. More GPIOs are available through pin multiplexing, and see ***document [1]*** for more details.

Table 28: Pin Description of GPIO Interfaces

Pin Name	Pin No.	I/O	Configurable Function	Comment
GPIO1	100	DI	WAKEUP_IN	Used as WAKEUP_IN by default. If the default function is not used, it can be configured to GPIO. Support wake-up interrupt.
		DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO2	101	DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO3	102	DIO	GPIO	General-purpose input/output **Not** support wake-up interrupt.
GPIO4	104	DO	SLEEP_SYS_IND	Used as SLEEP_SYS_IND by default. If the default function is not used, it can be configured to GPIO. Support wake-up interrupt.
		DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO5	116	DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO6	243	DO	STATUS	Used as STATUS by default. If the default function is not used, it can be configured to GPIO. **Not** support wake-up interrupt.
		DIO	GPIO	General-purpose input/output. **Not** support wake-up interrupt.
GPIO7	246	DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO8	249	DIO		
GPIO9	280	DIO		
GPIO10	283	DIO		
GPIO11	284	DIO		

GPIO12	289	DIO
GPIO13	64	DIO
GPIO14	432	DIO
GPIO15	433	DIO

NOTE

1. GPIO1 is used as WAKEUP_IN by default. GPIO4 is used as SLEEP_SYS_IND by default. For more details about WAKEUP_IN and SLEEP_SYS_IND, see ***document [5]***.
2. GPIO6 is used as STATUS by default. This pin is recommended to be used as an output signal.
3. If you intend to use GPIO1, GPIO4 and/or GPIO6 for other purposes, disable the corresponding default function first through software configuration.

4.13. ADC Interfaces

The module provides five analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read with related API. For more details, see ***document [9].***

To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 29: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	247	AI	General-purpose ADC interface	Voltage range: 0–1.875 V
ADC1	245	AI	General-purpose ADC interface	
ADC2	113	AI	General-purpose ADC interface	
ADC3	447	AI	General-purpose ADC interface	
ADC4	448	AI	General-purpose ADC interface	

The following table describes the characteristic of ADC interfaces.

Table 30: Characteristic of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0	-	1.875	V
ADC1 Input Voltage Range	0	-	1.875	V
ADC2 Input Voltage Range	0	-	1.875	V
ADC3 Input Voltage Range	0	-	1.875	V
ADC4 Input Voltage Range	0	-	1.875	V
ADC Resolution	-	15	-	bits
ADC Sample Rate	-	4.8	-	MHz

NOTE

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

4.14. USB_BOOT Interface

The module provides a USB_BOOT pin. Pull up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 31: Pin Description of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	83	DI	Force the module into download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference design of USB_BOOT interface.

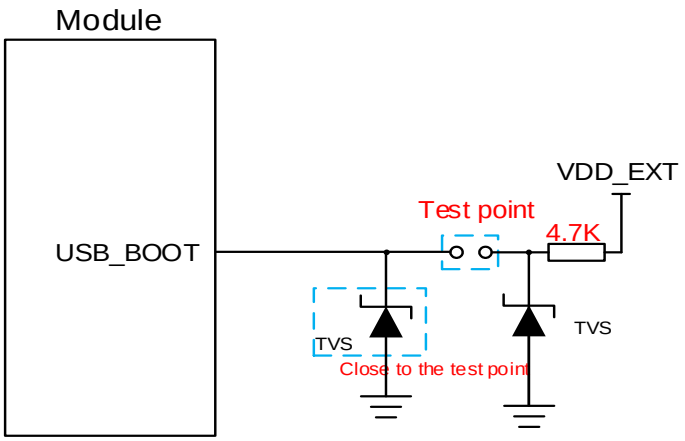


Figure 34: Reference Design of USB_BOOT Interface

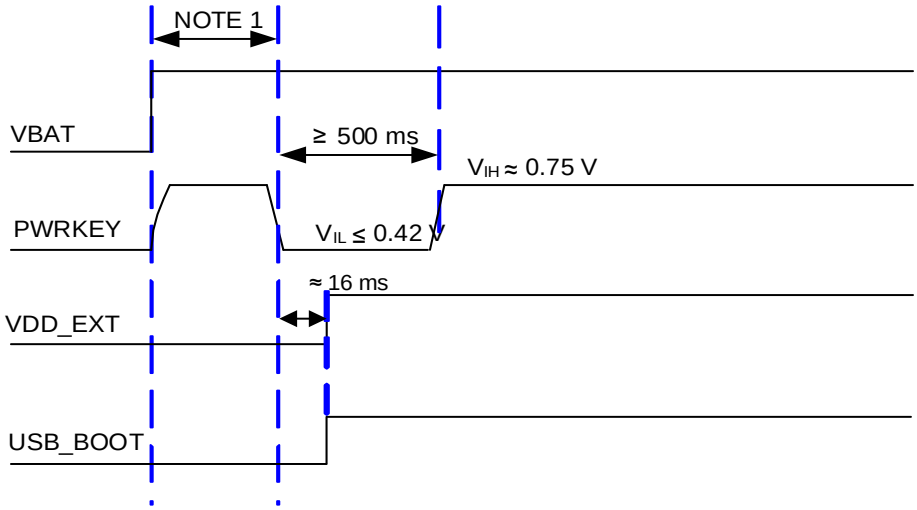


Figure 35: Forced Download Mode Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 50 ms.
2. When using MCU to control the module entering forced download mode, follow the above timing. It is not recommended to pull up USB_BOOT to VDD_EXT before VBAT powers up. Connecting the test points as shown in ***Figure 34*** can manually force the module into download mode.
3. Ensure that the RESET_N cannot be pulled up or down externally when the module enters forced download mode.

4.15. RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not maintain. If RTC is needed, then VBAT_BB must be powered. For more details, see ***document [11].***

4.16. DR_SYNC

The module obtains time through GNSS positioning and outputs 1PPS signal for clock synchronization. The DR_SYNC pin usually connects to an external AP and a MCU to maintain the time consistency between the three.

Table 32: Pin Description of DR_SYNC

Pin Name	Pin No.	I/O	Description
DR_SYNC	95	DO	Dead reckoning sync

A reference design of DR_SYNC interface for clock synchronization application is shown as below:

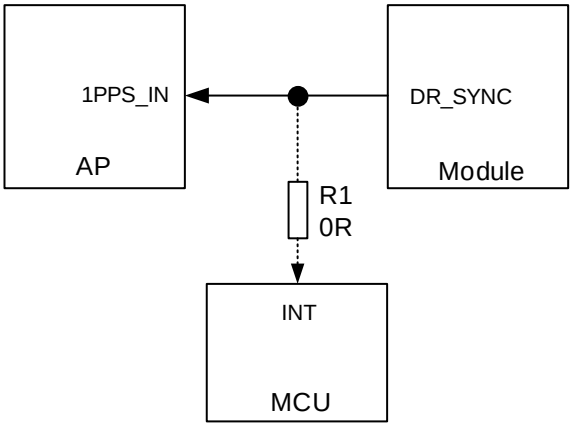


Figure 36: Reference Design of DR_SYNC for Clock Synchronization Application

NOTE

Pay attention to the level matching of the signal shown in dotted line between the module and the MCU.

4.17. IMU Interrupt Interface

The module realizes DR (dead-reckoning) function through an external IMU. For more details about IMU, see ***document [12]***.

Table 33: Pin Description of IMU Interrupt Interface

Pin Name	Pin No.	I/O	Description	Comment
IMU_PWR_EN	181	DO	IMU power enable control	1.8 V power domain. If unused, keep these pins open.
IMU_INT1	169	DI	IMU interrupt 1	
IMU_INT2	187	DI	IMU interrupt 2	

A reference design of IMU interrupt interface is shown as below:

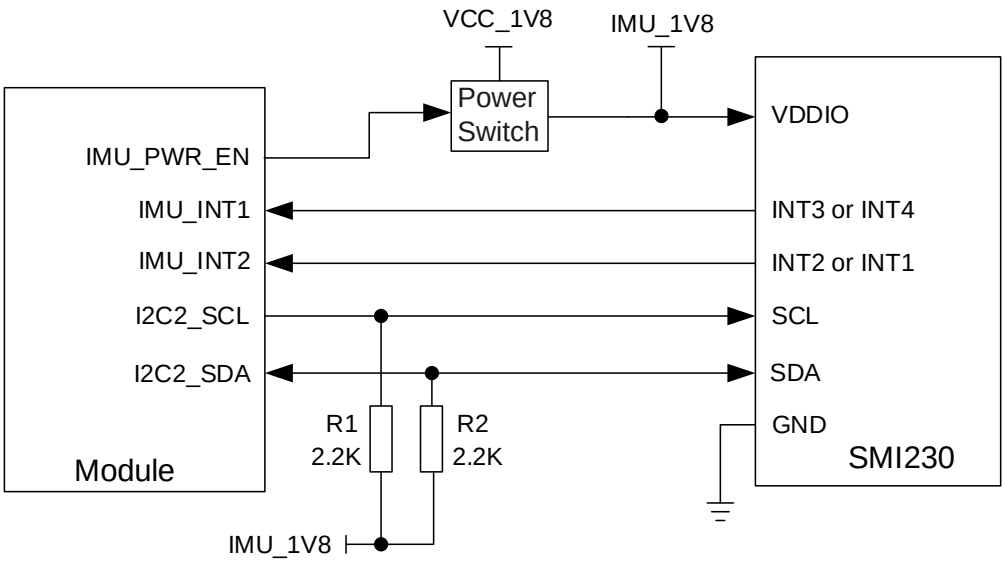


Figure 37: IMU Reference Design Circuit

NOTE

The module also supports TDK IAM-20680 and ST ASM330LHH sensors.

4.18. SEL_BOOT_PARTION*

The module sets the partitions involved in startup into two sets, namely, A system and B system. The two systems burn the same image and back up each other. The A/B system is switched by software by default. The module also supports switching A/B partition address through SEL_BOOT_PARTION in hardware. Partition address switching in hardware is disabled by default, if this function is required, please contact Quectel Technical Support.

See ***document [11]*** for details of A/B partition address.

Table 34: Pin Description of SEL_BOOT_PARTION

Pin Name	Pin No.	I/O	Description	Comment
SEL_BOOT_ PARTION	271	DI	Select to boot from A or B partition address	By default, the module boots from A partition address. When this pin is pulled high, the module will boot from B partition address when it restarts. If unused, keep it open.

A reference design of SEL_BOOT_PARTION interrupt interface is shown as below:

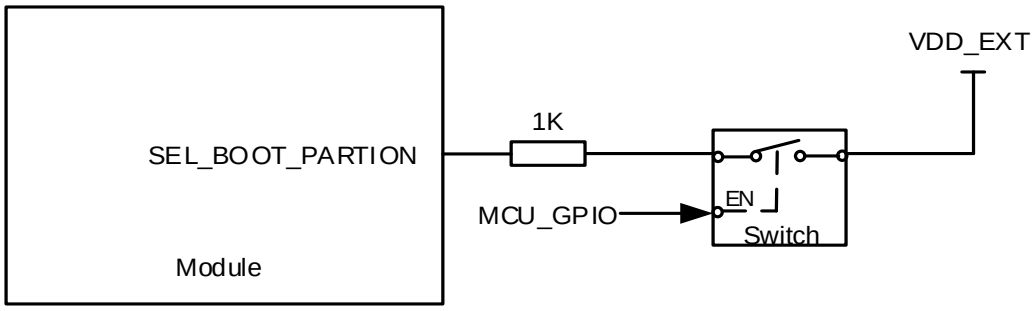


Figure 38: Reference Design of SEL_BOOT_PARTION

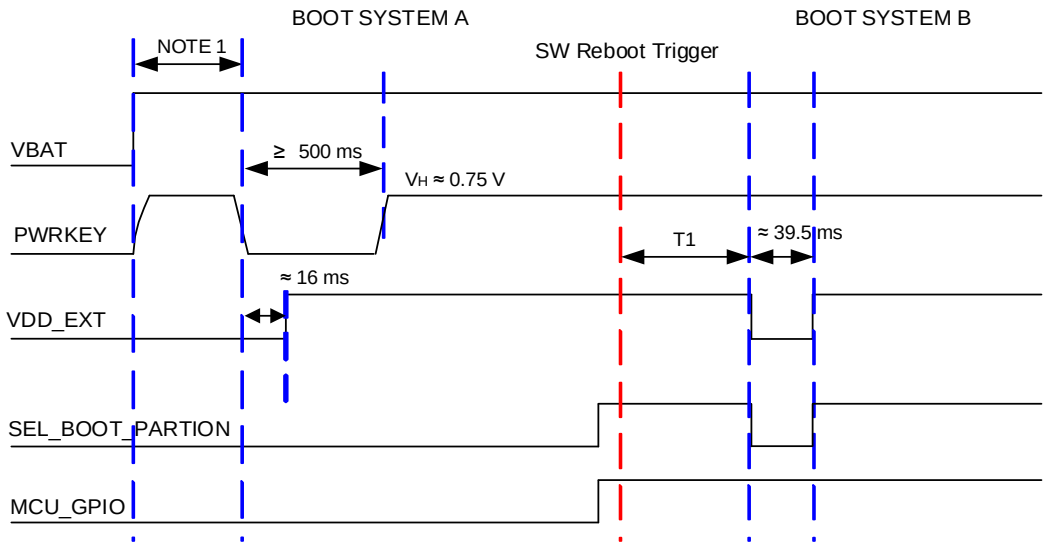


Figure 39: Timing of Switching A/B System

NOTE

1. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down the PWRKEY pin is not less than 50 ms.
2. The shutdown time (T1) of the power supply depend on the actual running business, and if the module has tasks to deal with during shutdown, the time may be longer.
3. It is recommended to restart the module by software mechanisms.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module supports main antenna interface, diversity antenna interface [15], MIMO antenna interface and GNSS antenna interface, and the impedance of antenna ports is 50 Ω.

NOTE

1. The module supports 4 × 4 MIMO antennas configuration (ANT_MAIN & ANT_DIV & ANT_MIMO3 & ANT_MIMO4) by default.
2. GNSS is supported by default.

[15] Diversity antenna interface is used to resist the fall of signals caused by high-speed movement and multipath effect.

5.1. Cellular Antenna Interfaces

5.1.1. Pin Definition[16]

The pin definition of cellular antenna interfaces is shown below.

Table 35: Pin Description of Cellular Antenna Interfaces – AG598E-ROWA

Pin Name	Pin No.	I/O	Description	LB (MHz)	MHB (MHz)	UHB (MHz)
ANT_MAIN	143	AIO	• **GSM DCS/PCS TX/PRX** • **WCDMA/LTE/NR(SA) MHB TX/PRX** • **NR n41 TX/PRX** • **NR n41(NSA) TX @ LB(LTE)+n41 ENDC Combos** **NR MHB(NSA) TX @LB(LTE)+MHB(NR) ENDC Combos**	617–960	1452–2690	3300–5000
			• WCDMA LB DRx • LTE LB DRx • LTE UHB DRX • 5G NR (SA) LB DRx • 5G NR n77/n78/n79 DRX			
ANT_DIV	152	AIO	• **GSM GSM850/GSM900 TX/PRX** • **WCDMA/LTE/NR(SA) LB TX/PRX** • **LTE UHB TX/PRX** • **NR n77/n78/n79(SA) TX/PRX** • **LTE UHB ULCA TX @MHB(LTE)+B42 ULCA** • **LTE UHB ENDC TX @MHB(NR)+B42 ENDC Combos** • **NR LB(NSA) TX @MHB(LTE)+LB(NR) ENDC Combos** **NR n77/n78/n79(NSA) TX @MHB(LTE)+n77/n78/n79 ENDC Combos**	617–960	1452–2690	3300–5000
			• WCDMA MHB DRx • LTE MHB DRx • 5G NR (SA) MHB DRx 5G NR n41 (SA) DRx			
ANT_MIMO3	161	AIO	• **LTE UHB ULCA @LB(LTE)+UHB(LTE) ULCA** • **LTE UHB ENDC TX @LB(NR)+B42 ENDC Combos** • **NR n77/n78(NSA) TX @ LB(LTE)+n77/n78 ENDC Combos**	/	1805-2690	3300–5000
			• LTE/NR(SA) MHB PRX-MIMO • LTE UHB PRX-MIMO • NR n41 PRX-MIMO • NR n77/n78/n79(SA) PRX-MIMO			
ANT_MIMO4	170	AIO	• LTE/NR(SA) MHB DRX-MIMO • LTE UHB DRX-MIMO • NR n41 DRX-MIMO • NR n77/n78/n79 DRX-MIMO	/	1805-2690	3300–5000

NOTE

1. The frequency bands in bold in the table above support both transmission and reception.
2. The module supports the four cellular antennas (ANT_MAIN, ANT_DIV, ANT_MIMO3, ANT_MIMO4) by default. The lack of any one antenna may cause the loss of performance and function.
3. Before designing and evaluating, see ***document [12]*** for more information on CA & EN-DC features.

[16] Frequency range of LB, MB, HB and UHB:
LB: < 1 GHz;
MB: 1–2.3 GHz;
HB: 2.3–2.7 GHz;
UHB: 3.3–6.0 GHz.

5.1.2. Operating Frequencies

Table 36: AG598E-ROWA- Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
DCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
WCDMA B19	830-845	875-890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B18	815-830	860-875	MHz
LTE-FDD B19	830-845	875-890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz

LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B32 [17]	-	1452–1496	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880-1920	1880-1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
LTE-TDD B42	3400-3600	3400-3600	MHz
LTE-FDD B66	1710–1780	2110–2200	MHz
LTE-FDD B71	663–698	617–652	MHz
5G NR FDD n1	1920–1980	2110–2170	MHz
5G NR FDD n2	1850-1910	1930-1990	MHz
5G NR FDD n3	1710–1785	1805–1880	MHz
5G NR FDD n5	824–849	869–894	MHz
5G NR FDD n7	2500–2570	2620–2690	MHz
5G NR FDD n8	880–915	925–960	MHz
5G NR FDD n12	699–716	729–746	MHz
5G NR FDD n18	815-830	860-875	MHz
5G NR FDD n20	832–862	791–821	MHz
5G NR FDD n25	1850–1915	1930–1995	MHz
5G NR FDD n26	814–849	859–894	MHz
5G NR FDD n28	703–748	758–803	MHz
5G NR TDD n38	2570–2620	2570–2620	MHz

[17] B32 supports Rx only.

5G NR TDD n40	2300–2400	2300–2400	MHz
5G NR TDD n41	2496–2690	2496–2690	MHz
5G NR FDD n66	1710–1780	2110–2200	MHz
5G NR FDD n71	663–698	617–652	MHz
5G NR TDD n77	3300–4200	3300–4200	MHz
5G NR TDD n78	3300–3800	3300–3800	MHz
5G NR TDD n79	4400–5000	4400–5000	MHz

5.1.3. Transmitting Power

The following table shows the transmitting power of the module.

Table 37: Transmitting Power (25 °C, 3.8 V Power Supply)

Type	Frequency Band	Max. Transmitting Power	Min. Transmitting Power
GSM	GSM850	33 dBm ±2 dB (Class 4)	5 dBm ±5 dB
	EGSM900	33 dBm ±2 dB (Class 4)	5 dBm ±5 dB
	DCS1800	30 dBm ±2 dB (Class 1)	0 dBm ±5 dB
	PCS1900	30 dBm ±2 dB (Class 1)	0 dBm ±5 dB
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	LTE TDD HPUE bands (B40/B41)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR FDD bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	5G NR TDD n38/n40	23 dBm ±2 dB (Class 3)	< -40 dBm
	5G NR TDD HPUE bands (n41/n79)	26 dBm ±2 dB (Class 2)	< -40 dBm
	5G NR TDD HPUE bands (n77/n78)	26 dBm +1/-2 dB (Class 2)	< -40 dBm

NOTE

1. For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.
2. For EDGE transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to 3GPP TS 51.010-1 ***subclause 13.17***.
3. WCDMA maximum transmitting power meets *3GPP TS 34.121-1* requirements.
4. LTE maximum transmitting power meets *3GPP TS 36.521-1* requirements and it is tested @ BW = 10 MHz,1 RB.
5. 5G NR maximum transmitting power meets *3GPP TS 38.521-1* requirements.

5.1.4. Receiver Sensitivity

Table 38: AG598E-ROWA RF Receiver Sensitivity (3.8 V, Room Temperature)

Frequency Band	SIMO [18] (dBm)			3GPP SIMO (dBm)
	Min. (Best Case)	Typ.	Max. (Worst Case)	
GSM850	TBD	TBD	TBD	-102
EGSM900	TBD	TBD	TBD	-102
DCS1800	TBD	TBD	TBD	-102
PCS1900	TBD	TBD	TBD	-102
WCDMA B1	TBD	TBD	TBD	-106.7
WCDMA B2	TBD	TBD	TBD	-104.7
WCDMA B4	TBD	TBD	TBD	-106.7
WCDMA B5	TBD	TBD	TBD	-104.7
WCDMA B8	TBD	TBD	TBD	-103.7
WCDMA B19	TBD	TBD	TBD	-106.7
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3

[18] Test conditions for the receiver sensitivity of AG598E-ROWA:
- GSM bands: tested with 1 antenna (1Rx);
- WCDMA bands: tested with 2 antennas (2Rx);
- LTE B1/3/4/7/38/40/41/42/66 bands: tested with 4 antennas (4Rx);
- NR N1/3/7/38/40/41/66/77/78/79 bands: tested with 4 antennas (4Rx);

LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B25 (10 MHz)	TBD	TBD	TBD	-92.8
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-FDD B32 (10 MHz) [19]	TBD	TBD	TBD	-96.3
LTE-TDD B34 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B39 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-TDD B42 (10 MHz)	TBD	TBD	TBD	-97.7
LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	-95.8
LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	-93.5
5G NR FDD n1 (20 MHz)	TBD	TBD	TBD	-93.8
5G NR FDD n2 (20 MHz)	TBD	TBD	TBD	-91.8
5G NR FDD n3 (20 MHz)	TBD	TBD	TBD	-90.8
5G NR FDD n5 (20 MHz)	TBD	TBD	TBD	-90.8

[19] LTE-FDD B32 supports Rx only, so the sensitivity of the bands is tested with CA combination, in which B32 are tested with 2 antennas (2Rx).

5G NR FDD n7 (20 MHz)	TBD	TBD	TBD	-91.8
5G NR FDD n8 (20 MHz)	TBD	TBD	TBD	-90.0
5G NR FDD n12 (15 MHz)	TBD	TBD	TBD	-84.0
5G NR FDD n18 (15 MHz)	TBD	TBD	TBD	-94.3
5G NR FDD n20 (10 MHz)	TBD	TBD	TBD	-93.8
5G NR FDD n25 (20 MHz)	TBD	TBD	TBD	-90.3
5G NR FDD n26 (20 MHz)	TBD	TBD	TBD	-87.6
5G NR FDD n28 (20 MHz)	TBD	TBD	TBD	-90.8
5G NR TDD n38 (20 MHz)	TBD	TBD	TBD	-93.8
5G NR TDD n40 (20 MHz)	TBD	TBD	TBD	-93.8
5G NR TDD n41 (100 MHz)	TBD	TBD	TBD	-84.7
5G NR FDD n66 (20 MHz)	TBD	TBD	TBD	-93.3
5G NR FDD n71 (20 MHz)	TBD	TBD	TBD	-86.0
5G NR TDD n77 (100 MHz)	TBD	TBD	TBD	-85.1
5G NR TDD n78 (100 MHz)	TBD	TBD	TBD	-85.6
5G NR TDD n79 (100 MHz)	TBD	TBD	TBD	-85.6

NOTE

1. GSM receiver sensitivity values meet *3GPP TS 51.010-1* requirements.
2. WCDMA receiver sensitivity values meet *3GPP TS 34.121-1* requirements.
3. LTE receiver sensitivity values meet *3GPP TS 36.521-1* requirements and it is tested under BW = 10 MHz according to 3GPP RB configuration.
4. 5G NR receiver sensitivity values meet *3GPP TS 38.521-1* requirements, FDD test @ SCS 15 kHz, TDD test @ SCS 30 kHz.

5.1.5. Reference Design

A reference design of main and diversity antenna interfaces is shown as below. Use a dual L-type matching circuit for the antenna interfaces for better RF performance and for the ease of debugging.

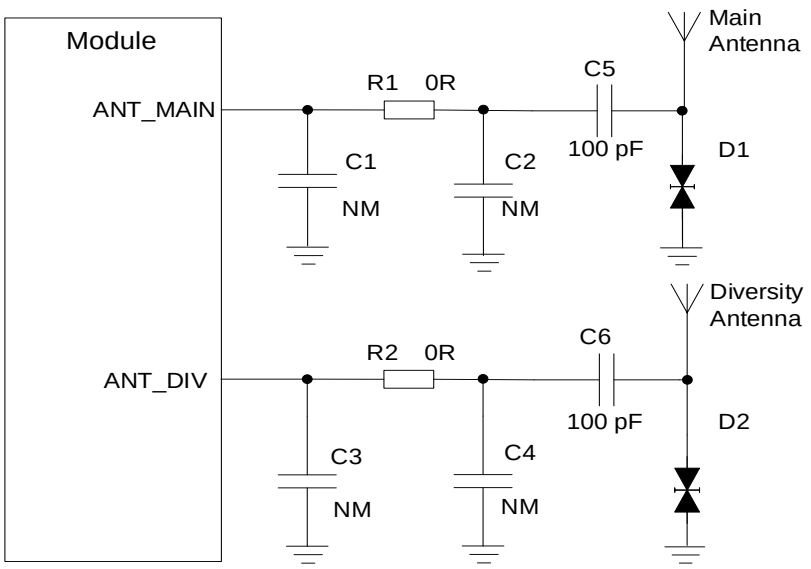


Figure 40: Reference Design of Main and Diversity Antenna Interfaces

NOTE

1. Keep a proper distance between each antenna to improve receiving sensitivity.
2. Place the dual L-type matching components (R1/C1/C2/C5, R2/C3/C4/C6) to antennas as close as possible.
3. Capacitors (C1–C4) are not mounted by default.
4. C5 and C6 are used for DC-blocking and the capacitance value is recommended to be 100 pF.
5. ESD protection components need to be added close to the antenna to effectively prevent static electricity. Junction capacitance of ESD protection components on the antenna interfaces is recommended to be 0.05 pF.

5.2. GNSS Antenna Interface (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, NavIC, Galileo and QZSS positioning system and SBAS augmentation system, and supports L1 + L5 (default) or L1 + L2* (optional) dual-band positioning.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1–10 Hz (1 Hz by default) data update rate via USB interface.

By default, GNSS engine of the module is switched off. It has to be switched on via an API function. For more details about GNSS engine technology and configurations, see ***document [13].***

5.2.1. Pin Definition

The following tables show the pin definition of GNSS antenna interface.

Table 39: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	GNSS L1 (MHz)	GNSS L5 (MHz)	Comment
ANT_GNSS	197	AI	GNSS antenna interface	1559–1606	1166–1187	50 Ω impedance.

5.2.2. Operating Frequency

Table 40: GNSS Operating Frequency

Type	Frequency Band	Unit
GPS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)	MHz
GLONASS	1601.7 ±4.2 (L1)	MHz
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)	MHz
NavIC	1176.45 ±10.23 (L5)	MHz
BDS	1561.098 ±2.046 (B1I) 1575.42 ±2.046 (B1C) 1176.45 ±10.23 (B2a)	MHz
QZSS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)	MHz

5.2.3. GNSS Performance

The module's internal GNSS path does not include an external LNA (eLNA), so an active antenna with an LNA must be used. The GNSS performance of the module is shown in the table below. The sensitivity test environment: an eLNA with approximately 18 dB gain is used outside the test instrument.

Table 41: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	dBm
	Tracking	Autonomous	TBD	dBm
TTFF	Cold start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	s
	Warm start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	s
	Hot start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	s
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (within 5 minutes, the GNSS signal lost lock times ≤ 3, and GNSS signal lost lock time cannot exceed 10 seconds each time).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 5 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.4. Reference Design

A reference design of GNSS antenna is shown as below.

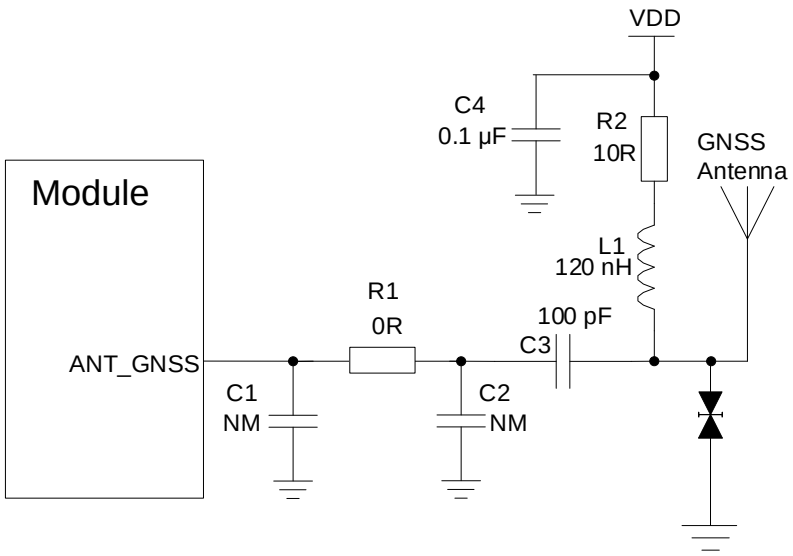


Figure 41: Reference Circuit of GNSS Antenna

NOTE

1. GNSS is an optional function. If unused, keep ANT_GNSS open.
2. An external LDO can be selected to supply power according to the active antenna requirement.
3. A ESD protection component need to be added close to the antenna to effectively prevent static electricity. Junction capacitance of ESD protection component on the antenna interface is recommended to be 0.05 pF.
4. C3 is used for DC-blocking and the capacitance value is recommended to be 100 pF.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

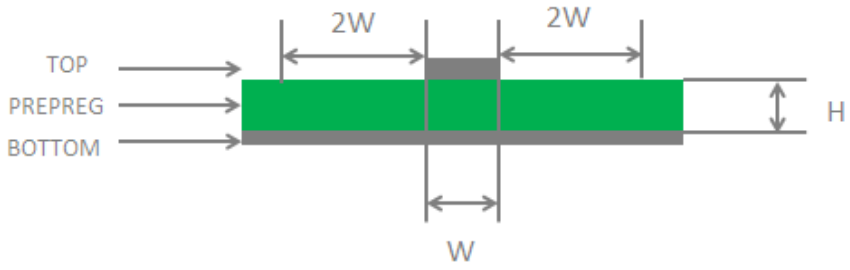


Figure 42: Microstrip Design on a 2-layer PCB

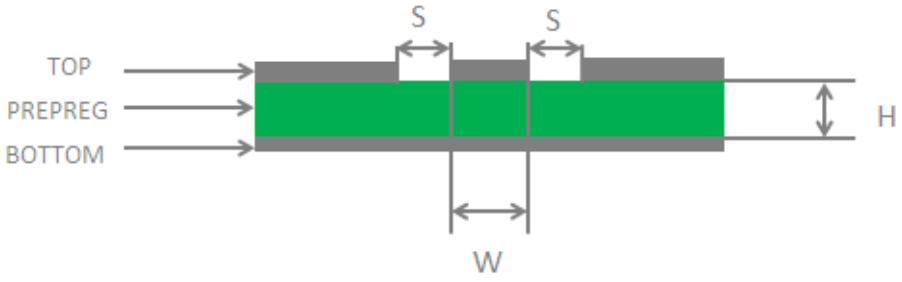


Figure 43: Coplanar Waveguide Design on a 2-layer PCB

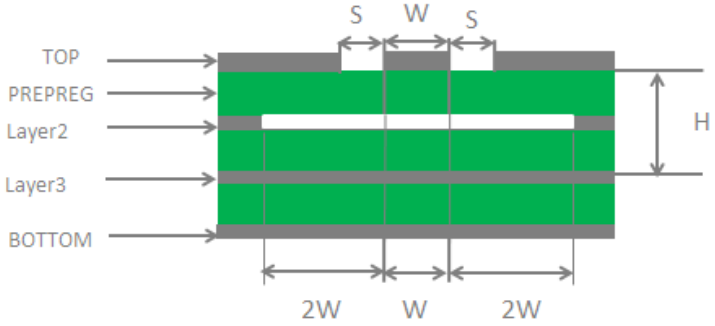


Figure 44: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

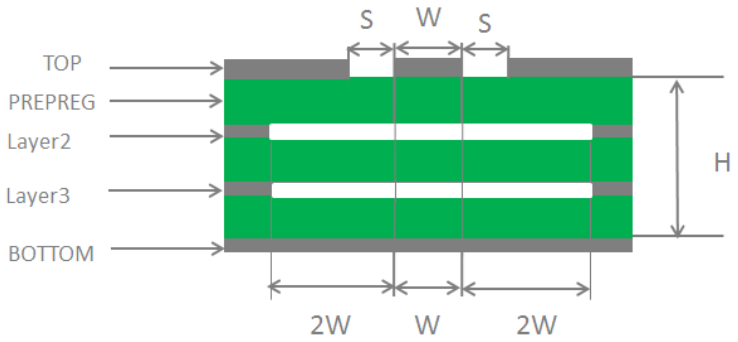


Figure 45: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [13]***.

5.4. Antenna Design Requirements

The following table shows the requirements on RF antenna design.

Table 42: Antenna Design Requirements

Type	Requirements
GNSS	Frequency range: L1: 1559–1606 MHz L5: 1166–1187 MHz Polarization: RHCP VSWR: ≤ 2 (Typ.) Antenna gain: > 0 dBi Active antenna embedded LNA noise figure: < 1.5 dB Active antenna embedded LNA gain: see **NOTE 4** & **NOTE 5** below for design considerations
Cellular	VSWR: ≤ 2 Efficiency: > 30 % Input impedance: 50 Ω Polarization: Vertical Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

NOTE

1. Maximize the distance among main antenna, diversity antenna and GNSS antenna.
2. Antenna isolation:
   > 20 dB @ above 1000 MHz;
   > 15 dB @ 600–1000 MHz;
   > 10 dB @ 400–600 MHz.
3. The isolation between each antenna traces on PCB is recommended to be over 75 dB.
4. GNSS receiver is designed to work with an external LNA (eLNA) in range of 15–20 dB. That is, ensure that the total gain from eLNA to GNSS receiver (including external active antenna, cable loss, connectors, PCB traces, and attenuator) meets 15–20 dB.
5. Attenuator (π-type attenuation circuit) can be used when the total gain exceeds 20 dB.

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by Rosenberger.

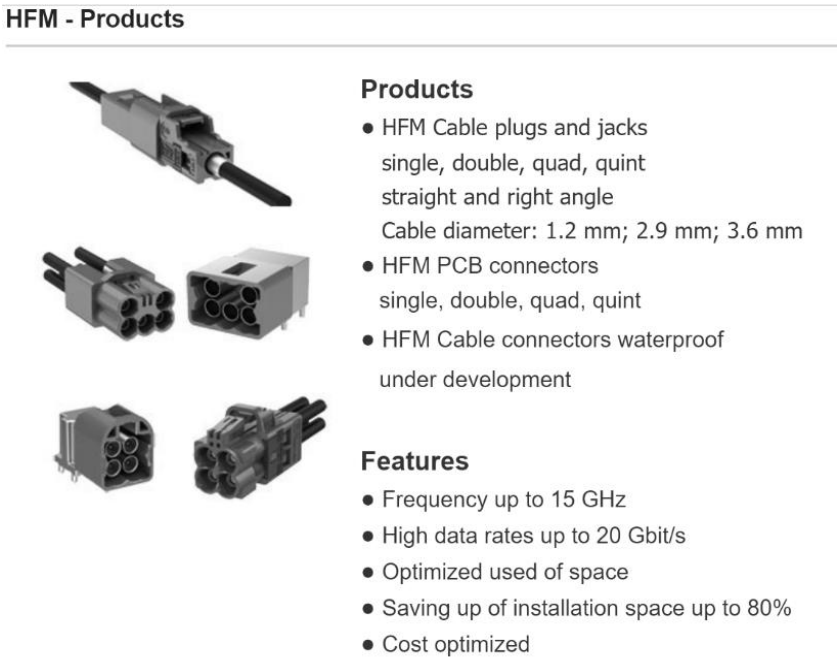


Figure 46: Feature of the HFM Connector

For more details, visit https://www.rosenbergerap.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 43: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.13	V
ADC	0	2.2	V

6.2. Power Supply Ratings

Table 44: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB, VBAT_RF	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst	Maximum	-	-	400	mV

	transmission	transmitted power.				
	Voltage drop during peak data rate	Peak DL data rate on EN-DC	-	-	400	mV
I_{VBAT_BB}, I_{VBAT_RF}	Peak supply current	-	-	-	4.0	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V
VDD_EXT	Provide 1.8 V for external circuits	-	-	1.8	-	V
			-	-	50	mA
VDD_WIFI_VL	Low-voltage power supply for Wi-Fi & Bluetooth module	-	-	0.976	-	V
			-	-	1.7	A
VDD_WIFI_VM	Medium-voltage power supply for Wi-Fi & Bluetooth module	-	-	1.28	-	V
			-	-	0.45	A
VDD_WIFI_VH	High-voltage power supply for Wi-Fi & Bluetooth module	-	-	1.88	-	V
			-	-	0.45	A
USIM_VDD	(U)SIM card power supply	1.8 V application	1.65	1.8	1.95	V
		3.0 V application	2.7	2.95	3.05	V

6.3. Power Consumption

Table 45: AG598E-ROWA Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	TBD	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	TBD	mA
	AT+CFUN=4 (USB disconnected)	TBD	mA
	GSM850 @ DRX = 2	TBD	mA
	GSM850 @ DRX = 5	TBD	mA
	GSM850 @ DRX = 5 (USB Suspend)	TBD	mA

	GSM850 @ DRX = 9	TBD	mA
	EGSM900 @ DRX = 2	TBD	mA
	EGSM900 @ DRX = 5	TBD	mA
	EGSM900 @ DRX = 5 (USB Suspend)	TBD	mA
	EGSM900 @ DRX = 9	TBD	mA
	DCS1800 @ DRX = 2	TBD	mA
	DCS1800 @ DRX = 5	TBD	mA
	DCS1800 @ DRX = 5 (USB Suspend)	TBD	mA
	DCS1800 @ DRX = 9	TBD	mA
	PCS1900 @ DRX = 2	TBD	mA
	PCS1900 @ DRX = 5	TBD	mA
	PCS1900 @ DRX = 5 (USB Suspend)	TBD	mA
	PCS1900 @ DRX = 9	TBD	mA
	WCDMA @ DRX = 0.64 s	TBD	mA
	WCDMA @ DRX = 0.64 s (USB Suspend)	TBD	mA
	WCDMA @ DRX = 1.28 s	TBD	mA
	WCDMA @ DRX = 2.56 s	TBD	mA
	WCDMA @ DRX = 5.12 s	TBD	mA
	LTE-FDD @ DRX = 0.32 s	TBD	mA
	LTE-FDD @ DRX = 0.64 s	TBD	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	TBD	mA
	LTE-FDD @ DRX = 1.28 s	TBD	mA
	LTE-FDD @ DRX = 2.56 s	TBD	mA
	LTE-TDD @ DRX = 0.32 s	TBD	mA
	LTE-TDD @ DRX = 0.64 s	TBD	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	TBD	mA

	LTE-TDD @ DRX = 1.28 s	TBD	mA
	LTE-TDD @ DRX = 2.56 s	TBD	mA
	5G NR FDD @ DRX = 0.32 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s (USB Suspend)	TBD	mA
	5G NR FDD @ DRX = 1.28 s	TBD	mA
	5G NR FDD @ DRX = 2.56 s	TBD	mA
	5G NR TDD @ DRX = 0.32 s	TBD	mA
	5G NR TDD @ DRX = 0.64 s	TBD	mA
	5G NR TDD @ DRX = 0.64 s (USB Suspend)	TBD	mA
	5G NR TDD @ DRX = 1.28 s	TBD	mA
	5G NR TDD @ DRX = 2.56 s	TBD	mA
Idle state	EGSM900 CH62 @ DRX = 5	TBD	mA
	EGSM900 CH62 @ DRX = 5 (USB Active)	TBD	mA
	WCDMA @ DRX = 0.64 s	TBD	mA
	WCDMA @ DRX = 0.64 s (USB Active)	TBD	mA
	LTE-FDD @ DRX = 0.64 s	TBD	mA
	LTE-FDD @ DRX = 0.64 s (USB Active)	TBD	mA
	LTE-TDD @ DRX = 0.64 s	TBD	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	TBD	mA
	5G NR FDD @ DRX = 0.64 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	TBD	mA
	5G NR TDD @ DRX = 0.64 s	TBD	mA
	5G NR TDD @ DRX = 0.64 s (USB Active)	TBD	mA
GSM max. power	EGSM850 CH189 PCL = 5	TBD	mA
	EGSM900 CH62 PCL = 5	TBD	mA

	DCS1800 CH698 PCL = 0	TBD	mA
	PCS1900 CH661 PCL = 0	TBD	mA
GPRS max. throughput	EGSM850 CH189 4DL/1UL	TBD	mA
	EGSM900 CH62 4DL/1UL	TBD	mA
	DCS1800 CH698 4DL/1UL	TBD	mA
	PCS1900 CH661 4DL/1UL	TBD	mA
EDGE max. throughput	EGSM850 CH189 4DL/1UL	TBD	mA
	EGSM900 CH62 4DL/1UL	TBD	mA
	DCS1800 CH698 4DL/1UL	TBD	mA
	PCS1900 CH661 4DL/1UL	TBD	mA
WCDMA max. power	WCDMA B1 CH10700	TBD	mA
	WCDMA B2 CH9800	TBD	mA
	WCDMA B4 CH1638	TBD	mA
	WCDMA B5 CH4408	TBD	mA
	WCDMA B8 CH3012	TBD	mA
	WCDMA B19 CH738	TBD	mA
WCDMA max. throughput	WCDMA B1 HSDPA CH10700	TBD	mA
	WCDMA B1 HSUPA CH10700	TBD	mA
	WCDMA B2 HSDPA CH9800	TBD	mA
	WCDMA B2 HSUPA CH9800	TBD	mA
	WCDMA B4 HSDPA CH1638	TBD	mA
	WCDMA B4 HSUPA CH1638	TBD	mA
	WCDMA B5 HSDPA CH4408	TBD	mA
	WCDMA B5 HSUPA CH4408	TBD	mA
	WCDMA B8 HSDPA CH3012	TBD	mA
	WCDMA B8 HSUPA CH3012	TBD	mA

	WCDMA B19 HSDPA CH738	TBD	mA
	WCDMA B19 HSUPA CH738	TBD	mA
LTE max. power	LTE-FDD B1 CH300	TBD	mA
	LTE-FDD B2 CH900	TBD	mA
	LTE-FDD B3 CH1575	TBD	mA
	LTE-FDD B4 CH2175	TBD	mA
	LTE-FDD B5 CH2525	TBD	mA
	LTE-FDD B7 CH3100	TBD	mA
	LTE-FDD B8 CH3625	TBD	mA
	LTE-FDD B12 CH5095	TBD	mA
	LTE-FDD B18 CH5925	TBD	mA
	LTE-FDD B19 CH6075	TBD	mA
	LTE-FDD B20 CH6300	TBD	mA
	LTE-FDD B25 CH8365	TBD	mA
	LTE-FDD B26 CH8865	TBD	mA
	LTE-FDD B28 CH9435	TBD	mA
	LTE-TDD B34 CH36275	TBD	mA
	LTE-TDD B38 CH38000	TBD	mA
	LTE-TDD B39 CH38450	TBD	mA
	LTE-TDD B40 CH39150	TBD	mA
	LTE-TDD B41 CH40620	TBD	mA
	LTE-TDD B42 CH42590	TBD	mA
	LTE-FDD B66 CH66886	TBD	mA
	LTE-FDD B71 CH68761	TBD	mA
LTE max. throughput	LTE-FDD B1 CH300	TBD	mA
	LTE-FDD B2 CH900	TBD	mA

	LTE-FDD B3 CH1575	TBD	mA
	LTE-FDD B4 CH2175	TBD	mA
	LTE-FDD B5 CH2525	TBD	mA
	LTE-FDD B7 CH3100	TBD	mA
	LTE-FDD B8 CH3625	TBD	mA
	LTE-FDD B12 CH5095	TBD	mA
	LTE-FDD B18 CH5925	TBD	mA
	LTE-FDD B19 CH6075	TBD	mA
	LTE-FDD B20 CH6300	TBD	mA
	LTE-FDD B25 CH8365	TBD	mA
	LTE-FDD B26 CH8865	TBD	mA
	LTE-FDD B28 CH9435	TBD	mA
	LTE-TDD B34 CH36275	TBD	mA
	LTE-TDD B38 CH38000	TBD	mA
	LTE-TDD B39 CH38450	TBD	mA
	LTE-TDD B40 CH39150	TBD	mA
	LTE-TDD B41 CH40620	TBD	mA
	LTE-TDD B42 CH42590	TBD	mA
	LTE-FDD B66 CH66886	TBD	mA
	LTE-FDD B71 CH68761	TBD	mA
5G NR SA max. power	n1A CH428000	TBD	mA
	n2A CH392000	TBD	mA
	n3A CH368500	TBD	mA
	n5A CH176300	TBD	mA
	n7A CH531000	TBD	mA
	n8A CH188500	TBD	mA

	n12A CH147500	TBD	mA
	n18A CH173500	TBD	mA
	n20A CH161200	TBD	mA
	n25A CH392500	TBD	mA
	n26A CH175300	TBD	mA
	n28A CH156100	TBD	mA
	n38A CH519000	TBD	mA
	n40A CH470000	TBD	mA
	n41A CH518598	TBD	mA
	n66A CH429000	TBD	mA
	n71A CH126900	TBD	mA
	n77A CH650000	TBD	mA
	n78A CH636666	TBD	mA
	n79A CH713334	TBD	mA
5G NR SA max. throughput	n1A CH428000	TBD	mA
	n2A CH392000	TBD	mA
	n3A CH368500	TBD	mA
	n5A CH176300	TBD	mA
	n7A CH531000	TBD	mA
	n8A CH188500	TBD	mA
	n12A CH147500	TBD	mA
	n18A CH173500	TBD	mA
	n20A CH161200	TBD	mA
	n25A CH392500	TBD	mA
	n26A CH175300	TBD	mA
	n28A CH156100	TBD	mA

	n38A CH519000	TBD	mA
	n40A CH470000	TBD	mA
	n41A CH518598	TBD	mA
	n66A CH429000	TBD	mA
	n71A CH126900	TBD	mA
	n77A CH650000	TBD	mA
	n78A CH636666	TBD	mA
	n79A CH713334	TBD	mA
5G NR NSA max. power	1A_n77A CH650000	TBD	mA
	2A_n77A CH650000	TBD	mA
	3A_n77A CH650000	TBD	mA
	5A_n77A CH650000	TBD	mA
	7A_n77A CH650000	TBD	mA
	8A_n77A CH650000	TBD	mA
	1A_n78A CH636666	TBD	mA
	2A_n78A CH636666	TBD	mA
	3A_n78A CH636666	TBD	mA
	5A_n78A CH636666	TBD	mA
	7A_n78A CH636666	TBD	mA
	8A_n78A CH636666	TBD	mA
	38A_n78A CH636666	TBD	mA
	40A_n78A CH636666	TBD	mA
	1A_n79A CH713334	TBD	mA
	3A_n79A CH713334	TBD	mA
	7A_n79A CH713334	TBD	mA
	41A_n79A CH713334	TBD	mA

	1A_n77A CH650000	TBD	mA
	2A_n77A CH650000	TBD	mA
	3A_n77A CH650000	TBD	mA
	5A_n77A CH650000	TBD	mA
	7A_n77A CH650000	TBD	mA
	8A_n77A CH650000	TBD	mA
	1A_n78A CH636666	TBD	mA
	2A_n78A CH636666	TBD	mA
5G NR NSA max. throughput	3A_n78A CH636666	TBD	mA
	5A_n78A CH636666	TBD	mA
	7A_n78A CH636666	TBD	mA
	8A_n78A CH636666	TBD	mA
	38A_n78A CH636666	TBD	mA
	1A_n79A CH713334	TBD	mA
	3A_n79A CH713334	TBD	mA
	7A_n79A CH713334	TBD	mA
	41A_n79A CH713334	TBD	mA

NOTE

1. The above power consumption data are all tested with the GNSS OFF by default.
2. The data of maximum throughput are tested at the condition of maximum power.
3. The above power consumption data are the typical values for your reference only. Actual values may vary among different modules due to differences in internal components, software versions and test ambient temperatures. For more details, please contact Quectel Technical Support.

6.4. Digital I/O Characteristics

Table 46: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.26	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.54	V
V_{OH}	High-level output voltage	1.35	1.8	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 47: (U)SIM High-voltage/Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	-	V
V_{OL}	Low-level output voltage	-	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatic discharge characteristics.

Table 48: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±10	kV
Antenna Interfaces	±6	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 49: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [20]	-35	+25	+75	ºC
Extended Temperature Range [21]	-40	-	+85	ºC
eCall Temperature Range [22]	-40	-	+95	°C
Storage Temperature Range	-40	-	+95	ºC

6.7. Thermal Dissipation

The module exhibits the best performance when all internal chips are working within their designated operating temperature ranges. However, if any chip reaches or exceeds its maximum temperature, the module may still work but its performance and functionalities (such as RF output power and data rate) will be compromised. Therefore, the thermal design should be maximally optimized to ensure that all internal chips consistently remain within their recommended operating temperature ranges.

The following principles for thermal consideration are provided for reference:

[20] Within the operating temperature range, the module meets 3GPP specifications.
[21] Within the extended temperature range, the module remains fully functional and the ability to establish and maintain functions such as voice, SMS, data transmission, eCall, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[22] Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of eCall.

- Keep the module away from heat sources on the PCBA main board, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper on the backside of the PCB where the module is mounted.
- Follow the principles below when designing the heatsink:
  1) It is recommended to integrate the heatsink with the outer shell of the device according to the module's application scenario. This allows for rapid transfer of the heat generated by the module to the outer shell, thus enhancing heat dissipation efficiency and eliminating the need for fixing the heatsink.
  2) The entire shell of the device or the shell of the area where the module is located must be made of materials with excellent heat dissipation properties. It is recommended to use die-cast aluminum with higher thermal conductivity.
  3) Based on the heat dissipation direction of the module, you can choose any of the following optional heatsink installation positions:
     a) The top surface of the module shielding cover;
     b) The bottom surface of the PCBA under the module;
     c) Both the top surface of the module shielding cover and the bottom surface of the PCBA under the module.

     If the situation allows, option c) is recommended; if the heatsink is located only on one side, option a) is recommended.
  4) The heatsink must meet the following requirements:
     a) The base plate area of the heatsink should be larger than the module area for full coverage;
     b) Choose a heatsink with adequate fins to ensure effective heat dissipation. The fins should be located within the area where the module is mounted.
  5) Since the heatsink is in contact with either the top surface of the shielding cover or the bottom surface of the PCBA under the module through the thermal interface material (TIM), it is necessary to choose a TIM with high thermal conductivity, good flexibility, and good wettability.
  6) Fasten the shell (heatsink) with screws around the device to prevent the heatsink from falling off during the drop tests, shock and vibration tests, or transportation.
- Implement other auxiliary cooling methods, such as air cooling or liquid cooling.

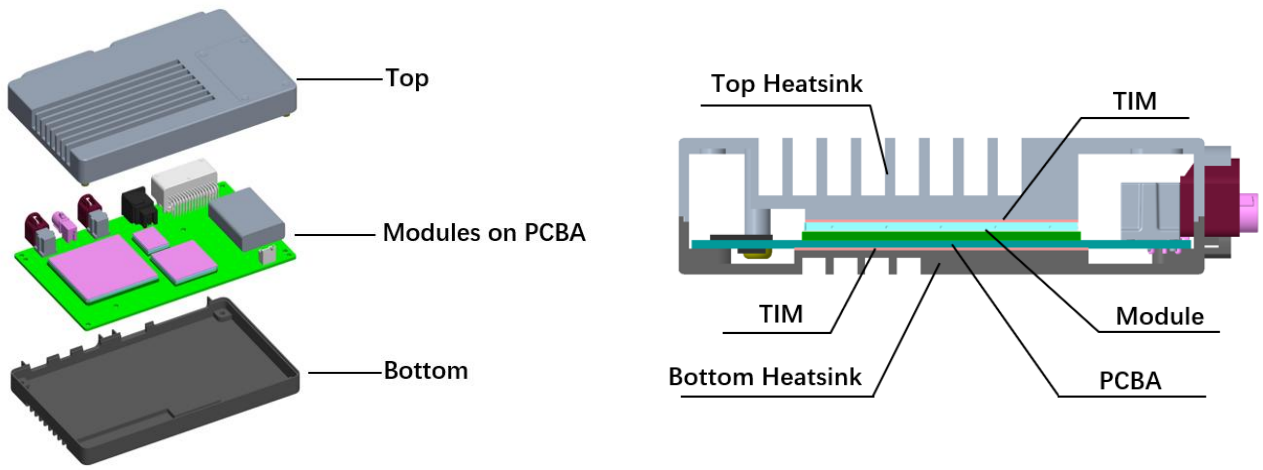


Figure 47: Heatsink Design Example

NOTE

1. When the maximum temperature of the baseband chip reaches or exceeds specified temperature threshold, the module will adopt different thermal management policies by default (such as speed reduction, power reduction and entering Limited Service Mode) to protect the module. When the maximum temperature of the baseband chip exceeds 120 °C, the module will enter Limited Service Mode (such as eCall). Therefore, the thermal dissipation design should be added as much as possible to maximize the module performance. See ***document [15]*** for details about the detailed information on software thermal management.
2. For more detailed introduction on thermal design, see ***document [16]*** and thermal simulation report of the module.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

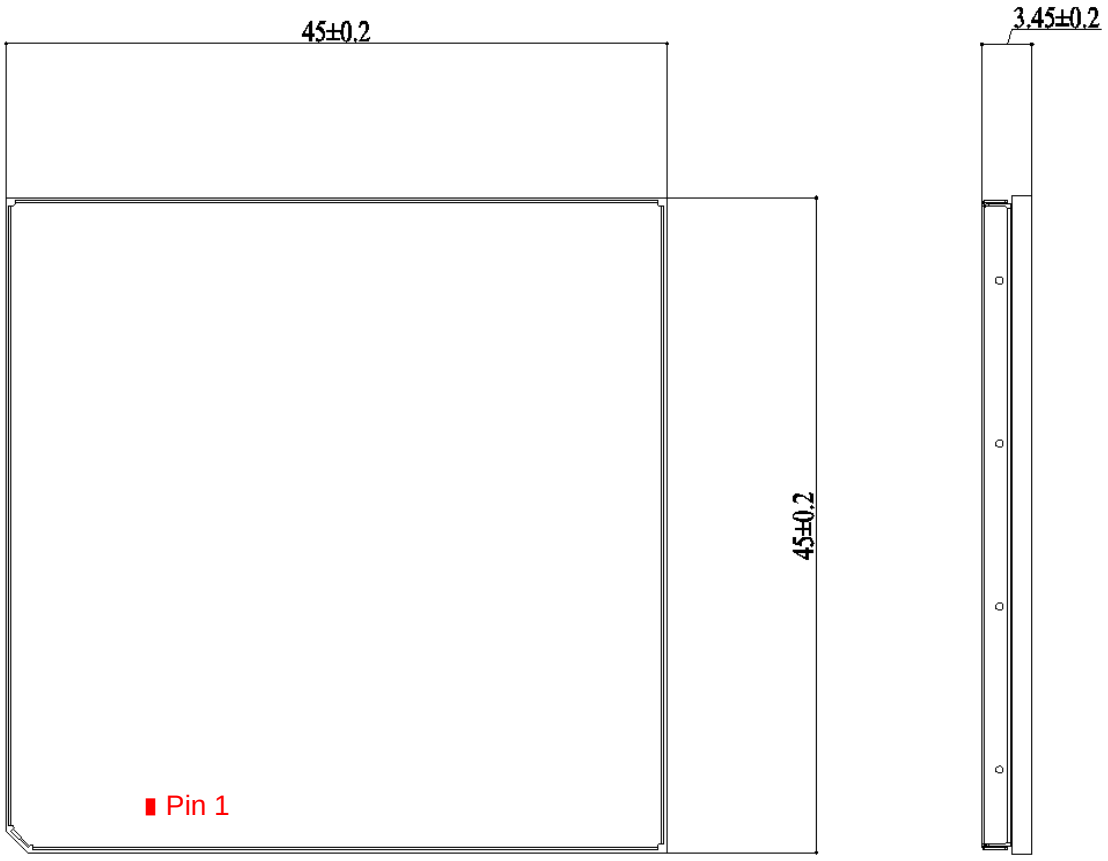


Figure 48: Module Top and Side Dimensions

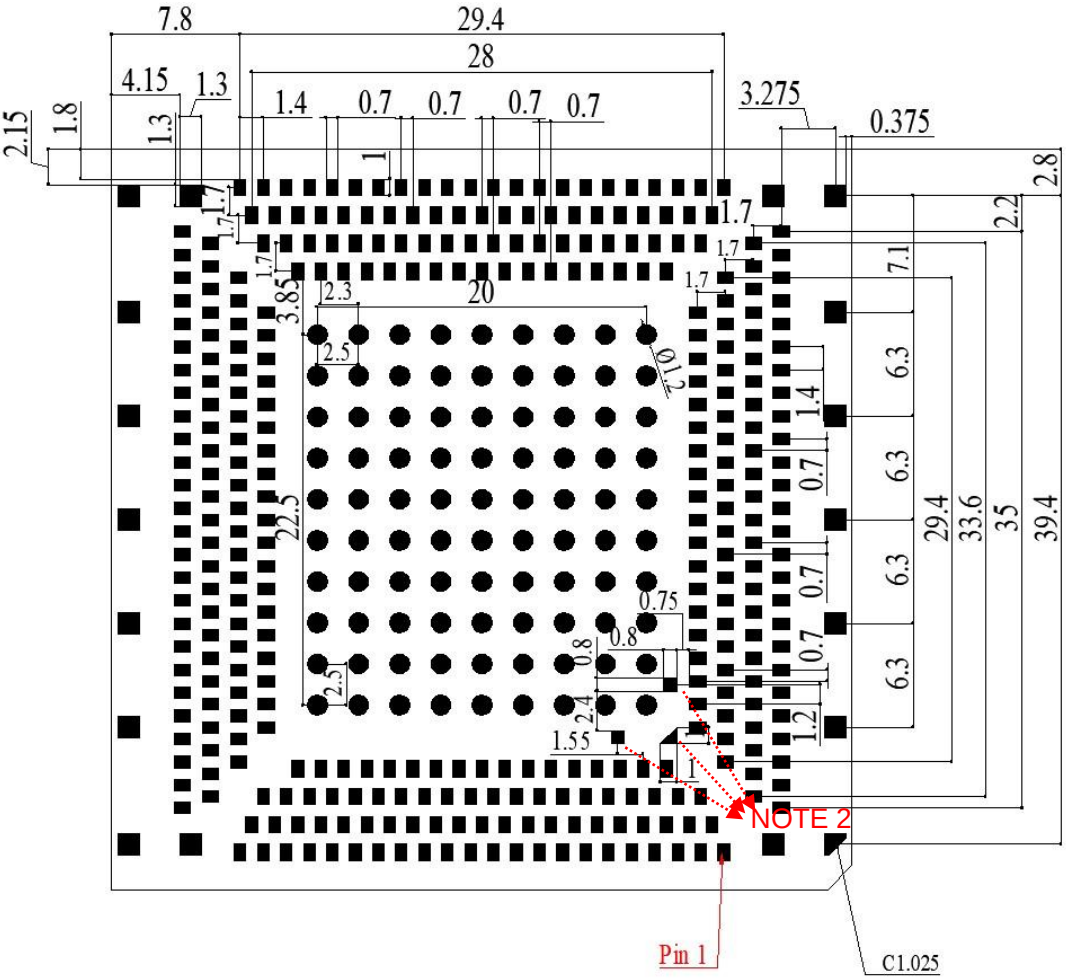


Figure 49: Module Bottom Dimensions (Unit: mm)

NOTE

1. The module's coplanarity standard: ≤ 0.13 mm.
2. Please note that the positions shown by the arrows in the above figure are the mark points of the module, and no additional design is required.

7.2. Recommended Footprint

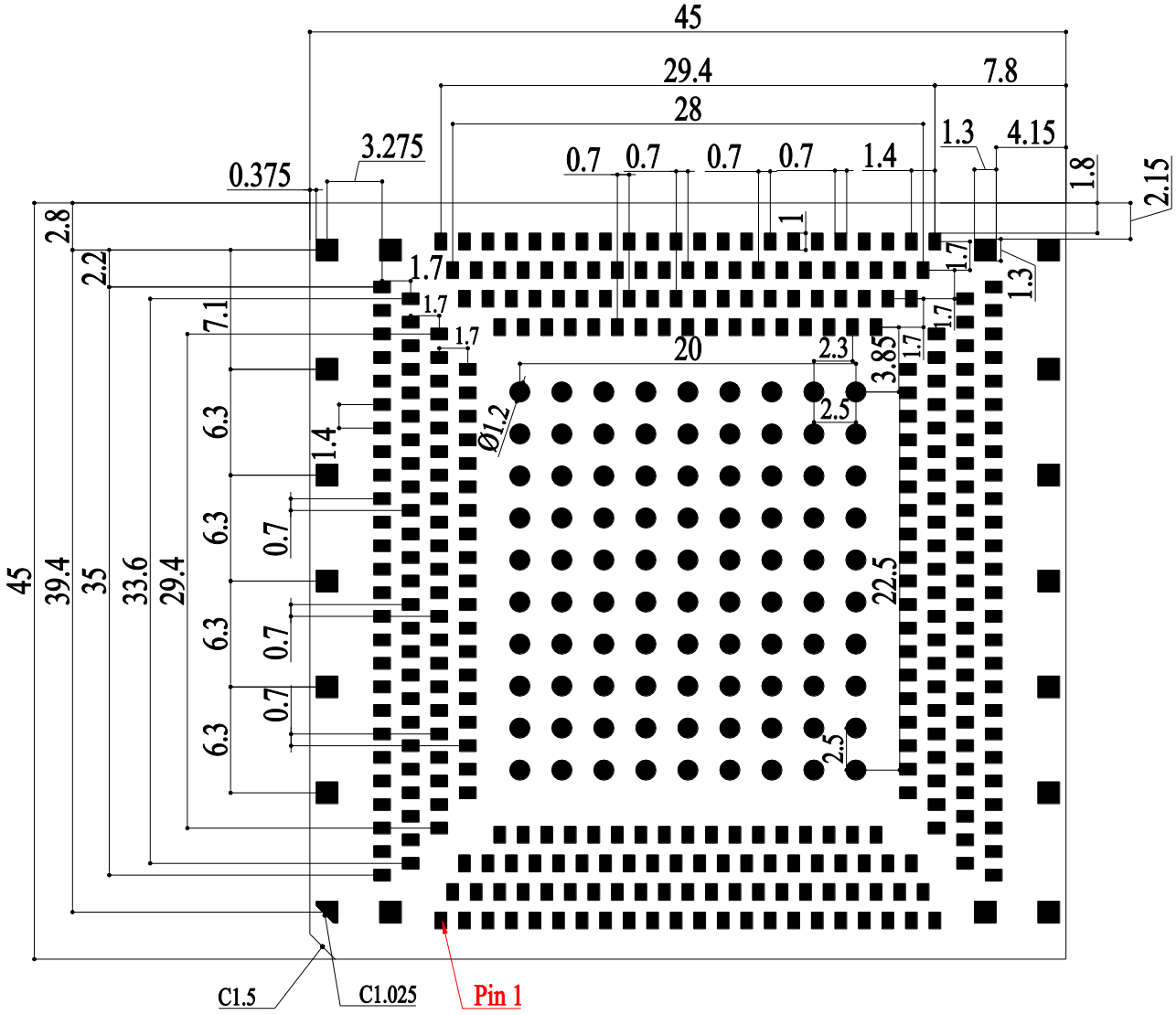


Figure 50: Recommended Footprint (Unit: mm)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.
2. Non-Solder Mask Defined (NSMD) pads preferred.

7.3. Top and Bottom Views

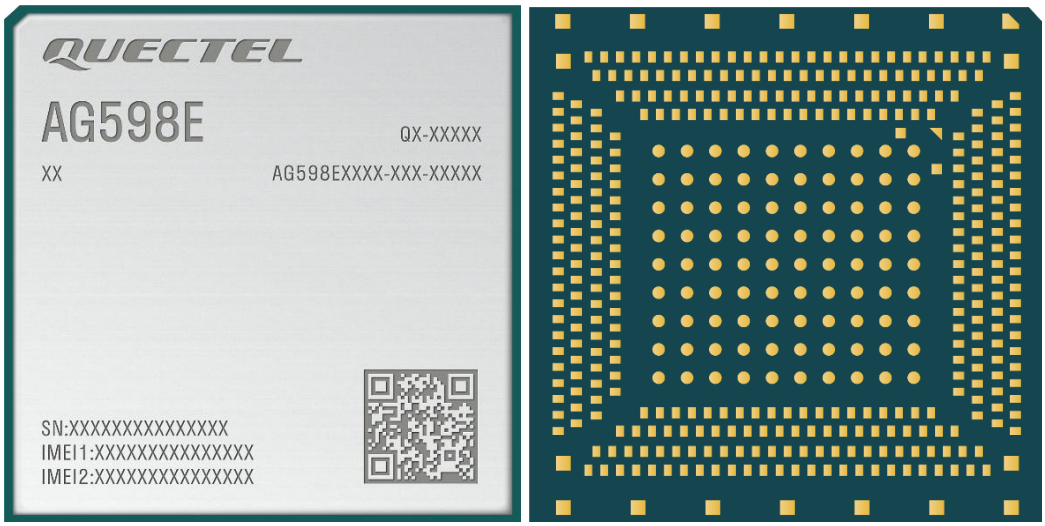


Figure 51: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours[23] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[23] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [17].***

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

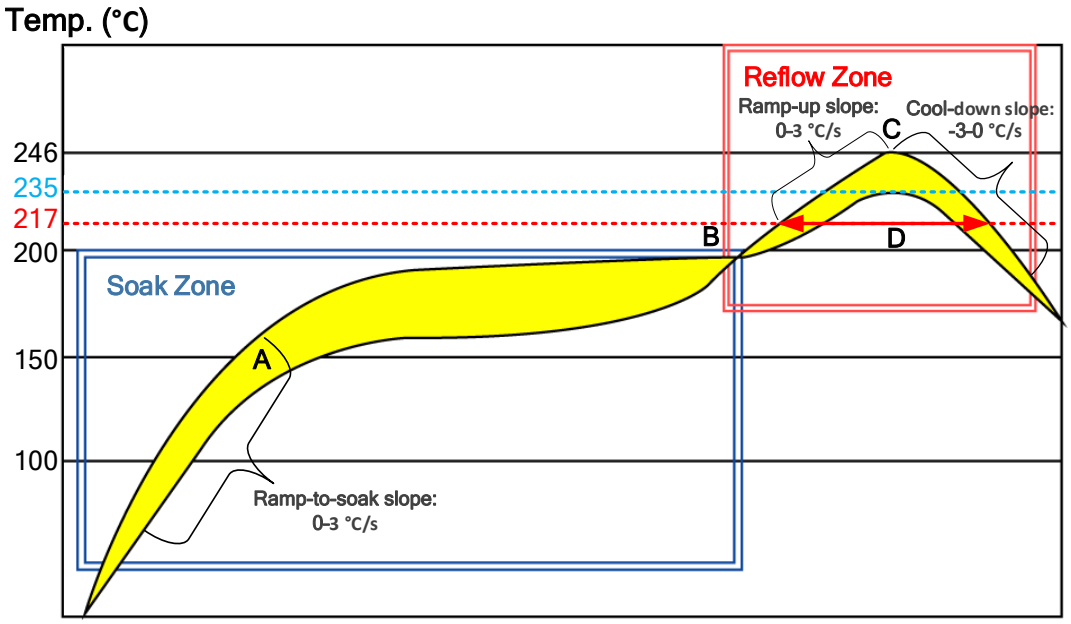


Figure 52: Recommended Reflow Soldering Thermal Profile

Table 50: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s (refer to NOTE 1 below)
Reflow Cycle	
Max reflow cycle	1

NOTE

1. For large-form-factor modules (that is, minimum side length ≥ 30 mm) with two-piece shielding covers, use a cool-down slope of -1~0 °C/s to reduce the thermal stress, preventing cover lifting. Due to the large-size factors of such modules, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Therefore, reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
2. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance

for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [16]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

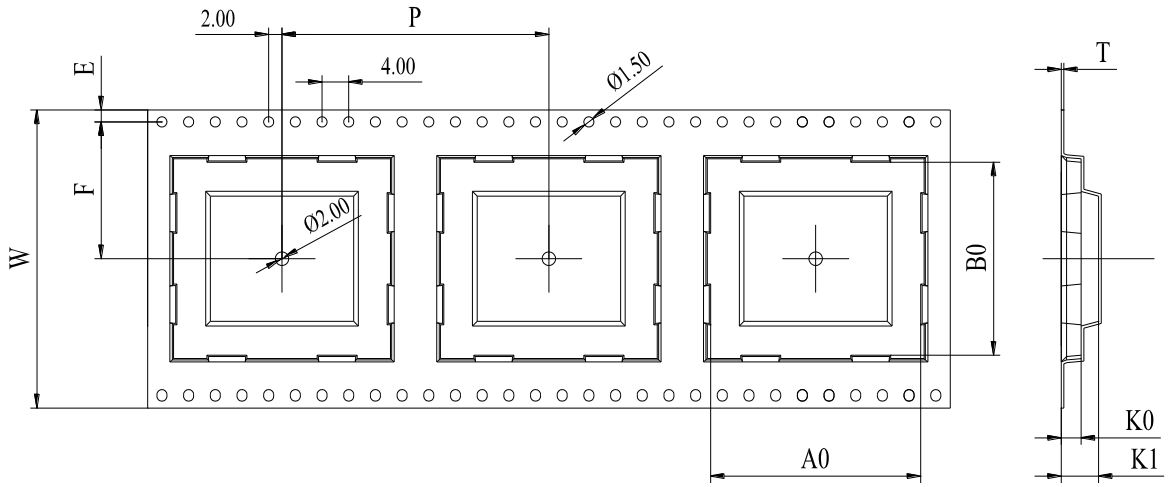


Figure 53: Carrier Tape Dimension Drawing (Unit: mm)

Table 51: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	64	0.4	45.8	45.8	4.7	6	34.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

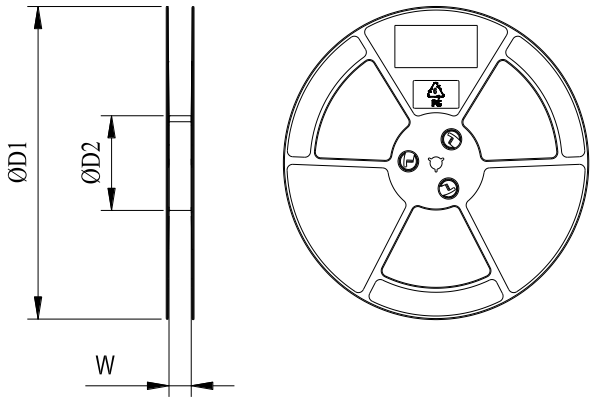


Figure 54: Plastic Reel Dimension Drawing

Table 52: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

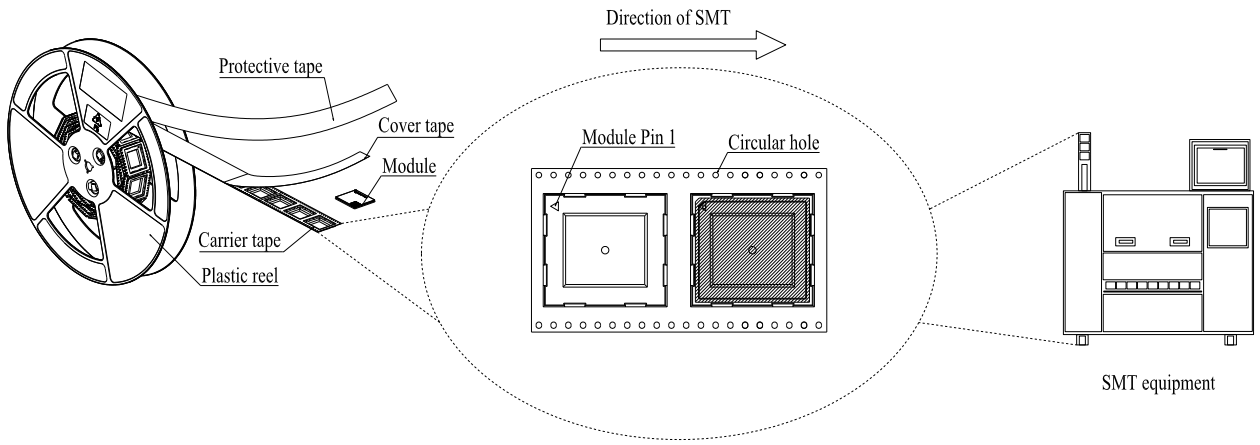
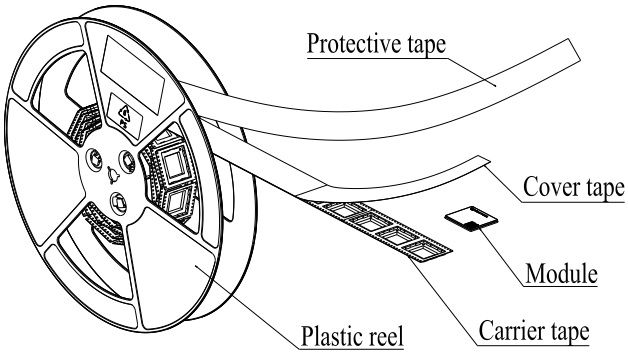


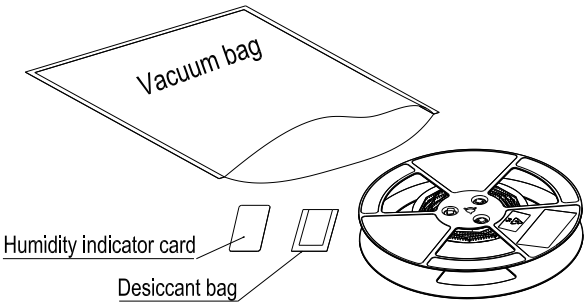
Figure 55: Mounting Direction

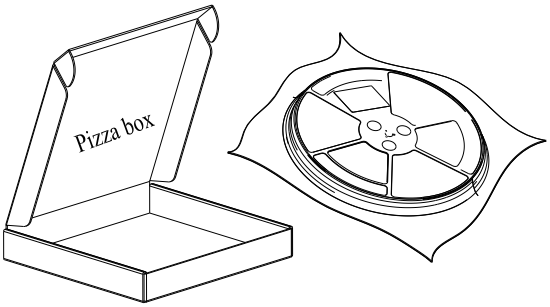
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 150 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 600 modules.

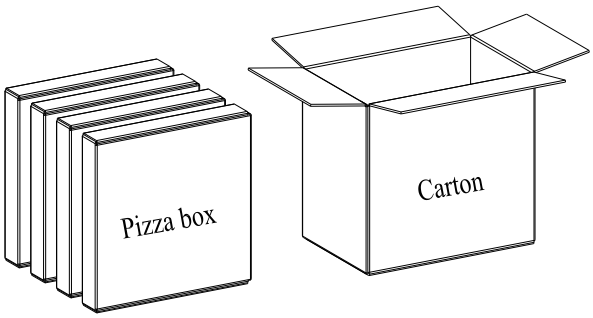


Figure 56: Packaging Process

9 Appendix References

Table 53: Related Documents

Document Name	
[1]	Quectel_AG598E-ROWA_Series_QuecOpen_GPIO_Configuration
[2]	Quectel_V2X&5G_EVB_User_Guide
[3]	Quectel_AG591E&AG598E_Series_QuecOpen(SDK)_Device_Management_Guide
[4]	Quectel_AG59xE_Series_QuecOpen(SDK)_Low_Power_Mode_Development_Guide
[5]	Quectel_AG59xE_Series_QuecOpen(SDK)_UART_Development_Guide
[6]	Quectel_AG59xE_Series_QuecOpen(SDK)_Audio_Development_Guide
[7]	Quectel_AG598E-ROWA_QuecOpen_Reference_Design
[8]	Quectel_AG59xE_Series_QuecOpen(SDK)_ADC_Development_Guide
[9]	Quectel_AG59xE_Series_QuecOpen(SDK)_RTC_Development_Guide
[10]	Quectel_AG59xE_Series_QuecOpen(SDK)_Sensor_Adaptation_Guide
[11]	Quectel_AG59xE_Series_QuecOpen(SDK)_AB_System_Update_Guide
[12]	Quectel_AG598E-ROWA_QuecOpen_CA&EN-DC_Features
[13]	Quectel_AG59xE_Series_QuecOpen(SDK)_GNSS_Development_Guide
[14]	Quectel_RF_Layout_Application_Note
[15]	Quectel_AG59xE_Series_QuecOpen(SDK)_Software_Thermal_Management_Guide
[16]	Quectel_Module_Thermal_Design_Guide
[17]	Quectel_Module_Stencil_Design_Requirements
[18]	Quectel_Module_SMT_Application_Note

Table 54: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
5G NR	5G New Radio
AC	Alternating Current
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
AP	Application Processor
API	Application Program Interface
AVTP	Audio/Video Transport Protocol
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BT	Bluetooth
CS	Coding Scheme
CTS	Clear to Send
DCE	Data Communications Equipment
DC-HSDPA	Dual Carrier High Speed Packet Access Plus
DCS	Data Communications Equipment
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DR	Dead Reckoning
DRX	Discontinuous Reception
DSDA	Dual SIM Dual Active
DSSS	Dual SIM Single Standby
DTE	Data Terminal Equipment

DTR	Data Terminal Ready
EAVB	Ethernet Audio Video Bridging
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Extended GSM900 Band (including standard GSM900 band)
EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
EN-DC	E-UTRA-NR Dual Connectivity
EP	PCIe Endpoint
ESD	Electrostatic Discharge
EVB	Evaluation Board
EOS	Electrical Over Stress
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
FTP	File Transfer Protocol
FQTSS	Forwarding and Queuing of Time Sensitive Streams
Galileo	Galileo Satellite Navigation System
GLONASS	Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications

gPTP	General Precise Time Protocol
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
Imax	Maximum Load Current
IMEI	International Mobile Equipment Identity
IMU	Inertial Measurement Unit
I/O	Input/Output
ITS	Intelligent Transportation System
Inom	Normal Current
LDO	Low-dropout Regulator
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPM	Low Power Mode
LTE	Long Term Evolution
MAC	Medium Access Control
MCS	Modulation and Coding Scheme
MDIO	Management Data Input/Output
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MHB	Middle/High Band

MO	Mobile Originated
MLCC	Multi-layer Ceramic Chip Capacitor
MT	Mobile Terminated
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NSA	Non-Standalone
NTP	Network Time Protocol
PA	Power Amplifier
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RC	PCIe Root Complex
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RSU	Roadside Units
RTC	Real-Time Clock
RTS	Ready To Send/Request to Send
RoHS	Restriction of Hazardous Substances

Rx	Receive
SA	Standalone
SCS	Sub-Carrier Space
SDIO	Secure Digital Input/Output
SIM	Subscriber Identity Module
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
SRP	Stream Reservation Protocol
TCP	Transmission Control Protocol
TCU	Telematics Control Units
TDD	Time Division Duplexing
TLS	Transport Layer Security
Tx	Transmitting Direction
XFEM	Extended Finite Element Method
t(ch)	Clock high
t(cl)	Clock low
t(mov)	Master Output Valid
t(mis)	Master Input Setup
t(mih)	Master Input Hold
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UL	Uplink

UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network

FCC Statement

FCC ID: XMR2025AG598EROWA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NetPrisma that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: XMR2025AG598EROWA”
“Contains IC: 10224A-AG598EROWA“
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Antenna Type	Max Gain	
External Antenna	GSM 850:0.3dBi GSM 1900:1.8dBi WCDMA Band2:1.8dBi WCDMA Band4:1.2dBi WCDMA Band5:0.3dBi LTE Band 2:1.8dBi LTE Band 4:1.2dBi LTE Band 5:0.3dBi LTE Band 7:1.4dBi LTE Band 12: -0.5dBi LTE Band 25:1.8dBi LTE Band 26:0.3dBi LTE Band 38:1.4dBi LTE Band 41:1.4dBi LTE Band 42:3.4dBi LTE Band 66:1.5dBi LTE Band 71: -0.9dBi	5G NR n2:1.8dBi 5G NR n5:0.3dBi 5G NR n7:1.4dBi 5G NR n12: -0.5dBi 5G NR n25:1.8dBi 5G NR n26:0.3dBi 5G NR n38:1.4dBi 5G NR n41:1.4dBi 5G NR n66:1.5dBi 5G NR n71:-0.9dBi 5G NR n77:1.88dBi 5G NR n78:1.88dBi

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part27 and part 90 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC Statement

IC: 10224A-AG598EROWA

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following

two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.
Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-AG598EROWA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-AG598EROWA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.