

EG800Z Series

Hardware Design

LTE Standard Module Series

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Quectel Wireless Solutions Co., Ltd.

Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China

Tel: +86 21 5108 6236

Email: info@quectel.com

Or our local offices. For more information, please visit:

<http://www.quectel.com/support/sales.htm>.

For technical support, or to report documentation errors, please visit:

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

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1 Introduction

This document defines the EG800Z series module and describes its air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD module with compact packaging.

Table 2: Basic Information

EG800Z Series	
Packaging	LGA
Pin counts	109
Dimensions	(17.7 +0.3/-0.15) mm × (15.8 +0.3/-0.15) mm × (2.4 ±0.2) mm
Weight	approx. 1.2 g
Wireless network function	LTE/Wi-Fi Scan
Model	● EG800Z-CN ● EG800Z-EU ● EG800Z-LA

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Mode	EG800Z-CN	EG800Z-EU	EG800Z-LA
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28	B2/B3/B4/B5/B7/B8/B28/B66
LTE-TDD	B34/B38/B39/B40/B41	B38/B40/B41	-
Wi-Fi Scan	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon

NOTE

1. EG800Z-CN B41 only supports 140 MHz (2535~2675 MHz).
2. EG800Z-EU B41 only supports 194 MHz (2496~2690 MHz).
3. The Wi-Fi scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported.

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: module by default
USB Interface	● Compliant with USB 2.0 specifications (only supports slave mode) ● Data rate: up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrading and logs outputting ● USB Serial Driver: Windows 10/11, Linux 2.6–6.7, Android 4.x–14.x
USIM Interfaces	● USIM1 supports 1.8 V and 3.0 V USIM cards ● USIM2 only supports 1.8 V USIM cards ● Support Dual SIM Single Standby ● If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards
UART Interfaces	Main UART: ● Used for AT command communication, firmware upgrade and data transmission ● Baud rate: 115200 bps by default ● RTS and CTS hardware flow control Debug UART: ● Used for logs outputting ● Baud rate: supports 115200 bps and 3 Mbps (3 Mbps by default) Auxiliary UART*: ● Baud rate: 115200 bps by default
PCM Interface*	Used for digital audio function with an external Codec
I2C Interface	● One I2C interface ● Compliant with I2C bus specification

ADC Interfaces	- Two Analog-to-Digital Converter (ADC) interfaces - Input voltage range: 0–1.6 V.
Network Indication	- NET_STATUS: indicate the network activity status - STATUS: indicate the operation status - MAIN_RI: indicate the URC information
AT Commands	- Compliant with 3GPP TS 27.007, 3GPP TS 27.005 - Compliant with Quectel enhanced AT commands
Antenna Interface	- LTE/Wi-Fi Scan antenna interface (ANT_MAIN) 50 Ω impedance
Transmitting Power	LTE: Class 3 (23 dBm $\pm$ 2 dB)
LTE Features	3GPP Rel-14 FDD and TDD - Max. LTE category: Cat 1bis 1.4/3/5/10/15/20 MHz RF bandwidth - UL modulations: QPSK, 16QAM - DL modulations: QPSK, 16QAM and 64QAM - LTE-FDD: Max. 10 Mbps (DL)/ 5 Mbps (UL) - LTE-TDD: Max. 8.96 Mbps (DL)/ 3.1 Mbps (UL)
Internet Protocol Features	- TCP/UDP/NTP/NITZ/FTP/HTTP/PING/HTTPS/FTPS/SSL/MQTT/FILE/UX/PPP protocols CM - PAP and CHAP for PPP connections
Temperature Range	- Normal operating temperature ¹: -35 °C to +75 °C - Extended operating temperature ²: -40 °C to +85 °C - Storage temperature: -40 °C to +90 °C
Firmware Upgrade	- USB 2.0 interface - DFOTA - Main UART
RoHS	All hardware components are fully compliant with EU RoHS directive

¹ Within this range, the module's indicators comply with 3GPP specification requirements.

² Within the range of -40 to -35 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as SMS* and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Pin Assignment

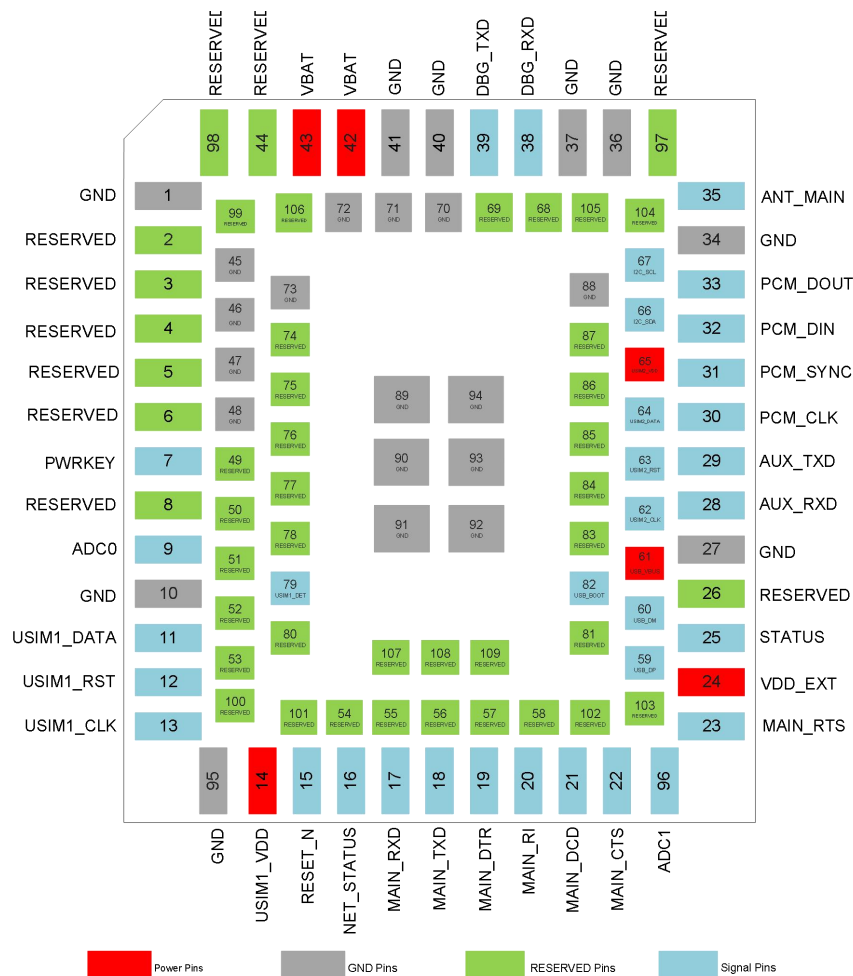


Figure 1: Pin Assignment (Top View)

NOTE

1. If the module does not need to enter forced download mode, USB_BOOT should not be pulled up to VDD_EXT before the module successfully starts up.
2. Please note the following when designing the circuit: In sleep mode, certain module pins will be powered down, including: pins 17³, 18, 22 and 23 of main UART interface, pins 28 and 29 of auxiliary UART interface*, pins 38 and 39 of debug UART interface, USB_BOOT (pin 82), pins 30–33 of PCM interface*, pins 66 and 67 of I2C interface, pins 21 of MAIN_DCD. These pins will lose drive capability, halt status indication or data transmission, and any high-level pins may generate periodic pulses during the paging cycle.
3. Keep all RESERVED pins and unused pins unconnected. Connect all GND pins to the ground.
4. Ensure an uninterrupted reference ground plane below the module, with minimal distance between

For details about the AT command, refer to [document \[1\]](#).

the ground plane and the module layer. Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.

2.4. Pin Definitions

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull Up
PD	Pull Down
NP	No-pull
H	High level
L	Low level

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
VBAT	42, 43	PI	-	Power supply for the module	V _{max} = 4.3 V V _{min} = 3.3 V V _{nom} = 3.8 V	External power supply is recommended to provide with sufficient current of 1.2 A. It is recommended to add an external TVS. A test point is recommended to be reserved.
VDD_EXT	24	PO	-	Provide 1.8 V for external pull-up circuit	V _{max} = 1.89 V V _{nom} = 1.8 V V _{min} = 1.71 V I _o max = 4 mA	A test point must be reserved. It is necessary to add a 1 μ F capacitor and a TVS when designing. It can only be used for external pull-up (pull-up resistance $\geq$ 4.7 k Ω). The output voltage can be configured to 1.8/3.3V by AT+QGP1OV . For more details, see document [2] . The pin maintains voltage output even in sleep/PSM mode.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95					Connect these pins to ground.

Turn-on/off

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
PWRKEY	7	DI	PU	Turn on/off the module	V _{IH} min = 1.7 V V _{IL} max = 1.1 V	After the module is powered up, the voltage is about 1.9 V. Active low.

						A test point is recommended to be reserved.
RESET_N	15	DI	PU	Reset the module	$V_{IHmin} = 1.0\text{ V}$ $V_{ILmax} = 0.3\text{ V}$	After the module is powered up, the voltage is about 1.15 V. Active low. A test point is recommended to be reserved if unused.

Indication Signals

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
STATUS	25	DO	NP	Indicate the module's operation status	VDD_EXT	If unused, keep them open.
NET_STATUS	16	DO	NP	Indicate the module's network activity status		

USB Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USB_VBUS	61	AI	PD	USB connection detect	Input voltage range: 3.0–5.25 V	A test point must be reserved.
USB_DP	59	AIO	NP	USB 2.0 differential data (+)		Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	60	AIO	NP	USB 2.0 differential data (-)		

USIM Interfaces ⁴

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USIM1_VDD	14	PO	-	USIM1 card power supply	$I_{Omax} = 34\text{ mA}$ Low-voltage: $V_{max} = 1.89\text{ V}$	Either 1.8 V or 3.0 V USIM1 card is supported and can be identified

⁴ If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards.

					Vmin = 1.71 V	automatically by the module.
					High-voltage: Vmax = 3.15 V Vmin = 2.85 V	
USIM1_DATA	11	DIO	PU	USIM1 card data	USIM1_VDD	
USIM1_CLK	13	DO	L	USIM1 card clock		
USIM1_RST	12	DO	H	USIM1 card reset		
USIM1_DET	79	DI	PU	USIM1 card hot-plug detect	V _{IH} min = 1.26 V V _{IL} max = 0.36 V	It is recommended to reserve the RC circuit and pull-up resistor externally. If unused, keep it open.
USIM2_VDD	65	PO	-	USIM2 card power supply	USIM1_VDD (Low-voltage)	Share the same power supply with USIM1_VDD.
USIM2_DATA	64	DIO	-	USIM2 card data	VDD_EXT	When using USIM2, pins of the VDD_EXT voltage domain can only be configured as 1.8 V.
USIM2_CLK	62	DO	-	USIM2 card clock		
USIM2_RST	63	DO	-	USIM2 card reset		
Auxiliary UART Interface*						
Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
AUX_TXD	29	DO	NP	Auxiliary UART transmit	VDD_EXT	If unused, keep them open.
AUX_RXD	28	DI	NP	Auxiliary UART receive		
Main UART Interface						
Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
MAIN_CTS	22	DO	NP	Clear to send signal from the module	VDD_EXT	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	NP	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.

MAIN_RXD	17	DI	NP	Main UART receive	VDD_EXT	When the module is in sleep mode and PSM, this pin can be used for interrupt wake-up. If unused, keep it open.
MAIN_TXD	18	DO	NP	Main UART transmit		If unused, keep it open.
MAIN_DCD	21	DO	PU	Main UART data carrier detect		If unused, keep it open.
MAIN_RI	20	DO	NP	Main UART ring indication		If unused, keep it open.
MAIN_DTR	19	DI	NP	Main UART data terminal ready	V _{IH} min = 1.26 V V _{IL} max = 0.36 V	It is recommended to reserve the RC circuit and pull-up resistor externally. If unused, keep it open.

Debug UART Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
DBG_RXD	38	DI	NP	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	39	DO	NP	Debug UART transmit		

I2C Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
I2C_SCL	67	OD	NP	I2C serial clock	1.8/3.3V	An external pull-up resistor is required. If unused, keep them open.
I2C_SDA	66	OD	NP	I2C serial data		

PCM Interface*

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
PCM_SYNC	31	DO	NP	PCM data frame sync	VDD_EXT	If unused, keep them open.
PCM_CLK	30	DO	NP	PCM clock		

PCM_DIN	32	DI	NP	PCM data input		
PCM_DOUT	33	DO	NP	PCM data output		
RF Antenna Interface						
Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
ANT_MAIN ⁵	35	AIO	-	Main antenna/ Wi-Fi Scan antenna interface		50 Ω impedance.
ADC Interfaces						
Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
ADC0	9	AI	NP	General-purpose ADC interface	Input voltage range: 0–1.6 V	If unused, keep them open.
ADC1	96	AI	NP	General-purpose ADC interface		
Other Interface						
Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USB_BOOT	82	DI	PD	Force the module into download mode	VDD_EXT	A test point must be reserved. Pull up this pin to VDD_EXT before the module is turned on, the module will enter forced download mode when it is turned on. Active High.
RESERVED						
Pin Name	Pin No.					Comment
RESERVED	2–6, 8, 26, 44, 49–58, 68, 69, 74–78, 80, 81, 83–87, 97–109					Keep these pins open.

⁵ The Wi-Fi scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported.

Some pins of the module are divided into three types: WAKEUP, AGPIO, and AGPIOWU pins. The pin characteristics of these three types are as follows.

Table 7: WAKEUP & AGPIO & AGPIOWU Pin Characteristics

WAKEUP Pins	Characteristics
• USB_VBUS • USIM1_DET	• Support wake-up interrupt function. • The voltage of USIM1_DET is about 1.2 V after the module is turned on. • USIM1_DET: It is recommended to reserve the RC circuit and pull-up resistor externally.
AGPIOWU Pin	Characteristics
• MAIN_DTR	• Supports wake-up interrupt function. • The voltage is about 1.2 V after the module is turned on. • The state of the pins will not be affected even if the module enters the sleep mode. • It is recommended to reserve the RC circuit and pull-up resistor externally.
AGPIO Pins	Characteristics
• STATUS • NET_STATUS • MAIN_RI	When the module is in sleep mode and PSM, the level status of these pins remains unchanged.

NOTE

1. The power domain of indication signals (pins 16 and 25), main UART (pins 17, 18 and 20–23), auxiliary UART (pins 28 and 29), debug UART (pins 38 and 39), PCM interface (pins 30–33) and I2C interface (pins 66 and 67) is 1.8 V by default and can be configured to 3.3 V by **AT+QGPIOV=1**. For more details, see *document [2]*.
2. To reduce the probability of module damage and extend module service life, do not power up and down frequently.

2.5. EVB Kit

Quectel supplies an evaluation board (UMTS<E EVB) with accessories to develop and test the module. For more details, see *document [3]*.

3 Operating Characteristics

3.1. Operating Modes

Table 8: Overview of Operating Modes

Mode	Details
Full Functionality Mode	Idle Software is active. The module is registered on the network but has no data interaction with the network.
	Data Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	● Executing AT+CFUN =0 sets the module to minimum functionality mode. ● Both RF function and USIM card are disabled.
Airplane Mode	● Executing AT+CFUN =4 sets the module to airplane mode. ● RF function is disabled.
Sleep Mode	Power consumption of the module is reduced to an ultra-low level, but the module can still receive paging, SMS* and TCP/UDP data from the network.
PSM	In this mode, the power consumption of the module will be reduced to an extremely low level. The network will be in a non-connected state, and no paging will be received.
Turn-off Mode	The VBAT pins are constantly turned on and the software stops working.

NOTE

For more details about **AT+CFUN**, see *document [2]*.

3.2. PSM

The module supports PSM (Power Saving Mode). When the module works normally, it can enter PSM if the following two conditions are met at the same time:

- Disconnect the module from the host's USB.
- Enable PSM by **AT+QSClk=3**.

The module can be awakened from PSM by any of the following methods:

- Wake-up by TAU periodic request timer (T3412);
- Wake-up by pulling down MAIN_DTR pin;
- Wake-up by connecting the module to the host's USB and then pulling up USB_VBUS pin.

NOTE

For details about PSM mode related AT commands, refer to *document [1]*.

3.3. Sleep Mode

The power consumption of the module is reduced to an ultra-low level during sleep mode.

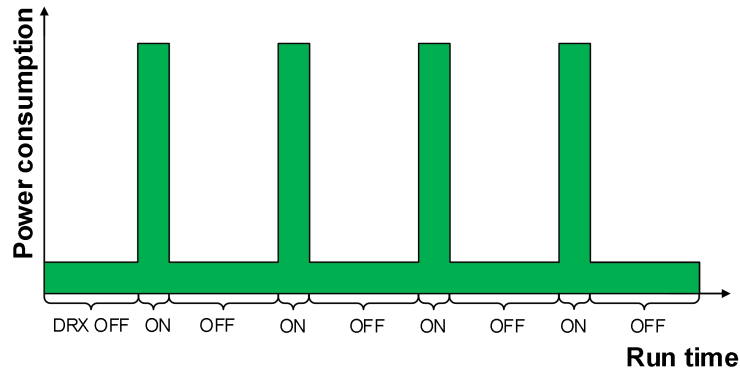


Figure 2: Power Consumption During Sleep Mode

NOTE

The DRX period value is sent by the base station over the wireless network.

3.3.1. UART Application Scenario

If the MCU communicates with the module via main UART interface, the following two preconditions should

be met to make the module enter sleep mode.

- Execute **AT+QSClk=1** ⁶.
- Ensure MAIN_DTR is held high or is kept unconnected.

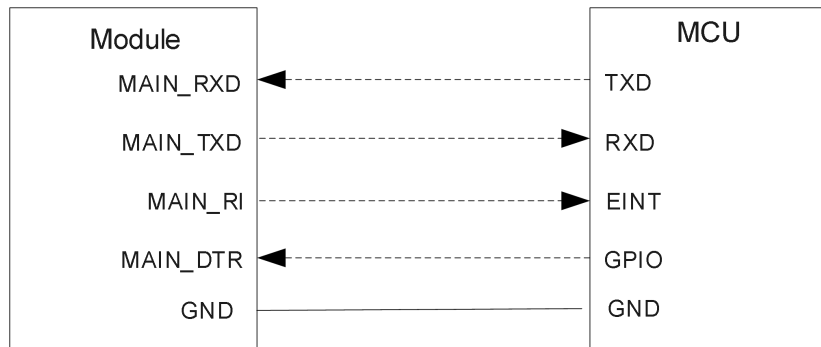


Figure 3: Sleep Mode Application via UART

- Driving the MAIN_DTR low will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the MCU. See **Chapter 4.7.3** for details about MAIN_RI behavior.

3.3.2. USB Application Scenarios

For the two situations below ('With USB Suspend/Resume and USB Remote Wakeup Function' and 'With USB Suspend/Resume and MAIN_RI Function'), three preconditions must be met to make the module enter sleep mode.

- Execute **AT+QSClk=1**.
- Ensure the MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters Suspend state.

3.3.2.1. With USB Suspend/Resume and USB Remote Wakeup Function

The host supports USB Suspend, Resume and remote wakeup function.

⁶ If the sleep function is enabled by **AT+QSClk=2**, the module can be awakened by sending any commands through the main UART.

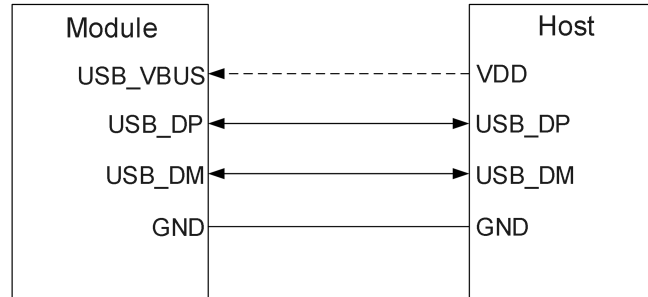


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.3.2.2. With USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend and Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

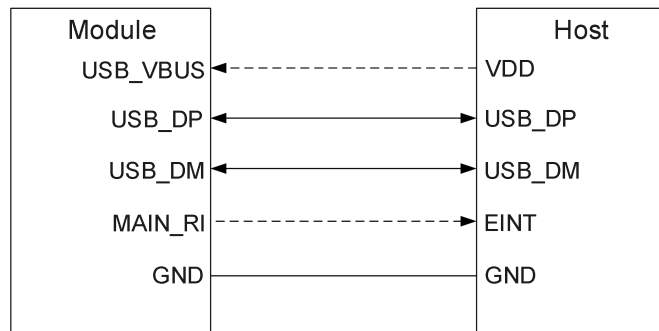


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the host.

3.3.2.3. Without USB Suspend Function

If the host does not support USB Suspend function, the following three preconditions should be met to make the module enter sleep mode.

- Execute **AT+QSClk=1**.
- Ensure the MAIN_DTR is held high or is kept unconnected.
- Disconnect the USB_VBUS power supply.

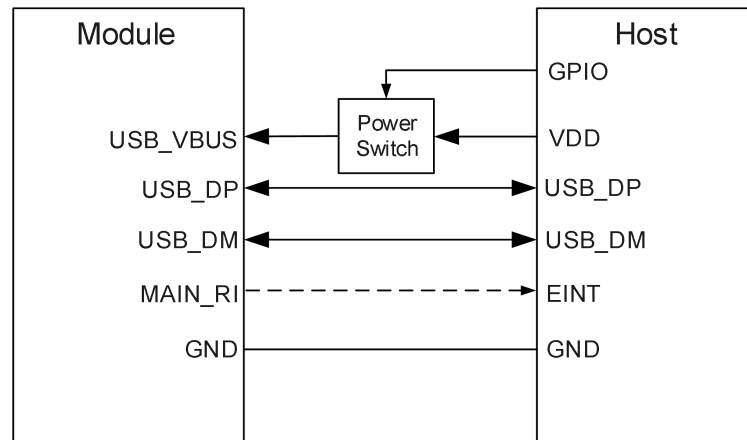


Figure 6: Sleep Mode Application without USB Suspend

Restoring the supply power of USB_VBUS will wake up the module.

NOTE

1. Note the level matching between signals connected by dotted lines between modules and MCU/host in **Chapters 3.3.1 and 3.3.2**.
2. For more information about the AT command, refer to **document [1]**.

3.4. Airplane Mode

When the module enters airplane mode, the RF function is disabled and all related AT commands cannot be executed. This mode can be set through **AT+CFUN=<fun>**, which allows you to choose the functionality level through setting **<fun>** as **0**, **1** or **4**.

- **AT+CFUN=0**: Minimum functionality mode. (Both RF and USIM functions are disabled)
- **AT+CFUN=1**: Full functionality mode. (Default).
- **AT+CFUN=4**: Airplane mode. (RF function is disabled)

For more details about AT commands, see **document [2]**.

3.5. Power Supply

3.5.1. Power Supply Interfaces

The module has two VBAT pins for connecting to external power supply.

Table 9: Pin Description of Power Supply and GND

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	42, 43	PI	Power supply for the module	3.3	3.8	4.3	V
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95						

3.5.2. Reference Design for Power Supply

Power supply design is essential for module performance. It is recommended to be provided with sufficient current of 1.2 A to the module. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

A reference design for +5 V input power source is illustrated in the following figure (Please adjust the parameters in accordance with the actual situation).

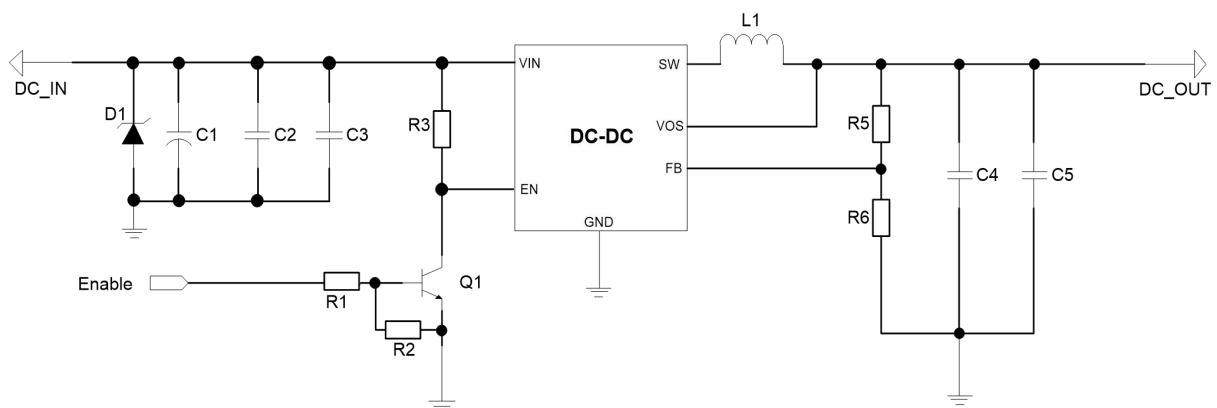


Figure 7: Power Supply Reference Design

3.5.3. Requirements for Voltage Stability

The power supply range of the module is 3.3–4.3 V. Make sure the input voltage never drops below 3.3 V. During the process in network search or data transmission, the input voltage should not fall below the module's minimum operating voltage of 3.3 V. Failure to maintain this voltage may result in module malfunction or unstable operation.

To decrease the voltage drop, use a bypass capacitor of about 100 μF with low ESR ($\text{ESR} \leq 0.7 \Omega$). A multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR is recommended. Use three ceramic capacitors (100 nF, 33 pF and 10 pF) to compose the array and place them close to VBAT pins. The width of VBAT trace should be at least 1.2 mm. In principle, the longer the VBAT trace is, the wider it should be.

To ensure the stability of the power supply, add a TVS with $V_{\text{RWM}} = 4.7 \text{ V}$, low clamping voltage and high reverse peak pulse current I_{pp} at the front end of the power supply. The reference design is shown as below.

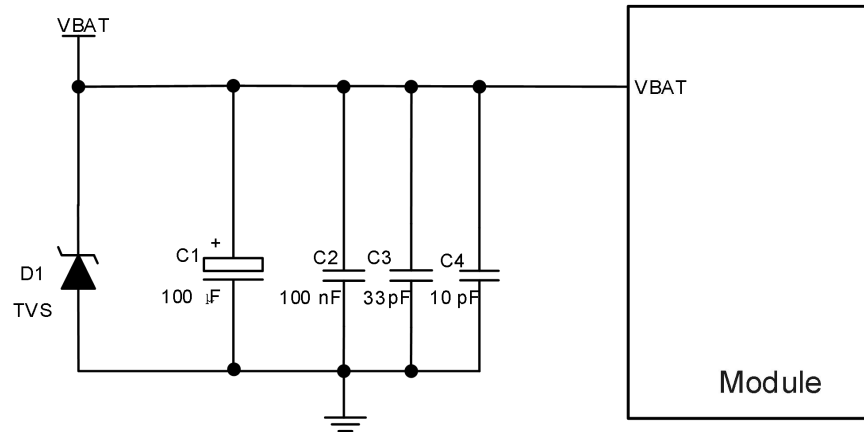


Figure 8: Power Supply Reference Design

3.6. Turn-on

3.6.1. Turn-on with PWRKEY

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	After the module is powered up, the voltage is about 1.9 V. Active low. A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open collector driver to control the PWRKEY.

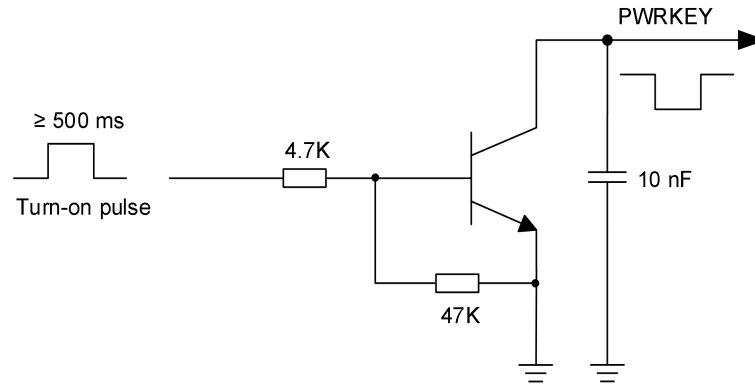


Figure 9: Reference Design of Turning on the Module with Driving Circuit

NOTE

Ensure that the capacitances connected to PWRKEY do not exceed 10 nF.

The module can also be turned on by pressing the PWRKEY button. A TVS diode should be placed near the button for protection against ESD.

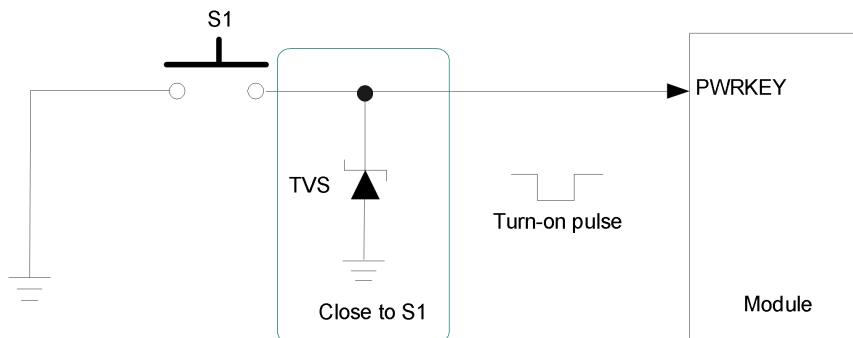


Figure 10: Reference Design of Turning on Module with Keystroke

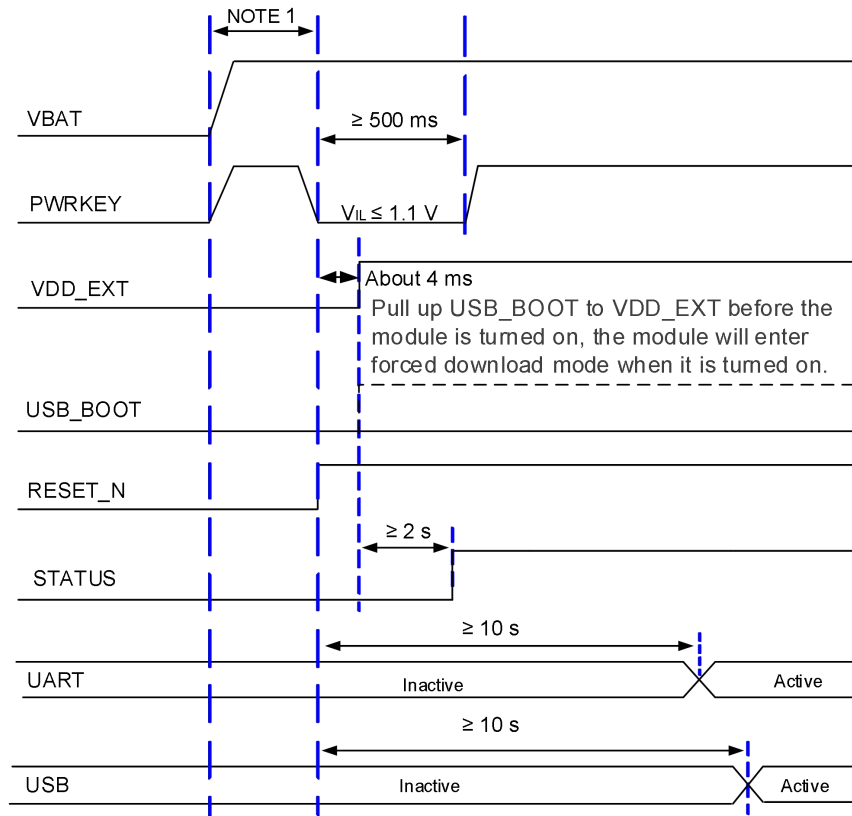


Figure 11: Turn-on Timing

NOTE

1. The PWRKEY pin is internally pulled up through a resistor with approximately 130 k Ω resistance inside the module.
2. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
3. If the module needs to turn on automatically but does not need turn-off function, you can drive PWRKEY pin low by connecting it directly to the ground with resistor not exceed 4.7 k Ω (4.7 k Ω is recommended by default), or by using a GPIO of an external MCU to drive PWRKEY low before the module powers up (PWRKEY needs to remain at low level after the module is turned on). Besides, before the module is turned on, it is necessary to ensure that the voltage of VBAT pin of the module is lower than 0.5 V.

3.7. Turn-off

3.7.1. Turn-off with PWRKEY

The module will execute turn-off procedure if you drive the PWRKEY pin low for at least 650 ms and then release it.

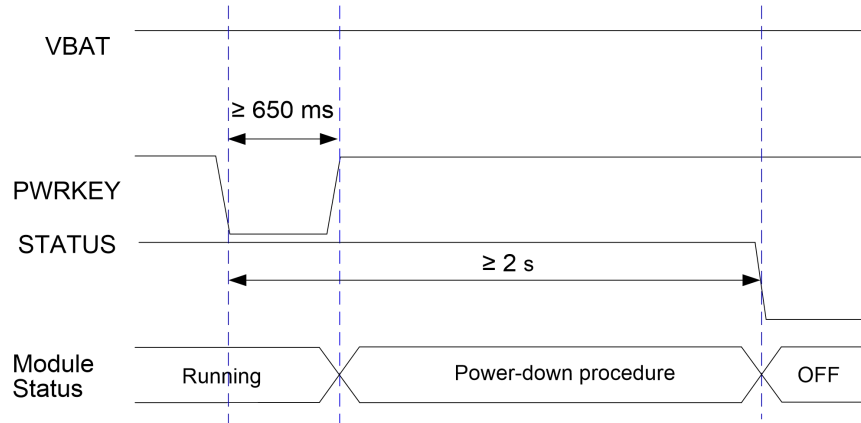


Figure 12: Timing of Turn-off with PWRKEY

3.7.2. Turn-off with AT Command

You can execute **AT+QPOWD**, to turn off the module, which is the same as turning off the module via the PWRKEY pin. See [document \[2\]](#) for details about **AT+QPOWD**.

NOTE

1. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.
2. When PWRKEY is pulled down to the ground, **AT+QPOWD** cannot be used to turn off the module.

3.8. RESET_N

Drive RESET_N low for at least 300 ms and then release it to reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the module	After the module is powered up, the voltage is about 1.15 V. Active low. A test point is recommended to be reserved if unused.

You can use an open collector driver to control RESET_N pin. The off-state leakage current of the selected triode should be less than 0.5 μ A.

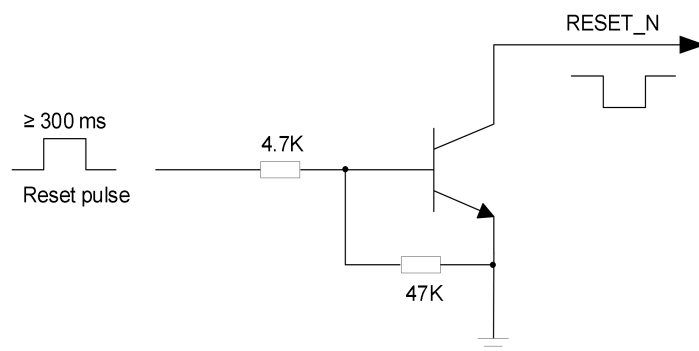


Figure 13: Reference Design of RESET_N with Driving Circuit

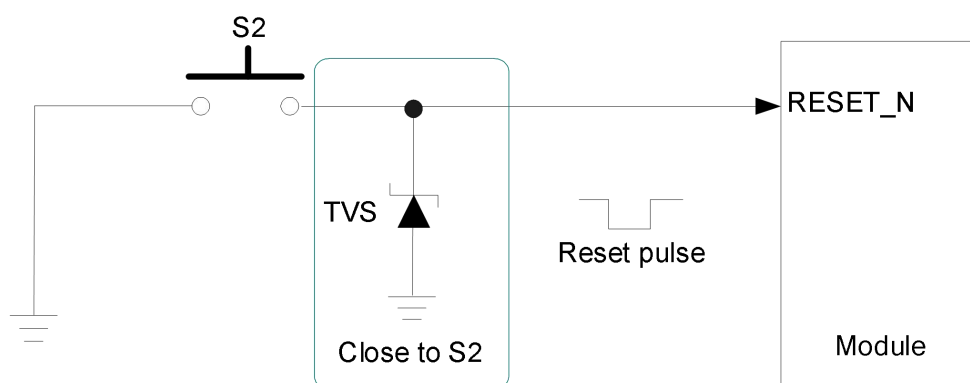


Figure 14: Reference Design of Reset with a Button

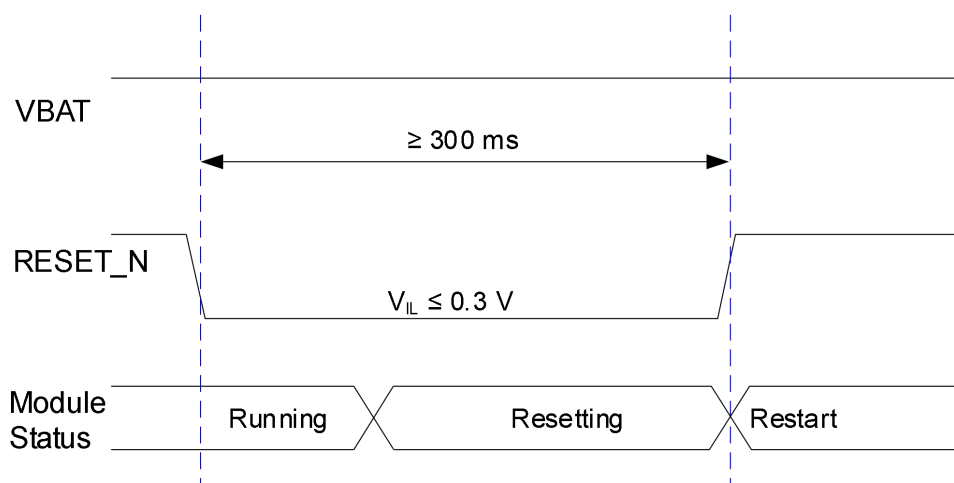


Figure 15: Reset Timing

NOTE

1. The RESET_N pin is internally pulled up through a resistor with approximately 80 k Ω resistance inside the module.
 2. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
 3. Ensure that the capacitances connected to RESET_N do not exceed 10 nF.
-

4 Application Interfaces

4.1. USB Interface

The module has one USB interface, which complies with the USB 2.0 specifications, and supports high speed (480 Mbps) and full speed (12 Mbps) on USB 2.0. The module only supports USB slave mode. The USB interface can be used for AT command communication, data transmission, software debugging, firmware upgrading and logs outputting.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	61	AI	USB connection detect	A test point must be reserved.
USB_DP	59	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω .
USB_DM	60	AIO	USB 2.0 differential data (-)	Test points must be reserved.

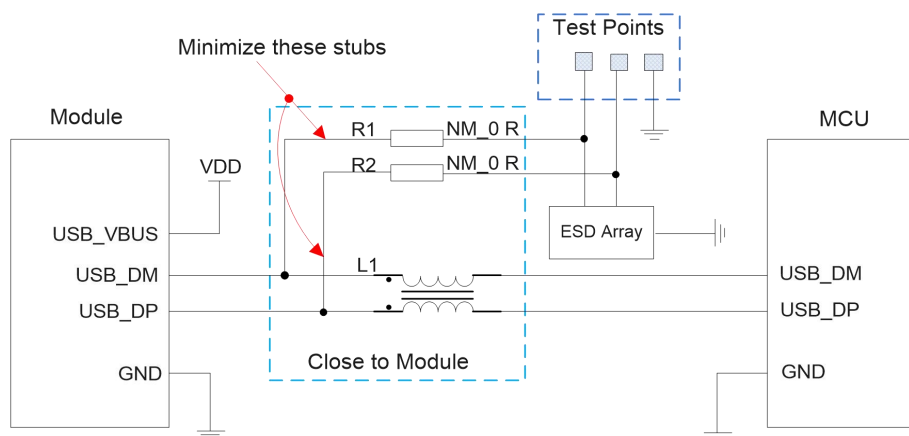


Figure 16: Reference Circuit of USB Interface

It is recommended to add a common-mode choke L1 in series between the module and MCU to suppress

EMI. In addition, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points for debugging. These resistors are not mounted by default. To ensure USB data transmission integrity, L1, R1 and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. Extra trace stubs must be as short as possible.

To ensure performance, you should follow the following principles when designing the USB interface:

- Route the USB signal traces as differential pairs surrounded by ground. The impedance of USB 2.0 differential trace is 90 Ω .
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in an inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, the stray capacitance should be less than 2 pF.
- Place ESD protection components as close to the USB interface as possible.

For more details about the USB specifications, visit <http://www.usb.org/home>.

NOTE

Test points must be reserved for USB ports to obtain logs and locate customers' problems.

4.2. Forced Download Interface

The module has a USB_BOOT for forced download. Pull up USB_BOOT to VDD_EXT before the module is turned on, the module will enter forced download mode when it is turned on. In this mode, the module can be upgraded via USB 2.0 interface.

Table 13: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	82	DI	Force the module into download mode	A test point must be reserved. Active High.

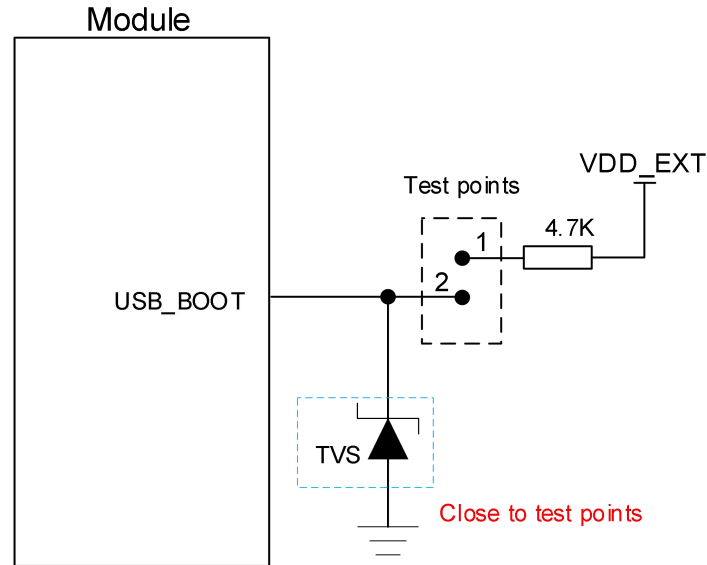


Figure 17: Reference Design of USB_BOOT Interface

4.3. USIM Interfaces

The module has two USIM interfaces, which meet ETSI and IMT-2000 requirements and support Dual SIM Single Standby. USIM1 interface supports 1.8 V and 3.0 V USIM cards; USIM2 interface only supports 1.8V USIM card.

In Dual Sim Single Standby or single USIM2 usage scenarios, pins of the VDD_EXT voltage domain can only be configured as 1.8 V (Keep the **AT+ QGPIOV=0**). See *document [2]* for details.

Table 14: Pin Description of USIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	14	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DATA	11	DIO	USIM1 card data	
USIM1_CLK	13	DO	USIM1 card clock	
USIM1_RST	12	DO	USIM1 card reset	
USIM1_DET	79	DI	USIM1 card hot-plug detect	It is recommended to reserve the RC circuit and pull-up resistor externally.

				If unused, keep it open.
USIM2_VDD	65	PO	USIM2 card power supply	Share the same power supply with USIM1_VDD.
USIM2_DATA	64	DIO	USIM2 card data	When using USIM2, pins of the VDD_EXT voltage domain can only be configured as 1.8 V.
USIM2_CLK	62	DO	USIM2 card clock	
USIM2_RST	63	DO	USIM2 card reset	

The module supports USIM card hot-plug ⁷ detection via the USIM1_DET pin, and both high and low level detection are supported. The function is disabled by default, and see **AT+QSIMDET** in *document [2]* for more details.

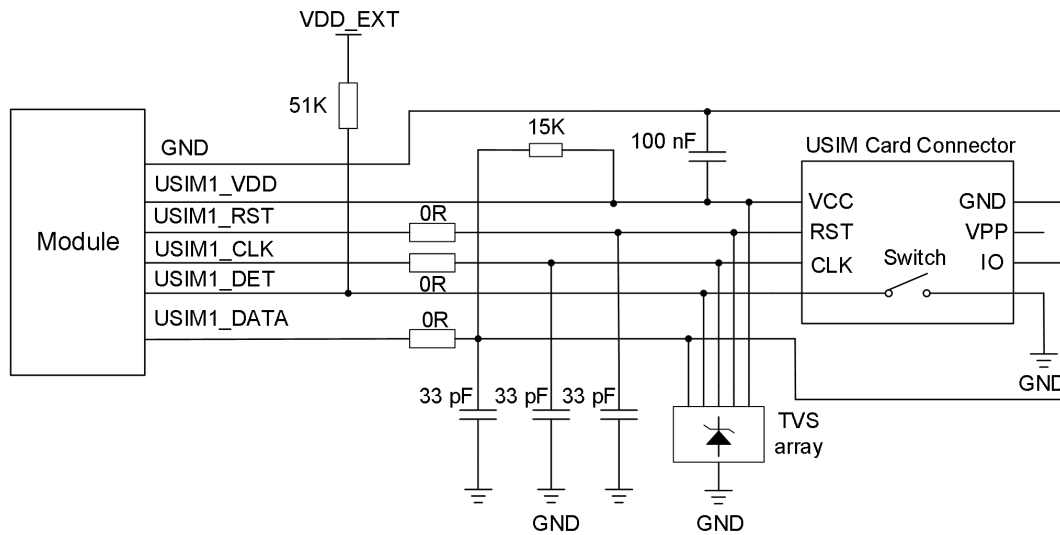
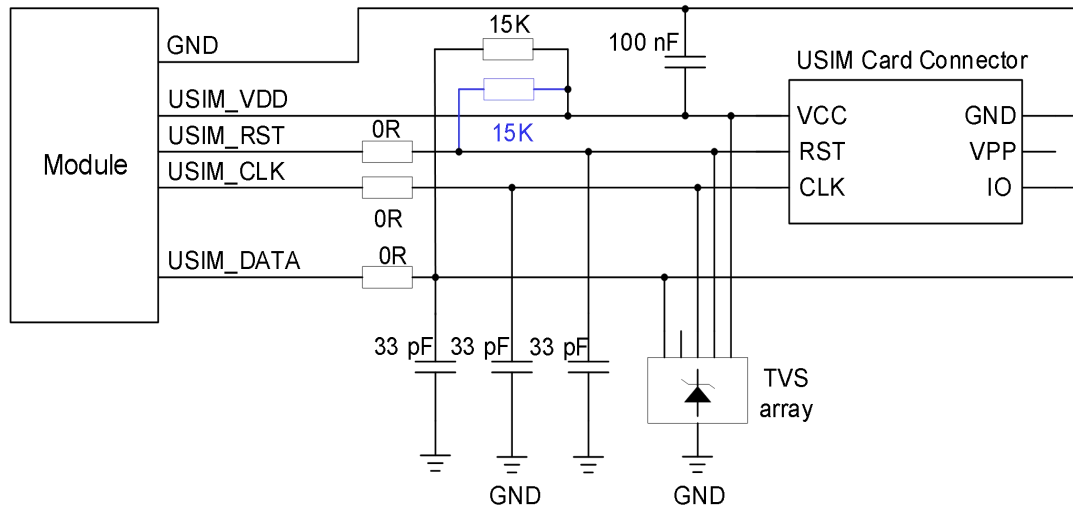


Figure 18: Reference Design of USIM1 Interface with an 8-Pin USIM Card Connector

If USIM card detection function is not needed, keep USIM1_DET disconnected.

⁷ Only USIM1 interface supports hot-plug detect.



OTE: Only when USIM2 is used should a 15 kΩ pull-up resistor be added On USIM2_RST trace.

Figure 19: Reference Design of USIM Interface with a 6-Pin USIM Card Connector

To enhance USIM card reliability and availability in applications, follow the principles below in the USIM circuit design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signal traces away from RF and power supply traces.
- Make sure that the bypass capacitor between USIM_VDD and GND does not exceed 1 μF, and should be placed close to the USIM card connector.
- To avoid cross talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them by surrounding them with ground.
- To improve ESD protection, it is recommended to add a TVS array on USIM pins. The parasitic capacitance of the TVS array should not exceed 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. The 33 pF capacitors on USIM_DATA, USIM_CLK and USIM_RST are used for filtering out RF interference. In addition, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the USIM card connector.

NOTE

The module supports Dual Sim Single Standby. USIM can be switched by **AT+QDSIM**. For details, see *document [2]*.

4.4. UART Interfaces

The module has 3 UART interfaces.

Table 15: UART Information

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART interface	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	- AT command communication, firmware upgrade and data transmission - RTS and CTS hardware flow control
Debug UART interface	115200, 3000000	3000000	Log output
Auxiliary UART interface*	115200	115200	General-purpose UART

Table 16: Pin Description of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	22	DO	Clear to send signal from the module	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module	Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	17	DI	Main UART receive	When the module is in sleep mode and PSM, this pin can be used for interrupt wake-up. If unused, keep it open.
MAIN_DCD	21	DO	Main UART data carrier detect	If unused, keep it open.
MAIN_TXD	18	DO	Main UART transmit	If unused, keep it open.
MAIN_RI	20	DO	Main UART ring indication	If unused, keep it open.
MAIN_DTR	19	DI	Main UART data terminal ready	It is recommended to reserve the RC circuit and pull-up resistor externally. If unused, keep it open.
AUX_TXD*	29	DO	Auxiliary UART transmit.	If unused, keep them open.

AUX_RXD*	28	DI	Auxiliary UART receive.	
DBG_RXD	38	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit	

If the level of the module's UART is the same as that of the MCU, and the MAIN_TXD of the module is connected to the RXD of the MCU, the MAIN_TXD should be connected to a 10 kΩ resistor and be pulled up to VDD_EXT to prevent the MCU from receiving error messages when the module is in sleep mode. A voltage-level translator should be used between the module and the MCU if the level is not the same.

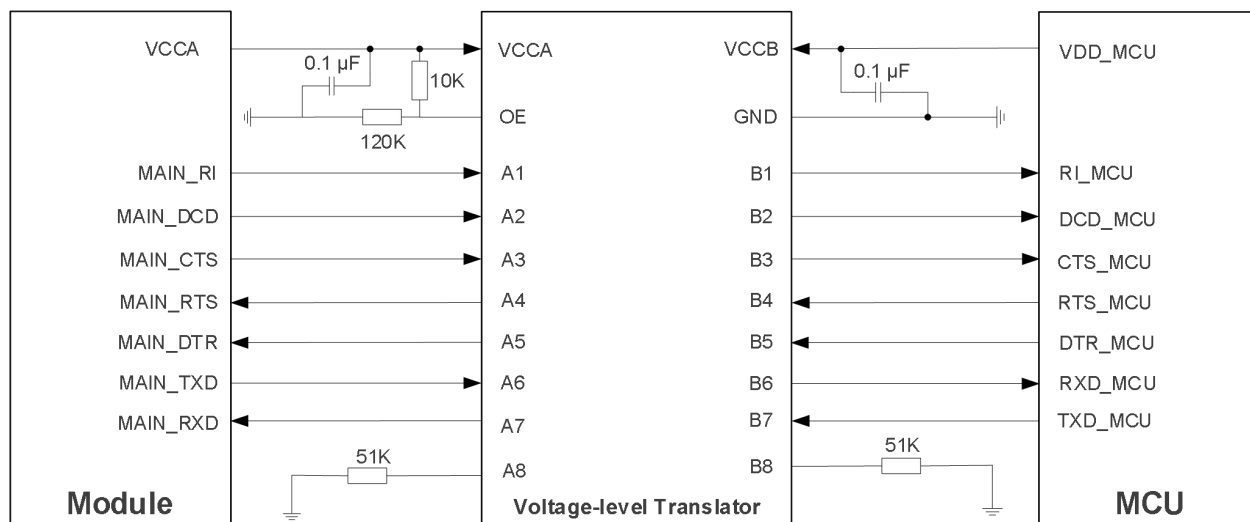


Figure 20: Reference Design of UART with a Voltage-Level Translator (Main UART)

NOTE

For this voltage-level translator, the input voltage of the power supply VCCA should be consistent with the UART level of the module, and be lower than the power supply voltage VDD_MCU connected to VCCB. In addition, to ensure the normal operation of the chip, the VCCA power supply capacity of the chip is recommended to be greater than 50 mA, and VCCA cannot be powered down when the module is in sleep mode.

Another example of level-shifting circuit is shown below. For the design of input/output circuits in dotted lines, see the ones in solid lines, but pay attention to the direction of the connection.

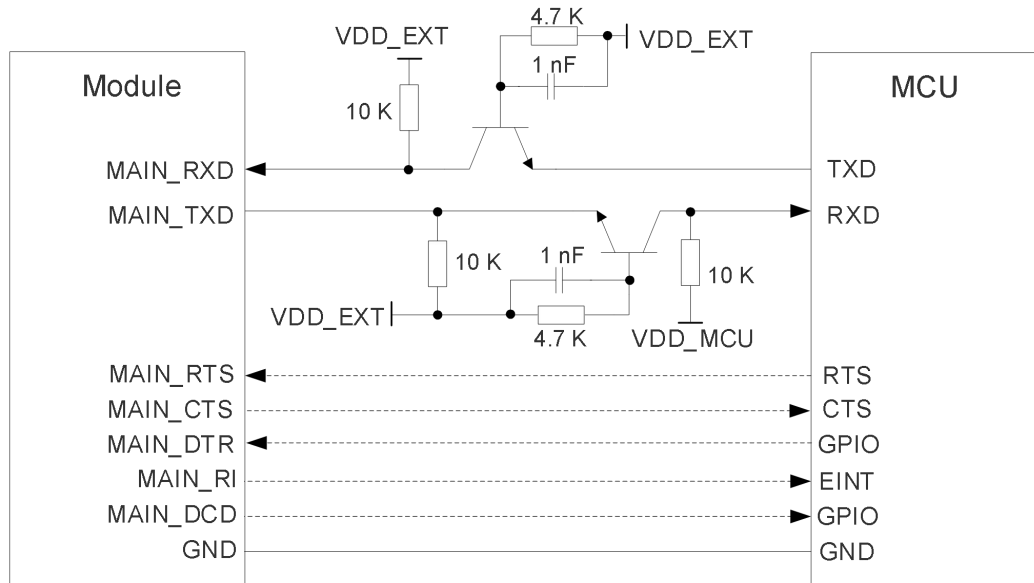


Figure 21: Reference Design of UART with Transistor Circuit (Main UART)

NOTE

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. The level-shifting circuits (**Figure 20** and **Figure 21**) take the main UART as an example. The circuits of the debug UART and the auxiliary UART are connected in the same way as the main UART.
4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. PCM* and I2C Interfaces

The module has one Pulse Code Modulation (PCM) digital interface and one I2C interface.

Table 17: Pin Description of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	31	DO	PCM data frame sync	If unused, keep them open.
PCM_CLK	30	DO	PCM clock	

PCM_DIN	32	DI	PCM data input
PCM_DOUT	33	DO	PCM data output

Table 18: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	67	OD	I2C serial clock	An external pull-up resistor is required. If unused, keep them open.
I2C_SDA	66	OD	I2C serial data	

A reference design of PCM and I2C interfaces with external Codec IC is illustrated in the following figure.

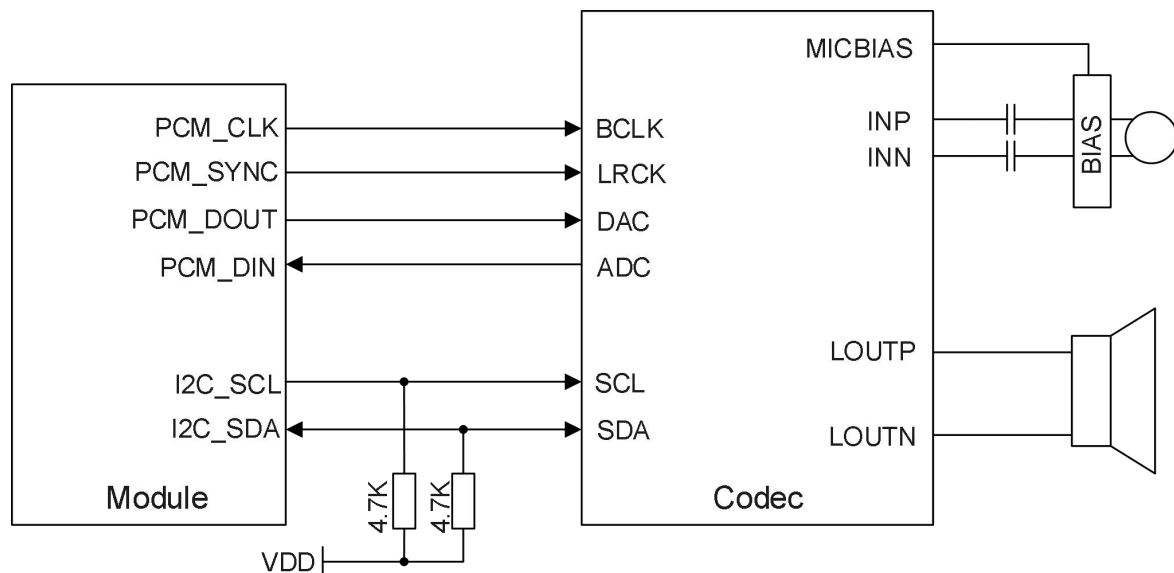


Figure 22: Reference Circuit of PCM and I2C Interfaces

NOTE

1. It is recommended to reserve RC circuits on the PCM signal traces, especially on the PCM_CLK pin.
2. The module can only be used as a master device in applications related to both the PCM interface and the I2C interface.
3. The PCM and I2C interface level of the module should be consistent with those of the Codec chip, and the level of the pull-up power supply VDD for the module's I2C interface should be consistent with the level of its I2C interface.

4.6. ADC Interfaces

The module has two Analog-to-Digital Converter (ADC) interfaces. To improve the voltage measurement accuracy, the trace of ADC interface should be surrounded by ground.

Table 19: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	96	AI	General-purpose ADC interface	

With **AT+QADC=<adc_id>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see *document [2]*.

Table 20: ADC Interface Features

Name	Min.	Typ.	Max.	Unit
ADC0 Input Voltage	0	-	1.6	V
ADC1 Input Voltage	0	-	1.6	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage range of ADC0 and ADC1 interfaces is 0–1.6 V. Please note that the effective input voltage range of ADC interfaces is 0.1–1.5 V. There may be relatively large errors in the ranges of 0–0.1 V and 1.5–1.6 V, and it is not recommended to use the ADC interfaces within these ranges.
2. When the collected voltage is greater than or equal to 1.5 V, it is recommended to use the resistor divider circuit for ADC application. The divider resistor accuracy should not exceed 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for the design.

4.7. Indication Signals

Table 21: Pin Description of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	16	DO	Indicate the module's network activity status	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status	
MAIN_RI	20	DO	Main UART ring indication	

4.7.1. Network Status Indication

The NET_STATUS pin indicates the module's network activity status, and can be used to drive network status indication LEDs.

Table 22: Network Connection Status/Activity Indicated by NET_STATUS Pin

Pin Name	Status	Description
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing

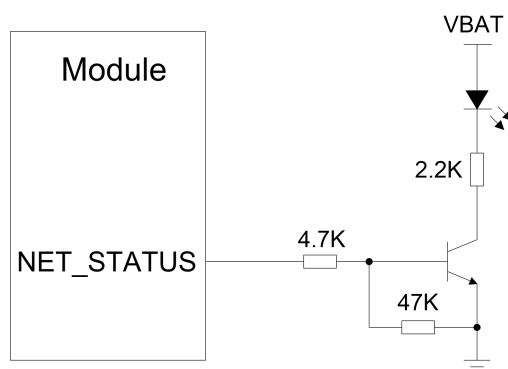


Figure 23: Reference Design of NET_STATUS

4.7.2. STATUS

The STATUS pin is used to indicate the module's operation status. It outputs high level when the module is turned on normally.

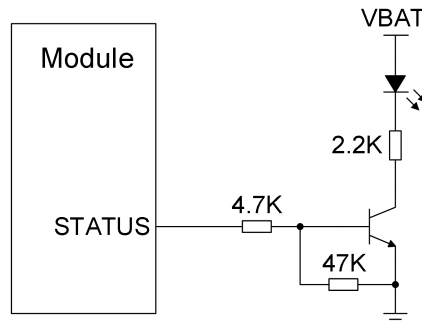


Figure 24: Reference Design of STATUS

4.7.3. MAIN_RI

AT+QCFG= "risignalttype", "physical" can be used to configure MAIN_RI as URC indication pin. An URC will trigger MAIN_RI regardless of the URC output port. For more details about **AT+QCFG**, see *document [2]*.

NOTE

The **AT+QURCCFG** allows you to configure the main UART, USB AT port or USB modem port as the URC output port. The USB AT port is the URC output port by default. For more details about **AT+QURCCFG**, see *document [2]*.

MAIN_RI can be configured flexibly. However, its default behaviors are:

Table 23: Behaviors of MAIN_RI

Module Status	MAIN_RI Level Status
Idle	High
URC/SMS*	MAIN_RI outputs at least 120 ms low level. After this pin changes to a high level, the module starts to output data.

The MAIN_RI can be configured as URC indication pin via **AT+QCFG="urc/ri/ring"**.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular/Wi-Fi Scan Antenna Interface

5.1.1. Antenna Interface and Frequency Bands

Table 24: Pin Description of Cellular/Wi-Fi Scan Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	35	AIO	Main antenna/Wi-Fi Scan antenna interface	50 Ω impedance.

NOTE

1. The Wi-Fi scan function utilizes the same antenna interface as the main antenna. Due to this shared interface, Time Division Multiplexing (TDM) is employed since the two functions cannot be used simultaneously. Wi-Fi Scan functionality only supports receiving. Transmitting is not supported.
2. Main antenna and Wi-Fi Scan antenna only support passive antennas.

Table 25: Operating Frequency of EG800Z-CN (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920~1980	2110~2170
LTE-FDD B3	1710~1785	1805~1880
LTE-FDD B5	824~849	869~894
LTE-FDD B8	880~915	925~960

LTE-TDD B34	2010~2025	2010~2025
LTE-TDD B38	2570~2620	2570~2620
LTE-TDD B39	1880~1920	1880~1920
LTE-TDD B40	2300~2400	2300~2400
LTE-TDD B41	2535~2675	2535~2675

NOTE

EG800Z-CN B41 only supports 140 MHz (2535~2675 MHz).

Table 26: Operating Frequency of EG800Z-EU (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920~1980	2110~2170
LTE-FDD B3	1710~1785	1805~1880
LTE-FDD B5	824~849	869~894
LTE-FDD B7	2500~2570	2620~2698
LTE-FDD B8	880~915	925~960
LTE-FDD B20	832~862	791~821
LTE-FDD B28	703~748	758~803
LTE-TDD B38	2570~2620	2570~2620
LTE-TDD B40	2300~2400	2300~2400
LTE-TDD B41	2496~2690	2496~2690

NOTE

EG800Z-EU B41 only supports 194 MHz (2496~2690 MHz).

Table 27: Operating Frequency of EG800Z-LA (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850~1910	1930~1990
LTE-FDD B3	1710~1785	1805~1880
LTE-FDD B4	1710~1755	2110~2155
LTE-FDD B5	824~849	869~894
LTE-FDD B7	2500~2570	2620~2698
LTE-FDD B8	880~915	925~960
LTE-FDD B28	703~748	758~803
LTE-FDD B66	1710~1780	2110~2180

5.1.2. Transmitting Power

Table 27: Tx Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
LTE bands	23 dBm $\pm$ 2 dB	< -39 dBm

5.1.3. Receiver Sensitivity

Table 28: EG800Z-CN Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B1 (10 MHz)	-98.0	-93.3
LTE-FDD B3 (10 MHz)	-98.0	-90.3
LTE-FDD B5 (10 MHz)	-98.0	-91.8
LTE-FDD B8 (10 MHz)	-98.0	-90.8
LTE-TDD B34 (10 MHz)	-99.5	-93.8

LTE-TDD B38 (10 MHz)	-99.0	-93.3
LTE-TDD B39 (10 MHz)	-99.5	-93.8
LTE-TDD B40 (10 MHz)	-99.0	-93.8
LTE-TDD B41 (10 MHz)	-98.5	-91.8

Table 29: EG800Z-EU Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B1 (10 MHz)	-98.0	-93.3
LTE-FDD B3 (10 MHz)	-98.5	-90.3
LTE-FDD B5 (10 MHz)	-99.0	-91.8
LTE-FDD B7 (10 MHz)	-96.5	-91.3
LTE-FDD B8 (10 MHz)	-99.0	-90.8
LTE-FDD B20 (10 MHz)	-99.0	-90.8
LTE-FDD B28 (10 MHz)	-99.0	-92.3
LTE-TDD B38 (10 MHz)	-98.0	-93.3
LTE-TDD B40 (10 MHz)	-98.5	-93.8
LTE-TDD B41 (10 MHz)	-98.0	-91.8

Table 30: EG800Z-LA Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP Requirements
	Primary	
LTE-FDD B2 (10 MHz)	-97.5	-91.3
LTE-FDD B3 (10 MHz)	-98	-90.3
LTE-FDD B4 (10 MHz)	-98.5	-93.3
LTE-FDD B5 (10 MHz)	-98	-91.8

LTE-FDD B7 (10 MHz)	-96.5	-91.3
LTE-FDD B8 (10 MHz)	-98.5	-90.8
LTE-FDD B28 (10 MHz)	-98.5	-92.3
LTE-FDD B66 (10 MHz)	-98.5	-92.8

5.1.4. Reference Design

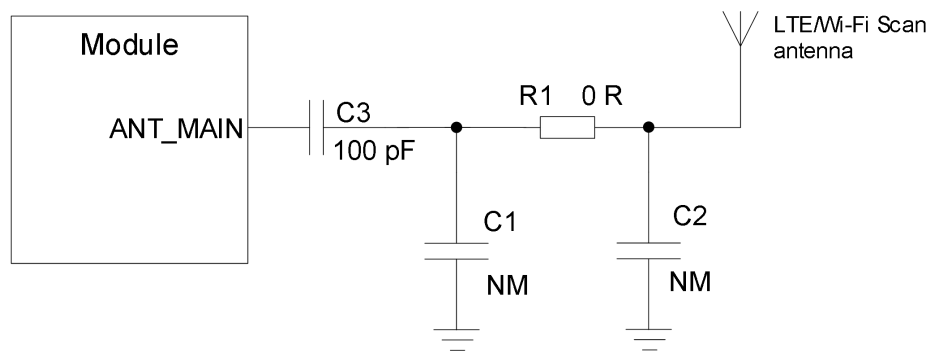


Figure 25: Reference Design of RF Antenna Interfaces

NOTE

- Place the dual L-type components (C3, C1, R1 and C2) to antennas as close as possible. Capacitors C1 and C2 are not mounted by default.
- Notes on C3:
 - If there is DC power at the antenna ports, place a capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
 - If there is no DC power in the peripheral design:
 - Do not reserve C3.
 - If C3 has already been reserved, it should be mounted with a component, and it is recommended to use a 0 Ω resistor. You can also match the component according to the debugging results.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω . The impedance of

the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

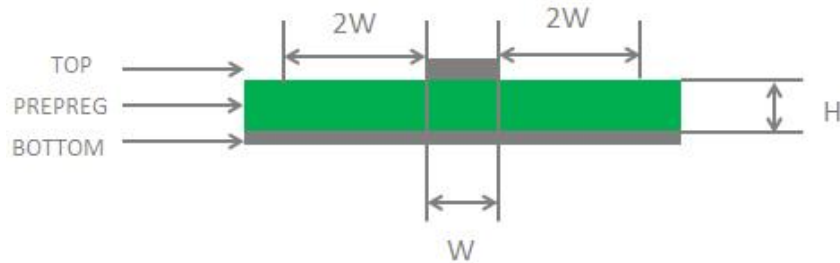


Figure 26: Microstrip Design on a 2-layer PCB

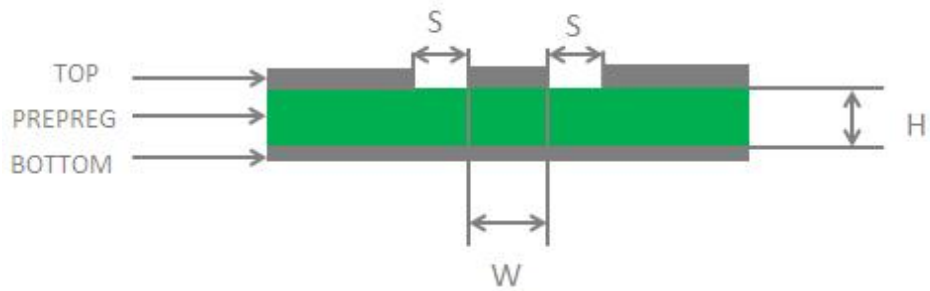


Figure 27: Coplanar Waveguide Design on a 2-layer PCB

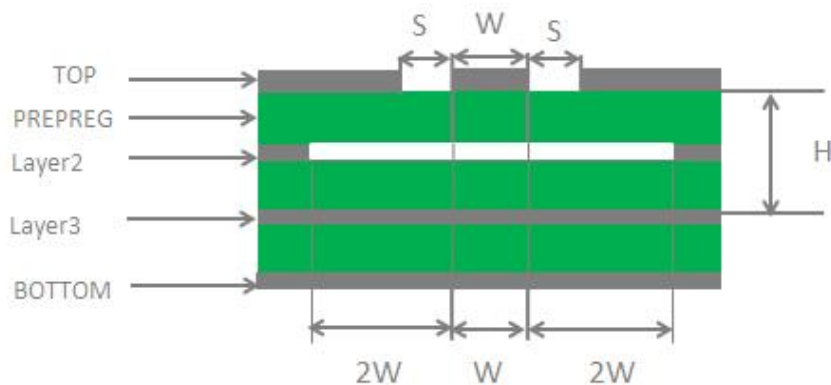


Figure 28: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

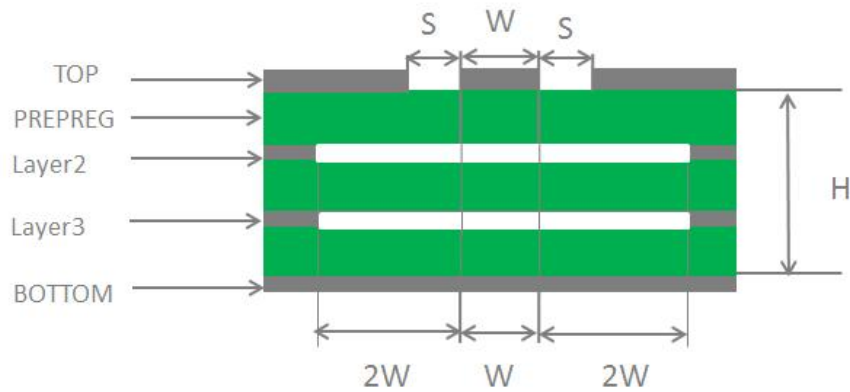


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces ($2 \times W$).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see *document [4]*.

5.3. Requirements for Antenna Design

Table 31: Antenna Design Requirements

Antenna Type	Requirements
Cellular/Wi-Fi Scan	● VSWR: ≤ 2 ● Efficiency: $> 30\%$ ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: – < 1 dB: LB (< 1 GHz)

- < 1.5 dB: MB (1–2.3 GHz)
- < 2 dB: HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

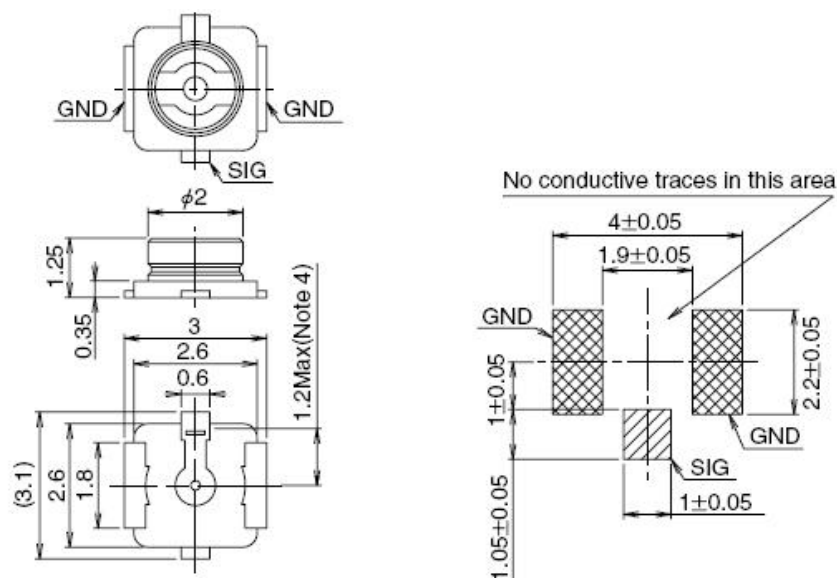


Figure 30: Receptacle Dimensions (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 31: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

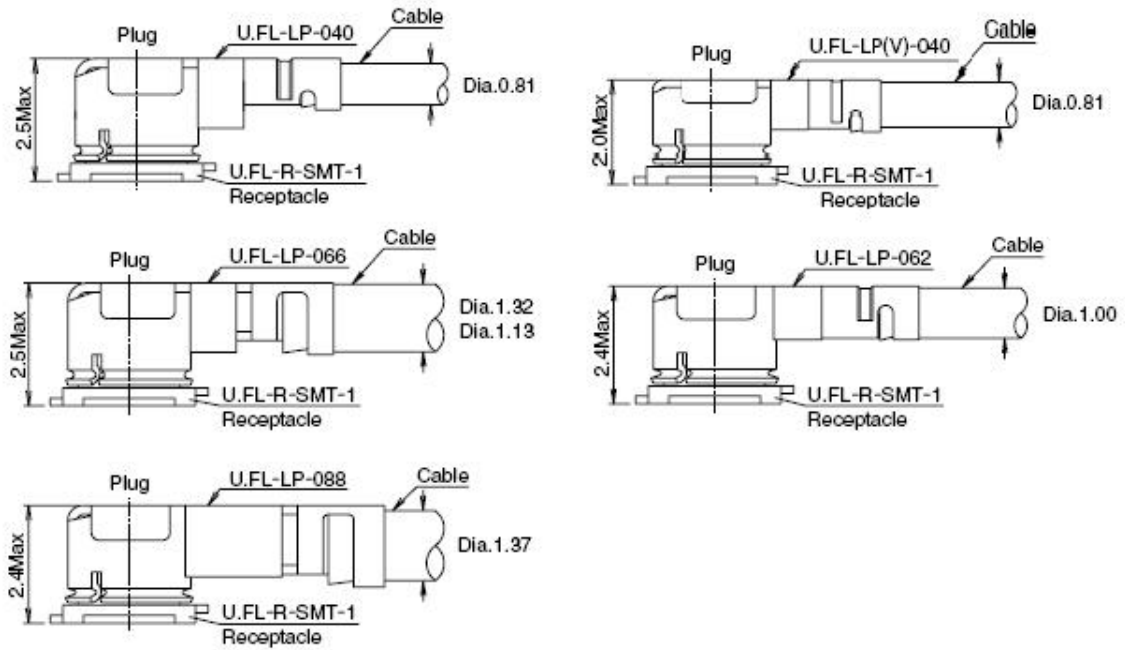


Figure 32: Space Factor of Mated Connectors (Unit: mm)

For more details, visit <http://www.hirose.com>.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 32: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT	-0.3	5	V
Voltage at USB_VBUS	-0.3	5.25	V
Voltage at digital pins	-0.3	3.6	V

NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

6.2. Power Supply Ratings

Table 33: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
I _{VBAT}	Peak supply current	At maximum power	-	-	1.2	A

	under BB and RF application scenarios	control level				
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 34: EG800Z-CN Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.4	μA
PSM	AT+QSClk=3 (USB disconnected)	4.11	μA
	AT+CFUN=0 (USB disconnected)	0.05	mA
	AT+CFUN=4 (USB disconnected)	0.15	mA
	LTE-FDD @ PF = 32 (USB disconnected)	0.97	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.63	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.44	mA
Sleep	LTE-FDD @ PF = 256 (USB disconnected)	0.34	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.06	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.56	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.36	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.3	mA
	LTE-FDD @ PF = 64 (USB disconnected)	4.22	mA
Idle	LTE-FDD @ PF = 64 (USB connected)	27.06	mA
	LTE-TDD @ PF = 64 (USB disconnected)	4.28	mA
	LTE-TDD @ PF = 64 (USB connected)	27.4	mA
LTE data transmission	LTE-FDD B1	500	mA
	LTE-FDD B3	480	mA

LTE-FDD B5	490	mA
LTE-FDD B8	550	mA
LTE-TDD B34	180	mA
LTE-TDD B38	180	mA
LTE-TDD B39	180	mA
LTE-TDD B40	180	mA
LTE-TDD B41 (140 MHz)	200	mA

Table 35: EG800Z-EU Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.4	μA
PSM	AT+QSCLK=3 (USB disconnected)	4.11	μA
	AT+CFUN=0 (USB disconnected)	0.05	mA
	AT+CFUN=4 (USB disconnected)	0.15	mA
	LTE-FDD @ PF = 32 (USB disconnected)	0.94	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.61	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.41	mA
Sleep	LTE-FDD @ PF = 256 (USB disconnected)	0.30	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.11	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.72	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.5	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.29	mA
	LTE-FDD @ PF = 64 (USB disconnected)	3.15	mA
	LTE-FDD @ PF = 64 (USB connected)	25.98	mA
Idle	LTE-TDD @ PF = 64 (USB disconnected)	3.88	mA
	LTE-TDD @ PF = 64 (USB connected)	26.73	mA

LTE data transmission	LTE-FDD B1	500	mA
	LTE-FDD B3	550	mA
	LTE-FDD B5	480	mA
	LTE-FDD B7	560	mA
	LTE-FDD B8	480	mA
	LTE-FDD B20	440	mA
	LTE-FDD B28	480	mA
	LTE-TDD B38	170	mA
	LTE-TDD B40	170	mA
	LTE-TDD B41 (140 MHz)	170	mA

Table 36: EG800Z-LA Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	0.4	μA
PSM	AT+QSCLK=3 (USB disconnected)	2.91	μA
Sleep	AT+CFUN=0 (USB disconnected)	0.6	mA
	AT+CFUN=4 (USB disconnected)	0.6	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.06	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.56	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.36	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.30	mA
	LTE-FDD @ PF = 64 (USB connected)	26.68	mA
Idle	LTE-FDD @ PF = 64 (USB disconnected)	3.60	mA
LTE data transmission	LTE-FDD B2	520	mA
	LTE-FDD B3	540	mA
	LTE-FDD B4	500	mA

LTE-FDD B5	490	mA
LTE-FDD B7	560	mA
LTE-FDD B8	480	mA
LTE-FDD B28	480	mA
LTE-FDD B66	510	mA

NOTE

The above power consumption data are tested under 50 Ω impedance.

6.4. Digital I/O Characteristics

Table 37: VDD_EXT I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	$0.7 \times VDD_EXT$	$VDD_EXT + 0.3$
V_{IL}	Low-level input voltage	-0.3	$0.2 \times VDD_EXT$
V_{OH}	High-level output voltage	$0.8 \times VDD_EXT$	-
V_{OL}	Low-level output voltage	-	$0.15 \times VDD_EXT$

Table 38: USIM Low/High-voltage I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	$0.7 \times USIM_VDD$	-
V_{IL}	Low-level input voltage	-	$0.2 \times USIM_VDD$
V_{OH}	High-level output voltage	$0.8 \times USIM_VDD$	-
V_{OL}	Low-level output voltage	-	$0.15 \times USIM_VDD$

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 39: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interface	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 40: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Normal operating temperature ⁸	-35	+25	+75	°C

⁸ Within this range, the module's indicators comply with 3GPP specification requirements.

Extended operating temperature ⁹	-40	-	+85	°C
Storage temperature	-40	-	+90	°C

⁹ Within the range of -40 to -35 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as SMS* and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out} , may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

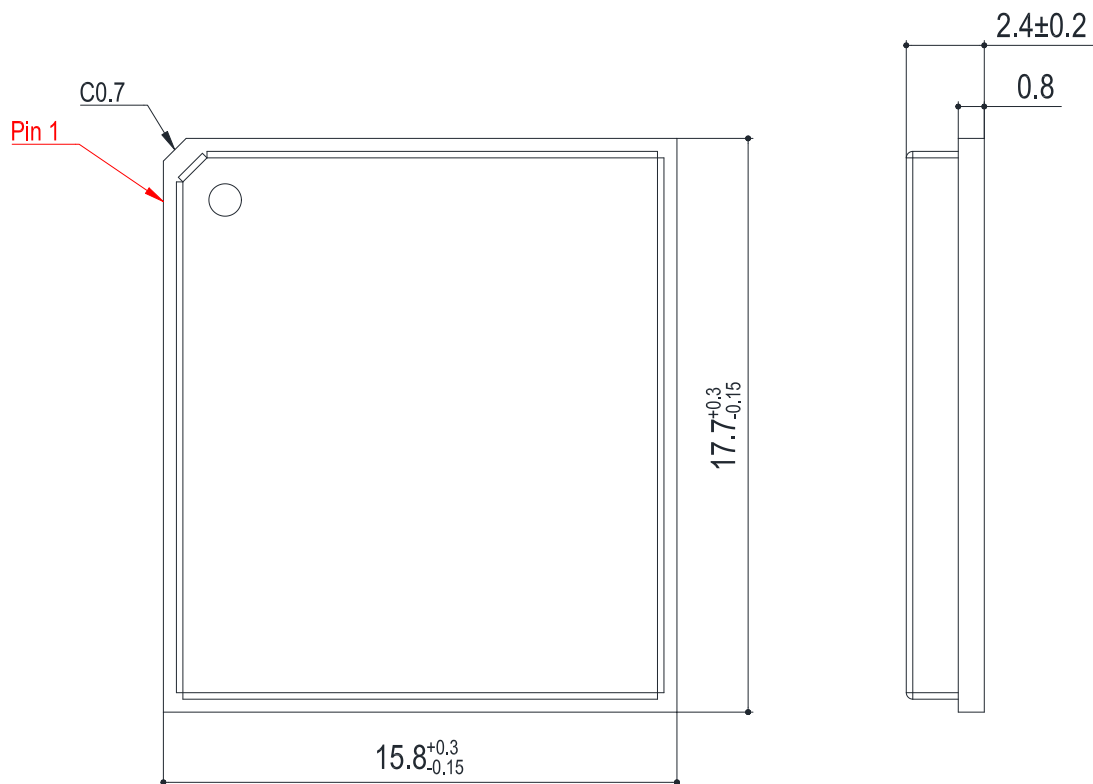


Figure 33: Module Top and Side Dimensions (Unit: mm)

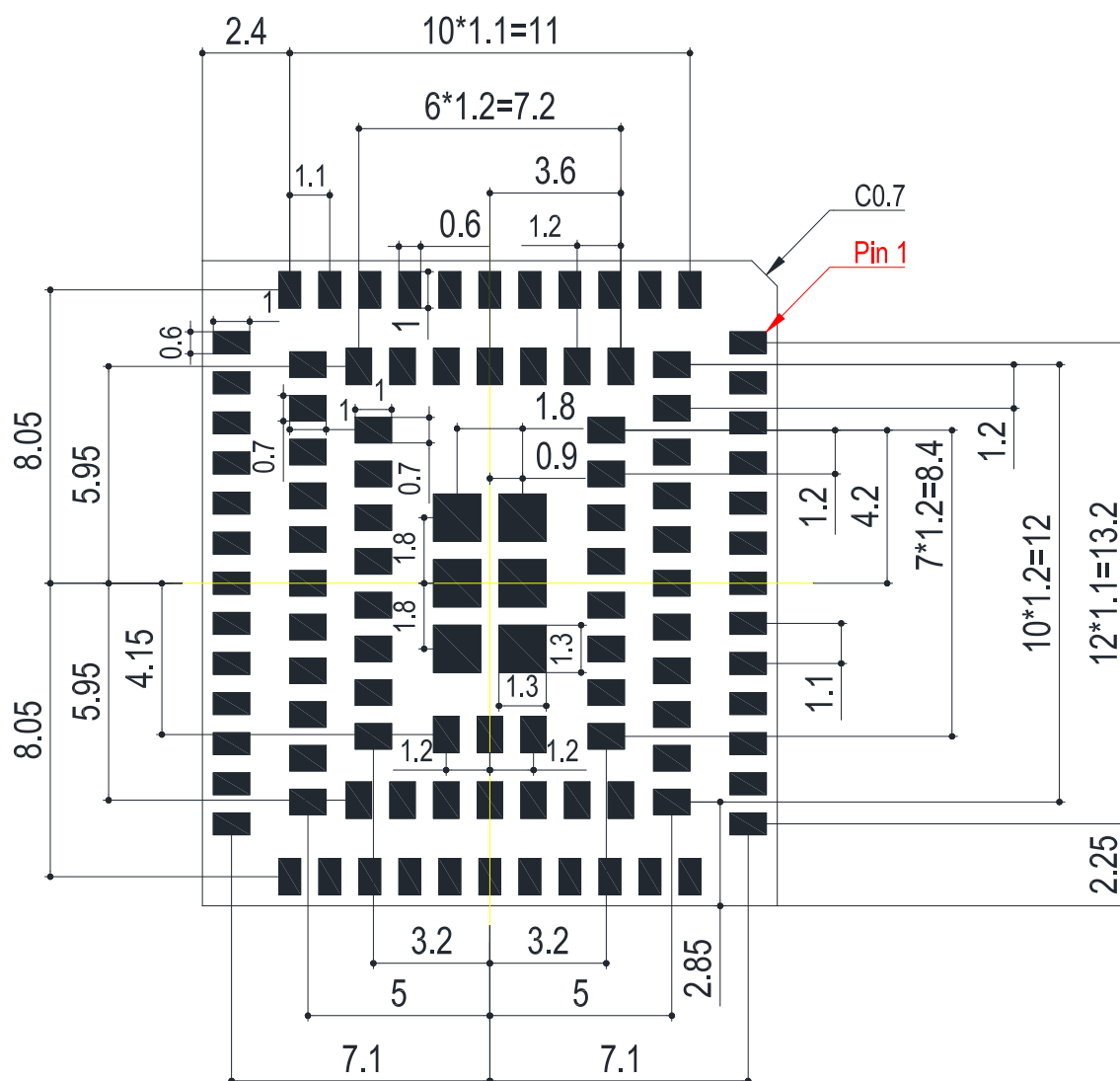


Figure 34: Bottom Dimension (Bottom View, Unit: mm)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

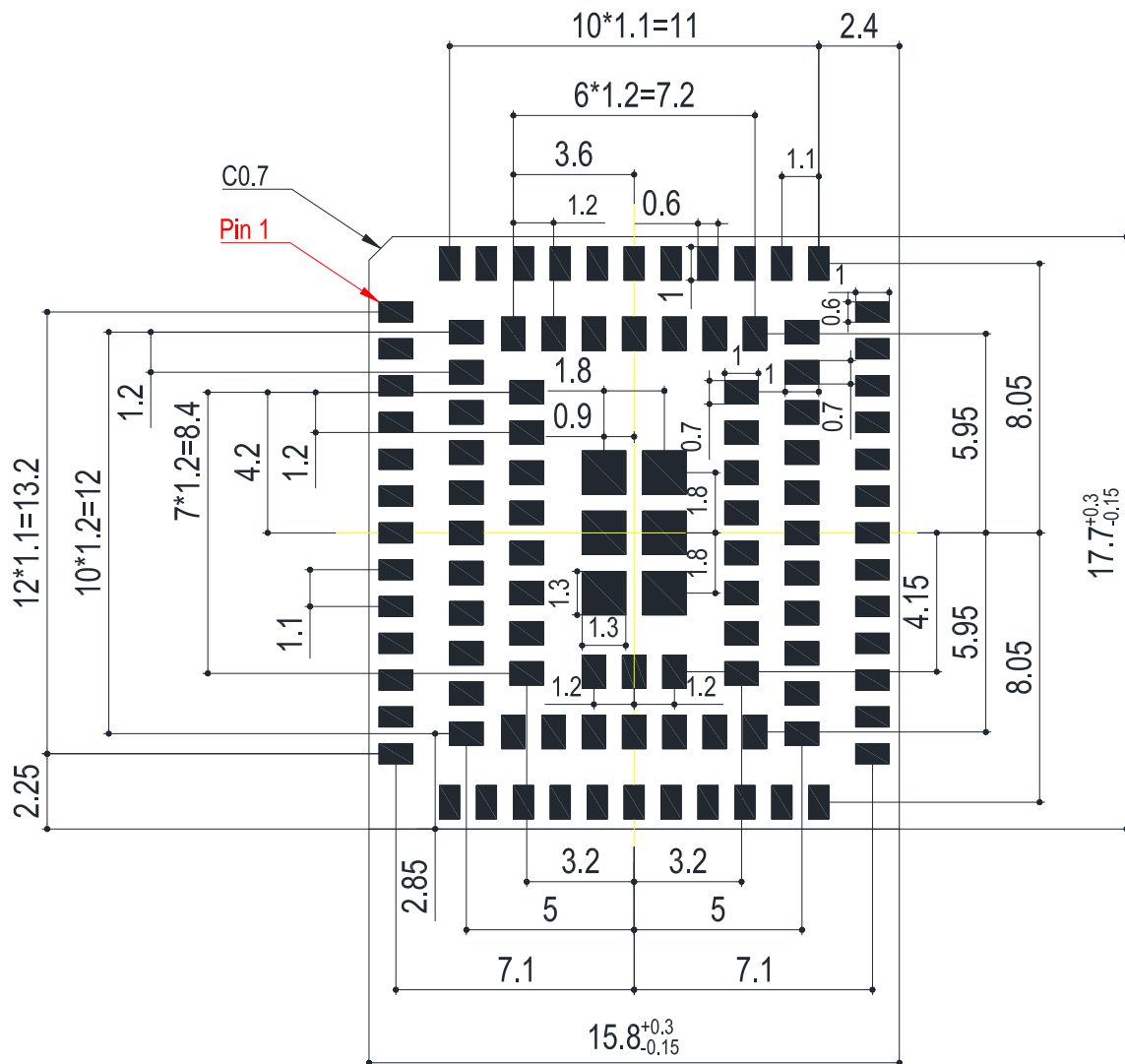


Figure 35: Recommended Footprint (Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

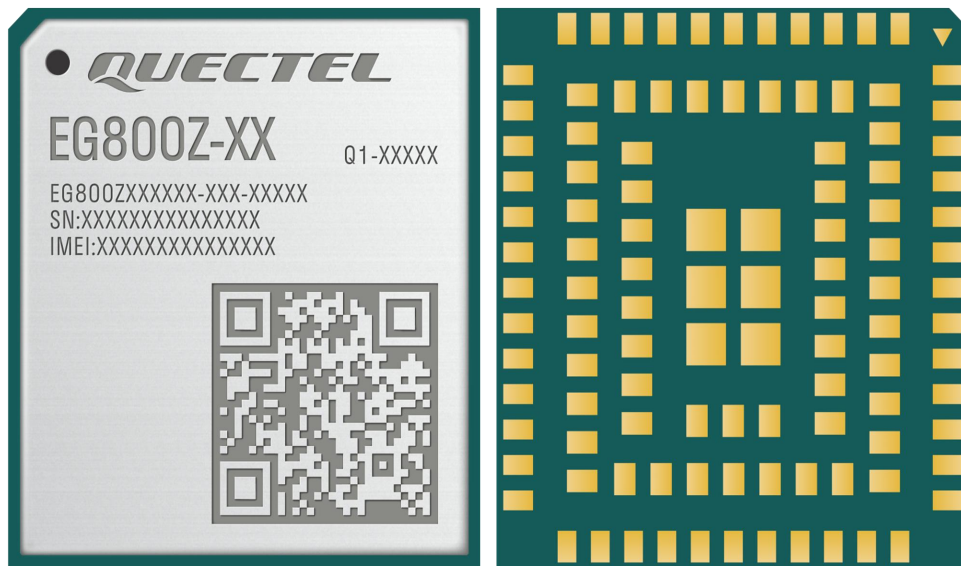


Figure 36: Module Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours ¹⁰ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 24 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in

¹⁰ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see *document [5]*.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

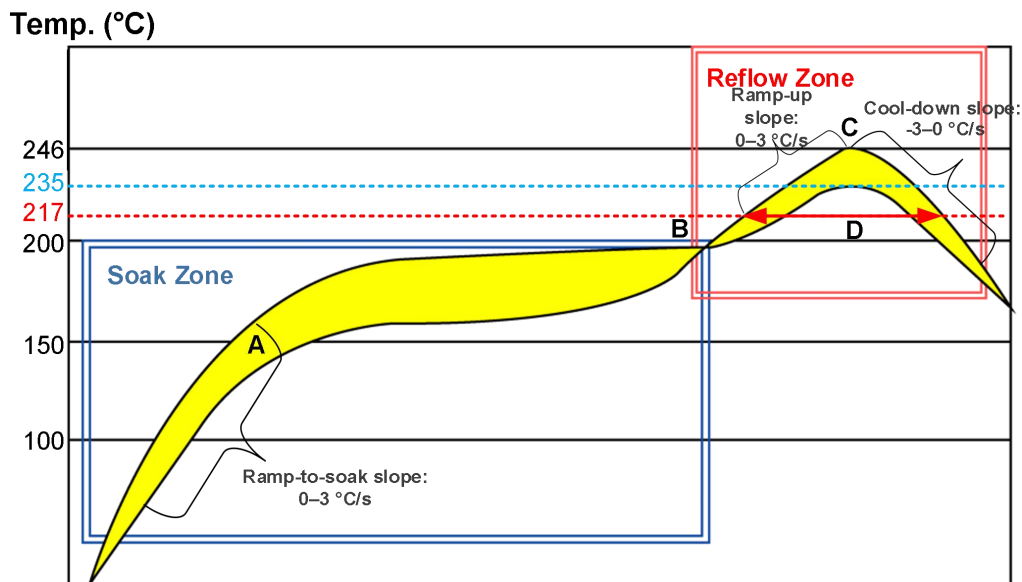


Figure 37: Recommended Reflow Soldering Thermal Profile

Table 41: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	–3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in *document [6]*.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

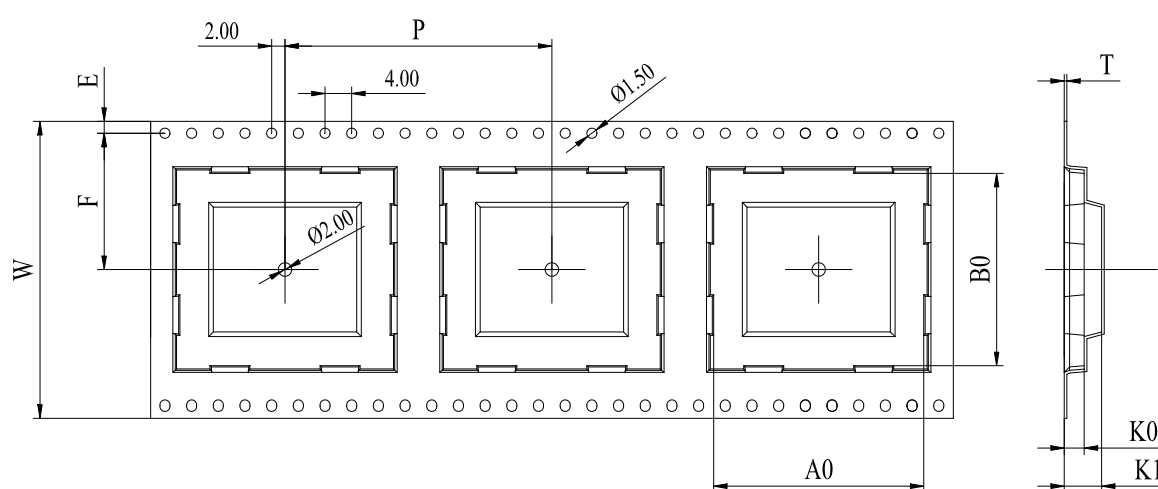


Figure 38: Carrier Tape Dimension Drawing (Unit: mm)

Table 42: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	4.6	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

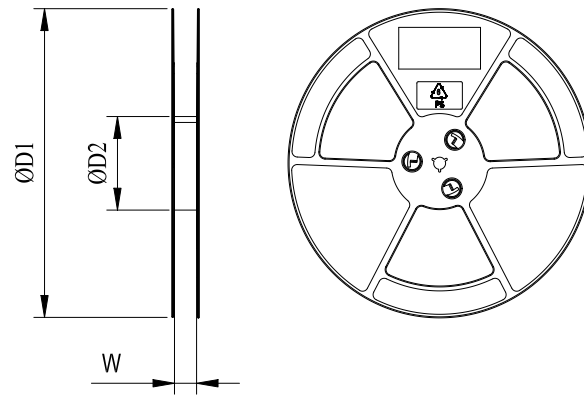


Figure 39: Plastic Reel Dimension Drawing

Table 43: Plastic Reel Dimension Table (Unit: mm)

ØD1	ØD2	W
330	100	32.5

8.3.3. Mounting Direction

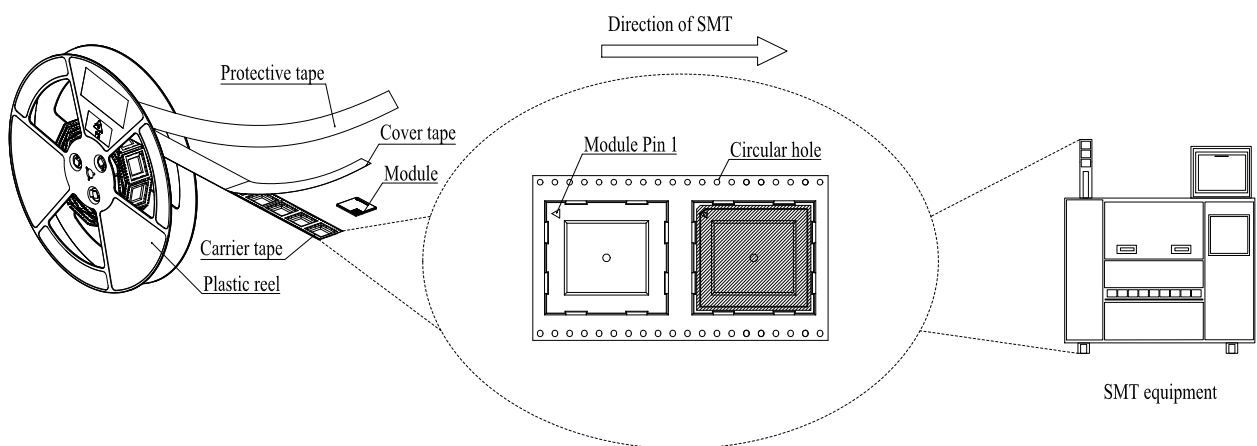
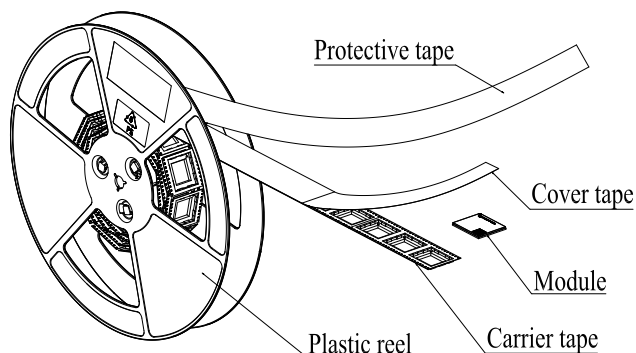


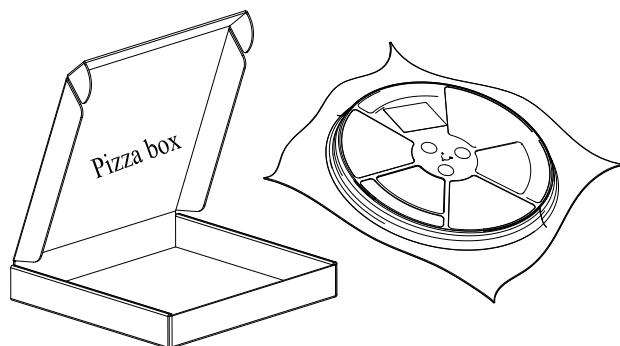
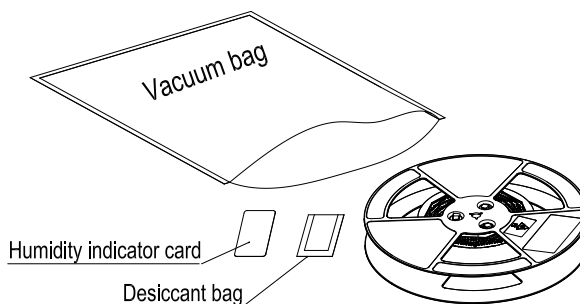
Figure 40: Mounting Direction

8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

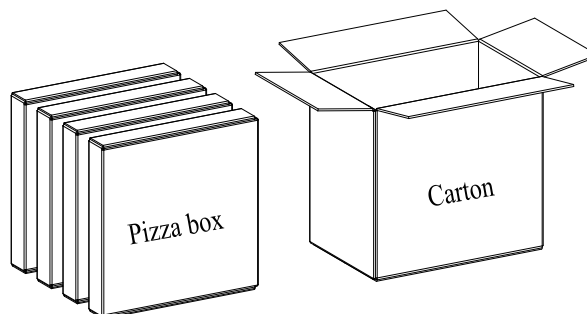


Figure 41: Packaging Process

9 Appendix References

Table 44: Related Documents

Document Name
[1] Quectel_EG800Z_Series_Low_Power_Mode_Application_Note
[2] Quectel_EG800Z_Series_AT_Commands_Manual
[3] Quectel_UMTS<E_EVB_User_Guide
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Stencil_Design_Requirements
[6] Quectel_Module_SMT_Application_Note

Table 45: Terms and Abbreviations

Abbreviation	Description
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CTS	Clear To Send
DRX	Discontinuous Reception
DSSS	Direct Sequence Spread Spectrum
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol

FTP	File Transfer Protocol
FTPS	FTP over SSL
GND	Ground
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMS	Short Message Service

SSL	Secure Sockets Layer
TAU	Tracking Area Update
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
V _{max}	Maximum Voltage
V _{nom}	Nominal Voltage
V _{min}	Minimum Voltage
VSWR	Voltage Standing Wave Ratio

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID XMR2025EG800ZLA procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: XMR2025EG800ZLA”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

- (1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
- (2) The transmitter module may not be co-located with any other transmitter or antenna.
- (3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Gain	LTE Band 2: 1.59dBi LTE Band 4: 2.00dBi LTE Band 5: 2.13dBi LTE Band 7: 3.00dBi LTE Band 38: 2.06dBi LTE Band 66: 2.00dBi
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In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Statement (FCC, US)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference
- (2) this device must accept any interference received, including interference that may cause undesired operation.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.209

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 3.00dBi antenna. The host manufacturer installing this module into their product must ensure that the final product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

2.4 Limited module procedures

Not applicable. The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable. The module has its own antenna, and doesn't need a host's printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and user's body; and if RF exposure statement or module layout is changed, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: External Antenna

Gain: 3.00 dBi Max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a "unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2025EG800ZLA " with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.209 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.