

FCM363X Hardware Design

Short-Range Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-11-11	Arrow HUANG/ Yuan ZHANG/ Andrew XIE	Creation of the document
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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the FCM363X and describes its hardware interfaces and air interfaces which are connected with your applications. With this document, you can quickly understand module interface specifications, RF performances, electrical and mechanical details, as well as other related information of the module.

Hereby, Quectel Wireless Solutions Co., Ltd. declares that the radio equipment type FCM363X is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address:
<http://www.quectel.com/support/technical.htm>

Disposal of old electrical appliances



The European directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), requires that old household electrical appliances must not be disposed of in the normal unsorted municipal waste stream. Old appliances must be collected separately in order to optimize the recovery and recycling of the materials they contain, and reduce the impact on human health and the environment.

The crossed out “wheeled bin” symbol on the product reminds you of your obligation, that when you dispose of the appliance, it must be separately collected.

Consumers should contact their local authority or retailer for information concerning the correct disposal of their old appliance.

	AT	BE	BG	HR	CY	CZ	DK
	EE	FI	FR	DE	EL	HU	IE
	IT	LV	LT	LU	MT	NL	PL
	PT	RO	SK	SI	ES	SE	UK(NI)

This equipment should be installed and operated with minimum distance 20cm between the radiator and your body. The device is restricted to indoor use only when operating in the 5150 to 5350 MHz frequency range.

FCC ID: XMR2025FCM363X

IC: 10224A-2025FCM363X



1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[...]	Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

FCM363X is a low-power and high-performance Wi-Fi and Bluetooth Combo module supporting IEEE 802.11a/b/g/n/ac/ax and BLE 5.4 protocols. The module provides multiple interfaces including SDIO, UART, SPI*, PCM*, I2C*, I2S*, PWM*, ADC*, DAC*, USB, JTAG/SWD*, LCD*, DMIC*, ACOMP*, UTICK*, (U)SIM*, WCI-2*, and PTA* for various applications.

It is an SMD module with compact packaging which includes:

- 260 MHz ARM Cortex-M33 with TrustZone-M
- CoreMark® score: 1033; 3.97 CoreMark/MHz
- Built-in 8 MB Flash, 1.2 MB integrated SRAM, 8 MB optional PSRAM
- FlexSPI external flash interface supports eXecute-In-Place (XIP) and on-the-fly firmware encryption/decryption and authentication
- FlexSPI external flash interface supports up to 128 MB.
- Support for secondary development

Table 2: Basic Information

FCM363X	
Packaging type	LCC + LGA
Pin counts	73
Dimensions	(25.5 ±0.2) mm × (18 ±0.2) mm × (3.16 ±0.2) mm
Weight	Approx. 1.51 g

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocols and Standard	● Wi-Fi Protocols: IEEE 802.11a/b/g/n/ac/ax ● Bluetooth protocol: BLE 5.4 ● All hardware components are fully compliant with EU RoHS directive
Supply Voltage	VBAT Power Supply: ● 3.14–3.46 V ● Typ.: 3.3 V
Temperature Ranges	● Normal operating temperature ¹: -40 °C to +85 °C ● Storage temperature: -45 °C to +95 °C
TE-B Kit	FCM363X-TE-B ²
Antenna/Antenna Interface ³	
Antenna/Antenna Interfaces	● PCB antenna ● RF coaxial connector ● 50 Ω characteristic impedance
Application Interface ⁴	
Application Interfaces	SDIO, UART, SPI*, PCM*, I2C*, I2S*, PWM*, ADC*, DAC*, USB, JTAG/SWD*, LCD*, DMIC*, ACOMP*, UTICK*, (U)SIM*, WCI-2*, and PTA*

¹ Within this range, the module's indicators comply with IEEE and Bluetooth specification requirements.

² For more details about the TE-B, see **document [1]**.

³ The module is provided with one of the two antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

⁴ For more details about the interfaces, see **Chapter 3.3** and **Chapter 3.4**.

3 Application Interfaces

3.1. Pin Assignment

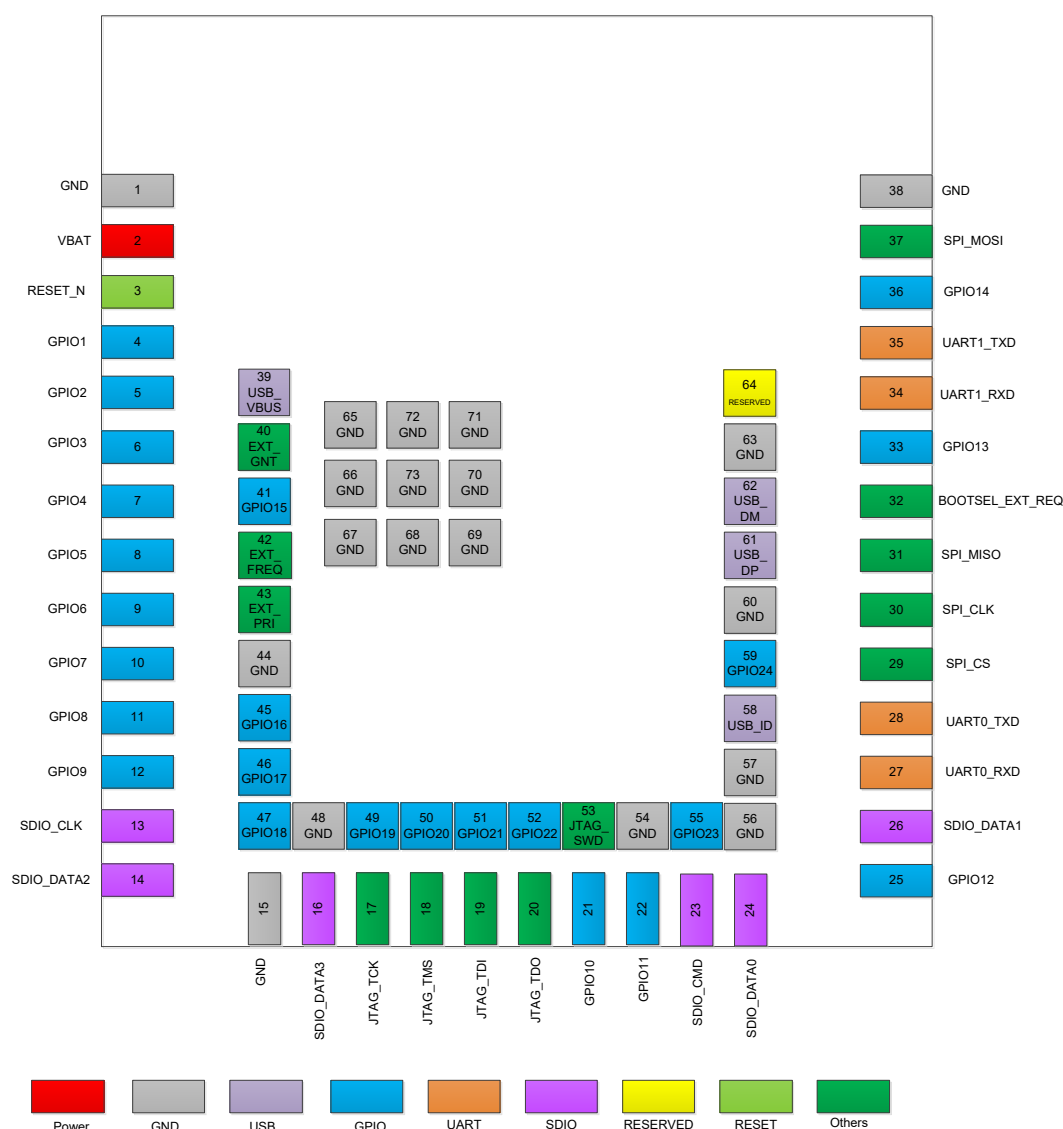


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. All GND pins should be connected to ground.
3. Ensure that there is no current sink on the module's pins before the module turns on.
4. The module has SDIO, UART, SPI*, USB, JTAG, and 24 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including PCM*, I2C*, I2S*, PWM*, ADC*, DAC*, SWD*, LCD*, DMIC*, ACOMP*, UTICK*, (U)SIM*, WCI-2*, and PTA*. For more details, see **Chapter 3.3** and **Chapter 3.4**.

3.2. Pin Definitions

Table 4: Parameter Definition

Parameter	Description
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PU	Pull-up
Hi-Z	High Impedence
H	High Level

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply and GND Pins						
Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
VBAT	2	PI	-	Power supply for	Vmin = 3.14 V	It is

				the module	Vnom = 3.3 V Vmax = 3.46 V	recommended to be provided with sufficient current of at least 0.6 A.
--	--	--	--	------------	-------------------------------	---

GND 1, 15, 38, 44, 48, 54, 56, 57, 60, 63, 65–73

Reset

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
RESET_N	3	DI	PU	Reset the module	VBAT	Active low. A test point is recommended to be reserved if unused.

UART Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
UART0_TXD	28	DO	PU	UART0 transmit	VBAT	
UART0_RXD	27	DI	PU	UART0 receive		
UART1_TXD	35	DO	PU	UART1 transmit		
UART1_RXD	34	DI	PU	UART1 receive		

USB Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USB_DP	61	AIO	TBD	USB 2.0 differential data (+)		Require differential impedance of 90 Ω.
USB_DM	62	AIO	TBD	USB 2.0 differential data (-)		USB 2.0 compliant. Test points must be reserved.
USB_VBUS	39	AIO	TBD	VBUS selection	4.75–5.25 V	5 V analog power supply.
USB_ID	58	AI	TBD	USB ID detect		

GPIO Interfaces

Pin Name	Pin	I/O	Status After	Description	DC	Comment
----------	-----	-----	--------------	-------------	----	---------

	No.	Reset		Characteristics		
GPIO1	4	DIO	Hi-Z	General-purpose input/output	VBAT	
GPIO2	5	DIO	Hi-Z	General-purpose input/output		
GPIO3	6	DIO	Hi-Z	General-purpose input/output		
GPIO4	7	DIO	Hi-Z	General-purpose input/output		
GPIO5	8	DIO	Hi-Z	General-purpose input/output		
GPIO6	9	DIO	Hi-Z	General-purpose input/output		
GPIO7	10	DIO	Hi-Z	General-purpose input/output		
GPIO8	11	DIO	Hi-Z	General-purpose input/output		
GPIO9	12	DIO	Hi-Z	General-purpose input/output		SDIO interrupt output (optional).
GPIO10	21	DIO	Hi-Z	General-purpose input/output		
GPIO11	22	DIO	Hi-Z	General-purpose input/output		Always on wake-up input signal pin (optional).
GPIO12	25	DIO	Hi-Z	General-purpose input/output		
GPIO13	33	DIO	Hi-Z	General-purpose input/output		
GPIO14	36	DIO	Hi-Z	General-purpose input/output		
GPIO15	41	DIO	Hi-Z	General-purpose input/output		
GPIO16	45	DIO	Hi-Z	General-purpose input/output		
GPIO17	46	DIO	Hi-Z	General-purpose input/output		
GPIO18	47	DIO	Hi-Z	General-purpose input/output		
GPIO19	49	DIO	Hi-Z	General-purpose input/output		
GPIO20	50	DIO	Hi-Z	General-purpose		

				input/output		
GPIO21	51	DIO	Hi-Z	General-purpose input/output		
GPIO22	52	DIO	Hi-Z	General-purpose input/output		
GPIO23	55	DIO	Hi-Z	General-purpose input/output		
GPIO24	59	DIO	Hi-Z	General-purpose input/output		

SDIO Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
SDIO_DATA0	24	DIO	Hi-Z	SDIO data bit 0	VBAT	
SDIO_DATA1	26	DIO	Hi-Z	SDIO data bit 1		
SDIO_DATA2	14	DIO	Hi-Z	SDIO data bit 2		
SDIO_DATA3	16	DIO	Hi-Z	SDIO data bit 3		
SDIO_CLK	13	DI	Hi-Z	SDIO clock		
SDIO_CMD	23	DIO	Hi-Z	SDIO command		

SPI Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
SPI_CS	29	DO	Hi-Z	SPI chip select	VBAT	
SPI_CLK	30	DO	Hi-Z	SPI clock		
SPI_MISO	31	DI	Hi-Z	SPI master-in slave-out		
SPI_MOSI	37	DO	Hi-Z	SPI master-out slave-in		

Other Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
JTAG_TCK	17	DI	Hi-Z	JTAG test clock	VBAT	
JTAG_TMS	18	DI	Hi-Z	JTAG test mode select		

JTAG_TDI	19	DI	Hi-Z	JTAG test data input		
JTAG_TDO	20	DO	Hi-Z	JTAG test data output		
JTAG_SWD	53	DI	Hi-Z	JTAG or SWD switching	VBAT	When the level is kept high, the module download debug interface is JTAG; when the level is kept low, the module download debug interface is SWD. High level by default.
BOOTSEL_EXT_REQ	32	DI	H	Boot mode selection; external radio coexistence request	1.71–1.89 V	High level by default. Pull it down to enter ISP boot mode and re-program Flash through UART/I2C*/SPI*/USB.
EXT_GNT	40	DO	H	External radio coexistence output		
EXT_FREQ	42	DI	H	External radio coexistence input	1.71–1.89 V	
EXT_PRI	43	DI	H	External radio input priority		
RESERVED Pin						
Pin Name	Pin No.		Comment			
RESERVED	64		Keep it open.			

3.3. GPIO Multiplexing

The module has SDIO, UART, SPI*, USB, JTAG, and 24 GPIO interfaces by default, and can support up to 42 GPIO interfaces in the case of multiplexing. Pins are defined as follows:

Table 6: GPIO Multiplexing

Pin Name	Pin No.	Alternate Function 0 (GPIO No.)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	Alternate Function 6	Alternate Function 7
SPI_CS	29	GPIO[0]	USART0_CTS	-	-	SPI0_CS	-	-	CT_INP0
GPIO17	46	GPIO[1]	-	-	-	-	-	-	CT_INP1
SPI_MOSI	37	GPIO[2]	USART0_RXD	I2C0_SDA	I2S0_SDA	SPI0_MOSI	PCM_DOUT/DIN	-	-
SPI_MISO	31	GPIO[3]	USART0_TXD	I2C0_SCL	I2S0_WS	MISO	PCM_SYNC	PWM0	-
SPI_CLK	30	GPIO[4]	USART0_SCK	EXT_STATE	I2S0_SCK	SCK	PCM_CLK	PWM1	WCI-2_SIN
GPIO13	33	GPIO[5]	USART0_RTS	-	-	-	MCLK	-	-
JTAG_TCK	17	GPIO[6]	USART1_CTS	-	-	SPI1_CS	-	-	-
JTAG_TMS	18	GPIO[7]	USART1_SCK	-	I2S1_SCK	SPI1_SCK	PCM_CLK	-	-
JTAG_TDI	19	GPIO[8]	USART1_TXD	I2C1_SCL	I2S1_WS	SPI1_MISO	PCM_SYNC	-	-
JTAG_TDO	20	GPIO[9]	USART1_RXD	I2C1_SDA	I2S1_SDA	SPI1_MOSI	PCM_DOUT/DIN	-	-
GPIO10	21	GPIO[10]	USART1_RTS	JTAG_SRST	-	-	-	-	-
GPIO18	47	GPIO[11]	-	-	-	-	-	PWM8	-
GPIO9	12	GPIO[12]	SD_HOST_INT	-	-	-	-	-	CT_INP2
UART0_RXD	27	GPIO[13]	USART2_RXD	I2C2_SDA	I2S2_SDA	SPI2_MOSI	PCM_DOUT/DIN	SWCLK	CT_INP3
UART0_TXD	28	GPIO[14]	USART2_TXD	I2C2_SCL	I2S2_WS	SPI2_MISO	PCM_SYNC	SWDIO	CT_INP4
SDIO_CLK	13	GPIO[15]	USART2_SCK	-	I2S2_SCK	SPI2_SCK	PCM_CLK	UCLK	UTICK_CAP0
SDIO_DATA3	16	GPIO[16]	USART2_CTS	I2C2_COPY_SDA	-	SPI2_CS	-	URST	UTICK_CAP1
SDIO_CMD	23	GPIO[17]	USART2_RTS	I2C2_COPY_SCL	-	-	-	UIO	UTICK_CAP2
SDIO_DATA2	14	GPIO[18]	-	-	-	-	-	-	UTICK_CAP3

SDIO_DATA0	24	GPIO[19]	USART3_RTS	I2C3_COPY_SCL	-	-	-	-	-
SDIO_DATA1	26	GPIO[20]	USART3_CTS	I2C3_COPY_SDA	-	SPI3_CS	-	-	-
GPIO19	49	GPIO[21]	-	-	-	-	-	-	CT_INP5
GPIO23	55	GPIO[22]	SLP_CLK_32K	AON_XTAL32K_IN	-	-	-	-	-
UART1_RXD	34	GPIO[24]	USART3_RXD	I2C3_SDA	I2S3_SDA	SPI3_MOSI	PCM_DOUT/DIN	-	CT_INP6
GPIO11	22	GPIO[25]	USART3_SCK		I2S3_SCK	SPI3_SCK	PCM_CLK	-	-
UART1_TXD	35	GPIO[26]	USART3_TXD	I2C3_SCL	I2S3_WS	SPI3_MISO	PCM_SYNC	PWM4	-
GPIO15	41	GPIO[27]	-	-	-	-	-	PWM5	CT_INP7
GPIO12	25	GPIO[29]	-	-	-	-	-	-	-
GPIO24	59	GPIO[42]	-		ADC0	ACOMP0	-	-	-
GPIO14	36	GPIO[43]	-	DAC_B	ADC1	ACOMP1	-	-	-
GPIO1	4	GPIO[44]	LCD_RESETN	DAC_A	ADC2	ACOMP2	-	-	-
GPIO2	5	GPIO[45]	LCD_TE	EXT_VREF_DAC	ADC3	ACOMP3	-	-	-
GPIO3	6	GPIO[46]	LCD_SPI_DATA	-	ADC4	ACOMP4	-	-	-
GPIO4	7	GPIO[47]	LCD_SPI_DC	-	ADC5	ACOMP5	-	-	-
GPIO5	8	GPIO[48]	LCD_SPI_SCK	-	ADC6	ACOMP6	-	-	-
GPIO6	9	GPIO[49]	LCD_SPI_SS	-	ADC7	ACOMP7	-	-	-
GPIO7	10	GPIO[50]	-	DAC_TRIGGER0	-	-	-	-	-
GPIO21	51	GPIO[51]	PDM_DATA01	-	-	ACOMP0_GPIO_OUT	-	-	CT_INP11
GPIO16	45	GPIO[52]	PDM_DATA23	-	-	ACOMP0_EDGE_PULSE	-	-	CT_INP12
GPIO20	50	GPIO[53]	PDM_CLK01	-	-	ACOMP1_GPIO_OUT	-	-	CT_INP13
GPIO22	52	GPIO[54]	PDM_CLK23	-	-	ACOMP1_EDGE_PULSE	-	-	CT_INP14
GPIO8	11	GPIO[55]	-	DAC_TRIGGER1	-	-	-	PWM9	-

NOTE

1. All GPIO supports wakeup.
2. After the module is powered off, all of its GPIOs must be driven low. Otherwise, the current leakage may make the module enter an abnormal state.
3. The maximum number of each application interface multiplexed with GPIOs is not available simultaneously. For more details, see **Chapter 3.4**.

3.4. Interface Definition

3.4.1. SDIO Interface

The module has one SDIO interface by default which complies with SDIO 3.0 specification. The interface supports slave mode with maximum clock rate of up to 208 MHz, 1-bit (by default) and 4-bit data bus modes.

Table 7: Pin Description of SDIO Interface

Pin Name	Pin No.	I/O	Description
SDIO_DATA0	24	DIO	SDIO data bit 0
SDIO_DATA1	26	DIO	SDIO data bit 1
SDIO_DATA2	14	DIO	SDIO data bit 2
SDIO_DATA3	16	DIO	SDIO data bit 3
SDIO_CLK	13	DI	SDIO clock
SDIO_CMD	23	DIO	SDIO command

The SDIO interface connection between the module and the host is shown below:

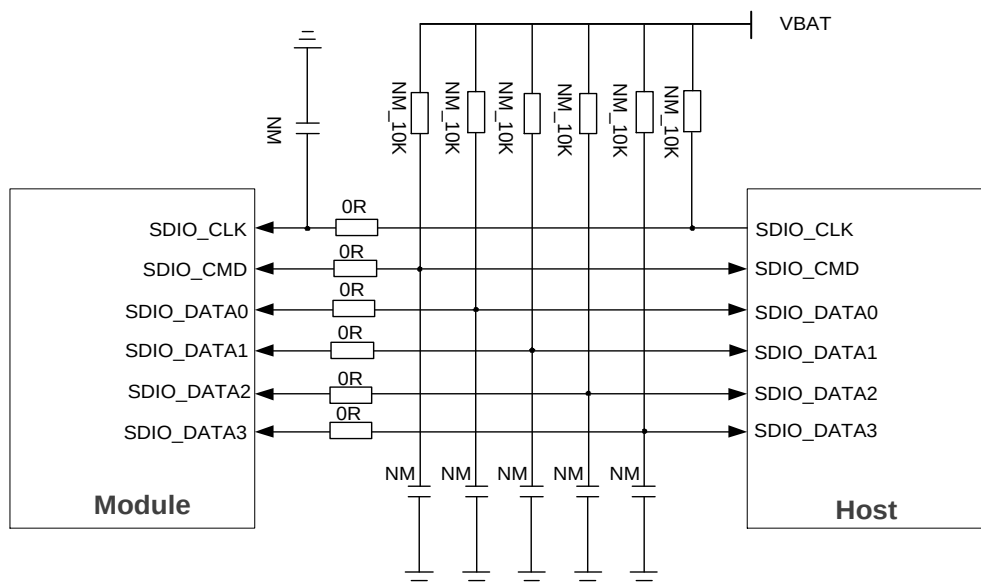


Figure 2: SDIO Interface Connection

To ensure communication performance, the following conditions should be taken into considerations when designing SDIO interface:

- To minimize bus jitter, reserve 10–100 k Ω pull-up resistors (with a recommended value of 10 k Ω) on the SDIO_CMD, SDIO_DATA[0:3], and SDIO_CLK signal traces and pull them up to VBAT of the module.
- Route SDIO signal traces at the inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. The impedance of SDIO signal trace is 50 $\Omega \pm 10\%$. And the SDIO_CLK signal trace should be routed with ground surrounded separately.
- Keep SDIO signal traces far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clock and DC-DC.
- SDIO_CLK, SDIO_DATA[0:3], and SDIO_CMD signal traces need to be of equal length (the distance between the traces should be less than 2.54 mm). Route SDIO traces on the same layer of the PCB as much as possible, keeping them parallel and ensuring that there are enough ground vias around the SDIO traces and connecting them to a ground plane.
- The total trace length inside the module is 16.16 mm. According to the transmission mode, the exterior total trace length should follow the following rules:
 - 1) SDR104 mode: the recommended total trace length is less than 50 mm;
 - 2) Other modes (such as DDR50 and SDR50): the recommended total trace length is less than 150 mm.
- Keep the adjacent trace clearance twice the trace width and the load capacitance of SDIO bus less than 15 pF.

3.4.2. UART Interfaces

The module supports two UART interfaces (UART0 and UART1) by default. In the case of multiplexing, it can support up to four UART interfaces (USART0, USART1, USART2, and USART3).

Table 8: Pin Description of UART Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
UART0_TXD	28	USART2_TXD	DO	USART2 transmit	Other UART configurations, see Table 6 .
UART0_RXD	27	USART2_RXD	DI	USART2 receive	
UART1_TXD	35	USART3_TXD	DO	USART3 transmit	
UART1_RXD	34	USART3_RXD	DI	USART3 receive	
SPI_MISO	31	USART0_TXD	DO	USART0 transmit	
SPI_MOSI	37	USART0_RXD	DI	USART0 receive	

JTAG_TDI	19	USART1_TXD	DO	USART1 transmit
JTAG_TDO	20	USART1_RXD	DI	USART1 receive

UART0 can be used for AT command communication and data transmission. The default baud rate is 115200 bps.

The UART connection between the module and MCU is illustrated below.

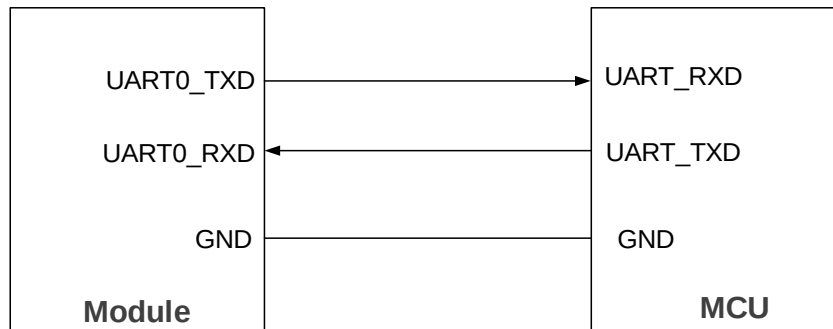


Figure 3: UART0 Interface Connection

UART1 supports 115200 bps baud rate by default, and is used for outputting partial logs with debugging tools. The following is a reference design of debug UART1.

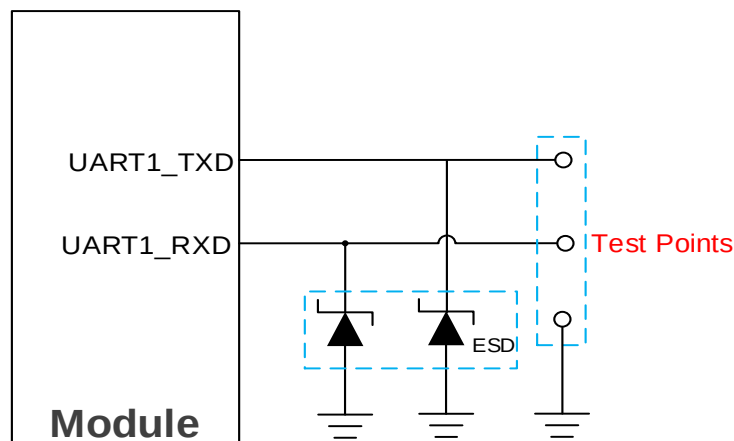


Figure 4: UART1 Interface Reference Design

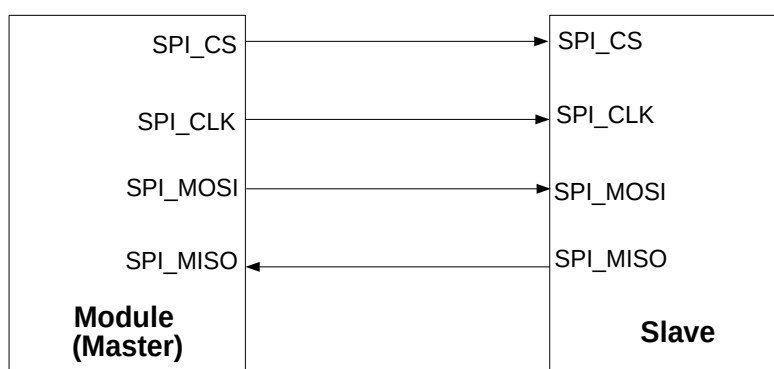
3.4.3. SPI Interface*

The module provides one SPI interface which only supports master mode with a maximum clock frequency of up to 30 MHz.

Table 9: Pin Description of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	29	DO	SPI chip select	Other SPI configurations, see Table 6 .
SPI_CLK	30	DO	SPI clock	
SPI_MISO	31	DI	SPI master-in slave-out	
SPI_MOSI	37	DO	SPI master-out slave-in	

The following figure shows the connection between the host and the slave:


Figure 5: SPI Interface Connection

3.4.4. PCM Interface*

The PCM function is implemented through two I2S plus MCLK combinations, one I2S is set to PCM_DOUT, and the other I2S is set to the peripheral PCM_DIN. The timing specification follows the I2S bus Interface specification.

Table 10: Pin Description of PCM Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
JTAG_TMS	18	I2S1_SCK	DIO	PCM clock	When the module's PCM_SYNC is as central, they are output signals; when as peripheral,
JTAG_TDI	19	I2S1_WS	DIO	PCM data frame sync	

					they are input signals.
JTAG_TDO	20	I2S1_SDA	DIO	PCM data output/input	
SPI_CLK	30	I2S0_SCK	DIO	PCM clock	When the module's PCM_SYNC is as central, they are output signals; when as peripheral, they are input signals.
SPI_MISO	31	I2S0_WS	DIO	PCM data frame sync	
SPI_MOSI	37	I2S0_SDA	DIO	PCM data output/input	
SDIO_CLK	13	I2S2_SCK	DIO	PCM clock	When the module's PCM_SYNC is as central, they are output signals; when as peripheral, they are input signals.
UART0_TXD	28	I2S2_WS	DIO	PCM data frame sync	
UART0_RXD	27	I2S2_SDA	DIO	PCM data output/input	
GPIO11	22	I2S3_SCK	DIO	PCM clock	When the module's PCM_SYNC is as central, they are output signals; when as peripheral, they are input signals.
UART1_TXD	35	I2S3_WS	DIO	PCM data frame sync	
UART1_RXD	34	I2S3_SDA	DIO	PCM data output/input	
GPIO13	33	MCLK	DO	Master clock output for codec	

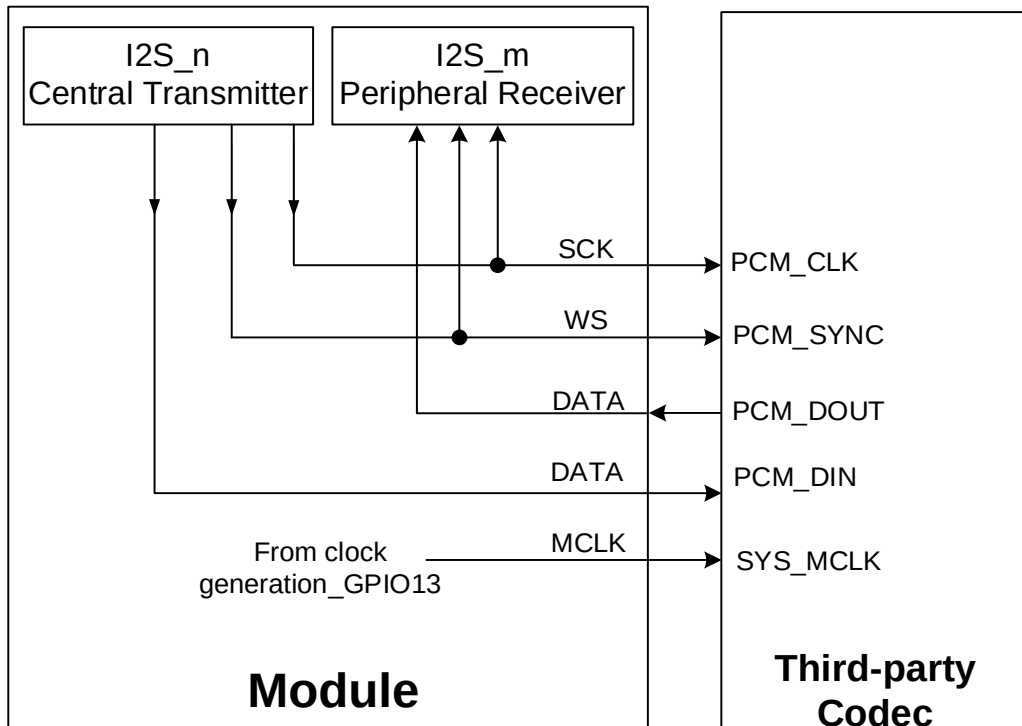


Figure 6: PCM Codec Connection (Module's PCM_SYNC as Central)

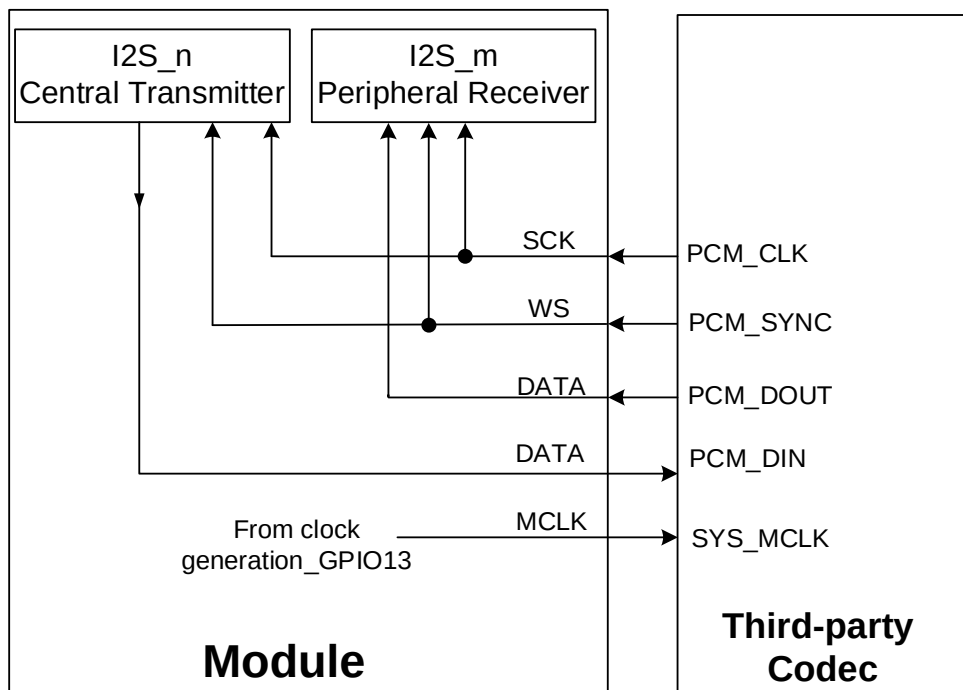


Figure 7: PCM Codec Connection (Module's PCM_SYNC as Peripheral)

3.4.5. I2C Interface*

In the case of multiplexing, the module provides up to four I2C interfaces that support both master and slave modes. It supports:

- AMBA 2.0 APB bus protocol
- Standard-speed mode (100 kbps), high-speed mode (400 kbps) and fast-speed mode (3400 kbps) protocols
- Programmable master and slave modes
- 7-bit and 10-bit addressing modes
- Programmable clock and data timing
- DMA
- Universal call address

Table 11: Pin Description of I2C Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
SPI_MISO	31	I2C0_SCL	OD	I2C0 serial clock
SPI_MOSI	37	I2C0_SDA	OD	I2C0 serial data
JTAG_TDI	19	I2C1_SCL	OD	I2C1 serial clock
JTAG_TDO	20	I2C1_SDA	OD	I2C1 serial data
UART1_TXD	35	I2C3_SCL	OD	I2C3 serial clock
UART1_RXD	34	I2C3_SDA	OD	I2C3 serial data
SDIO_CMD	23	I2C2_COPY_SCL	OD	Backup-I2C2 serial clock
SDIO_DATA3	16	I2C2_COPY_SDA	OD	Backup-I2C2 serial data
SDIO_DATA0	24	I2C3_COPY_SCL	OD	Backup-I2C3 serial clock
SDIO_DATA1	26	I2C3_COPY_SDA	OD	Backup-I2C3 serial data
UART0_TXD	28	I2C2_SCL	OD	I2C2 serial clock
UART0_RXD	27	I2C2_SDA	OD	I2C2 serial data

3.4.6. I2S Interface*

In the case of multiplexing, the module provides four I2S interfaces which supports both master and slave modes with sampling rates from 8 kHz to 384 kHz.

Table 12: Pin Description of I2S Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
SPI_CLK	30	I2S0_SCK	DIO	I2S0 bit clock
SPI_MISO	31	I2S0_WS	DIO	I2S0 word select
SPI_MOSI	37	I2S0_SDA	DIO	I2S0 data
JTAG_TMS	18	I2S1_SCK	DIO	I2S1 bit clock
JTAG_TDI	19	I2S1_WS	DIO	I2S1 word select
JTAG_TDO	20	I2S1_SDA	DIO	I2S1 data
SDIO_CLK	13	I2S2_SCK	DIO	I2S2 bit clock
UART1_TXD	35	I2S3_WS	DIO	I2S3 word select
UART1_RXD	34	I2S3_SDA	DIO	I2S3 data
GPIO11	22	I2S3_SCK	DIO	I2S3 bit clock
UART0_TXD	28	I2S2_WS	DIO	I2S2 word select
UART0_RXD	27	I2S2_SDA	DIO	I2S2 data

3.4.7. PWM Interface*

In the case of multiplexing, the module supports up to six PWM channels.

Table 13: Pin Description of PWM Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
SPI_MISO	31	PWM0	DO	PWM0 out
SPI_CLK	30	PWM1	DO	PWM1 out
GPIO18	47	PWM8	DO	PWM8 out

UART1_TXD	35	PWM4	DO	PWM4 out
GPIO15	41	PWM5	DO	PWM5 out
GPIO8	11	PWM9	DO	PWM9 out

3.4.8. ADC Interface*

In the case of multiplexing, the module provides eight 16-bit ADC interfaces with an internal reference voltage of 1.2 V. In order to improve the accuracy of the ADC interface voltage measurement, the ADC interface needs to be grounded during wiring.

Table 14: Pin Description of ADC Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
GPIO24	59	ADC0	AI	General-purpose ADC0 interface
GPIO14	36	ADC1	AI	General-purpose ADC1 interface
GPIO1	4	ADC2	AI	General-purpose ADC2 interface
GPIO2	5	ADC3	AI	General-purpose ADC3 interface
GPIO3	6	ADC4	AI	General-purpose ADC4 interface
GPIO4	7	ADC5	AI	General-purpose ADC5 interface
GPIO5	8	ADC6	AI	General-purpose ADC6 interface
GPIO6	9	ADC7	AI	General-purpose ADC7 interface

Table 15: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC Input Voltage Range	0	-	1.8	V
ADC Resolution	-	12 or 16	-	bit

NOTE

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC interface when the module is not powered by the VBAT.

3.4.9. DAC Interface*

In the case of multiplexing, the module integrates a register string-based DAC with 10-bit resolution. The DAC includes two channels. Each channel can output a single-ended signal or combine both channels to output a differential signal.

Table 16: Pin Description of DAC Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
GPIO14	36	DAC_B	AO	DAC channel B
GPIO1	4	DAC_A	AO	DAC channel A
GPIO2	5	EXT_VREF_DAC	AI	DAC external voltage reference input
GPIO7	10	DAC_TRIGGER0	DI	Bit 2 of DAC external trigger
GPIO8	11	DAC_TRIGGER1	DI	Bit 3 of DAC external trigger

3.4.10. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface as device which complies with the USB 2.0 specification and supports high-speed (480 Mbps) mode and is backward-compatible with full-speed (12 Mbps) mode.

Table 17: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	61	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω .
USB_DM	62	AIO	USB 2.0 differential data (-)	USB 2.0 compliant. Test points must be reserved.
USB_VBUS	39	AIO	VBUS selection	5 V analog power supply.

USB_ID	58	AI	USB ID detect
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The following figure shows the USB interface connection between the module and the host.

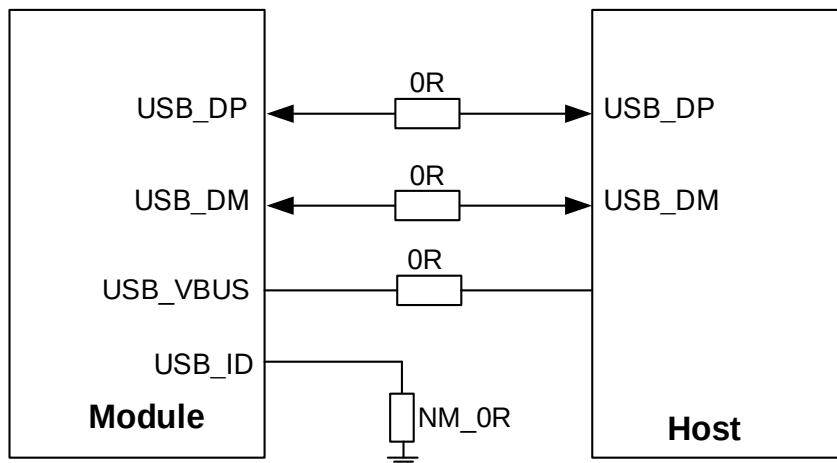


Figure 8: USB Interface Connection

When designing the USB interface, you should follow the following principles to meet USB 2.0 specifications.

- Route the USB signal traces as differential pairs with ground on the same layer and with ground planes above and below. The differential impedance of USB 2.0 is $90\ \Omega \pm 10\%$.
- Do not route signal traces under crystals, oscillators, magnetic devices, sensitive circuits/signals, such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- Reserve a $0\ \Omega$ resistor on USB_DP and USB_DM traces respectively if possible.

For more details about the USB 2.0 specifications, visit <http://www.usb.org/home>.

3.4.11. JTAG Interface

The module provides a set of JTAG Interface for downloading and debugging. Keep JTAG_SWD at high level, the downloading and debugging interface is JTAG. JTAG_SWD is active high by default.

Table 18: Pin Description of JTAG Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
JTAG_TCK	17	-	DI	JTAG test clock	
JTAG_TMS	18	-	DI	JTAG test mode select	
JTAG_TDI	19	-	DI	JTAG test data input	
JTAG_TDO	20	-	DO	JTAG test data output	
GPIO10	21	JTAG_SRST	DI	JTAG test reset	Optional.

3.4.12. SWD Interface*

The module supports 2-line Serial Wire Debug interface (SWD). Keep JTAG_SWD at low level, the downloading and debugging interface is SWD.

Table 19: Pin Description of SWD Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
UART0_RXD	27	SWCLK	DI	Serial wire clock input
UART0_TXD	28	SWDIO	DIO	Serial wire debug data input/output

3.4.13. LCD Interface*

In the case of multiplexing, the module provides a set of LCD SPI Interface.

Table 20: Pin Description of LCD Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
GPIO1	4	LCD_RESETN	DO	LCD output signal to reset the device
GPIO2	5	LCD_TE	DI	LCD tearing effect
GPIO3	6	LCD_SPI_DATA	DIO	LCD SPI data
GPIO4	7	LCD_SPI_DC	DO	LCD SPI data/command select
GPIO5	8	LCD_SPI_SCK	DO	LCD SPI clock
GPIO6	9	LCD_SPI_SS	DO	LCD SPI chip select

3.4.14. DMIC Interface*

In the case of multiplexing, the module provides Pulse-density Modulation (PDM) data input for left and/or right channels on one or two buses.

Table 21: Pin Description of DMIC Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
GPIO21	51	PDM_DATA01	DI	PDM data input for DMIC channels 0 and 1
GPIO16	45	PDM_DATA23	DI	PDM data input for DMIC channels 2 and 3
GPIO20	50	PDM_CLK01	DO	PDM clock output for DMIC channels 0 and 1
GPIO22	52	PDM_CLK23	DO	PDM clock output for DMIC channels 2 and 3

3.4.15. ACOMP Interface*

In the case of multiplexing, the module has two analog identical comparators, ACOMP0 and ACOMP1. The comparators are designed to have true rail-to-rail inputs and operate over the full voltage range of the power supply IO voltage. The comparator outputs are latched and can be used as interrupts.

Table 22: Pin Description of ACOMP Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIO21	51	ACOMP0_GPIO_OUT	DO	Analog comparator 0 level output	Other ACOMP configurations, see Table 6.
GPIO16	45	ACOMP0_EDGE_PULSE	DO	Analog comparator 0 edge pulse	
GPIO20	50	ACOMP1_GPIO_OUT	DO	Analog comparator 1 level output	
GPIO22	52	ACOMP1_EDGE_PULSE	DO	Analog comparator 1 edge pulse	

3.4.16. UTICK Interface*

In the case of multiplexing, the module provides four timers.

Table 23: Pin Description of UTICK Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
SDIO_CLK	13	UTICK_CAP0	DI	Micro-tick timer capture input 0
SDIO_DATA3	16	UTICK_CAP1	DI	Micro-tick timer capture input 1
SDIO_CMD	23	UTICK_CAP2	DI	Micro-tick timer capture input 2
SDIO_DATA2	14	UTICK_CAP3	DI	Micro-tick timer capture input 3

3.4.17. (U)SIM Interface*

In the case of multiplexing, the module provides a set of (U)SIM Interface.

Table 24: Pin Description of (U)SIM Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
SDIO_CLK	13	UCLK	DO	(U)SIM clock
SDIO_DATA3	16	URST	DO	(U)SIM reset
SDIO_CMD	23	UIO	DIO	(U)SIM transmit receive

3.4.18. WCI-2 Coexistence Interface*

In the case of multiplexing, the module provides a set of WCI-2 coexistence interface.

Table 25: Pin Description of WCI-2 Coexistence Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
SPI_CLK	30	WCI-2_SIN	DI	External radio coexistence input	
EXT_FREQ	42	-	DO	External radio coexistence output	WCI-2_SOUT

3.4.19. PTA Coexistence Interface*

In the case of multiplexing, the module provides a set of PTA coexistence interface.

Table 26: Pin Description of PTA Coexistence Interface

Pin Name	Pin No.	Alternate Function	I/O	Description
SPI_CLK	30	EXT_STATE	DI	External radio state input (optional)
EXT_FREQ	42	-	DI	External radio coexistence input (optional).
EXT_GNT	40	-	DO	External radio coexistence output (mandatory)
BOOTSEL_EXT_REQ	32	-	DI	External radio coexistence request (mandatory)
EXT_PRI	43	-	DI	External radio input priority (optional)

4 Operating Characteristics

4.1. Power Supply Interface

Table 27: Pin Description of Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	2	PI	Power supply for the module	3.14	3.3	3.46	V
GND	1, 15, 38, 44, 48, 54, 56, 57, 60, 63, 65–73						

4.1.1. Reference Design for Power Supply

The module is powered by VBAT, and it is recommended to use a power supply chip that provides at least 0.6 A to ensure sufficient current. For better power supply performance, it is recommended to parallel a 22 μ F decoupling capacitor, and two filter capacitors (1 μ F and 100 nF) near the module's VBAT pin. And C4 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VBAT reference circuit is shown below:

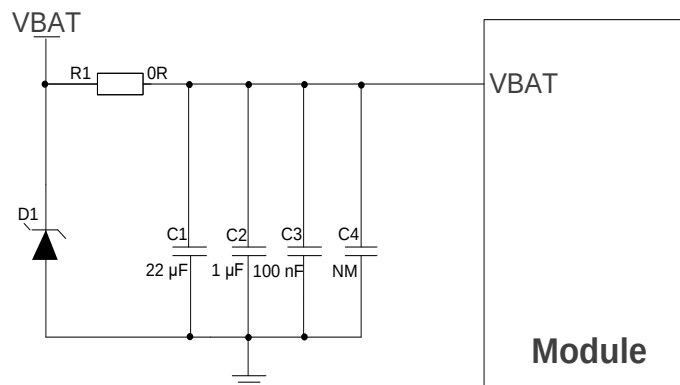


Figure 9: Reference Design of Power Supply

4.2. RESET_N

After the module VBAT is powered on, keep the RESET_N at high level for more than 5 ms to realize the automatic startup of the module; keep the RESET_N at low level to realize the automatic shutdown of the module.

Table 28: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	3	DI	Reset the module	Active low. A test point is recommended to be reserved if unused.

The module turn-on, turn-off and reset timing diagram is as follows:

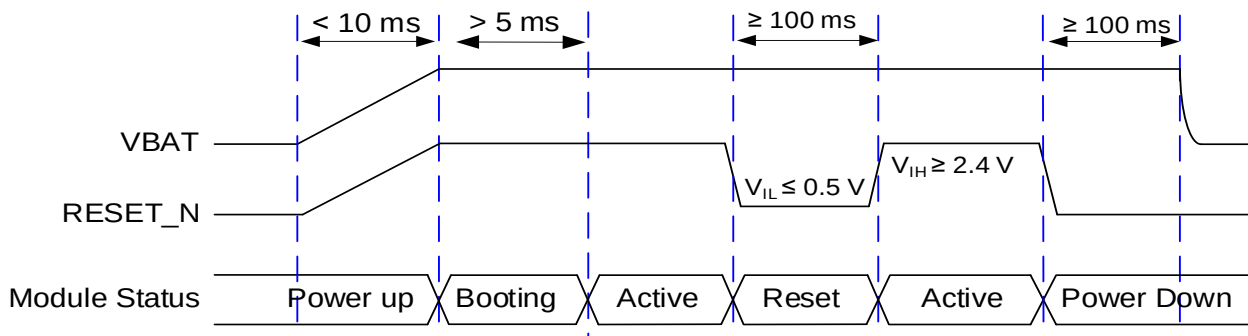


Figure 10: Turn-on/off and Reset Timing Diagram

NOTE

PWRKEY is internally integrated with a 51 kΩ pull-up resistor to VBAT.

4.3. Boot Mode

The module boots from the internal Flash partition by default. When the internal Flash cannot be started normally due to programming errors, you can first pull down the module's BOOTSEL_EXT_REQ pin, and then pull RESET_N down for at least 100 ms before releasing it. This will reset the module and enter ISP boot mode, and re-program Flash through UART*/I2C*/SPI*/USB.

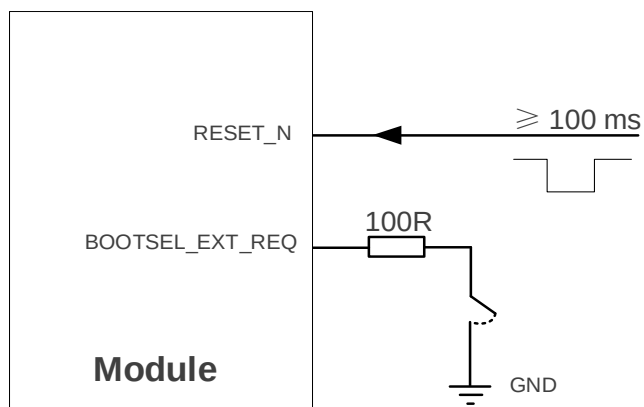


Figure 11: Reference Design for Boot Mode

5 RF Specifications

5.1. Wi-Fi Performances

Table 29: Wi-Fi Performances

Operating Frequency			
2.4 GHz: 2.400–2.4835 GHz 5 GHz: 5.150~5.850 GHz			
Modulation			
DSSS, OFDM, DBPSK, DQPSK, CCK, BPSK, QPSK, 16QAM, 64QAM, 256QAM			
Encryption Mode			
WPA-PSK, WPA2-PSK, WPA3-SAE, AES-128			
Operating Mode			
- AP - STA			
Transmission Data Rate			
802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps 802.11a/g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps 802.11n: HT20 (MCS 0–MCS 7) 802.11ac: VHT20 (MCS 0–MCS 8) 802.11ax: HE20 (MCS 0–MCS 9)			
Condition (VBAT = 3.3 V, Temp.: 25 °C)	EVM	Typ.; Unit: dBm; Tolerance: ±2 dB	
		Transmitting Power	Receiver Sensitivity
2.4 GHz	≤ 35 %	802.11b @ 1 Mbps	19
		802.11b @ 11 Mbps	-96
	≤ -5 dB	802.11g @ 6 Mbps	19
			-87
			-90

5 GHz	802.11g @ 54 Mbps	≤ -25 dB	17	-73
	802.11n, HT20 @ MCS 0, BPSK	≤ -5 dB	18	-90
	802.11n, HT20 @ MCS 7, 64QAM	≤ -27 dB	16	-71
	802.11ax, HE20 @ MCS 0, BPSK	≤ -5 dB	18	-90
	802.11ax, HE20 @ MCS 9, 256QAM	≤ -32 dB	15	-66
	802.11a @ 6 Mbps	≤ -5 dB	18	-90
	802.11a @ 54 Mbps	≤ -25 dB	16	-73
	802.11n, HT20 @ MCS 0, BPSK	≤ -5 dB	18	-90
	802.11n, HT20 @ MCS 7, 64QAM	≤ -27 dB	15.5	-71
	802.11ac, VHT20 @ MCS 0, BPSK	≤ -5 dB	18	-90
	802.11ac, VHT20 @ MCS 8, 256QAM	≤ -30 dB	14.5	-67
	802.11ax, HE20 @ MCS 0, BPSK	≤ -5 dB	18	-88
	802.11ax, HE20 @ MCS 9, 256QAM	≤ -32 dB	13.5	-65

5.2. Bluetooth Performances

Table 30: Bluetooth Performances

Operating Frequency
2.400~2.4835 GHz
Modulation
GFSK
Operating Mode
Bluetooth Low Energy (BLE)

Condition (VBAT = 3.3 V; Temp.: 25 °C)	Unit: dBm; Tolerance: ±3 dB	
	Transmitting Power	Receiver Sensitivity
BLE (1 Mbps)	13	-97
BLE (2 Mbps)	13	-95
BLE (S = 2)	13	-98
BLE (S = 8)	13	-104

5.3. Antenna/Antenna Interfaces ⁵

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module is provided with one of the two antenna/antenna interface designs: PCB antenna and RF coaxial connector. The RF coaxial connector is not soldered when the module is designed with a PCB antenna.

5.3.1. PCB Antenna

Table 31: Requirements for PCB Antenna

Parameter	Requirements
Frequency Range (GHz)	● 2.4 GHz: 2.400–2.500 GHz ● 5 GHz: 5.150–5.850 GHz
Input Impedance (Ω)	50
VSWR	● 2.4 GHz: < 5 ● 5 GHz: < 3.5
Maximum Gain (dBi)	3.1
Average Efficiency	● 2.4 GHz: 45 % ● 5 GHz: 50 %

⁵ The module is provided with one of the two antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

The performance of the PCB antenna depends on the entire product, including the motherboard, case, other RF signals, and it is recommended to verify it at the early stage of design. To ensure the performance and reliability when designed with PCB antenna, follow the basic principles below for module's placement and layout:

- The module should be placed on the edge of the motherboard.
- The PCB antenna should protrude 6.3 mm from the motherboard.
- On the motherboard, ensure a minimum clearance of 16 mm between the PCB antenna and power connectors, Ethernet ports, USB ports, and other large form-factor components (if any).
- If using a plastic case, ensure a minimum clearance of 10 mm between the PCB antenna and the plastic case. If using a metal case, it is recommended to use an external antenna.

NOTE

If any of the above principles cannot be guaranteed, it is advisable to explore alternative antenna solutions for the module or seek assistance from the Quectel Antenna Team, who can offer design assistance and recommend suitable external antennas. Please feel free to contact Quectel Technical Support if necessary.

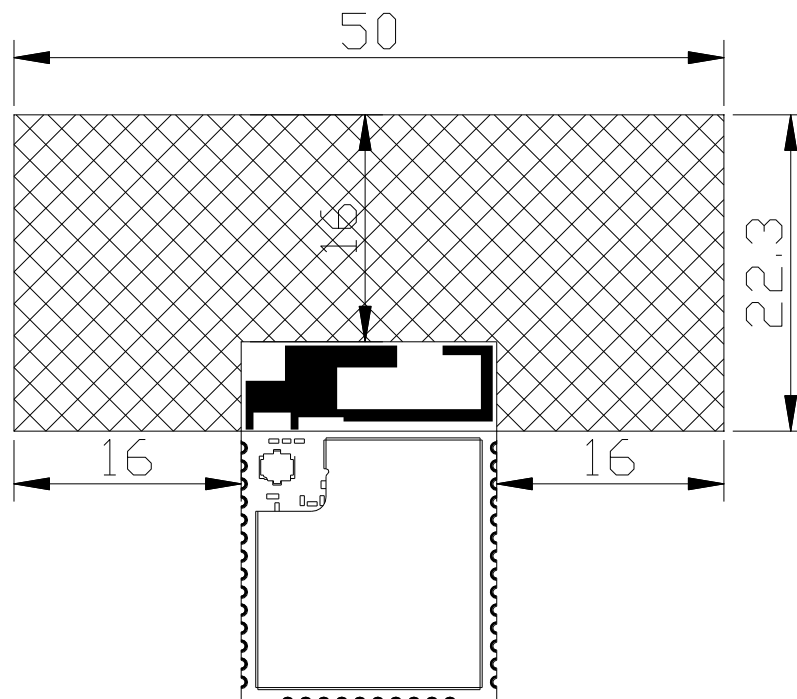


Figure 12: Antenna Area on Motherboard

5.3.2. RF Coaxial Connector

5.3.2.1. Antenna Connector Specifications

The mechanical dimensions of the receptacle supported by the module are as follows.

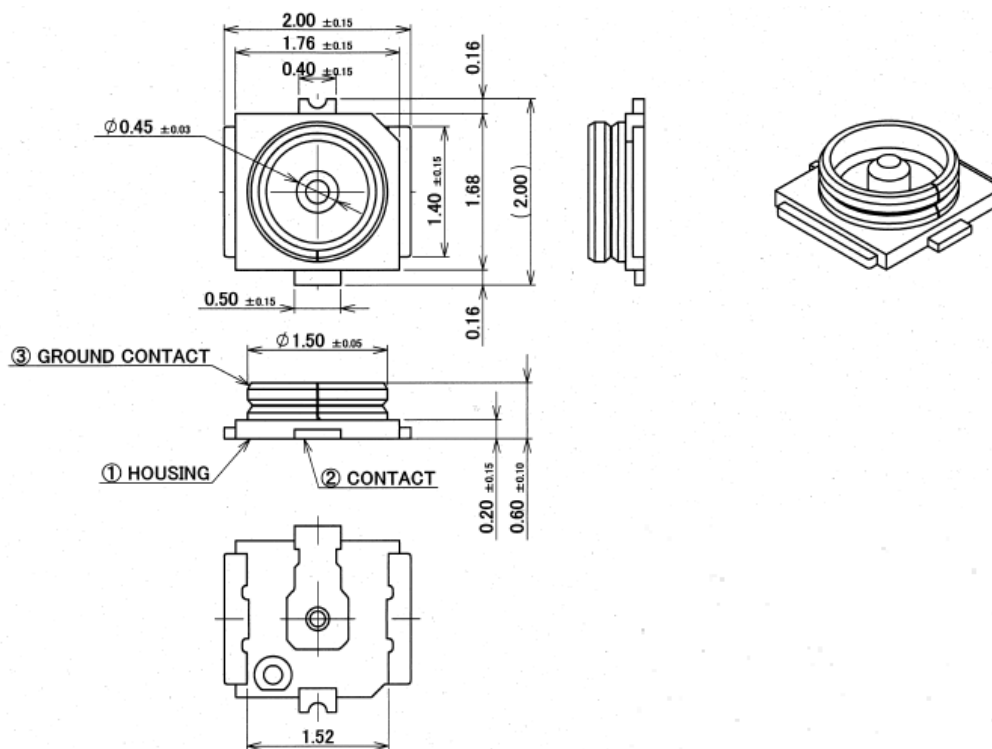


Figure 13: Dimensions of the Receptacle (Unit: mm)

Table 32: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

5.3.2.2. Antenna Connector Installation

The receptacle mounted on the module accepts two types of mated plugs that will meet a maximum height of 1.2 mm using a $\varnothing$ 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a $\varnothing$ 1.13 mm coaxial cable.

The following figure shows the dimensions of mated plugs using $\varnothing$ 0.81 mm/ $\varnothing$ 1.13 mm coaxial cables.

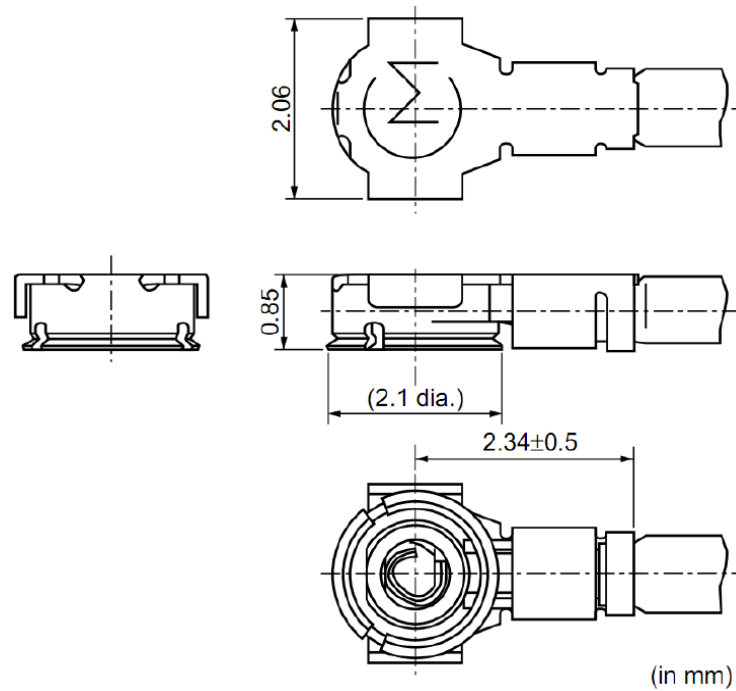


Figure 14: Dimensions of Mated Plugs ($\varnothing$ 0.81 mm/ $\varnothing$ 1.13 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle on the module and the mated plug using a $\varnothing$ 0.81 mm coaxial cable.

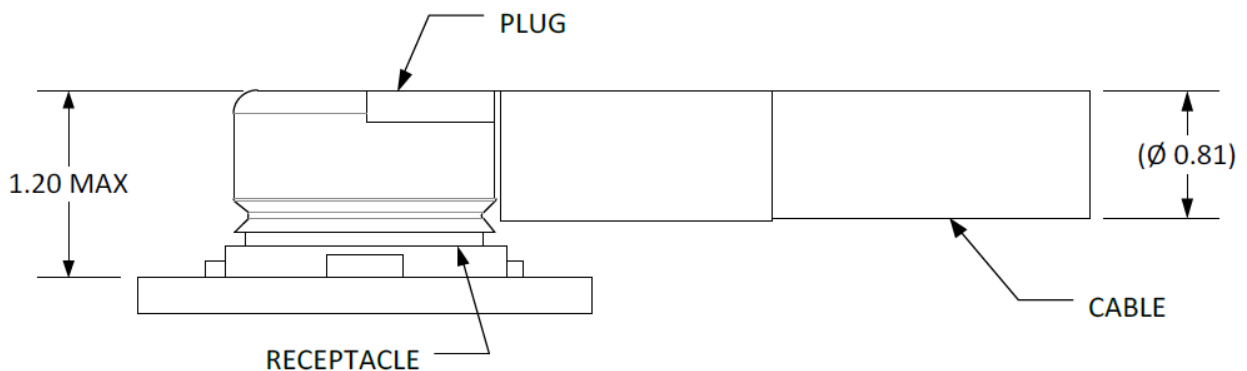


Figure 15: Space Factor of Mated Connectors ($\varnothing$ 0.81 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle mounted on the module and the mated plug using a $\varnothing 1.13$ mm coaxial cable.

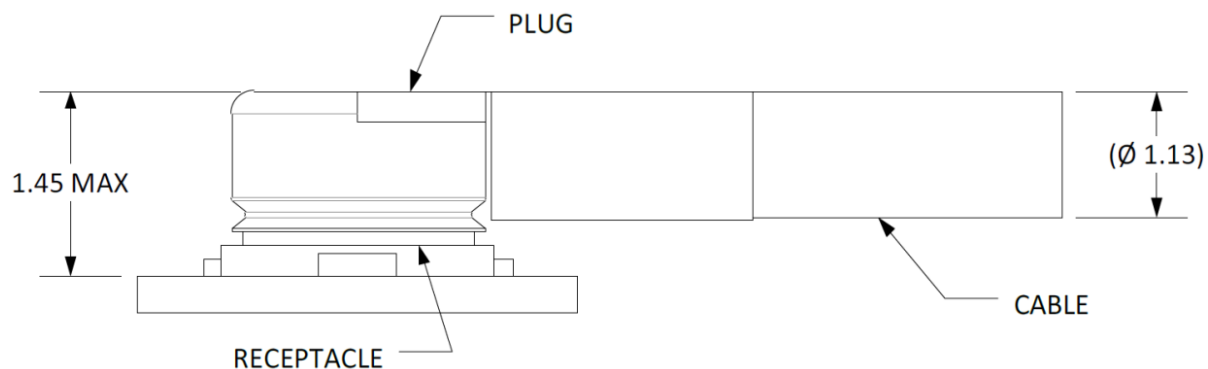


Figure 16: Space Factor of Mated Connectors ($\varnothing 1.13$ mm Coaxial Cables) (Unit: mm)

5.3.2.3. Recommended RF Connector Installation

The pictures for manually plugging in a coaxial cable plug is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

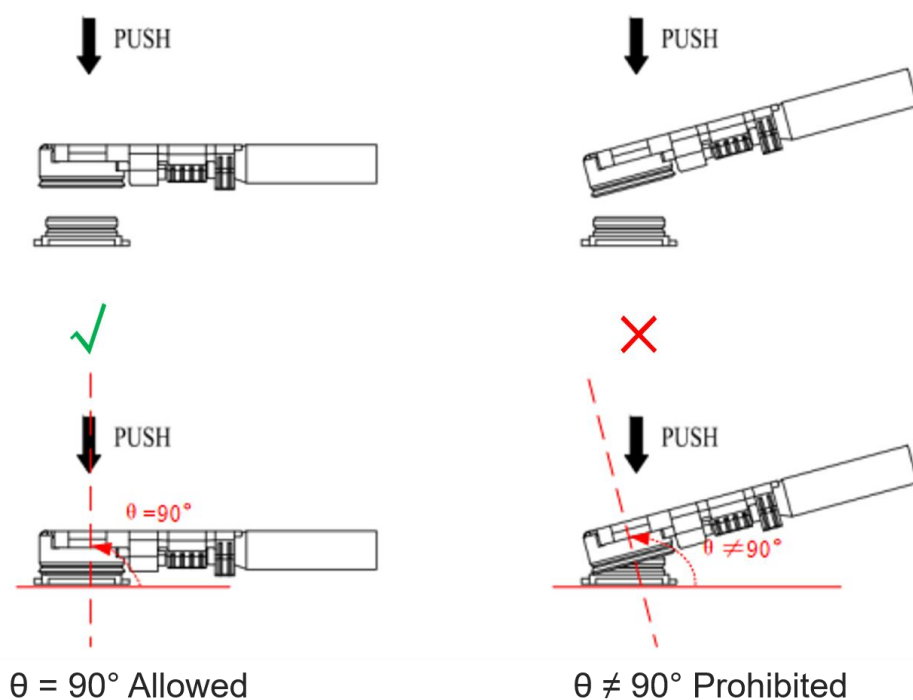


Figure 17: Plug in a Coaxial Cable Plug

The pictures of manually pulling out the coaxial cable plug is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

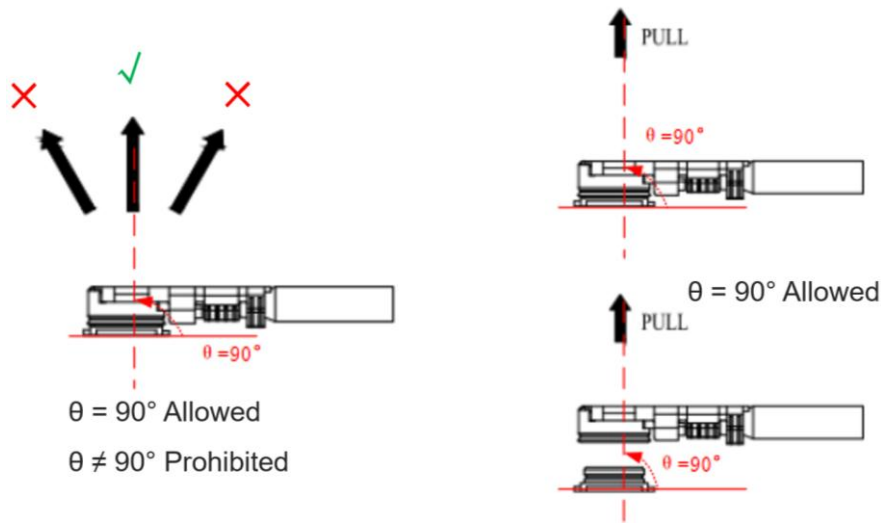


Figure 18: Pull out a Coaxial Cable Plug

The pictures of installing the coaxial cable plug with a jig is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

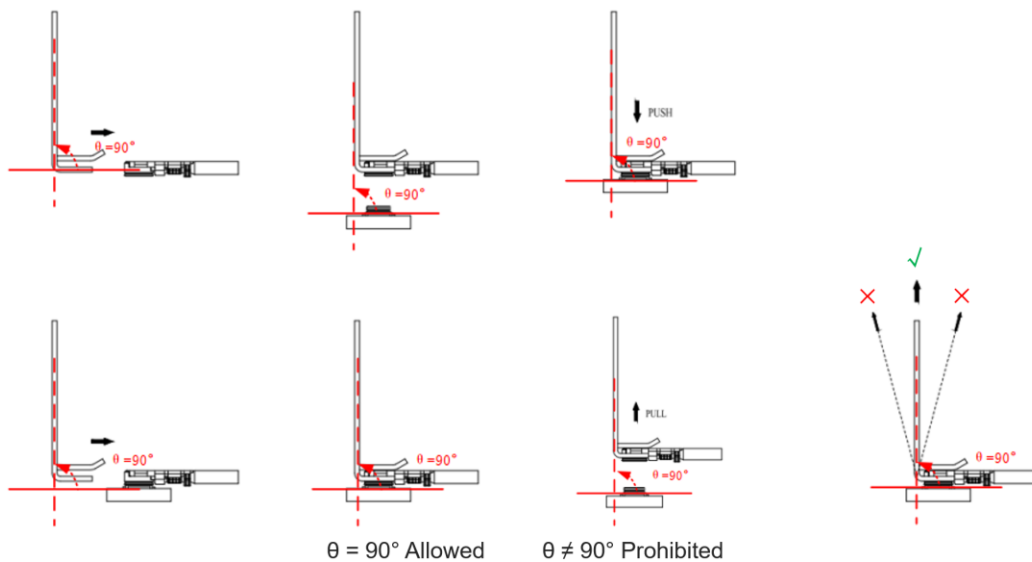


Figure 19: Install the Coaxial Cable Plug with Jig

5.3.2.4. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit <https://www.i-pex.com>.

5.3.2.5. Requirements for Antenna Design

Table 33: Requirements for Antenna Design

Parameter	Requirements
Frequency Range (GHz)	● 2.4 GHz: 2.400–2.4835 GHz ● 5 GHz: 5.150–5.850 GHz
RF Coaxial Connector	● VSWR: ≤ 2 ● Gain: 1 dBi (Typ.) ● Max. Input Power: 50 W ● Input Impedance: 50 Ω ● Vertical polarization ● Cable Insertion Loss: < 1 dB

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 34: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	3.6
Voltage at Digital Pins	-0.3	3.6
Voltage at ADC[0:7]	0	1.8

6.2. Power Supply Ratings

Table 35: Module Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.14	3.3	3.46

6.3. Power Consumption

6.3.1. Wi-Fi Power Consumption ⁶

Table 36: Wi-Fi Power Consumption in Non-signaling Mode (Unit: mA)

Condition (VBAT = 3.3 V, Temp.: 25 °C)			I _{VBAT} (AVG)
2.4 GHz	802.11b	Tx @ 1 Mbps	317.38
		Tx @ 11 Mbps	322.03
	802.11g	Tx @ 6 Mbps	308.55
		Tx @ 54 Mbps	288.83
	802.11n	Tx HT20 @ MCS0	308.73
		Tx HT20 @ MCS 7	272.63
	802.11ax	Tx HE20 @ MCS 0	310.46
		Tx HE20 @ MCS 9	258.37
	802.11a	Tx @ 6 Mbps	455.08
		Tx @ 54 Mbps	400.57
5 GHz	802.11n	Tx HT20 @ MCS 0	483.98
		Tx HT20 @ MCS 7	404.25
	802.11ac	Tx VHT20 @ MCS 0	515.09
		Tx VHT20 @ MCS 8	368.56
	802.11ax	Tx HE20 @ MCS 0	485.88
		Tx HE20 @ MCS 9	354.06

NOTE

The above power consumption data is the typical value for your reference only. Actual values may vary among different modules due to differences in internal components, software versions and test ambient temperatures. For more details, please contact Quectel Technical Support.

⁶ The Bluetooth function is disabled when the Wi-Fi power consumption is tested.

6.3.2. Bluetooth Power Consumption ⁷

Table 37: Bluetooth Power Consumption in Non-signaling Mode (Unit: mA)

Condition (VBAT = 3.3 V, Temp.: 25 °C)	I _{VBAT} (AVG)
BLE (1 Mbps)	105.58
BLE (2 Mbps)	95.91
BLE (S = 2)	108.59
BLE (S = 8)	103.55

NOTE

The above power consumption data is the typical value for your reference only. Actual values may vary among different modules due to differences in internal components, software versions and test ambient temperatures. For more details, please contact Quectel Technical Support.

6.4. Digital I/O Characteristics

Table 38: VBAT I/O Requirements (Unit: V)

Parameters	Descriptions	Min.	Max.
V _{IH}	High-level Input Voltage	0.7 × VBAT	VBAT
V _{IL}	Low-level Input Voltage	0	0.3 × VBAT
V _{OH}	High-level Output Voltage	0.9 × VBAT	VBAT
V _{OL}	Low-level Output Voltage	-0	0.1 × VBAT

⁷ The Wi-Fi function is disabled when the Bluetooth power consumption is tested.

6.5. ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

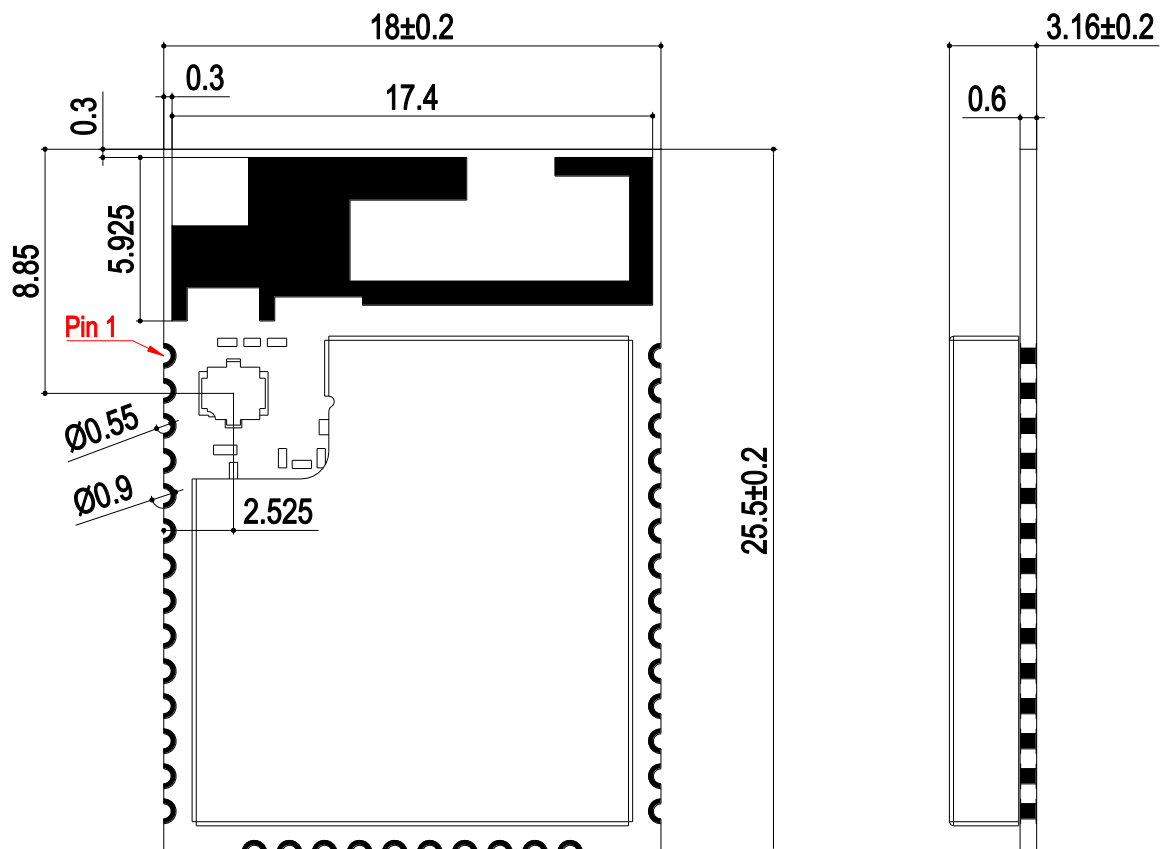
Table 39: ESD Characteristics (Unit: kV)

Model	Test Result	Standard
Human Body Model (HBM)	± 2	ANSI/ESDA/JEDEC JS-001
Charged Device Model (CDM)	± 0.5	ANSI/ESDA/JEDEC JS-002

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions



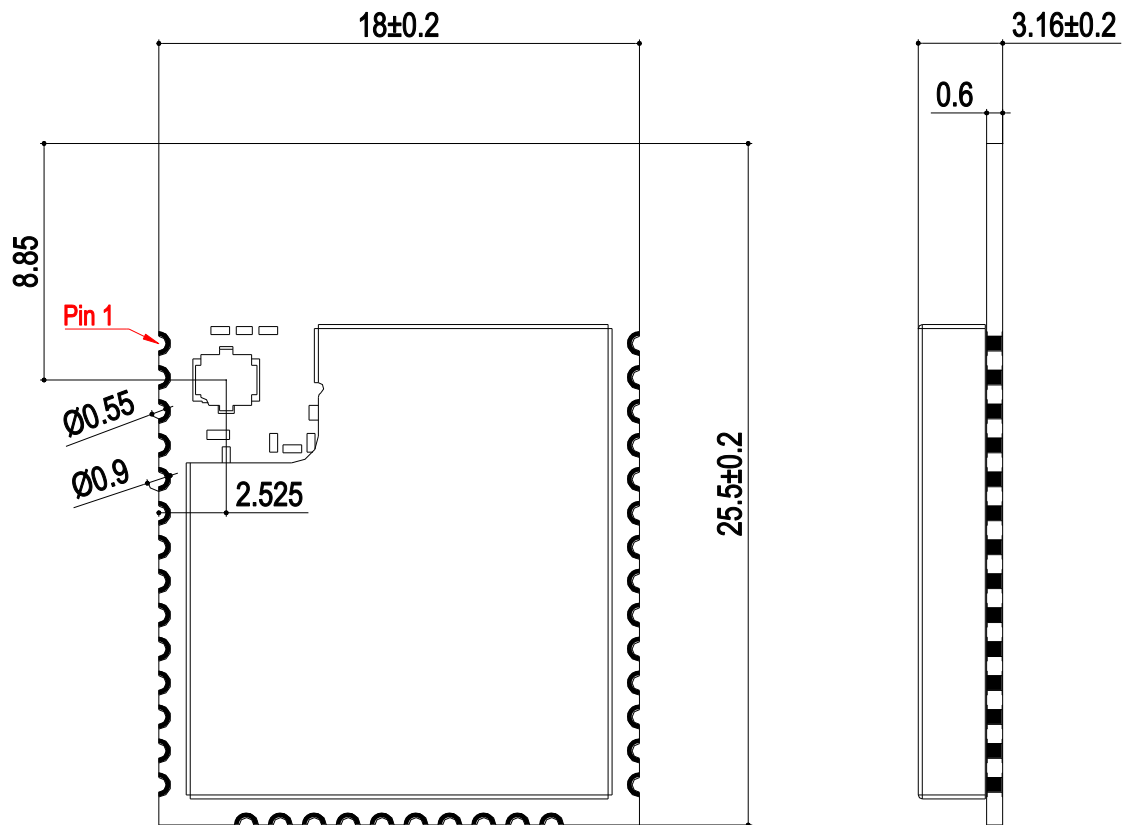


Figure 22: Top and Side Dimensions (RF Coaxial Connector)

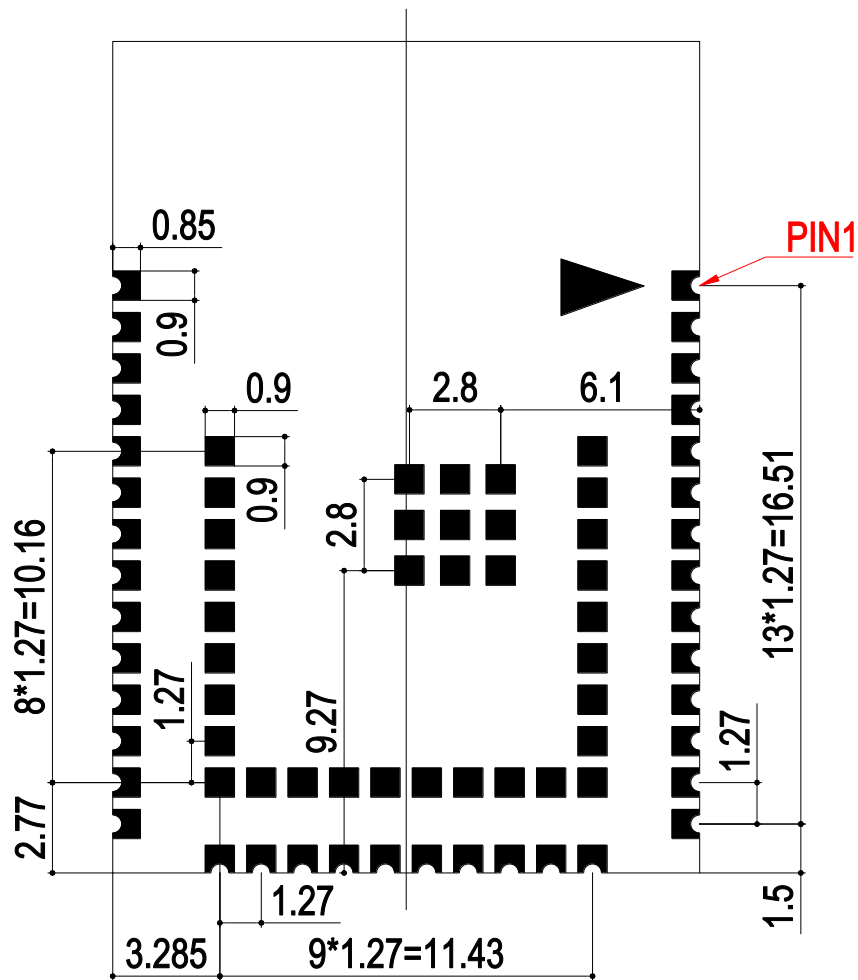


Figure 23: Bottom Dimensions (RF Coaxial Connector)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

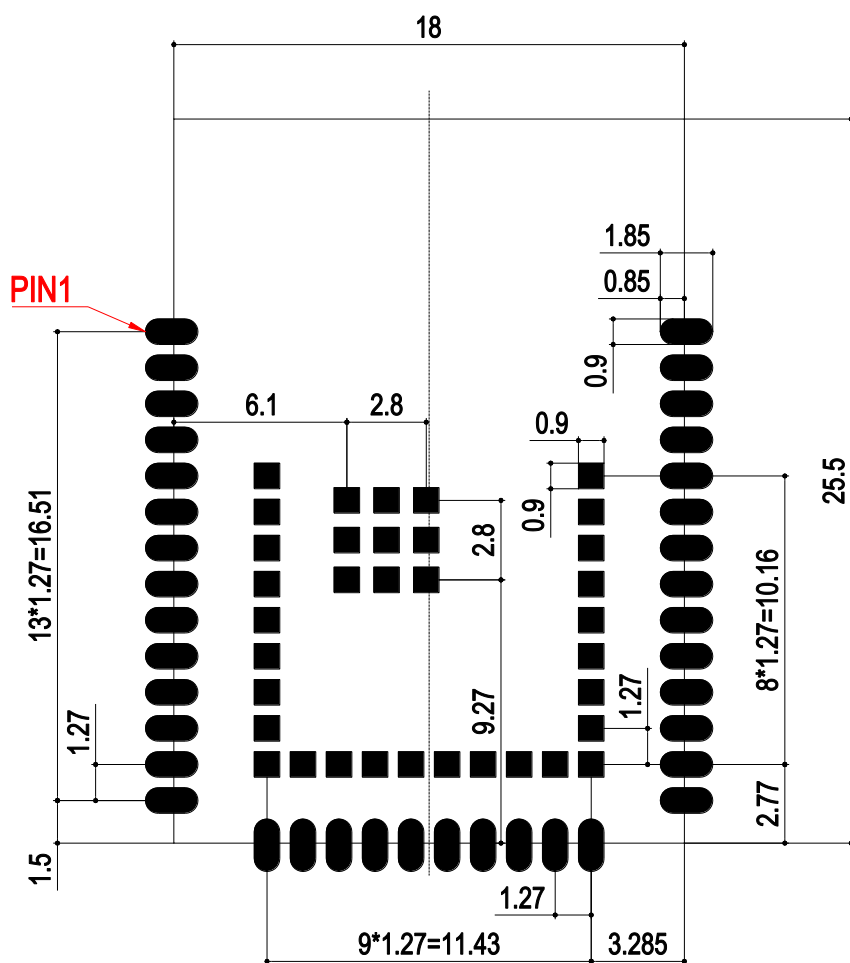


Figure 24: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

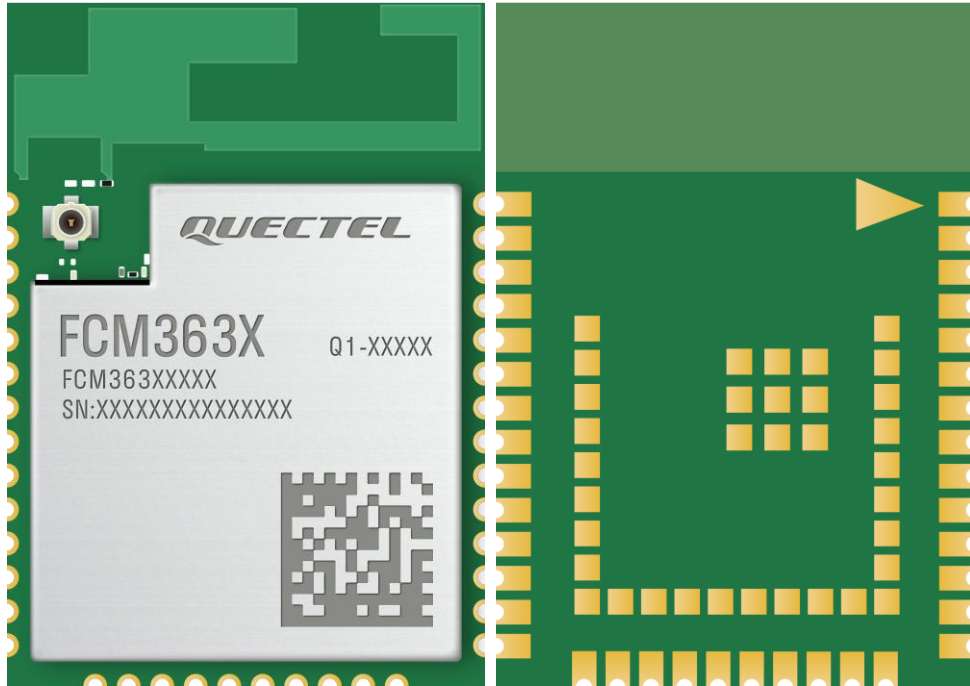


Figure 25: Top and Bottom Views (PCB Antenna)

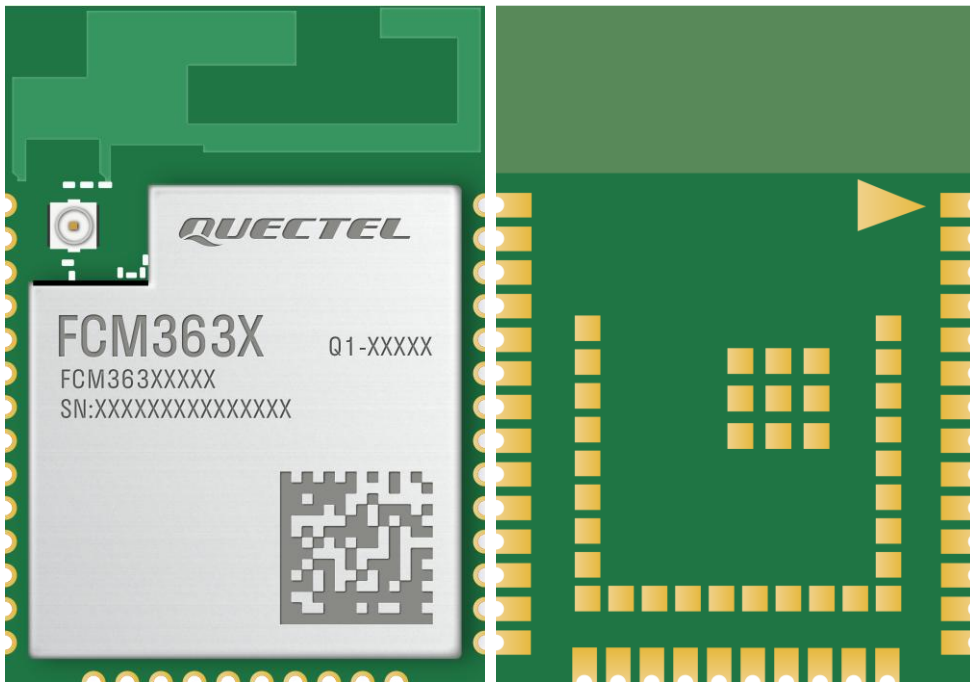


Figure 26: Top and Bottom Views (RF Coaxial Connector)

NOTE

1. Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.
2. The RF coaxial connector is not soldered when the module is designed with a PCB antenna.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours ⁸ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 24 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

⁸ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see **document [3]**.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Temp. (°C)

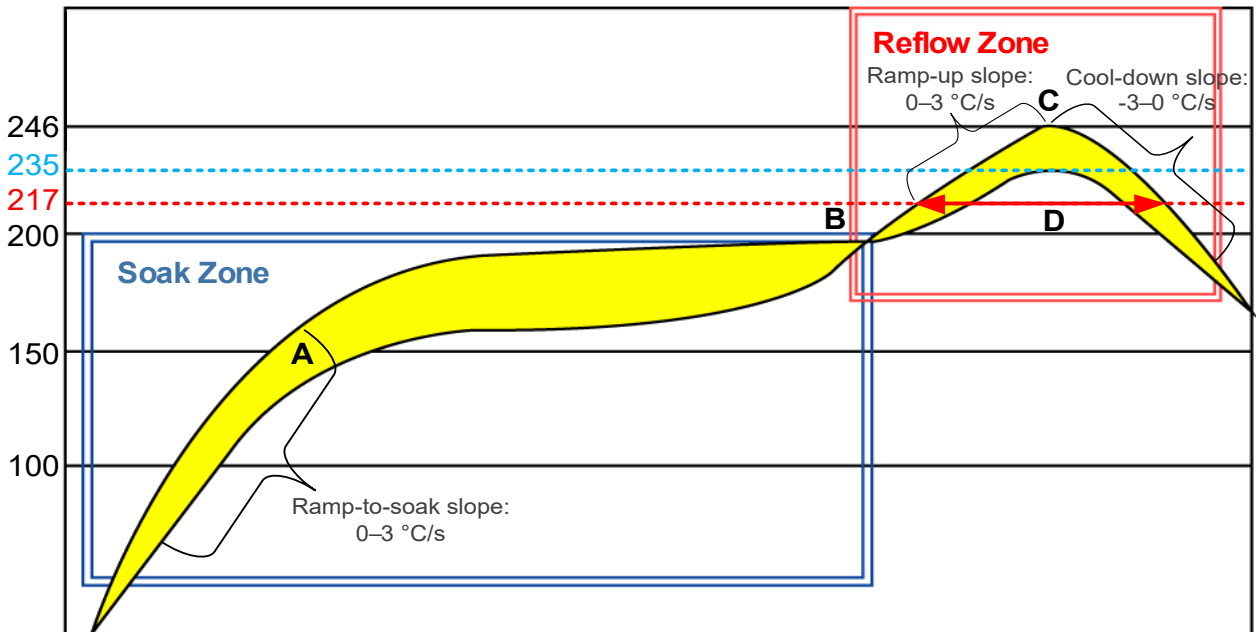


Figure 27: Recommended Reflow Soldering Thermal Profile

Table 40: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic

soldering) that is not mentioned in *document [4]*.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

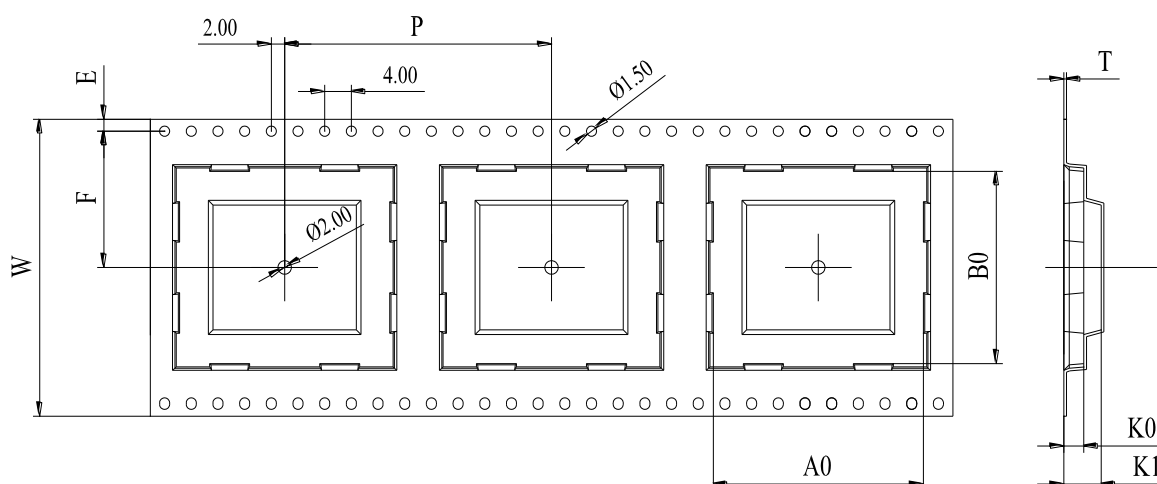


Figure 28: Carrier Tape Dimension Drawing (Unit: mm)

Table 41: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	18.4	25.9	3.7	4.4	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

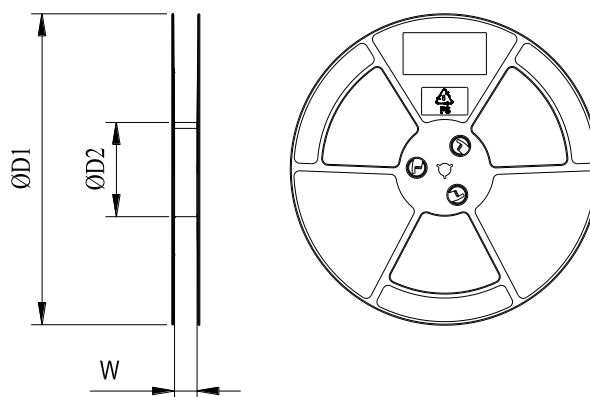


Figure 29: Plastic Reel Dimension Drawing

Table 42: Plastic Reel Dimension Table (Unit: mm)

ØD1	ØD2	W
380	100	44.5

8.3.3. Mounting Direction

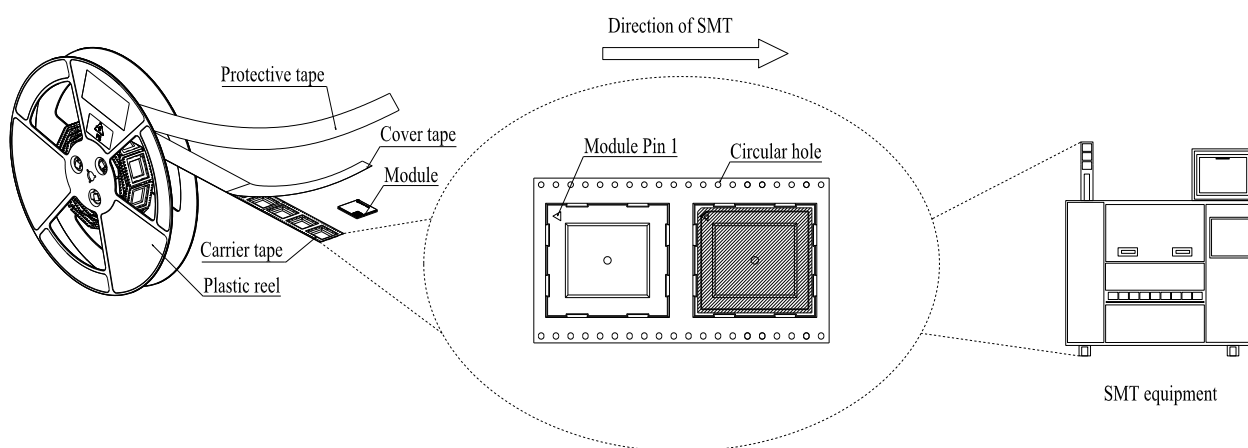
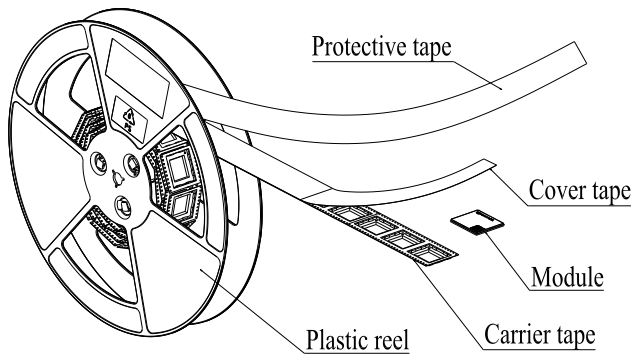


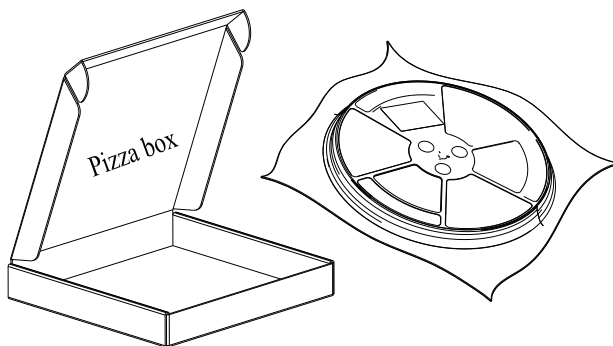
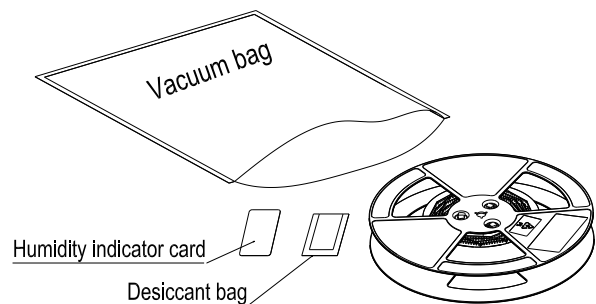
Figure 30: Mounting Direction

8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

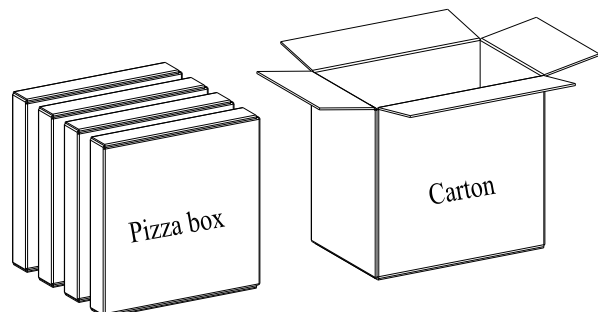


Figure 31: Packaging Process

9 Appendix References

Table 43: Reference Documents

Document Name
[1] Quectel_FCM363X_TE-B_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_Stencil_Design_Requirements
[4] Quectel_Module_SMT_Application_Note

Table 44: Terms and Abbreviations

Abbreviation	Description
ACOMP	Analog Comparator
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
AP	Access Point
APB	Advanced Peripheral Bus
BLE	Bluetooth Low Energy
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CDM	Charged Device Model
DAC	Digital-to-analog Converter
DMA	Direct Memory Access
DMIC	Digital Microphone

DQPSK	Differential Quadrature Reference Phase Shift Keying
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
GFSK	Gauss frequency Shift Keying
GND	Ground
GPIO	General-Purpose Input/Output
HBM	Human Body Model
HT	High Throughput
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
ISP	In-System Programming
kbps	Kilobits Per Second
LCC	Leadless Chip Carrier (package)
Mbps	Million Bits Per Second
MCU	Microcontroller Unit
OTA	Over The Air
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDM	Pulse-density Modulation
PTA	Packet Traffic Arbitration
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances

SAE	Simultaneous Authentication of Equals
SD	Secure Digital
SDIO	Secure Digital Input/Output
SMD	Surface Mount Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
UTICK	Micro-tick Timer
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{max}	Maximum Voltage
V_{min}	Minimum Voltage
V_{nom}	Normal Voltage Value
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCI	Wireless Coexistence Interface
Wi-Fi	Wireless Fidelity
WPA	Wi-Fi Protected Access

FCC Statement

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

The device must not be co-located or operating in conjunction with any other antenna or transmitter. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement

This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Does not comply with the use restrictions of the product:

Portable devices used close with human's body (within 20cm), Like Cell phone, Notebook etc.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.247 & 15.209 & 15.407.

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 3.1dBi antenna. The host manufacturer installing this module into their product must ensure that the final product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules,

including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

2.4 Limited module procedures

Not applicable. The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable. The module has its own antenna, and doesn't need a host's printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users' body; and if RF exposure statement or module layout is changed, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: PCB Antenna

Gain: 3.1dBi

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a "unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2025FCM363X" with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, etc according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15.209 & 15.407 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Federal Communication Commission Statement (FCC, US)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

IMPORTANT NOTES**Co-location warning:**

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

OEM integration instructions:

This device is intended only for OEM integrators under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.

As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance.

requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End product labeling:

The final end product must be labeled in a visible area with the following: "Contains Transmitter Module **FCC ID: XMR2025FCM363X**"

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

IC Statement

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

The device is compliance with RF field strength limits, users can obtain Canadian information on RF exposure and compliance.

IC Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d' exposition aux radiations:

Cet équipement est conforme aux limites d' exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

The user manual for local area network devices shall contain instructions related to the restrictions

mentioned in the above sections, namely that:

- (i) the device for operation in the band 5150-5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
- (ii) the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall comply with the e.i.r.p. limit; and
- (iii) the maximum antenna gain permitted for devices in the band 5725-5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

(i) Les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux.

(ii) le gain d'antenne maximal autorisé pour les appareils dans les bandes 5250-5350 MHz et 5470-5725 MHz doivent respecter le pire limiter; et

(iii) le gain d'antenne maximal autorisé pour les appareils dans la bande 5725-5825 MHz doivent respecter le pire limites spécifiées pour le point-à-point et l'exploitation non point à point, le cas échéant.

Users should also be advised that high-power radars are allocated as primary users (i.e. priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

Les utilisateurs de radars de haute puissance sont désignés utilisateurs principaux (c.-à-d., qu'ils ont la priorité) pour les bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer du brouillage et/ou des dommages aux dispositifs LAN-EL.