

SG555D&SG565D Series

Hardware Design

Smart Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

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1 Introduction

This document defines Quectel SG555D & SG565D series modules and details their air interfaces and hardware interfaces that are connected to your applications, which can help you quickly understand the hardware interface characteristics, RF characteristics, electrical characteristics, mechanical specifications and other relevant information of the modules.

Hereby, Quectel Wireless Solutions Co., Ltd. declares that the radio equipment type SG555D & SG565D series is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: <http://www.quectel.com/support/technical.htm>

Disposal of old electrical appliances



The European directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), requires that old household electrical appliances must not be disposed of in the normal unsorted municipal waste stream. Old appliances must be collected separately in order to optimize the recovery and recycling of the materials they contain, and reduce the impact on human health and the environment.

The crossed out “wheeled bin” symbol on the product reminds you of your obligation, that when you dispose of the appliance, it must be separately collected.

Consumers should contact their local authority or retailer for information concerning the correct disposal of their old appliance.

**UK
CA**

	AT	BE	BG	HR	CY	CZ	DK
	EE	FI	FR	DE	EL	HU	IE
	IT	LV	LT	LU	MT	NL	PL
	PT	RO	SK	SI	ES	SE	UK(NI)

This equipment should be installed and operated with minimum distance 20cm between the radiator and your body. The device is restricted to indoor use only when operating in the 5150 to 5350 MHz frequency range.

1.1. Special Marks

Table 1: Special Marks

Marks	Definitions
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[...]	Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is an industrial-grade Smart module, supporting Ubuntu operating system. It is an SMD module with compact packaging and it supports built-in high performance Adreno™ 642L/643 graphics processing unit (GPU), multiple audio and video codecs, and multiple audio and video input/output interfaces as well as abundant GPIOs.

Table 2: Basic Information

SG555D & SG565D Series	
Packaging type	LGA
Pin counts	636 pins
Dimensions	(42.5 ±0.2) mm × (56.5 ±0.2) mm × (2.95 ±0.2) mm
Weight	SG565D-AP, SG555D-AP: approx. 16.2 g SG565D-WF, SG555D-WF: approx. 16.6 g
Models	SG555D series: SG555D-AP, SG555D-WF SG565D series: SG565D-AP, SG565D-WF

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

SG555D-AP/SG565D-AP		SG555D-WF/SG565D-WF
Wi-Fi	-	802.11a/b/g/n/ac
Bluetooth	-	Bluetooth 5.0 ¹ (BR/EDR + BLE)

¹ This module is compatible with all mandatory functions of Bluetooth 5.0, but it does not support the optional functions of Bluetooth 5.0, such as 2 Mbps BLE, advanced broadcast extension.

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Application Processor	SG555D series (FP1): 6-core 64-bit ARM v8 Kryo 670 processor 2 MB L3 cache ● 2 × Kryo Gold: high performance processor @ 2.13 GHz and 256 KB L2 cache ● 4× Kryo Silver: low power consumption processor @ 1.8 GHz and 128 KB L2 cache
	SG555D series (FP2.5*): 8-core 64-bit ARM v8 Kryo 670 processor 2 MB L3 cache ● 1 × Kryo Prime: high performance processor @ 2.38 GHz and 256 KB L2 cache ● 3 × Kryo Gold: high performance processor @ 2.4 GHz and 256 KB L2 cache ● 4 × Kryo Silver: low power consumption processor @ 1.8 GHz and 128 KB L2 cache
	SG565D series: 8-core 64-bit ARM v8 Kryo 670 processor and 2 MB L3 cache ● 1 × Kryo Prime: high performance processor @ 2.7 GHz and 256 KB L2 cache ● 3 × Kryo Gold: high performance processor @ 2.4 GHz and 256 KB L2 cache ● 4 × Kryo Silver: low power consumption processor @ 1.9 GHz and 128 KB L2 cache
GPU	SG555D series (FP1): ● Adreno™ 642L GPU ● Operating frequency: 315 MHz
	SG555D series (FP2.5*): ● Adreno™ 642L GPU ● Operating frequency: 550 MHz
	SG565D series: ● Adreno™ 643 GPU ● Operating frequency: 812 MHz
NPU	SG555D-AP/SG555D-WF (FP1): ● 3.5 Tops @ int8
	SG555D-AP/SG555D-WF (FP2.5*): ● 6 Tops @ int8
	SG565D series: ● 12.15 Tops @ int8

Memory	SG555D series:
	64 GB UFS + 6 GB LPDDR4X (default)
	SG565D-AP:
	64 GB UFS + 4 GB LPDDR4X (Default) 128 GB UFS + 8 GB LPDDR4X (Optional)
	SG565D-WF:
	128 GB UFS + 8 GB LPDDR4X (Default)
Operating System	Ubuntu 20.04
Supply Voltage	3.55–4.4 V
	Typ.: 4 V
USB Interfaces	Supports 2 USB interfaces: USB0 and USB1
	- USB0 interface: - Complies with USB 3.1 Gen 1 and USB 2.0 specifications - Data rate: up to 5 Gbps for USB 3.1 and 480 Mbps for USB 2.0 - Supports USB OTG (external VBUS power supply is required), USB Type-C, Micro USB - Used for AT command communication, data transmission, software debugging, firmware upgrade and voice over USB
	- USB1 interface: - Complies with USB 2.0 specification - Data rate: up to 480 Mbps for USB 2.0 - Supports master mode only (external VBUS power supply is required)
	Display Port V1.4 interface function can be realized by USB_SS2 interface
	Supports DP standard interface only
	- Supports up to 3840 × 2160 @ 60 fps - Display Port can be used with USB 3.1 simultaneously
SD Card Interface	Complies with SD 3.0 specification
	1.8/ 2.95 V SD card
	SD card hot-plug
UART ²	- Supports up to 12 groups of UART, 2 of them are configured by default, and 10 of them are multiplexed from other interfaces: - UART: 4-wire UART with the speed rate up to 4 Mbps, which supports RTS and CTS hardware flow control - DBG_UART: 2-wire UART, dedicated for debugging
	For details about UART multiplexed from other interfaces, see Table 21
	Supports up to 10 groups of SPI, 1 of them are configured by default, and 9 of them are multiplexed from other interfaces:
	- The default SPI supports master mode only - For details about SPI multiplexed from other interfaces, see Table 21
I2C Interfaces ²	- Supports up to 16 groups of I2C interfaces: 5 groups of dedicated I2C interfaces for cameras and sensors 3 groups of general-purpose I2C interfaces for touch panels, NFC and

² For details about the multiplexing and conflict relationships of UART, I2C, SPI and I2S interfaces, see **Table 21**.

	- other peripheral circuits 8 groups of I2C interfaces are multiplexed from other interfaces
I2S Interfaces ²	- Supports up to 4 groups of I2S interfaces: 2 groups are configured by default 2 groups are multiplexed from other interfaces
ADC Interfaces	6 general-purpose ADC interfaces - Resolution: up to 15 bits
LCM Interface	SG555D series: 1 group of 4-lane MIPI_DSI - Data rate: up to 2.5 Gbps/lane - Supports up to FHD + (1200 × 2520) @ 120 fps SG565D series: 1 group of 4-lane MIPI_DSI - Data rate: up to 2.5 Gbps/lane - Supports up to FHD + (1200 × 2520) @ 144 fps
Camera Interfaces	SG555D series (FP1): 4 groups of 4-lane MIPI_CSI - Data rate: up to 2.5 Gbps/lane - Supports up to 5 cameras, and 2 cameras can work simultaneously - Dual-ISP, supporting up to 2 concurrent cameras at 22 MP + 22 MP or a single camera at 36 MP SG555D series (FP2.5*), SG565D series: 4 groups of 4-lane MIPI_CSI - Data rate: up to 2.5 Gbps/lane - Supports up to 5 cameras, and 3 cameras can work simultaneously - Tri-ISP, supporting up to 3 concurrent cameras at 22 MP+ 22 MP + 22 MP or at 36 MP + 22 MP
PCIe Interfaces	- PCIe0 (1-lane, Gen 3) - PCIe1 (2-lane, Gen 3) - Data rate: up to 8 Gbps
Video Codec	- Video decoding: 4K @ 60 fps, H.264/H.265/VP9 - Video encoding: 4K @ 30 fps, H.264/H.265 - Encoding + Decoding: 1080P @ 60 fps decoding + 1080P @ 60 fps encoding or 4K @ 30 fps decoding + 1080P @ 30 fps encoding
Audio Interfaces	Audio inputs: 3 digital microphone inputs
Audio Codec	- EVRC, EVRC-B, EVRC-WB, G.711, G.729, PCM, EVS - GSM-FR, GSM-EFR, GSM-HR - AMR-NB, AMR-WB, QCELP
Antenna Interface	- Wi-Fi & Bluetooth antenna interface (ANT_WIFI/BT) 50 Ω characteristic impedance
WLAN Features	- Operating modes: AP and STA - Operating frequency: 2.4 GHz, 5 GHz - Protocol features: IEEE 802.11a/b/g/n/ac

	● Data rate: up to 433 Mbps
Bluetooth Features	● <i>Bluetooth Core Specification Version 5.0</i> ● Bluetooth Classic & Bluetooth Low Energy (BLE)
RTC	The module supports RTC function
Temperature Ranges	● Normal operating temperature ³: -35 °C to +75 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	SG555D-WF/SG565D-WF: ● USB interfaces ● OTA SG555D-AP/SG565D-AP: ● USB interfaces
RoHS	All hardware components fully comply with EU RoHS directive

³ Within this range, the module's indicators comply with IEEE specification requirements.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- LPDDR4X + UFS flash
- Radio frequency part
- Peripheral interfaces

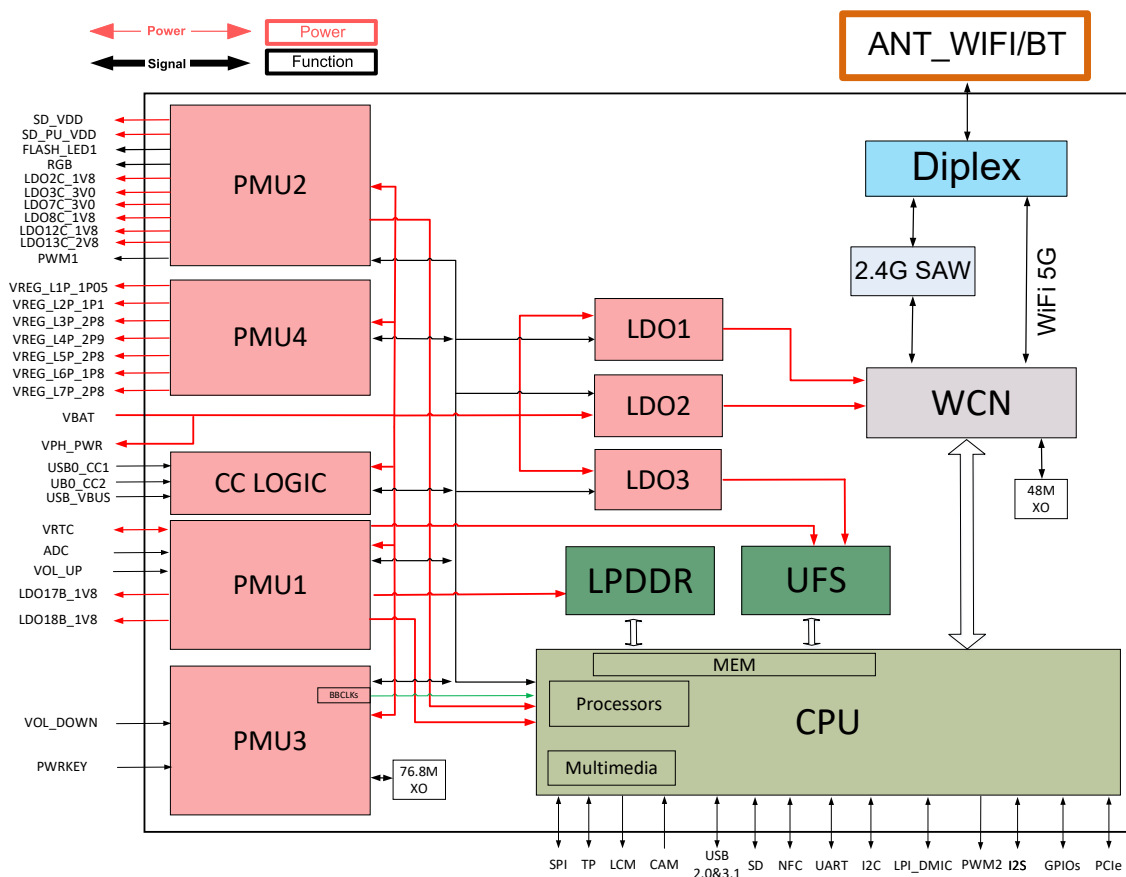


Figure 1: Functional Diagram

2.4. Pin Assignment

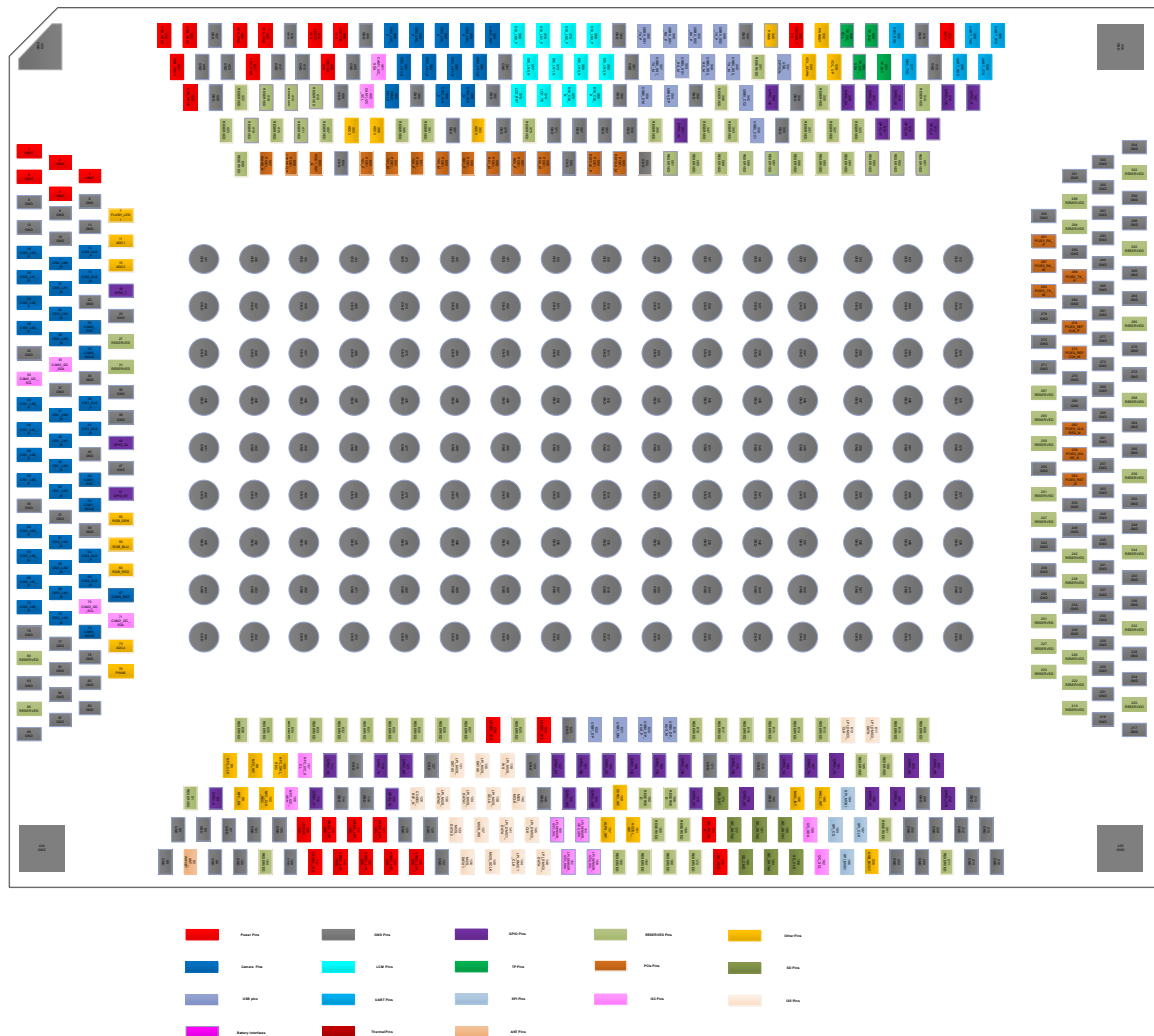


Figure 2: Pin Assignment

NOTE

Keep all RESERVED pins and unused pins open.

2.5. Pin Definitions

Table 5: I/O Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output
PU	Pull-up
PD	Pull-down

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply & GND						
Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
VBAT ⁴	1–5	PI	-	Power supply for the module	Vmin = 3.55 V Vnom = 4.0 V Vmax = 4.4 V	It is recommended to use a TVS diode for surge protection.
VPH_PWR	420,	PO	-	Power supply for	Vnom = VBAT	So long as the module

⁴ The current value is to be measured.

	421, 424			peripherals	I _{omax} = 1500 mA	is powered up, the pin retains its power whether the module is turned on or turned off. The total current should be 1.5 A.
LDO7C_3V0	412	PO	-	3.0 V output power for sensor and touch panel	V _{nom} = 3.0 V I _{omax} = 600 mA	Add a 1.0–4.7 µF bypass capacitor if used. The total capacitance should not exceed 18.8 µF.
LDO13C_2V8	409	PO	-	2.8 V output power for LCM	V _{nom} = 2.8 V I _{omax} = 150 mA	Add a 1.0–4.0 µF bypass capacitor if used. The total capacitance should not exceed 4 µF.
LDO18B_1V8	336	PO	-	1.8 V output power for I/O's pull-up circuit	V _{nom} = 1.8 V I _{omax} = 20 mA	Keeps ON; Add a 1.0–4.7 µF bypass capacitor if used. The total capacitance should not exceed 14.1 µF.
LDO17B_1V8	408	PO	-	1.8 V output power for I/O's pull-up circuit	V _{nom} = 1.8 V I _{omax} = 600 mA	Add a 1.0–4.7 µF bypass capacitor if used. The total capacitance should not exceed 18.8 µF.
LDO12C_1V8	109	PO	-	1.8 V output power for I/O's pull-up circuit of LCM	V _{nom} = 1.8 V I _{omax} = 150 mA	Add a 1.0–4.0 µF bypass capacitor if used. The total capacitance should not exceed 4 µF.
LDO8C_1V8	112	PO	-	1.8 V output power for sensor	V _{nom} = 1.8 V I _{omax} = 150 mA	Add a 1.0–4.7 µF bypass capacitor if used. The total capacitance should not exceed 18.8 µF.
LDO3C_3V0	624	PO	-	3.0 V output power (reserved)	V _{nom} = 3.0 V I _{omax} = 150 mA	Add a 1.0–4.0 µF bypass capacitor if used. The total capacitance should not exceed 4 µF.
LDO2C_1V8	626	PO	-	1.8 V output power (reserved)	V _{nom} = 1.8 V I _{omax} = 150 mA	
VRTC	312	PIO	-	Power supply for	V _{min} = 2.0 V	

	RTC	Vnom = 3.0 V Vmax = 3.25 V
GND	6, 8–10, 12, 13, 22, 23, 32, 34, 35, 37, 39, 46, 47, 56–58, 76–78, 81–85, 87–90, 93, 96, 97, 100, 101, 105, 108, 114, 115, 118, 125, 127, 129, 132, 143, 146, 171, 179, 182, 204–206, 208, 209, 212–218, 221, 224, 225, 228–230, 233–237, 239–241, 243, 245, 246, 248–250, 252, 253, 255, 257, 260, 261, 264–266, 269–273, 275–277, 279, 281, 282, 284, 285, 288–290, 293, 295–297, 299–301, 303, 304, 313, 316, 334, 335, 344, 350, 359, 361–364, 367, 371, 379, 381, 382, 387, 394, 404–406, 413, 416, 417, 425–428, 433–580, 592, 595, 604, 623	Connect them to GND.

Keypad Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
PWRKEY	332	DI	-	Turn on/off the module		Pull it up to 1.1 V internally. Active low.
VOL_DOWN	333	DI	-	Volume down		Pull it up to 1.8 V internally. Active low.
VOL_UP	329	DI	-	Volume up		

USB Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
USB_VBUS	429–432	PIO	-	USB/adaptor insertion detection; OTG is supported. External power supply is not supported	Vmax = 12.6 V Vmin = 3.7 V Vnom = 5.0 V	A test point must be reserved.
USB0_DP	354	AIO	-	USB0 2.0 differential data (+)		90 Ω differential impedance. USB 2.0 standard compliant. OTG is supports.
USB0_DM	358	AIO	-	USB0 2.0 differential data (-)		Test points must be reserved.
USB0_SS1_TX_P	360	AO	-	USB 3.1 channel 1 SuperSpeed transmit (+)		90 Ω differential impedance. USB 3.1

USB0_SS1_TX_M	357	AO	-	USB 3.1 channel 1 SuperSpeed transmit (-)	Gen 1 compliant.
USB0_SS1_RX_P	356	AI	-	USB 3.1 channel 1 SuperSpeed receive (+)	
USB0_SS1_RX_M	353	AI	-	USB 3.1 channel 1 SuperSpeed receive (-)	
USB0_SS2_TX_P	348	AO	-	USB 3.1 channel 2 SuperSpeed transmit (+)	
USB0_SS2_TX_M	345	AO	-	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB0_SS2_RX_P	352	AI	-	USB 3.1 channel 2 SuperSpeed receive (+)	
USB0_SS2_RX_M	349	AI	-	USB 3.1 channel 2 SuperSpeed receive (-)	
USB0_CC1	339	AI	-	USB Type-C configuration channel 1	
USB0_CC2	342	AI	-	USB Type-C configuration channel 2	In Micro USB mode, it can be used as USB_ID.
USB_OPTION	337	AI	-	Initial configuration of mode selection when USB is powered up	In USB Type-C mode, keep it open. In Micro USB mode, connect it to GND.
USB1_DP	622	AIO	-	USB1 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 compliant. Supports master mode only. Test points must be reserved.
USB1_DM	621	AIO	-	USB1 2.0 differential data (-)	
USB0_DP_AUX_P	620	AIO	-	DisplayPort auxiliary channel (+)	

USB0_DP_AUX_M	619	AIO	-	DisplayPort auxiliary channel (-)		
PCIe Interfaces						
Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
PCIE0_REFCLK_P	278	AIO	-	PCIE0 reference clock (+)		
PCIE0_REFCLK_M	274	AIO	-	PCIE0 reference clock (-)		
PCIE0_RX_P	291	AI	-	PCIE0 receive (+)		85 Ω differential impedance.
PCIE0_RX_M	287	AI	-	PCIE0 receive (-)		
PCIE0_TX_P	286	AO	-	PCIE0 transmit (+)		
PCIE0_TX_M	283	AO	-	PCIE0 transmit (-)		
PCIE0_RST_N	254	DO	PD	PCIE0 reset		
PCIE0_CLKREQ_N	262	DI	PU	PCIE0 clock request	LDO18B_1V8	Pull it up internally by default.
PCIE0_WAKE_N	258	DI	PD	PCIE0 wake up		
PCIE1_REFCLK_P	594	AIO	-	PCIE1 reference clock (+)		
PCIE1_REFCLK_M	593	AIO	-	PCIE1 reference clock (-)		
PCIE1_RX0_P	597	AI	-	PCIE1 receive 0 (+)		85 Ω differential impedance. PCIE1 is not supported by default for SG555D series, and you can contact Quectel Technical Support if necessary. SG565D series supports PCIe1.
PCIE1_RX0_M	596	AI	-	PCIE1 receive 0 (-)		
PCIE1_RX1_P	599	AI	-	PCIE1 receive 1 (+)		
PCIE1_RX1_M	598	AI	-	PCIE1 receive 1 (-)		
PCIE1_TX0_P	601	AO	-	PCIE1 transmit 0 (+)		
PCIE1_TX0_M	600	AO	-	PCIE1 transmit 0 (-)		
PCIE1_TX1_P	603	AO	-	PCIE1 transmit 1 (+)		

PCIE1_TX1_M	602	AO	-	PCle1 transmit 1 (-)		
PCIE1_RST_N	605	DO	PD	PCle1 reset		
PCIE1_CLKREQ_N	606	DI	PU	PCle1 clock request	LDO18B_1V8	
PCIE1_WAKE_N	607	DI	PD	PCle1 wake up		

LCM Interface

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
DSI_CLK_P	366	AO	-	LCD MIPI clock (+)		
DSI_CLK_N	370	AO	-	LCD MIPI clock (-)		
DSI_LN0_P	380	AO	-	LCD MIPI data 0 (+)		
DSI_LN0_N	377	AO	-	LCD MIPI data 0 (-)		
DSI_LN1_P	376	AO	-	LCD MIPI data 1 (+)		85 Ω differential impedance.
DSI_LN1_N	373	AO	-	LCD MIPI data 1 (-)		
DSI_LN2_P	372	AO	-	LCD MIPI data 2 (+)		
DSI_LN2_N	369	AO	-	LCD MIPI data 2 (-)		
DSI_LN3_P	368	AO	-	LCD MIPI data 3 (+)		
DSI_LN3_N	365	AO	-	LCD MIPI data 3 (-)		
LCD_TE	374	DI	PD	LCD tearing effect		
LCD_RST	378	DO	PD	LCD reset	LDO18B_1V8	External pull-up is not required.

Camera Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
CSI0_CLK_P	14	AI	-	MIPI CSI0 clock		85 Ω differential

				(+)		impedance.
CSI0_CLK_N	18	AI	-	MIPI CSI0 clock (-)		
CSI0_LN0_P	16	AI	-	MIPI CSI0 data 0 (+)		
CSI0_LN0_N	17	AI	-	MIPI CSI0 data 0 (-)		
CSI0_LN1_P	20	AI	-	MIPI CSI0 data 1 (+)		
CSI0_LN1_N	21	AI	-	MIPI CSI0 data 1 (-)		
CSI0_LN2_P	24	AI	-	MIPI CSI0 data 2 (+)		
CSI0_LN2_N	25	AI	-	MIPI CSI0 data 2 (-)		
CSI0_LN3_P	28	AI	-	MIPI CSI0 data 3 (+)		
CSI0_LN3_N	29	AI	-	MIPI CSI0 data 3 (-)		
CAM0_MCLK	30	DO	PD	Master clock of camera 0	LDO18B_1V8	
CAM0_RST	26	DO	PD	Reset of camera 0		
CSI1_CLK_P	38	AI	-	MIPI CSI1 clock (+)		
CSI1_CLK_N	42	AI	-	MIPI CSI1 clock (-)		
CSI1_LN0_P	40	AI	-	MIPI CSI1 data 0 (+)		
CSI1_LN0_N	41	AI	-	MIPI CSI1 data 0 (-)		
CSI1_LN1_P	44	AI	-	MIPI CSI1 data 1 (+)		85 Ω differential impedance.
CSI1_LN1_N	45	AI	-	MIPI CSI1 data 1 (-)		
CSI1_LN2_P	48	AI	-	MIPI CSI1 data 2 (+)		
CSI1_LN2_N	49	AI	-	MIPI CSI1 data 2 (-)		
CSI1_LN3_P	52	AI	-	MIPI CSI1 data 3 (+)		

CSI1_LN3_N	53	AI	-	MIPI CSI1 data 3 (-)	
CAM1_MCLK	54	DO	PD	Master clock of camera 1	LDO18B_1V8
CAM1_RST	50	DO	PD	Reset of camera 1	
CSI2_CLK_P	390	AI	-	MIPI CSI2 clock (+)	
CSI2_CLK_N	386	AI	-	MIPI CSI2 clock (-)	
CSI2_LN0_P	392	AI	-	MIPI CSI2 data 0 (+)	
CSI2_LN0_N	389	AI	-	MIPI CSI2 data 0 (-)	
CSI2_LN1_P	388	AI	-	MIPI CSI2 data 1 (+)	85 Ω differential impedance.
CSI2_LN1_N	385	AI	-	MIPI CSI2 data 1 (-)	
CSI2_LN2_P	396	AI	-	MIPI CSI2 data 2 (+)	
CSI2_LN2_N	393	AI	-	MIPI CSI2 data 2 (-)	
CSI2_LN3_P	400	AI	-	MIPI CSI2 data 3 (+)	
CSI2_LN3_N	397	AI	-	MIPI CSI2 data 3 (-)	
CAM2_MCLK	398	DO	PD	Master clock of camera 2	LDO18B_1V8
CAM2_RST	384	DO	PD	Reset of camera 2	
CSI3_CLK_P	62	AI	-	MIPI CSI3 clock (+)	
CSI3_CLK_N	66	AI	-	MIPI CSI3 clock (-)	
CSI3_LN0_P	60	AI	-	MIPI CSI3 data 0 (+)	85 Ω differential impedance.
CSI3_LN0_N	61	AI	-	MIPI CSI3 data 0 (-)	
CSI3_LN1_P	68	AI	-	MIPI CSI3 data 1 (+)	
CSI3_LN1_N	69	AI	-	MIPI CSI3 data 1 (-)	

CSI3_LN2_P	64	AI	-	MIPI CSI3 data 2 (+)		
CSI3_LN2_N	65	AI	-	MIPI CSI3 data 2 (-)		
CSI3_LN3_P	72	AI	-	MIPI CSI3 data 3 (+)		
CSI3_LN3_N	73	AI	-	MIPI CSI3 data 3 (-)		
CAM3_MCLK	74	DO	PD	Master clock of camera 3	LDO18B_1V8	
CAM3_RST	67	DO	PD	Reset of camera 3		
CAM2_I2C_SDA	71	OD	-	Cameras 2&3 I2C data		
CAM2_I2C_SCL	70	OD	-	Cameras 2&3 I2C clock		
CAM1_I2C_SDA	401	OD	-	Camera1 I2C data	LDO18B_1V8	
CAM1_I2C_SCL	402	OD	-	Camera1 I2C clock		
CAM0_I2C_SDA	33	OD	-	Camera0 I2C data		
CAM0_I2C_SCL	36	OD	-	Camera0 I2C clock		
VREG_L1P_1P05	116	PO	-	Power supply for DVDD of cameras 1 and 2	Vnom = 1.05 V Iomax = 600 mA	
VREG_L2P_1P1	121	PO	-	Power supply for DVDD of cameras 0 and 3	Vnom = 1.1 V Iomax = 600 mA	
VREG_L3P_2P8	113	PO	-	Power supply for AVDD of cameras 1 and 3	Vnom = 2.8 V Iomax = 300 mA	
VREG_L4P_2P9	124	PO	-	Power supply for AVDD of camera 0	Vnom = 2.9 V Iomax = 300 mA	
VREG_L5P_2P8	128	PO	-	Power supply for AFVDD of camera 0	Vnom = 2.8 V Iomax = 300 mA	
VREG_L6P_1P8	117	PO	-	Power supply for DOVDD of cameras 0–3	Vnom = 1.8 V Iomax = 300 mA	
VREG_L7P_2P8	120	PO	-	Power supply for AVDD of camera 2	Vnom = 2.8 V Iomax = 300 mA	

Dedicated for cameras. External pull-up to 1.8 V with 2.2 kΩ resistors is required. If unused, keep them open.

Add a bypass capacitor if used. The total capacitance should not exceed 45.3 μF.

Add a bypass capacitor if used. The total capacitance should not exceed 19 μF.

SD Card Interface

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
SD_CLK	188	DO	-	SD card clock	SD_PU_VDD	45 Ω characteristic impedance.
SD_CMD	180	DIO	-	SD card command		
SD_DATA0	184	DIO	-	SDIO data bit 0		
SD_DATA1	185	DIO	-	SDIO data bit 1		
SD_DATA2	177	DIO	-	SDIO data bit 2		
SD_DATA3	181	DIO	-	SDIO data bit 3		
SD_DET	174	DI	-	SD card hot-plug detect	LDO18B_1V8	Active low by default. Externally pull it up to 1.8 V.
SD_VDD	176	PO	-	SD card power supply	Vnom = 2.95 V Iomax = 600 mA	Add a 1.0–4.7 μ F bypass capacitor if used. The total capacitance should not exceed 18.8 μ F.
SD_PU_VDD	173	PO	-	Power supply for SD card pull-up circuit	Iomax = 150 mA High-voltage: Vmin = 2.72 V Vnom = 2.95 V Vmax = 3.54 V Low-voltage: Vmin = 1.65 V Vnom = 1.8 V Vmax = 1.9 V	Only for SD card pull-up circuit. Add a 1.0–3.0 μ F bypass capacitor if used. The total capacitance should not exceed 3.0 μ F.

UARTs

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
DBG_TXD	317	DO	-	Debug UART transmit	LDO18B_1V8	Cannot be used for generic GPIO.
DBG_RXD	320	DI	-	Debug UART receive		Test points must be reserved.
UART_TXD	308	DO	PD	UART transmit		If unused, keep them

UART_RXD	309	DI	PD	UART receive	open.
UART_RTS	305	DO	PD	Request to send signal from the module	
UART_CTS	306	DI	PD	Clear to send signal to the module	

I2C Interface

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
I2C_SCL	192	OD	PD	I2C serial clock	LDO18B_1V8	External pull-up to 1.8 with 2.2 kΩ resistors is required. If unused, keep them open.
I2C_SDA	189	OD	PD	I2C serial data		

I2S Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
MI2S_MCLK	142	DO	PD	I2S master clock	LDO18B_1V8	
MI2S_SCLK	140	DO	PD	I2S clock		
MI2S_WS	137	DO	PD	I2S word select		
MI2S_DATA0	133	DIO	PD	I2S data channel 0		
MI2S_DATA1	136	DIO	PD	I2S data channel 1		
LPI_MI2S_SCLK	138	DO	PD	LPI I2S serial clock		
LPI_MI2S_WS	139	DO	PD	LPI I2S word select		
LPI_MI2S_DATA0	135	DIO	PD	LPI I2S data channel 0		
LPI_MI2S_DATA1	134	DIO	PD	LPI I2S data channel 1		
LPI_MI2S_DATA2	130	DIO	PD	LPI I2S data channel 2		

LPI_MI2S_DATA3	131	DIO	PD	LPI I2S data channel 3		
CODEC_RST_N	126	DO	-	Audio Codec reset		Cannot be pulled up during the turn-on process.

Digital Microphone Interface

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
LPI_DMIC1_CLK	144	DO	PD	Digital MIC1 clock for LPI	LDO18B_1V8	
LPI_DMIC1_DATA	141	DI	PD	Digital MIC1 data for LPI		
LPI_DMIC2_CLK	145	DO	PD	Digital MIC2 clock for LPI		
LPI_DMIC2_DATA	148	DI	PD	Digital MIC2 data for LPI		
LPI_DMIC3_CLK	612	DO	PD	Digital MIC3 clock for LPI		
LPI_DMIC3_DATA	611	DI	PD	Digital MIC3 data for LPI		

Touch Panel Interface

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
TP_RST	324	DO	PD	TP reset	LDO18B_1V8	
TP_INT	321	DI	PD	TP interrupt		
TP_I2C_SCL	328	OD	PD	TP I2C clock		External pull-up to 1.8 V with 2.2 kΩ resistors is required. If unused, keep them open.
TP_I2C_SDA	325	OD	PD	TP I2C data		

SPI

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
SPI_CLK	197	DO	PD	SPI clock	LDO18B_1V8	Supports master mode only.

SPI_CS	193	DO	PU	SPI chip select		Supports master mode only. Pull it up internally by default.
SPI_MISO	196	DI	PD	SPI master-in slave-out		Supports master mode only.
SPI_MOSI	194	DO	PD	SPI master-out slave-in		

ADC Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
ADC0	399	AI	-	General-purpose ADC interface		The maximum input voltage is 1.8 V.
ADC1	11	AI	-			
ADC2	15	AI	-			
ADC3	403	AI	-			
ADC4	75	AI	-			
ADC5	383	AI	-			

PWM Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
PWM2	79	DO	PD	PWM2 output	LDO18B_1V8	
PWM1	340	DO	-	PWM1 output	VPH_PWR	Backlight control.

RGB Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
RGB_BLU	59	AO	-	Current output for blue LED	I _{omax} = 12 mA	
RGB_GRN	55	AO	-	Current output for green LED		
RGB_RED	63	AO	-	Current output for red LED		

NFC Interfaces*

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
NFC_CLK	95	DO	-	NFC clock		
NFC_CLK_REQ	102	DI	PD	NFC clock request		
NFC_DWL_REQ	103	DO	PD	NFC download control request		
NFC_EN	98	DO	PU	NFC enable	LDO18B_1V8	Pull it up internally by default.
NFC_INT	99	DI	PD	NFC interrupt		
NFC_I2C_SDA	106	OD	PD	NFC I2C data		External pull-up to 1.8 V with 2.2 kΩ resistors is required.
NFC_I2C_SCL	107	OD	PD	NFC I2C clock		If unused, keep them open.

Sensor Interrupt Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
GYRO_INT	158	DI	PD	Gyroscope sensor interrupt		
ACCEL_INT	161	DI	PD	Acceleration sensor interrupt		
MAG_INT	186	DI	PD	Magnetic sensor interrupt		
ALPS_INT	157	DI	PD	Light/proximity sensor interrupt	LDO18B_1V8	
HALL_INT	190	DI	PD	Hall sensor interrupt		
LPI_SENSOR_I2C1_SDA	152	OD	PD	I2C1 data for external sensor		Dedicated for sensors. External pull-up to 1.8 V with 2.2 kΩ resistors is required.
LPI_SENSOR_I2C1_SCL	149	OD	PD	I2C1 clock for external sensor		If unused, keep them open.
LPI_SENSOR_I2C2_SDA	153	OD	PD	I2C2 data for external sensor		

LPI_SENSOR_
I2C2_SCL 156 OD PD I2C2 clock for
external sensor

GPIOs

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
GPIO_6	94	DIO	PD	General-purpose input/output	LDO18B_1V8	Interrupt wakeup is supported.
GPIO_7	19	DIO	PD			
GPIO_8	311	DIO	PD			
GPIO_9	307	DIO	PD			
GPIO_12	198	DIO	PD			Interrupt wakeup is supported.
GPIO_13	191	DIO	PD			Cannot be pulled up during the turn-on process.
GPIO_14	183	DIO	PD			
GPIO_15	187	DIO	PD			Cannot be pulled up during the turn-on process. Interrupt wakeup is supported.
GPIO_16	111	DIO	PD			Interrupt wakeup is supported.
GPIO_17	110	DIO	PD			Interrupt wakeup is supported.
GPIO_18	122	DIO	PD			
GPIO_19	119	DIO	PD			
GPIO_24	43	DIO	PD			
GPIO_32	351	DIO	PD			Interrupt wakeup is supported.
GPIO_33	170	DIO	PD			
GPIO_34	315	DIO	PD			
GPIO_35	178	DIO	PD			
GPIO_42	318	DIO	PD			

GPIO_43	155	DIO	PD	Interrupt wakeup is supported. Do not pull GPIO_45 up during the turn-on process.
GPIO_44	202	DIO	PD	
GPIO_45	203	DIO	PD	
GPIO_46	207	DIO	PD	
GPIO_47	319	DIO	PD	Interrupt wakeup is supported.
GPIO_61	51	DIO	PD	
GPIO_62	322	DIO	PD	Cannot be pulled up during the turn-on process. Interrupt wakeup is supported.
GPIO_63	326	DIO	PD	
GPIO_68	123	DIO	PD	Interrupt wakeup is supported.
GPIO_93	147	DIO	PD	Cannot be pulled up during the turn-on process. Interrupt wakeup is supported.
GPIO_112	163	DIO	PD	Interrupt wakeup is supported.
GPIO_116	159	DIO	PD	
GPIO_119	210	DIO	PD	
GPIO_121	310	DIO	PD	
GPIO_133	175	DIO	PD	Interrupt wakeup is supported.
GPIO_134	167	DIO	PD	
GPIO_140	338	DIO	PD	Interrupt wakeup is supported.
GPIO_158	151	DIO	PD	
GPIO_165	150	DIO	PD	Interrupt wakeup is supported.
GPIO_166	154	DIO	PD	

RF Antenna Interface

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
ANT_WIFI/BT	92	AIO	-	Wi-Fi/Bluetooth antenna interface		50 Ω impedance.

Other Interfaces

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
FLASH_LED1	7	AO	-	Flash/torch driver output	I _{omax} = 850 mA	
USB_BOOT	200	DI	-	Force the module into download mode	LDO18B_1V8	A test point is recommended to be reserved.

RESERVED Pins

Pin Name	Pin No.	Comment
RESERVED	27, 31, 80, 86, 91, 104, 160, 162, 164–166, 168, 169, 172, 195, 199, 201, 211, 219, 220, 222, 223, 226, 227, 231, 232, 238, 242, 244, 247, 251, 256, 259, 263, 267, 268, 280, 292, 294, 298, 302, 314, 323, 327, 330, 331, 341, 343, 346, 347, 355, 375, 391, 395, 407, 410, 411, 414, 415, 418, 419, 422, 423, 581–591, 608–610, 613–618, 625, 627–636	Keep them open.

NOTE

To reduce the probability of module damage and extend module service life, do not power up and down frequently.

2.6. EVB Kit

Quectel supplies an evaluation board (Smart 5G EVB) with accessories to develop and test the module. For more details, see **document [1]**.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Interface

The module provides 5 VBAT pins dedicated to connecting with the external power supply. The power supply range of the module is 3.55–4.4 V, and the recommended value is 4 V.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT ⁵	1–5	PI	Power supply for the module	It is recommended to add a TVS diode externally.

3.1.2. Reference Design for Power Supply

The power source is critical to the module's performance. If the voltage difference between the input voltage and the supply voltage is small, it is recommended to use an LDO; If the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design of 5 V input power supply:

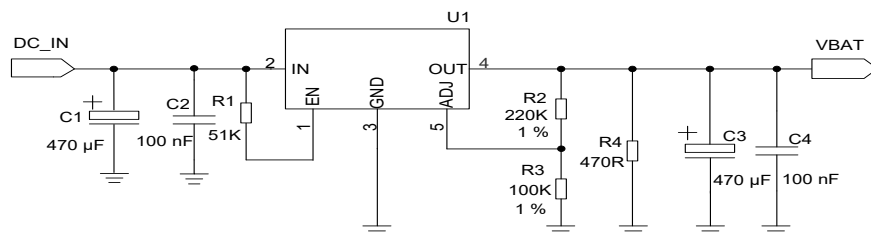


Figure 3: Reference Design of Power Input

⁵ The current value is to be measured.

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. It is essential to first shut down the module using PWRKEY before safely cutting off the power supply.

3.1.3. Requirements for Voltage Stability

The recommended power supply voltage of the module is 4 V. The power supply performance, such as load capacity, voltage ripple will directly influence the module's performance and stability. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.2 V, the module will turn off automatically. Therefore, ensure the input voltage never drops below 3.2 V.

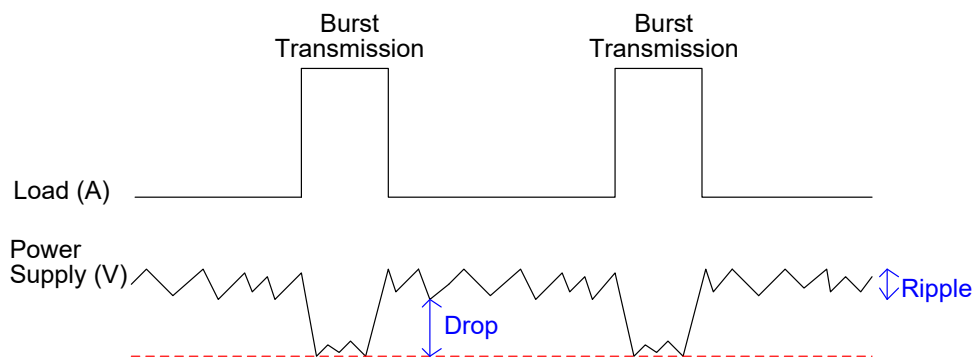


Figure 4: Power Supply Limits During Burst Transmission

To prevent the voltage from dropping below 3.2 V, it is recommended to connect a 100 μ F bypass capacitor with low ESR as well as 100 nF, 33 pF, 4.7 μ F and 10 pF filter capacitors in parallel near the VBAT pins of the module. It is also recommended that the PCB traces of VBAT should be as short as possible and wide enough to reduce the equivalent impedance of the VBAT traces and ensure that there will be no large voltage drop under high current at the maximum transmission power. The width of VBAT trace should be at least 5 mm. As per design rules, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

To suppress the impact of power fluctuations and ensure the stability of the output power supply, it is suggested to add a TVS diode and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows a reference circuit:

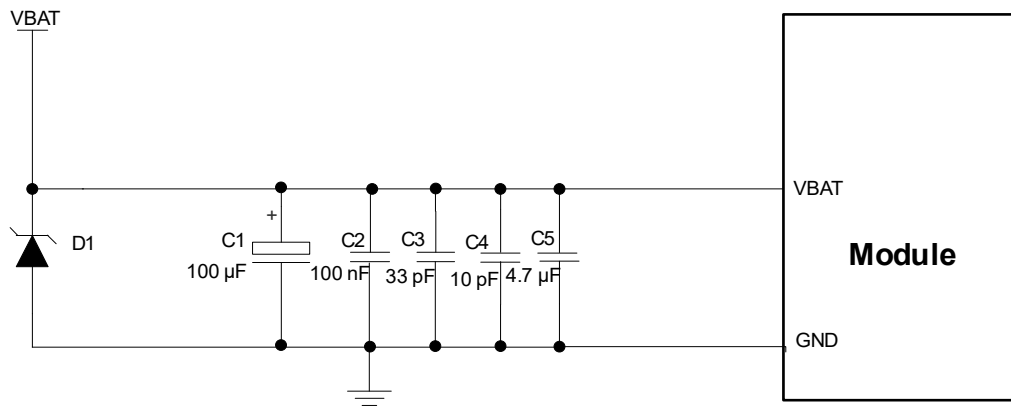


Figure 5: Reference Design of Power Supply

3.2. Turn-On

3.2.1. Turn On with PWRKEY

Table 8: Pin Description of PWRKEY Interface

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	332	DI	Turn on/off the module	Pull it up to 1.1 V internally, Active low.

When powering up the VBAT, the module can be turned on by driving PWRKEY low for at least 1.6 s. It is recommended to use an open drain/collector driver to control the PWRKEY. PWRKEY is pulled up to VBAT internally.

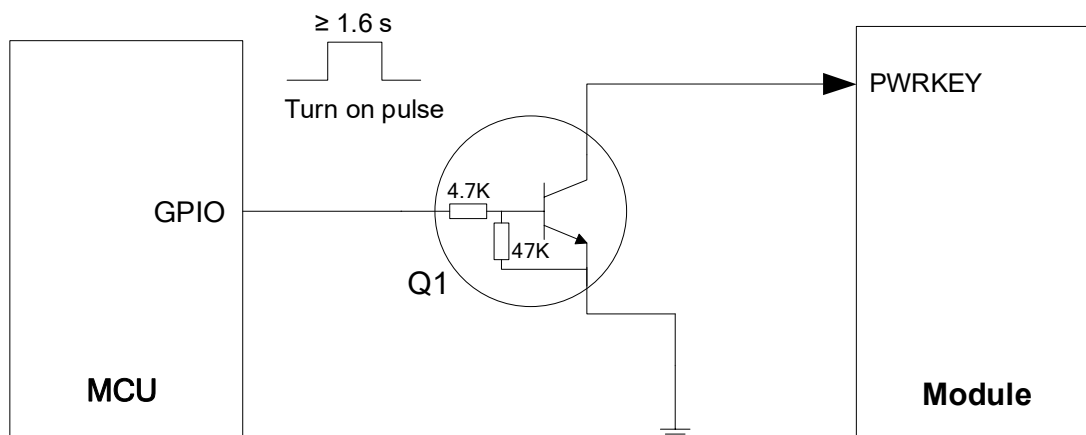


Figure 6: Reference Design of Turn-on with Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, you should place a TVS diode near the button for ESD protection. Additionally, a 1 k Ω resistor is connected in series to PWRKEY for ESD protection.

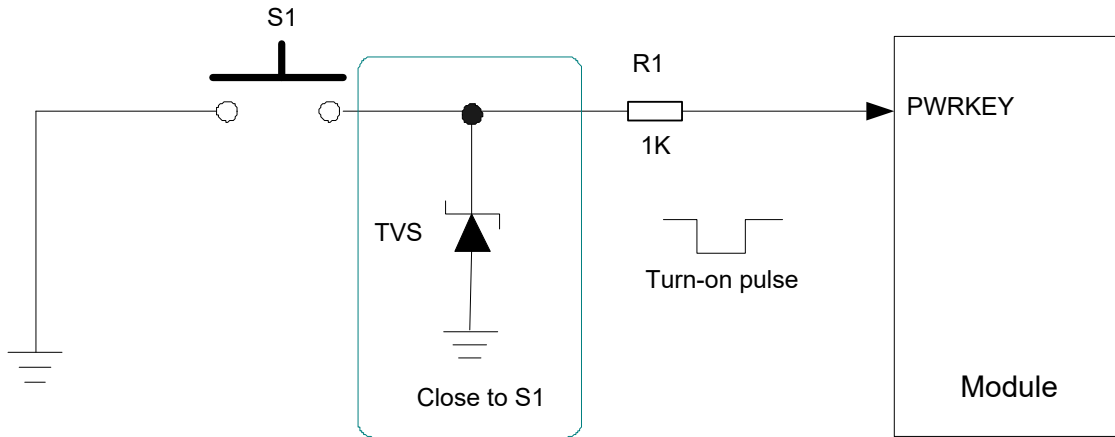


Figure 7: Reference Design of Turn-on with Button

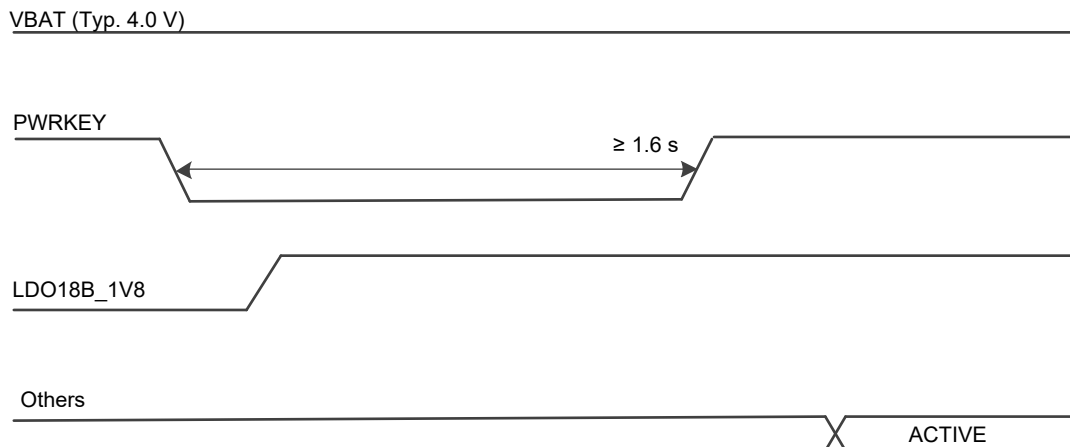


Figure 8: Turn-on Timing with PWRKEY

NOTE

1. When the module is powered up for the first time, its turn-on timing may be different from that shown in the figure above.
2. Ensure the voltage of VBAT is stable before driving PWRKEY low. It is recommended to drive PWRKEY low after VBAT reaches 4 V and remains stable for 30 ms. PWRKEY cannot be driven low all the time.

3.3. Restart/Turn Off

The module can be turned off by driving the PWRKEY low for at least 3 s, and then choose to turn off or to restart the module when the prompt window comes up. In addition, you can execute the forced restart by driving PWRKEY low for at least 8 s.

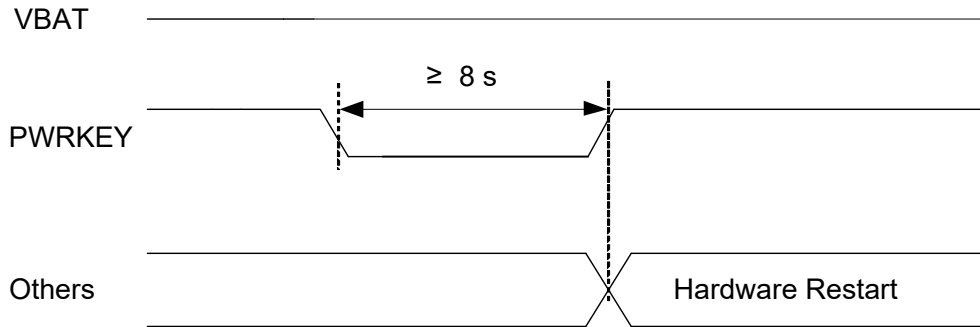


Figure 9: Timing of Restart

3.4. VRTC

The RTC of the module can be powered by an external power supply pin: VRTC. When VBAT is disconnected and you need to reserve RTC function, VRTC cannot be kept open. The power source can be an external battery or capacitor according to application demands. The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

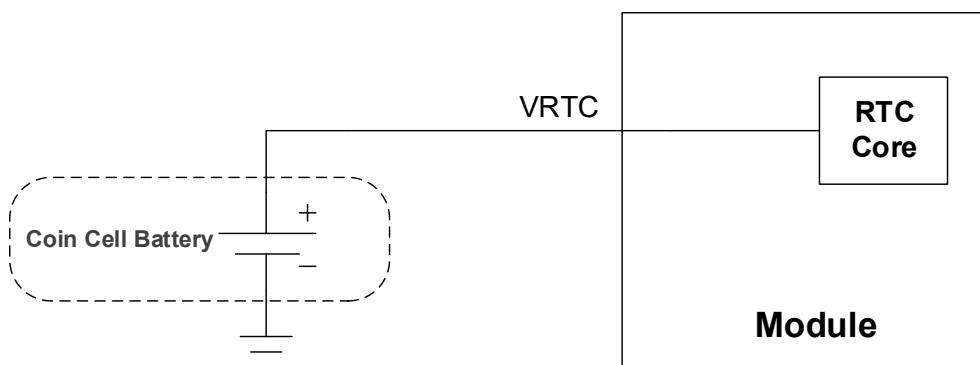


Figure 10: RTC Powered by Rechargeable Cell Battery

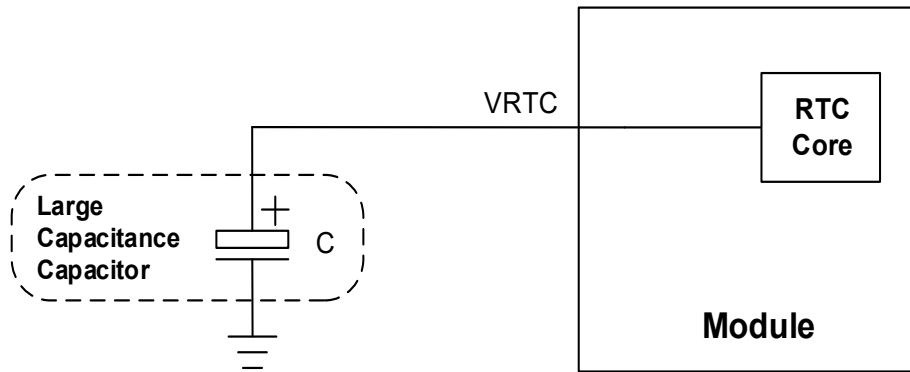


Figure 11: RTC Powered by Large Capacitance Capacitor

If RTC fails, the module can synchronize time over the network after being powered up.

- The recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3.0 V. The average power consumption is 10.6 μ A when VBAT is disconnected.
- When powered by VBAT, the error of RTC is 50 ppm; When powered by VRTC, the error of RTC is 500 ppm.
- If a rechargeable button battery is used, ESR of the battery should be less than 2 k Ω . It is recommended to use MS621FE FL11E of SEIKO.
- When a large capacitance capacitor is connected, it is recommended to use the 10 μ F capacitor of low ESR, which can keep the RTC running for about 1 s.

3.5. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In practical application, it is recommended to use a 10-pF and a 33-pF capacitor in parallel to suppress high-frequency noise.

Table 9: Power Supply Information

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
VPH_PWR	Vnom = VBAT	I _{Omax} = 1500 mA	So long as the module is powered up, the pin retains its power whether the module is turned on or turned off.
LDO7C_3V0	Vnom = 3.0 V	I _{Omax} = 600 mA	
LDO13C_2V8	Vnom = 2.8 V	I _{Omax} = 150 mA	

LDO18B_1V8	Vnom = 1.8 V	I _o max = 20 mA	Keeps ON.
LDO17B_1V8	Vnom = 1.8 V	I _o max = 600 mA	
LDO12C_1V8	Vnom = 1.8 V	I _o max = 150 mA	
LDO8C_1V8	Vnom = 1.8 V	I _o max = 150 mA	
LDO3C_3V0	Vnom = 3.0 V	I _o max = 150 mA	
LDO2C_1V8	Vnom = 1.8 V	I _o max = 150 mA	

4 Application Interfaces

4.1. USB Interfaces

The module provides 2 USB interfaces: USB0 and USB1. USB0 complies with USB 3.1 Gen1 and USB 2.0 specifications and supports OTG. It also supports USB Type-C interface, Native DP mode and Micro USB interface. USB1 complies with USB 2.0 specification, and supports master mode only. It also supports SuperSpeed mode (5 Gbps) for USB 3.1 Gen 1, high-speed (480 Mbps) and full-speed (12 Mbps) modes for USB 2.0. USB0 interface can be used for AT command transmission, data transmission, software debugging, firmware upgrade and voice over USB.

4.1.1. USB0 Interface

Table 10: Pin Description of USB0 Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	429–432	PIO	USB/adaptor insertion detection; OTG is supported. External power supply is not supported	A test point must be reserved.
USB0_DP	354	AIO	USB0 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 standard compliant. OTG is supported. Test points must be reserved.
USB0_DM	358	AIO	USB0 2.0 differential data (-)	
USB0_SS1_TX_P	360	AO	USB 3.1 channel 1 SuperSpeed transmit (+)	90 Ω differential impedance. USB 3.1 Gen 1 compliant.
USB0_SS1_TX_M	357	AO	USB 3.1 channel 1 SuperSpeed transmit (-)	
USB0_SS1_RX_P	356	AI	USB 3.1 channel 1 SuperSpeed receive (+)	
USB0_SS1_RX_M	353	AI	USB 3.1 channel 1 SuperSpeed receive (-)	

USB0_SS2_TX_P	348	AO	USB 3.1 channel 2 SuperSpeed transmit (+)	
USB0_SS2_TX_M	345	AO	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB0_SS2_RX_P	352	AI	USB 3.1 channel 2 SuperSpeed receive (+)	
USB0_SS2_RX_M	349	AI	USB 3.1 channel 2 SuperSpeed receive (-)	
USB0_CC1	339	AI	USB Type-C configuration channel 1	In Micro USB mode, it can be used as USB_ID.
USB0_CC2	342	AI	USB Type-C configuration channel 2	
USB_OPTION	337	AI	Initial configuration of mode selection when USB is powered up	In USB Type-C mode, keep it open. In Micro USB mode, connect it to GND.
USB0_DP_AUX_P	620	AIO	DisplayPort auxiliary channel (+)	
USB0_DP_AUX_M	619	AIO	DisplayPort auxiliary channel (-)	

4.1.1.1. USB0 Type-C Mode

The reference design of USB0 Type-C mode is shown below:

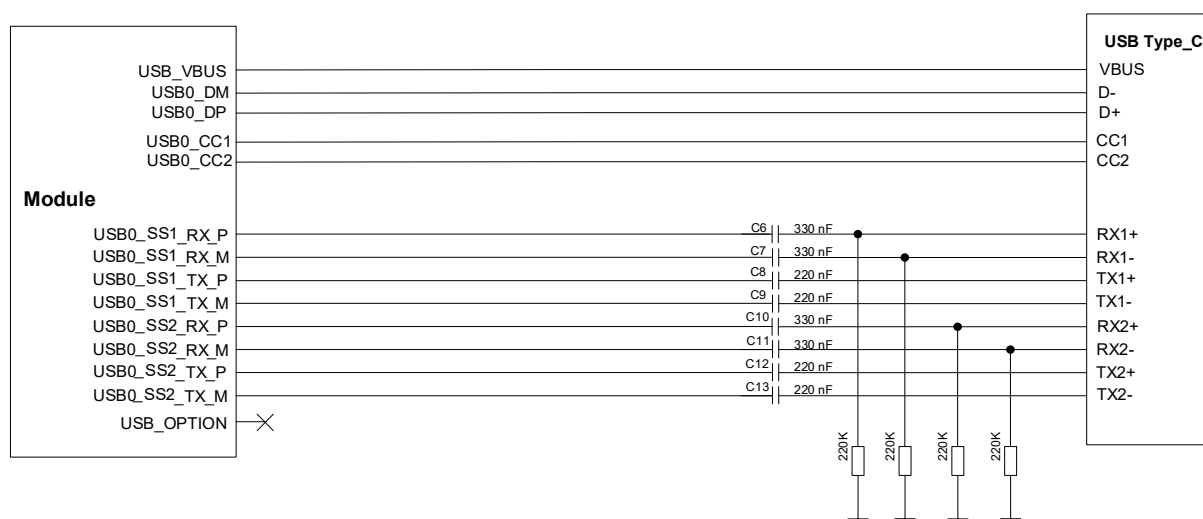


Figure 12: Reference Design of USB0 Type-C Mode

4.1.1.2. USB0 Micro USB Mode

The default USB0 interface of the module is Type-C interface. If Micro USB interface is used, it can be realized via hardware configuration. The reference design of Micro USB interface realized by USB0 is shown below:

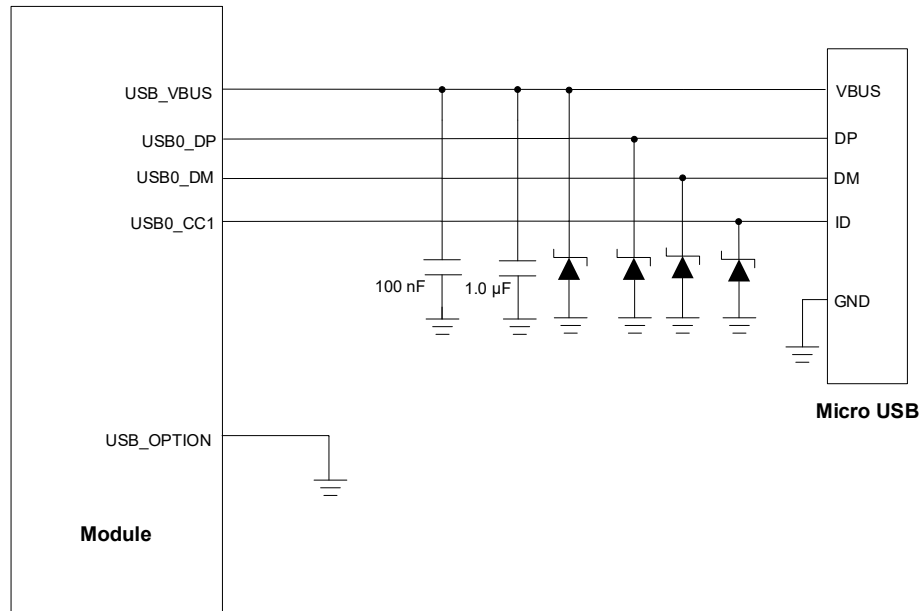


Figure 13: Reference Design of USB0 Micro USB Mode

4.1.1.3. USB0 Display Port Mode

Display Port V1.4 interface function can be realized by USB_SS2 of USB0. DP function supports up to 3840 × 2160 @ 60 fps. DP function can be used with USB 3.1 simultaneously. The module only supports native DP, and DP of Type-C interface is not supported. See the following table for more details:

Table 11: Pin Description of DP Interface

Pin Name	Pin No.	I/O	Description	Comment
USB0_SS2_TX_P	348	AO	USB 3.1 channel 2 SuperSpeed transmit (+)	90 Ω differential impedance.
USB0_SS2_TX_M	345	AO	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB0_SS2_RX_P	352	AI	USB 3.1 channel 2 SuperSpeed receive (+)	
USB0_SS2_RX_M	349	AI	USB 3.1 channel 2 SuperSpeed receive (-)	

USB0_DP_AUX_P	620	AIO	DisplayPort auxiliary channel (+)
USB0_DP_AUX_M	619	AIO	DisplayPort auxiliary channel (-)

The following figure shows the reference design of DP function:

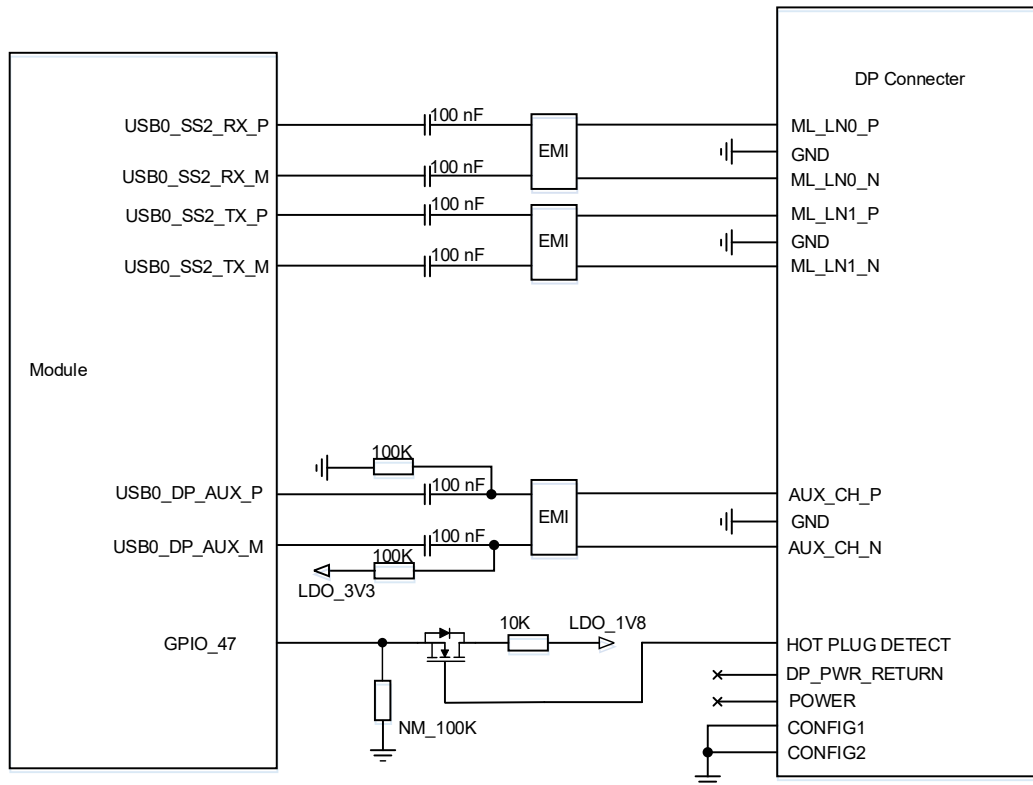


Figure 14: Reference Design of USB0 DP Mode

4.1.2. USB1 Micro USB Interface

The following table shows the pin definition of USB1 interface:

Table 12: Pin Description of Micro USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB1_DP	622	AIO	USB1 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 compliant.
USB1_DM	621	AIO	USB1 2.0 differential data (-)	Supports master mode only. Test points must be reserved.

4.1.3. USB Interface Design Considerations

Table 13: USB Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching
USB0_DP	354	74.44	0.32
USB0_DM	358	74.76	
USB0_SS1_TX_P	360	74.91	0.02
USB0_SS1_TX_M	357	74.93	
USB0_SS1_RX_P	356	69.83	0.01
USB0_SS1_RX_M	353	69.82	
USB0_SS2_TX_P	348	75.46	0.18
USB0_SS2_TX_M	345	75.64	
USB0_SS2_RX_P	352	71.60	0.01
USB0_SS2_RX_M	349	71.61	
USB1_DP	622	17.11	0.35
USB1_DM	621	16.76	
USB0_DP_AUX_P	620	14.10	0.09
USB0_DP_AUX_M	619	14.01	

To ensure performance, you should follow the principles below when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω .
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide spacing from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- The reference ground plane under the USB signal traces must be continuous without any cuts or vias to ensure impedance continuity.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, stray capacitance should be less than 2 pF for USB 2.0, and less than 0.5 pF for USB 3.1 Gen 1.

- Do not route USB 3.1 Gen 1 signal traces under RF signal traces. Crossing or being parallel with RF signal traces is forbidden. Isolation between USB 3.1 Gen 1 signals and RF signals should be over 90 dB. Otherwise, the RF signals will be seriously affected.
- For USB 3.1 Gen1 signal traces, length matching of each differential data pair (TX_P and TX_M, RX_P and RX_M) should be less than 0.7 mm.
- For USB 3.1 Gen 1, the spacing between RX and TX signal traces should be 3 times the signal trace width. The spacing between USB 3.1 Gen1 signal traces and other signal traces should be 4 times the signal trace width.
- For USB 2.0 signal traces, the differential data pair matching (DP/DM) should not exceed 2 mm.
- For USB 2.0, the spacing between DP and DM signal traces should be 3 times the signal trace width and the spacing between USB 2.0 signal traces and other signal traces should be 4 times the signal trace width.
- For DisplayPort, the length matching between DP_AUX_N and DP_AUX_P should not exceed 7 mm.

4.2. USB_BOOT

The module provides a USB_BOOT for forced download. Pull USB_BOOT up to LDO18B_1V8 before turning on the module, and then the module enters forced download mode. This is a final approach when failures such as abnormal start-up or running occur. For firmware upgrade and software debugging in the future, reserve the following reference design.

Table 14: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	200	DI	Force the module into download mode	A test point is recommended to be reserved.

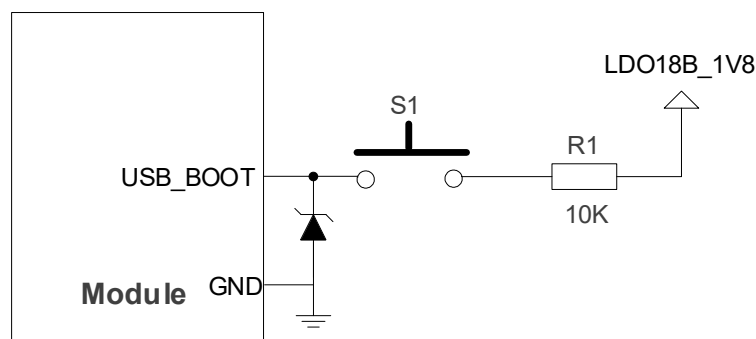


Figure 15: Reference Design of USB_BOOT

4.3. SD Card Interface

SD card interface of the module complies with SD 3.0 specifications:

Table 15: Pin Description of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	188	DO	SD card clock	
SD_CMD	180	DIO	SD card command	
SD_DATA0	184	DIO	SDIO data bit 0	45 Ω characteristic impedance.
SD_DATA1	185	DIO	SDIO data bit 1	
SD_DATA2	177	DIO	SDIO data bit 2	
SD_DATA3	181	DIO	SDIO data bit 3	
SD_DET	174	DI	SD card hot-plug detect	Active low by default. Externally pull it up to 1.8 V.
SD_VDD	176	PO	SD card power supply	Add a 1.0–4.7 μ F bypass capacitor if used. The total capacitance should not exceed 18.8 μ F.
SD_PU_VDD	173	PO	Power supply for SD card pull-up circuit	Only for SD card pull-up circuit. Add a 1.0–3.0 μ F bypass capacitor if used. The total capacitance should not exceed 3.0 μ F.

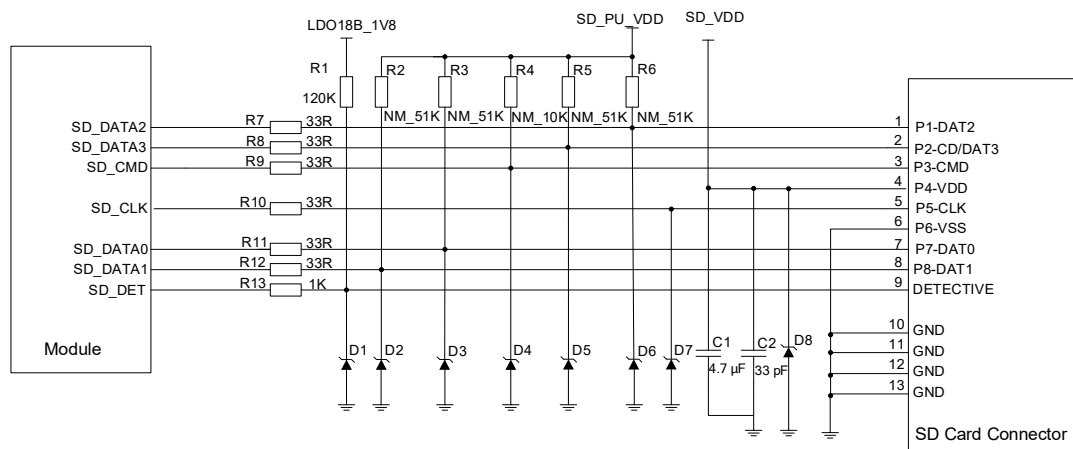


Figure 16: Reference Design of SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the high drive current, it is recommended to keep the trace width as at least 0.6 mm. To ensure the stability of drive power, you should add a 4.7 μ F and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK and SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces as 45 Ω , shield them and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 45 $\Omega \pm 10\%$, and add ground shielding.
- Trace length matching between SD_CLK and SD_CMD/SD_DATA should not exceed 2 mm.
- Trace length requirements: less than 150 mm for SDR50 mode; less than 50 mm for SDR104 mode.
- Spacing between signal traces should be 1.5 times the trace width.
- The capacitive reactance of SD_DATA[0:3], SD_CLK and SD_CMD traces should be less than 8 pF.

Table 16: SD Card Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length
SD_CLK	188	28.74
SD_CMD	180	28.71
SD_DATA0	184	29.06
SD_DATA1	185	29.34
SD_DATA2	177	29.02
SD_DATA3	181	29.18

4.4. UARTs

The module supports up to 12 groups of UART. 2 groups are configured by default, see the following table for details. and 10 of them are multiplexed from other interfaces, see **Table 21**.

2 groups of UART:

- UART: 4-wire UART with the speed rate up to 4 Mbps, which supports RTS and CTS hardware flow control
- DBG_UART: 2-wire UART, dedicated for debugging.

Table 17: Pin Description of UARTs

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	317	DO	Debug UART transmit	Cannot be used for generic GPIO. If unused, keep them open. Test points must be reserved.
DBG_RXD	320	DI	Debug UART receive	
UART_TXD	308	DO	UART transmit	
UART_RXD	309	DI	UART receive	
UART_RTS	305	DO	Request to send signal from the module	If unused, keep them open.
UART_CTS	306	DI	Clear to send signal to the module	

UART is a 4-wire UART with 1.8 V power domain. You can use a level-shifting chip between the module and peripheral's UART if the peripheral is equipped with a 3.3 V UART:

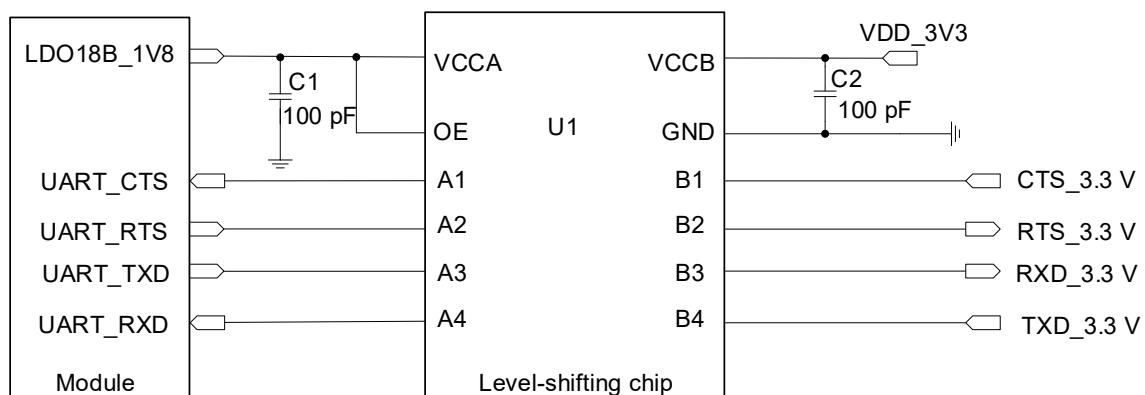


Figure 17: Reference Design of UART with Level-shifting Chip (UART)

The following circuit shows a reference design for the communication between the module and a PC with a standard RS-232 level-shifting chip.

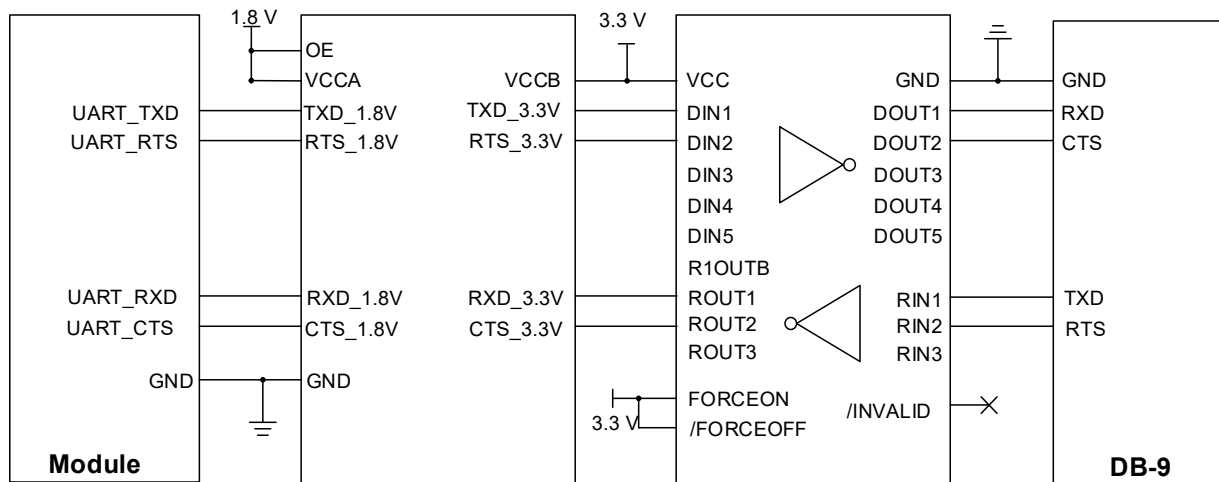


Figure 18: Reference Design of UART with RS-232 Level-shifting Chip (UART)

NOTE

The level-shifting circuits of debug UART are similar to that of UART. For the reference designs, refer to that of UART (**Figure 17** and **Figure 18**).

4.5. SPI

The module provides 10 groups of SPI, 1 group is configured by default, and supports master mode only. Other 9 groups are multiplexed from GPIO pins, see **Table 21** for more details.

Table 18: Pin Description of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	197	DO	SPI clock	Supports master mode only.
SPI_CS	193	DO	SPI chip select	Supports master mode only. Pull it up internally by default.
SPI_MISO	196	DI	SPI master-in slave-out	Supports master mode only.
SPI_MOSI	194	DO	SPI master-out slave-in	

4.6. I2C Interfaces

The module supports up to 16 groups of I2C interfaces.

- 3 of them are generic I2C interfaces for TP, NFC and other peripheral circuits, see **Table 19**, **Table 30** and **Table 32** for details.
- 5 of them are dedicated I2C interfaces for cameras and sensors, see **Table 24** and **Table 31** for details.
- 8 of them are multiplexed from other interfaces, see **Table 21**.

All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. SENSOR_I2C only supports sensors of ADSP architecture. CAM_I2C signals are controlled by Linux Kernel code and supports connection with video output related devices.

Table 19: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	192	OD	I2C serial clock	External pull-up to 1.8 V with 2.2 kΩ resistors is required. If unused, keep them open.
I2C_SDA	189	OD	I2C serial data	

4.7. I2S Interfaces

The module supports up to 4 groups of I2S interfaces. 2 of them are default I2S interfaces. The reference power domain is 1.8 V, see the table below. 2 of them are multiplexed from other interfaces, see **Table 21**.

Table 20: Pin Description of I2S Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MI2S_MCLK	142	DO	I2S master clock	
MI2S_SCLK	140	DO	I2S clock	
MI2S_WS	137	DO	I2S word select	
MI2S_DATA0	133	DIO	I2S data channel 0	
MI2S_DATA1	136	DIO	I2S data channel 1	

LPI_MI2S_SCLK	138	DO	LPI I2S serial clock	
LPI_MI2S_WS	139	DO	LPI I2S word select	
LPI_MI2S_DATA0	135	DIO	LPI I2S data channel 0	
LPI_MI2S_DATA1	134	DIO	LPI I2S data channel 1	
LPI_MI2S_DATA2	130	DIO	LPI I2S data channel 2	
LPI_MI2S_DATA3	131	DIO	LPI I2S data channel 3	
CODEC_RST_N	126	DO	Audio Codec reset	Cannot be pulled up during the turn-on process.

4.8. UART/SPI/I2C/I2S Multiplexing Relationship

The module supports up to 15 configurable interfaces, which can be configured as UART, SPI, I2C or I2S interfaces. Specific multiplexing relationship is shown in the following table (dedicated I2C interfaces, dedicated debug UART and interfaces already used inside the module are not included):

Table 21: UART/SPI/I2C/I2S Multiplexing Relationship

Channel	Pin No.	Pin Name	GPIO No.	Multiplexing Function			
				UART	SPI	I2C	I2S
QUP0-SE0	189	I2C_SDA	GPIO_0	UART00_CTS	SPI00_MISO	I2C00_SDA	-
	192	I2C_SCL	GPIO_1	UART00_RTS	SPI00_MOSI	I2C00_SCL	-
	605	PCIE1_RST_N	GPIO_2	UART00_TXD	SPI00_CLK	-	-
	607	PCIE1_WAKE_N	GPIO_3	UART00_RXD	SPI00_CS0	-	-
QUP0-SE2	311	GPIO_8	GPIO_8	-	-	I2C02_SDA	-
	307	GPIO_9	GPIO_9	-	-	I2C02_SCL	-
QUP0-SE3	198	GPIO_12	GPIO_12	UART03_CTS	SPI03_MISO	I2C03_SDA	-
	191	GPIO_13	GPIO_13	UART03_RTS	SPI03_MOSI	I2C03_SCL	-
	183	GPIO_14	GPIO_14	UART03_TXD	SPI03_CLK	-	-

	187	GPIO_15	GPIO_15	UART03_RXD	SPI03_CS0	-	-
QUP0-SE4	111	GPIO_16	GPIO_16	UART04_CTS	SPI04_MISO	I2C04_SDA	-
	110	GPIO_17	GPIO_17	UART04_RTS	SPI04_MOSI	I2C04_SCL	-
	122	GPIO_18	GPIO_18	UART04_TXD	SPI04_CLK	-	-
	119	GPIO_19	GPIO_19	UART04_RXD	SPI04_CS0	-	-
QUP1-SE0	351	GPIO_32	GPIO_32	UART10_CTS	SPI10_MISO	I2C10_SDA	-
	170	GPIO_33	GPIO_33	UART10_RTS	SPI10_MOSI	I2C10_SCL	-
	315	GPIO_34	GPIO_34	UART10_TXD	SPI10_CLK	-	-
	178	GPIO_35	GPIO_35	UART10_RXD	SPI10_CS0	-	-
QUP1-SE1	106	NFC_I2C_SDA*	GPIO_36	UART11_CTS	SPI11_MISO	I2C11_SDA	-
	107	NFC_I2C_SCL*	GPIO_37	UART11_RTS	SPI11_MOSI	I2C11_SCL	-
	98	NFC_EN*	GPIO_38	UART11_TXD	SPI11_CLK	-	-
	102	NFC_CLK_REQ*	GPIO_39	UART11_RXD	SPI11_CS0	-	-
QUP1-SE2	103	NFC_DWL_REQ*	GPIO_40	UART12_CTS	SPI12_MISO	I2C12_SDA	-
	99	NFC_INT*	GPIO_41	UART12_RTS	SPI12_MOSI	I2C12_SCL	-
	318	GPIO_42	GPIO_42	UART12_TXD	SPI12_CLK	-	-
	155	GPIO_43	GPIO_43	UART12_RXD	SPI12_CS0	-	-

QUP1-SE3	202	GPIO_44	GPIO_44	UART13_CTS	SPI13_MISO	I2C13_SDA	-
	203	GPIO_45	GPIO_45	UART13_RTS	SPI13_MOSI	I2C13_SCL	-
	207	GPIO_46	GPIO_46	UART13_TXD	SPI13_CLK	-	-
	319	GPIO_47	GPIO_47	UART13_RXD	SPI13_CS0	-	-
QUP1-SE4	306	UART_CTS	GPIO_48	UART14_CTS	SPI14_MISO	I2C14_SDA	-
	305	UART_RTS	GPIO_49	UART14_RTS	SPI14_MOSI	I2C14_SCL	-
	308	UART_TXD	GPIO_50	UART14_TXD	SPI14_CLK	-	-
	309	UART_RXD	GPIO_51	UART14_RXD	SPI14_CS0	-	-
	324	TP_RST	GPIO_55	-	SPI14_CS1	-	-
	378	LCD_RST	GPIO_54	-	SPI14_CS2	-	-
	98	NFC_EN*	GPIO_38	-	SPI14_CS3	-	-
QUP1-SE5	325	TP_I2C_SDA	GPIO_52	UART15_CTS	SPI15_MISO	I2C15_SDA	-
	328	TP_I2C_SCL	GPIO_53	UART15_RTS	SPI15_MOSI	I2C15_SCL	-
	378	LCD_RST	GPIO_54	UART15_TXD	SPI15_CLK	-	-
	324	TP_RST	GPIO_55	UART15_RXD	SPI15_CS0	-	-
QUP1-SE6	196	SPI_MISO	GPIO_56	UART16_CTS	SPI16_MISO	I2C16_SDA	-
	194	SPI_MOSI	GPIO_57	UART16_RTS	SPI16_MOSI	I2C16_SCL	-

	197	SPI_CLK	GPIO_58	UART16_TXD	SPI16_CLK	-	-
	193	SPI_CS	GPIO_59	UART16_RXD	SPI16_CS0	-	-
	322	GPIO_62	GPIO_62	-	SPI16_CS1	-	-
	326	GPIO_63	GPIO_63	-	SPI16_CS2	-	-
	308	UART_TXD	GPIO_50	-	SPI16_CS3	-	-
LPI_QUP0_SE1	152	LPI_SENSOR_I2C1_SDA	GPIO_161	-	-	LPI_I2C01_SDA	-
	149	LPI_SENSOR_I2C1_SCL	GPIO_162	-	-	LPI_I2C01_SCL	-
LPI_QUP0_SE2	153	LPI_SENSOR_I2C2_SDA	GPIO_163	LPI_UART02_CTS	LPI_SPI02_MISO	LPI_I2C02_SDA	-
	156	LPI_SENSOR_I2C2_SCL	GPIO_164	LPI_UART02_RTS	LPI_SPI02_MOSI	LPI_I2C02_SCL	-
	150	GPIO_165	GPIO_165	LPI_UART02_TXD	LPI_SPI02_SCLK	-	-
	154	GPIO_166	GPIO_166	LPI_UART02_RXD	LPI_SPI02_CS_0	-	-
	152	LPI_SENSOR_I2C1_SDA	GPIO_161	-	LPI_SPI02_CS_1	-	-
	144	LPI_DMIC1_CLK	GPIO_150	-	-	-	LPI_I2S1_SCLK
	141	LPI_DMIC1_DATA	GPIO_151	-	-	-	LPI_I2S1_WS
	145	LPI_DMIC2_CLK	GPIO_152	-	-	-	LPI_I2S1_DATA0
	148	LPI_DMIC2_DATA	GPIO_153	-	-	-	LPI_I2S1_DATA1
	142	MI2S_MCLK	GPIO_96	-	-	-	PRI_MI2S_MCLK

140	MI2S_SCLK	GPIO_97	-	-	-	MI2S0_SCLK
137	MI2S_WS	GPIO_100	-	-	-	MI2S0_WS
133	MI2S_DATA0	GPIO_98	-	-	-	MI2S0_DATA0
136	MI2S_DATA1	GPIO_99	-	-	-	MI2S0_DATA1
190	HALL_INT	GPIO_101	-	-	-	MI2S2_SCLK
158	GYRO_INT	GPIO_102	-	-	-	MI2S2_DATA0
161	ACCEL_INT	GPIO_103	-	-	-	MI2S2_WS
186	MAG_INT	GPIO_104	-	-	-	MI2S2_DATA1
138	LPI_MI2S_SCLK	GPIO_144	-	-	-	LPI_MI2S_SCLK
139	LPI_MI2S_WS	GPIO_145	-	-	-	LPI_MI2S_WS
135	LPI_MI2S_DATA0	GPIO_146	-	-	-	LPI_MI2S_DATA0
134	LPI_MI2S_DATA1	GPIO_147	-	-	-	LPI_MI2S_DATA1
130	LPI_MI2S_DATA2	GPIO_148	-	-	-	LPI_MI2S_DATA2
131	LPI_MI2S_DATA3	GPIO_149	-	-	-	LPI_MI2S_DATA3

NOTE

1. QUP-SE is flexible and supports four types of interfaces: UART, SPI, I2C and I2S.
2. Note that the same set of QUP-SE cannot support two protocols at the same time. For example: the same set of QUP cannot support UART and I2C at the same time. If a protocol only occupies part of the pins of this group of QUP, other pins can only be used for GPIO.
3. For more information about multiplexing, see **document [2]**.

4.9. ADC Interfaces

The module provides 6 ADC interfaces which support up to 15-bit resolution.

Table 22: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	399	AI	General-purpose ADC interface	The maximum input voltage is 1.8 V.
ADC1	11	AI		
ADC2	15	AI		
ADC3	403	AI		
ADC4	75	AI		
ADC5	383	AI		

4.10. LCM Interface

The module provides one LCM interface, which is MIPI_DSI standard compliant. The interface supports four data lines for high-speed differential data transmission. The data rate can reach up to 2.5 Gbps per lane. SG555D series module supports FHD+ display (1200 × 2520 @ 120 fps). SG565D series module supports FHD+ display (1200 × 2520 @ 144 fps).

Table 23: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PWM1	340	DO	PWM1 output	Backlight control.
DSI_CLK_P	366	AO	LCD MIPI clock (+)	85 Ω differential impedance.
DSI_CLK_N	370	AO	LCD MIPI clock (-)	
DSI_LN0_P	380	AO	LCD MIPI data 0 (+)	
DSI_LN0_N	377	AO	LCD MIPI data 0 (-)	

DSI_LN1_P	376	AO	LCD MIPI data 1 (+)	
DSI_LN1_N	373	AO	LCD MIPI data 1 (-)	
DSI_LN2_P	372	AO	LCD MIPI data 2 (+)	
DSI_LN2_N	369	AO	LCD MIPI data 2 (-)	
DSI_LN3_P	368	AO	LCD MIPI data 3 (+)	
DSI_LN3_N	365	AO	LCD MIPI data 3 (-)	
LCD_TE	374	DI	LCD tearing effect	
LCD_RST	378	DO	LCD reset	External pull-up is not required.

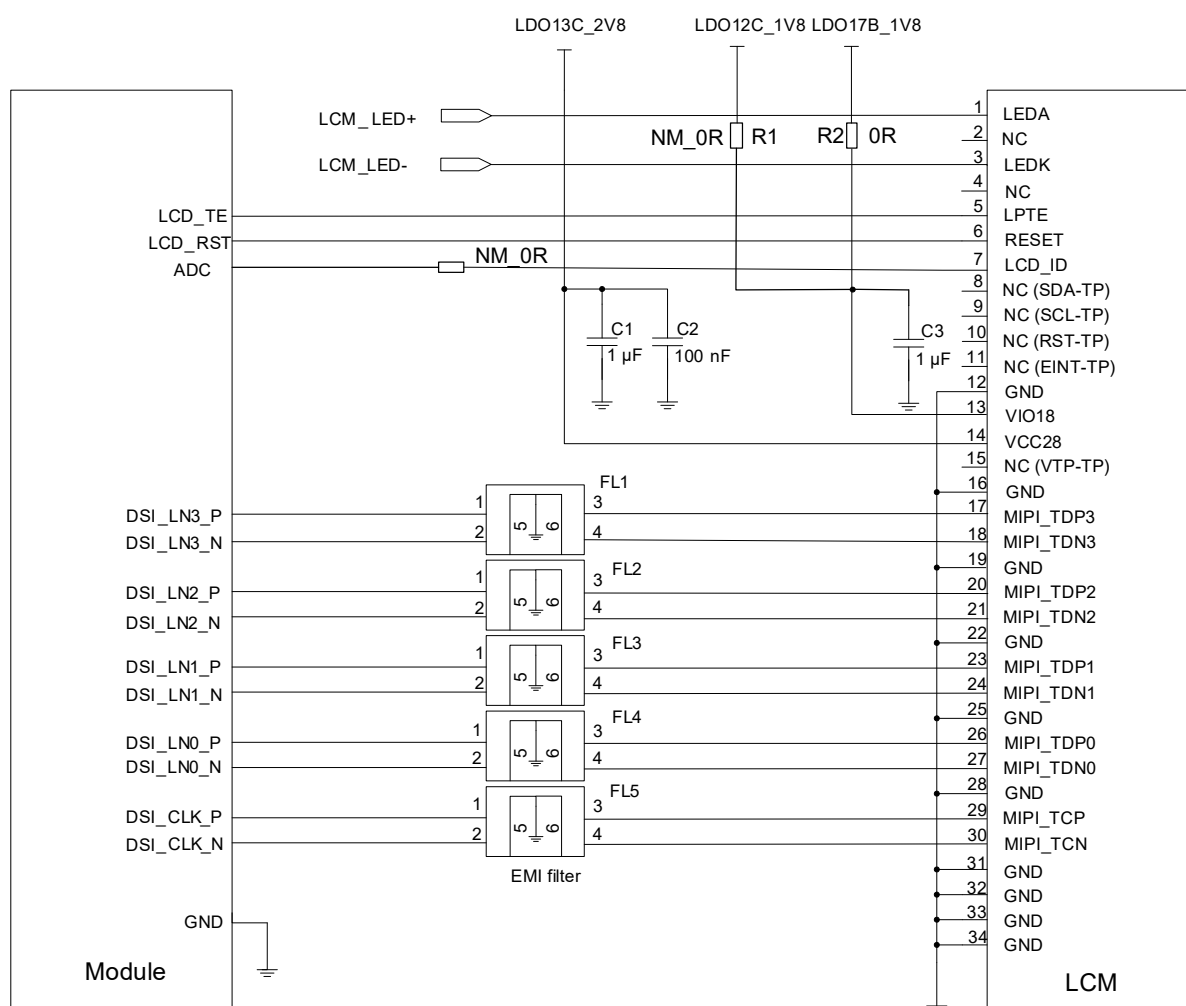


Figure 19: Reference Design of LCM Interface

MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID of LCM to the GPIO of the module to distinguish different screens by high/low level detection. But note that the output voltage of LCD_ID should not exceed the voltage range of the GPIO.

You can design an external backlight driver circuit for LCM according to the actual requirement. PWM can be used for backlight brightness adjustment.

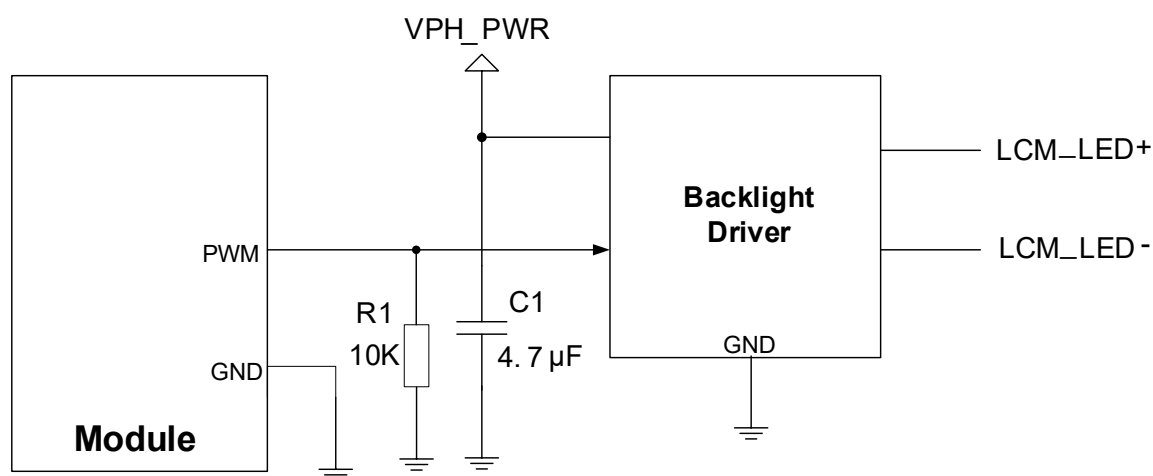


Figure 20: Reference Design of LCM Interface External Backlight Driver

4.11. Camera Interfaces

Based on MIPI_CSI standard, the data rate is up to 2.5 Gbps/lane. The module supports 2 cameras (4 lane + 4 lane) or 3 cameras (4 lane + 4 lane + 4 lane) or 5 cameras (4 lane + 4 lane + 4 lane + 2 lane + 1 lane). SG555D series module (FP1) supports up to 2 concurrently working cameras (22 MP + 22 MP @ 30 fps ZSL), and the single camera supports up to 36 MP @ 30 fps ZSL. SG555D series module (FP2.5*) and SG565D series module support up to 3 concurrently working cameras (22 MP + 22 MP + 22 MP @ 30 fps ZSL or 36 MP + 22 MP @ 30 fps ZSL). And the single camera supports up to 36 MP @ 30 fps ZSL. The video and photo quality are determined by various factors such as the camera sensor, camera lens.

Table 24: Pin Description of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI0_CLK_P	14	AI	MIPI CSI0 clock (+)	
CSI0_CLK_N	18	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	16	AI	MIPI CSI0 data 0 (+)	
CSI0_LN0_N	17	AI	MIPI CSI0 data 0 (-)	
CSI0_LN1_P	20	AI	MIPI CSI0 data 1 (+)	85 Ω differential impedance.
CSI0_LN1_N	21	AI	MIPI CSI0 data 1 (-)	
CSI0_LN2_P	24	AI	MIPI CSI0 data 2 (+)	
CSI0_LN2_N	25	AI	MIPI CSI0 data 2 (-)	
CSI0_LN3_P	28	AI	MIPI CSI0 data 3 (+)	
CSI0_LN3_N	29	AI	MIPI CSI0 data 3 (-)	
CAM0_MCLK	30	DO	Master clock of camera 0	
CAM0_RST	26	DO	Reset of camera 0	
CSI1_CLK_P	38	AI	MIPI CSI1 clock (+)	
CSI1_CLK_N	42	AI	MIPI CSI1 clock (-)	
CSI1_LN0_P	40	AI	MIPI CSI1 data 0 (+)	
CSI1_LN0_N	41	AI	MIPI CSI1 data 0 (-)	
CSI1_LN1_P	44	AI	MIPI CSI1 data 1 (+)	85 Ω differential impedance.
CSI1_LN1_N	45	AI	MIPI CSI1 data 1 (-)	
CSI1_LN2_P	48	AI	MIPI CSI1 data 2 (+)	
CSI1_LN2_N	49	AI	MIPI CSI1 data 2 (-)	
CSI1_LN3_P	52	AI	MIPI CSI1 data 3 (+)	
CSI1_LN3_N	53	AI	MIPI CSI1 data 3 (-)	
CAM1_MCLK	54	DO	Master clock of camera 1	
CAM1_RST	50	DO	Reset of camera 1	

CSI2_CLK_P	390	AI	MIPI CSI2 clock (+)	85 Ω differential impedance.
CSI2_CLK_N	386	AI	MIPI CSI2 clock (-)	
CSI2_LN0_P	392	AI	MIPI CSI2 data 0 (+)	
CSI2_LN0_N	389	AI	MIPI CSI2 data 0 (-)	
CSI2_LN1_P	388	AI	MIPI CSI2 data 1 (+)	
CSI2_LN1_N	385	AI	MIPI CSI2 data 1 (-)	
CSI2_LN2_P	396	AI	MIPI CSI2 data 2 (+)	
CSI2_LN2_N	393	AI	MIPI CSI2 data 2 (-)	
CSI2_LN3_P	400	AI	MIPI CSI2 data 3 (+)	
CSI2_LN3_N	397	AI	MIPI CSI2 data 3 (-)	
CAM2_MCLK	398	DO	Master clock of camera 2	
CAM2_RST	384	DO	Reset of camera 2	
CSI3_CLK_P	62	AI	MIPI CSI3 clock (+)	85 Ω differential impedance.
CSI3_CLK_N	66	AI	MIPI CSI3 clock (-)	
CSI3_LN0_P	60	AI	MIPI CSI3 data 0 (+)	
CSI3_LN0_N	61	AI	MIPI CSI3 data 0 (-)	
CSI3_LN1_P	68	AI	MIPI CSI3 data 1 (+)	
CSI3_LN1_N	69	AI	MIPI CSI3 data 1 (-)	
CSI3_LN2_P	64	AI	MIPI CSI3 data 2 (+)	
CSI3_LN2_N	65	AI	MIPI CSI3 data 2 (-)	
CSI3_LN3_P	72	AI	MIPI CSI3 data 3 (+)	
CSI3_LN3_N	73	AI	MIPI CSI3 data 3 (-)	
CAM3_MCLK	74	DO	Master clock of camera 3	
CAM3_RST	67	DO	Reset of camera 3	
VREG_L1P_1P05	116	PO	Power supply for DVDD of cameras 1 and 2	Add a bypass capacitor if used. The total capacitance should not exceed 45.3 μ F.
VREG_L2P_1P1	121	PO	Power supply for DVDD of cameras 0 and 3	

VREG_L3P_2P8	113	PO	Power supply for AVDD of cameras 1 and 3	Add a bypass capacitor if used. The total capacitance should not exceed 19 μ F.
VREG_L4P_2P9	124	PO	Power supply for AVDD of camera 0	
VREG_L5P_2P8	128	PO	Power supply for AFVDD of camera 0	
VREG_L6P_1P8	117	PO	Power supply for DOVDD of cameras 0–3	
VREG_L7P_2P8	120	PO	Power supply for AVDD of camera 2	
CAM2_I2C_SDA	71	OD	Cameras 2&3 I2C data	Dedicated for camera. External pull-up to 1.8 V with 2.2 k Ω resistors is required. If unused, keep them open.
CAM2_I2C_SCL	70	OD	Cameras 2&3 I2C clock	
CAM1_I2C_SDA	401	OD	Camera1 I2C data	
CAM1_I2C_SCL	402	OD	Camera1 I2C clock	
CAM0_I2C_SDA	33	OD	Camera0 I2C data	
CAM0_I2C_SCL	36	OD	Camera0 I2C clock	

The following is a reference design of dual-camera application:

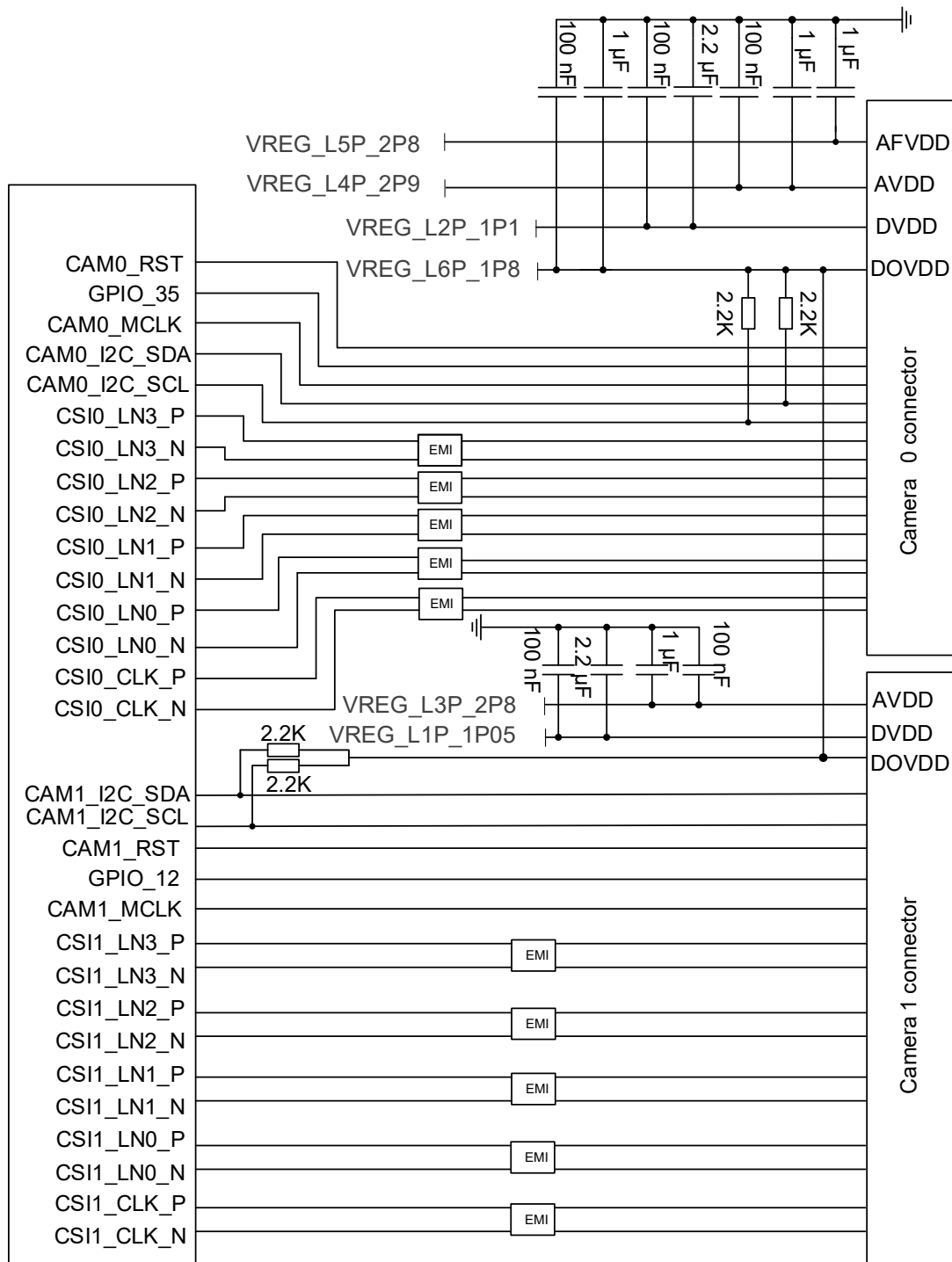


Figure 21: Reference Design of Two-Camera Application

The following is a reference design of triple-camera application:



4.11.1. MIPI Design Considerations

To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Pay attention to the pin description of LCM and camera interfaces. Different video devices may vary in the definitions of their connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential impedance should be controlled to 85 Ω . Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. For the same video device, keep all the MIPI traces be of the same length. To avoid crosstalk, a spacing of 1.5 times the trace width is recommended among MIPI signal traces. During 85 Ω impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- Route MIPI traces according to the following requirements:
 - a) Control the differential impedance to 85 $\Omega \pm 10\%$;
 - b) Control intra-lane length matching within 0.7 mm;
 - c) Control inter-lane length matching within 2.1 mm.

Table 25: MIPI Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching
DSI_CLK_N	370	47.22	0.01
DSI_CLK_P	366	47.21	
DSI_LN0_N	377	47.11	0.03
DSI_LN0_P	380	47.14	
DSI_LN1_N	373	47.46	0.06
DSI_LN1_P	376	47.40	
DSI_LN2_N	369	46.95	0.03
DSI_LN2_P	372	46.92	
DSI_LN3_N	365	47.23	0.03
DSI_LN3_P	368	47.20	
CSI0_CLK_N	18	53.00	0
CSI0_CLK_P	14	53.00	

CSI0_LN0_N	17	52.92	0
CSI0_LN0_P	16	52.92	
CSI0_LN1_N	21	53.04	0.03
CSI0_LN1_P	20	53.01	
CSI0_LN2_N	25	53.19	0.04
CSI0_LN2_P	24	53.15	
CSI0_LN3_N	29	53.02	0
CSI0_LN3_P	28	53.02	
CSI1_CLK_N	42	37.25	0.01
CSI1_CLK_P	38	37.24	
CSI1_LN0_N	41	37.29	0.04
CSI1_LN0_P	40	37.33	
CSI1_LN1_N	45	37.05	0.09
CSI1_LN1_P	44	37.14	
CSI1_LN2_N	49	37.45	0.07
CSI1_LN2_P	48	37.38	
CSI1_LN3_N	53	37.32	0.06
CSI1_LN3_P	52	37.38	
CSI2_CLK_N	386	38.67	0
CSI2_CLK_P	390	38.67	
CSI2_LN0_N	389	38.75	0.15
CSI2_LN0_P	392	38.90	
CSI2_LN1_N	385	38.99	0.01
CSI2_LN1_P	388	38.98	
CSI2_LN2_N	393	38.63	0.01

CSI2_LN2_P	396	38.64	
CSI2_LN3_N	397	39.09	
CSI2_LN3_P	400	38.90	0.19
CSI3_CLK_N	66	57.71	
CSI3_CLK_P	62	57.61	0.1
CSI3_LN0_N	61	57.67	
CSI3_LN0_P	60	57.69	0.02
CSI3_LN1_N	69	57.75	
CSI3_LN1_P	68	57.73	0.02
CSI3_LN2_N	65	57.77	
CSI3_LN2_P	64	57.83	0.06
CSI3_LN3_N	73	57.87	
CSI3_LN3_P	72	57.84	0.03

Table 26: Mapping of CSI Data Rates and Trace Length (D-PHY)

Data Rates	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.5	< 260
	152.4	-1	< 190
750 Mbps/lane	76.2	-0.7	< 210
	152.4	-1.15	< 155
1.0 Gbps/lane	76.2	-0.75	< 200
	152.4	-1.4	< 125
1.5 Gbps/lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/lane	76.2	-1.3	< 170
	152.4	-2.3	< 90

2.5 Gbps/lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 27: Mapping of DSI Data Rates and Trace Length (D-PHY)

Data Rates	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	3	-0.8	< 280
	6	-1.4	< 210
750 Mbps/lane	3	-1	< 210
	6	-1.5	< 150
1.0 Gbps/lane	3	-1.1	< 200
	6	-1.7	< 100
1.5 Gbps/lane	3	-1.2	< 135
	6	-2.2	< 40
2.1 Gbps/lane	3	-1.6	< 110
	6	-2.8	< 80
2.5 Gbps/lane	76.2	-2.1	< 70
	152.4	-3.5	< 0

4.12. PCIe Interfaces

The module provides 2 PCIe interfaces: PCIe0 (1-lane, Gen3), and PCIe1 (2-lane, Gen3), its maximum rate is 8 Gbps.

Table 28: Pin Description of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE0_REFCLK_P	278	AIO	PCIe0 reference clock (+)	
PCIE0_REFCLK_M	274	AIO	PCIe0 reference clock (-)	
PCIE0_RX_P	291	AI	PCIe0 receive 0 (+)	85 Ω differential impedance.
PCIE0_RX_M	287	AI	PCIe0 receive 0 (-)	
PCIE0_TX_P	286	AO	PCIe0 transmit 0 (+)	
PCIE0_TX_M	283	AO	PCIe0 transmit 0 (-)	
PCIE0_RST_N	254	DO	PCIe0 reset	
PCIE0_CLKREQ_N	262	DI	PCIe0 clock request	Pull it up internally by default.
PCIE0_WAKE_N	258	DI	PCIe0 wake up	
PCIE1_REFCLK_P	594	AIO	PCIe1 reference clock (+)	
PCIE1_REFCLK_M	593	AIO	PCIe1 reference clock (-)	
PCIE1_RX0_P	597	AI	PCIe1 receive 0 (+)	85 Ω differential impedance. PCIe1 is not supported by default for SG555D series, and you can contact Quectel Technical Support if necessary. SG565D series supports PCIe1.
PCIE1_RX0_M	596	AI	PCIe1 receive 0 (-)	
PCIE1_RX1_P	599	AI	PCIe1 receive 1 (+)	
PCIE1_RX1_M	598	AI	PCIe1 receive 1 (-)	
PCIE1_TX0_P	601	AO	PCIe1 transmit 0 (+)	
PCIE1_TX0_M	600	AO	PCIe1 transmit 0 (-)	
PCIE1_TX1_P	603	AO	PCIe1 transmit 1 (+)	
PCIE1_TX1_M	602	AO	PCIe1 transmit 1 (-)	

PCIE1_RST_N	605	DO	PCle1 reset
PCIE1_CLKREQ_N	606	DI	PCle1 clock request
PCIE1_WAKE_N	607	DI	PCle1 wake up

Table 29: PCIe Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching
PCIE0_REFCLK_P	278	54.21	0.08
PCIE0_REFCLK_M	274	54.29	
PCIE0_RX_P	291	55.75	0.05
PCIE0_RX_M	287	55.70	
PCIE0_TX_P	286	54.53	0.14
PCIE0_TX_M	283	54.39	
PCIE1_REFCLK_P	594	58.44	0.18
PCIE1_REFCLK_M	593	58.26	
PCIE1_TX0_P	601	58.29	0.06
PCIE1_TX0_M	600	58.35	
PCIE1_TX1_P	603	57.52	0.13
PCIE1_TX1_M	602	57.39	
PCIE1_RX0_P	597	57.31	0.17
PCIE1_RX0_M	596	57.48	
PCIE1_RX1_P	599	59.52	0.04
PCIE1_RX1_M	598	59.56	

4.13. Touch Panel Interface

The module provides 1 I2C interface for connection with the Touch Panel (TP), and provides the corresponding power supply and interrupt pins.

Table 30: Pin Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	324	DO	TP reset	
TP_INT	321	DI	TP interrupt	
TP_I2C_SCL	328	OD	TP I2C clock	External pull-up to 1.8 V with 2.2 kΩ resistors is required. If unused, keep them open.
TP_I2C_SDA	325	OD	TP I2C data	

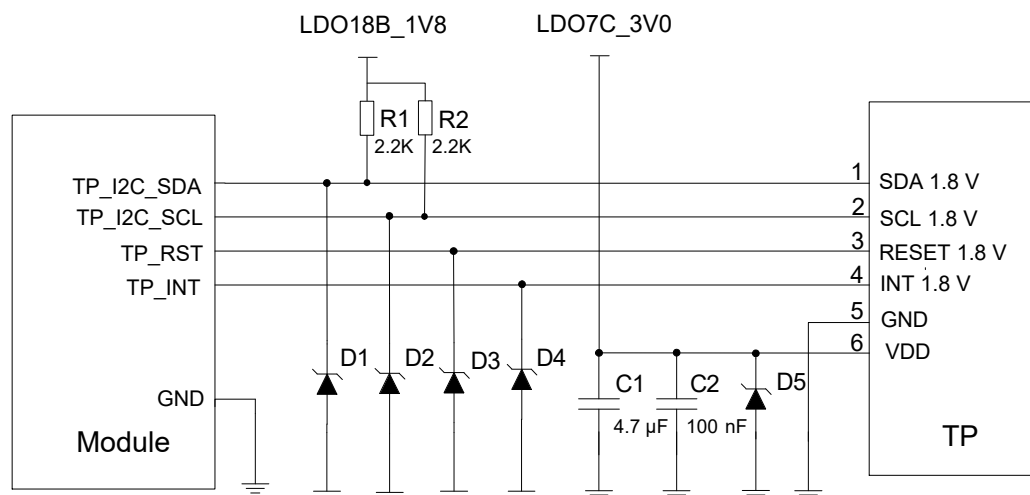


Figure 23: Reference Design of Touch Panel Interface

4.14. Sensor Interfaces

The module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, pressure sensor.

Table 31: Pin Description of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LPI_SENSOR_I2C1_SDA	152	OD	I2C1 data for external sensor	Dedicated for sensors. External pull-up to 1.8 V with 2.2 kΩ resistors is required. If unused, keep them open.
LPI_SENSOR_I2C1_SCL	149	OD	I2C1 clock for external sensor	
LPI_SENSOR_I2C2_SDA	153	OD	I2C2 data for external sensor	
LPI_SENSOR_I2C2_SCL	156	OD	I2C2 clock for external sensor	
GYRO_INT	158	DI	Gyroscope sensor interrupt	
ACCEL_INT	161	DI	Acceleration sensor interrupt	
MAG_INT	186	DI	Magnetic sensor interrupt	
ALPS_INT	157	DI	Light/proximity sensor interrupt	
HALL_INT	190	DI	Hall sensor interrupt	

4.15. NFC Interface*

The module provides 1 NFC interface.

Table 32: Pin Description of NFC Interface

Pin Name	Pin No.	I/O	Description	Comment
NFC_CLK	95	DO	NFC clock	
NFC_CLK_REQ	102	DI	NFC clock request	
NFC_DWL_REQ	103	DO	NFC download control request	

NFC_EN	98	DO	NFC enable	Pull it up internally by default.
NFC_INT	99	DI	NFC interrupt	
NFC_I2C_SDA	106	OD	NFC I2C data	External pull-up to 1.8 V with 2.2 k Ω resistors is required.
NFC_I2C_SCL	107	OD	NFC I2C clock	If unused, keep them open.

4.16. GPIOs

The module provides 38 GPIOs with the power domain of 1.8 V:

Table 33: Pin Description of GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO_6	94	DIO	General-purpose input/output	Interrupt wakeup is supported.
GPIO_7	19	DIO		
GPIO_8	311	DIO		
GPIO_9	307	DIO		
GPIO_12	198	DIO		Interrupt wakeup is supported.
GPIO_13	191	DIO		
GPIO_14	183	DIO		Cannot be pulled up during the turn-on process.
GPIO_15	187	DIO		Cannot be pulled up during the turn-on process. Interrupt wakeup is supported.
GPIO_16	111	DIO		Interrupt wakeup is supported.
GPIO_17	110	DIO		
GPIO_18	122	DIO		
GPIO_19	119	DIO		Interrupt wakeup is supported.
GPIO_24	43	DIO		
GPIO_32	351	DIO		

GPIO_33	170	DIO	
GPIO_34	315	DIO	
GPIO_35	178	DIO	Interrupt wakeup is supported.
GPIO_42	318	DIO	
GPIO_43	155	DIO	Interrupt wakeup is supported.
GPIO_44	202	DIO	Do not pull GPIO_45 up during the turn-on process.
GPIO_45	203	DIO	
GPIO_46	207	DIO	
GPIO_47	319	DIO	
GPIO_61	51	DIO	Interrupt wakeup is supported.
GPIO_62	322	DIO	
GPIO_63	326	DIO	Cannot be pulled up during the turn-on process. Interrupt wakeup is supported.
GPIO_68	123	DIO	Interrupt wakeup is supported.
GPIO_93	147	DIO	Cannot be pulled up during the turn-on process. Interrupt wakeup is supported.
GPIO_112	163	DIO	
GPIO_116	159	DIO	
GPIO_119	210	DIO	Interrupt wakeup is supported.
GPIO_121	310	DIO	
GPIO_133	175	DIO	
GPIO_134	167	DIO	
GPIO_140	338	DIO	
GPIO_158	151	DIO	Interrupt wakeup is supported.
GPIO_165	150	DIO	
GPIO_166	154	DIO	Interrupt wakeup is supported.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to conduct a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Wi-Fi & Bluetooth

The module provides a shared antenna interface: ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The impedance shall be kept as 50 Ω . You can connect external antennas such as PCB antenna, sucker antenna or ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 34: Pin Description of Wi-Fi & Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	92	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance.

Table 35: Wi-Fi & Bluetooth Frequency (Unit: MHz)

Types	Operating Frequency
Wi-Fi 802.11	2400–2483.5 5150–5850
Bluetooth	2400–2483.5

5.1.1. Wi-Fi Overview

The module supports 2.4 GHz & 5 GHz dual-band WLAN wireless communication based on Wi-Fi 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433 Mbps. It supports following features:

- Wake-on-WLAN (WoWLAN)

- AP and STA modes
- Wi-Fi Direct
- MCS 0–MCS 7: HT20 and HT40
- MCS 0–MCS 8: VHT20
- MCS 0–MCS 9: VHT40 and VHT80

Table 36: Wi-Fi Transmitting Performance

Operating Frequency	Modulation	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	17 dBm $\pm$ 2.5 dB
	802.11b	11 Mbps	17 dBm $\pm$ 2.5 dB
	802.11g	6 Mbps	16 dBm $\pm$ 2.5 dB
	802.11g	54 Mbps	13 dBm $\pm$ 2.5 dB
	802.11n @ HT20	MCS 0	16 dBm $\pm$ 2.5 dB
	802.11n @ HT20	MCS 7	13 dBm $\pm$ 2.5 dB
	802.11n @ HT40	MCS 0	16 dBm $\pm$ 2.5 dB
	802.11n @ HT40	MCS 7	13 dBm $\pm$ 2.5 dB
5 GHz	802.11a	6 Mbps	14 dBm $\pm$ 2.5 dB
	802.11a	54 Mbps	12 dBm $\pm$ 2.5 dB
	802.11n @ HT20	MCS 0	13 dBm $\pm$ 2.5 dB
	802.11n @ HT20	MCS 7	11 dBm $\pm$ 2.5 dB
	802.11n @ HT40	MCS 0	13 dBm $\pm$ 2.5 dB
	802.11n @ HT40	MCS 7	10 dBm $\pm$ 2.5 dB
	802.11ac @ VHT20	MCS 0	13 dBm $\pm$ 2.5 dB
	802.11ac @ VHT20	MCS 8	10 dBm $\pm$ 2.5 dB
	802.11ac @ VHT40	MCS 0	13 dBm $\pm$ 2.5 dB
	802.11ac @ VHT40	MCS 9	9 dBm $\pm$ 2.5 dB
	802.11ac @ VHT80	MCS 0	11.5 dBm $\pm$ 2.5 dB

802.11ac @ VHT80

MCS 9

8 dBm $\pm$ 2.5 dB

Table 37: Wi-Fi Receiving Performance

Operating Frequency	Modulation	Rate	Sensitivity (dBm)
2.4 GHz	802.11b	1 Mbps	-93
	802.11b	11 Mbps	-86
	802.11g	6 Mbps	-87
	802.11g	54 Mbps	-72
	802.11n @ HT20	MCS 0	-87
	802.11n @ HT20	MCS 7	-69
	802.11n @ HT40	MCS 0	-84
	802.11n @ HT40	MCS 7	-66
5 GHz	802.11a	6 Mbps	-86
	802.11a	54 Mbps	-71
	802.11n @ HT20	MCS 0	-86
	802.11n @ HT20	MCS 7	-67
	802.11n @ HT40	MCS 0	-84
	802.11n @ HT40	MCS 7	-65
	802.11ac @ VHT20	MCS 0	-86
	802.11ac @ VHT20	MCS 8	-64
	802.11ac @ VHT40	MCS 0	-83
	802.11ac @ VHT40	MCS 9	-59
	802.11ac @ VHT80	MCS 0	-81
	802.11ac @ VHT80	MCS 9	-55

NOTE

The product complies with the IEEE specifications.

5.1.2. Bluetooth Overview

With built-in Bluetooth function, the module supports Bluetooth 5.0 ⁶ (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, $\pi/4$ -DQPSK modulations. It supports following features:

- Up to 7-lane wireless connections.
- Up to 3.5 Piconets simultaneously.
- One SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 38: Bluetooth Data Rates and Versions

Version	Data Rates (Mbit/s)	Maximum Application Throughput
1.2	1	> 80 kbit/s
2.0 + EDR	3	> 80 kbit/s
3.0 + HS	24	Refer to 3.0 + HS
4.0	24	Refer to 4.0 LE
5.0	24	Refer to 5.0 LE

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

⁶ This module is compatible with all mandatory functions of Bluetooth 5.0, but it does not support the optional functions of Bluetooth 5.0, such as 2 Mbps BLE, advanced broadcast extension.

Table 39: Bluetooth Transmitting and Receiving Performance (Unit: dBm)

Condition (VBAT= 4.0; Temp.: 25 °C)	Transmitting Power	Receiver sensitivity
BR	8 ±2.5 dB	-91
EDR (π/4-DQPSK)	5 ±2.5 dB	-90
EDR (8-DQPSK)	5 ±2.5 dB	-84
BLE (1 Mbps)	0 ±2.5 dB	-93

5.1.3. Reference Design

A reference design of Wi-Fi & Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default. Only a 0 Ω resistor is mounted on R1.

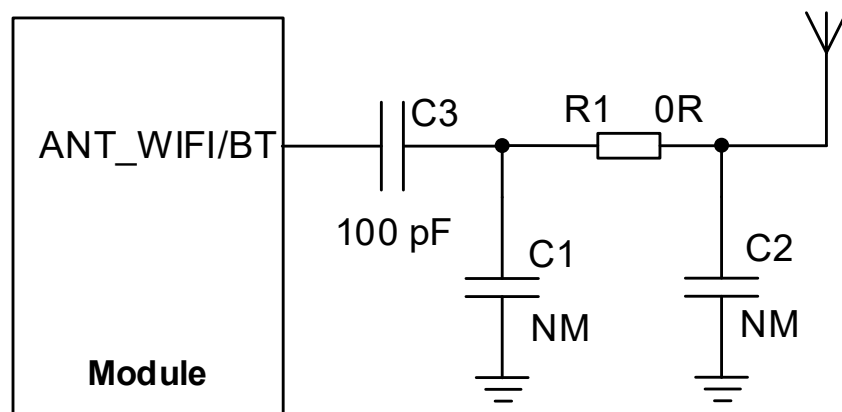


Figure 24: Reference Design of Wi-Fi & Bluetooth Antenna

NOTE

Notes on C3:

- 1) If there is DC power at the antenna port, place a capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
- 2) If there is no DC power in the peripheral design:
 - a) Do not reserve C3.
 - b) If C3 has already been reserved, it should be mounted with a component, and it is recommended to use a 0 Ω resistor. You can also match the component according to the debugging results.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to $50\ \Omega$. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

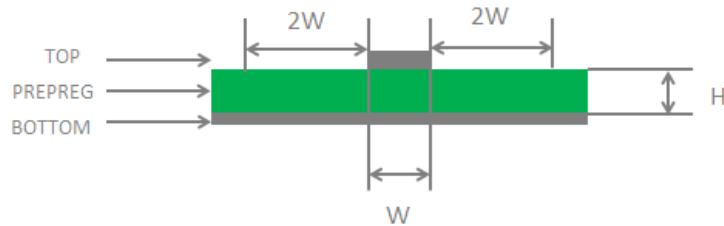


Figure 25: Microstrip Design on a 2-layer PCB

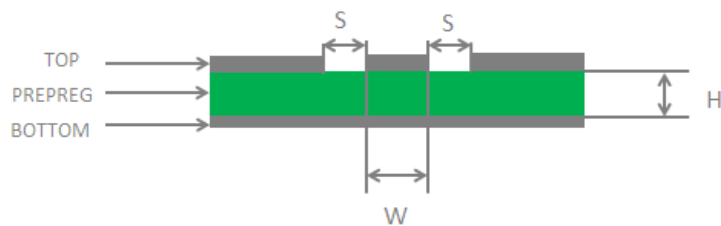


Figure 26: Coplanar Waveguide Design on a 2-layer PCB

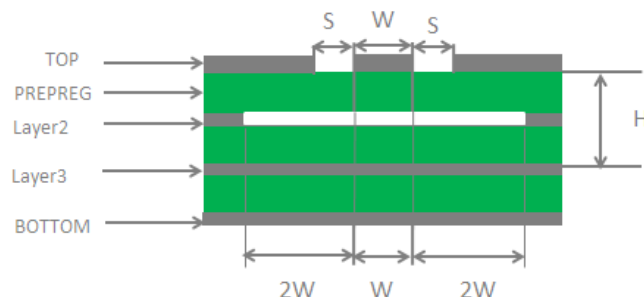


Figure 27: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

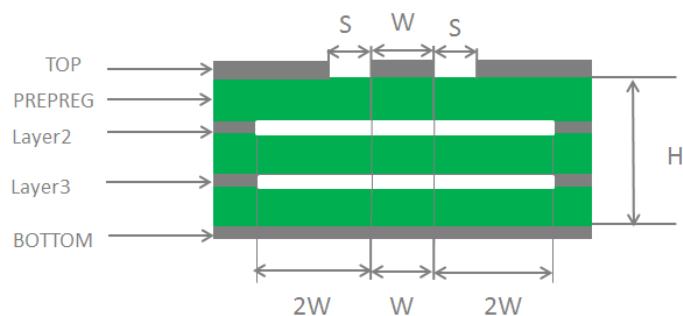


Figure 28: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to $50\ \Omega$.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135° .
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces ($2 \times W$).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document [3]**.

5.3. Requirements for Antenna Design

Table 40: Requirements for Antenna Design

Antenna Types	Requirements
Wi-Fi & Bluetooth	VSWR: ≤ 2
	Gain: 1 dBi
	Max. input power: 50 W
	Input impedance: $50\ \Omega$
	Vertical polarization
	Cable insertion loss: $< 1\ \text{dB}$

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

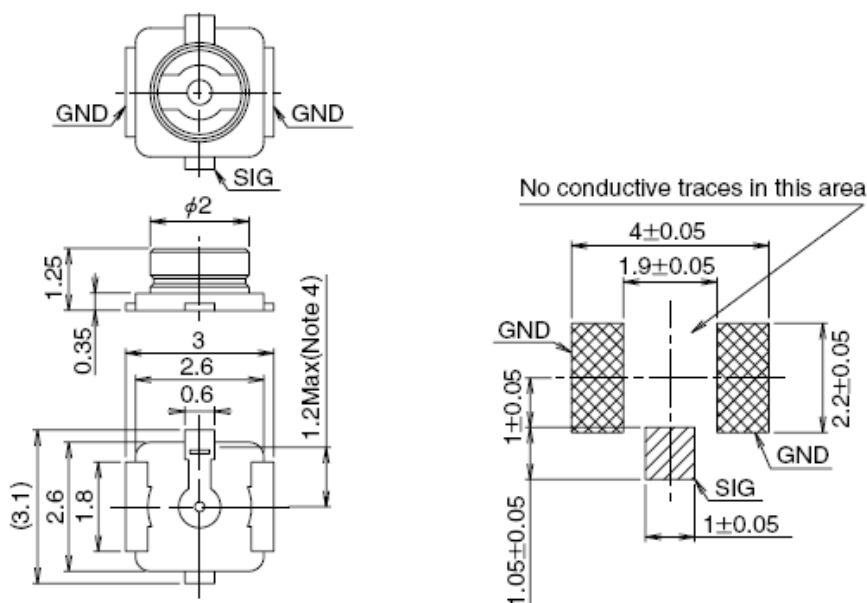


Figure 29: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 30: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector:

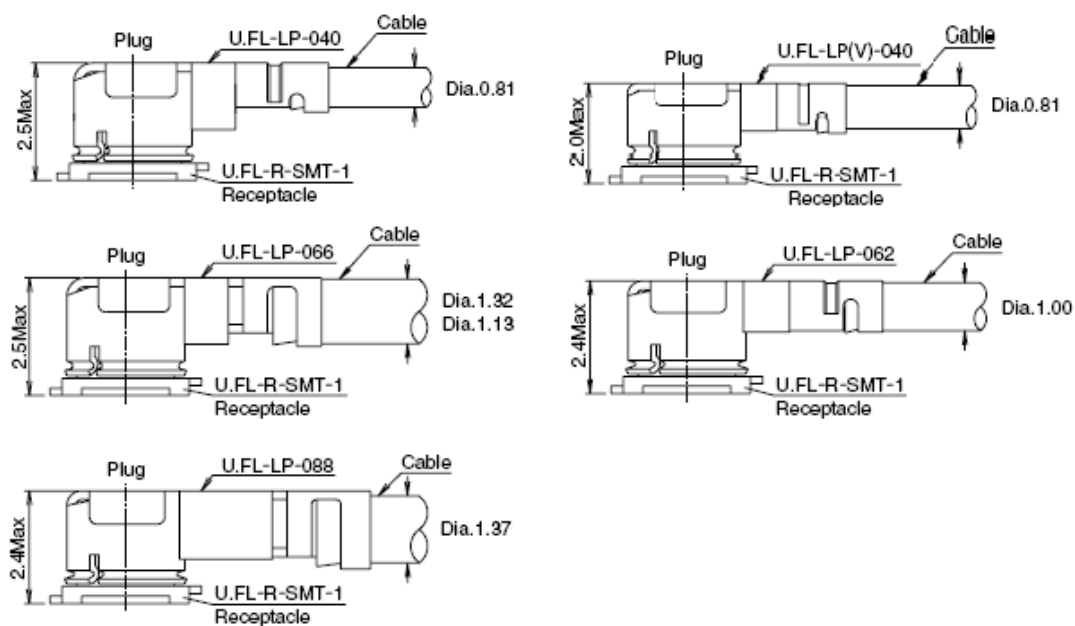


Figure 31: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit <http://www.hirose.com>.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 41: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT	-0.5	4.8	V
Voltage at USB_VBUS	-0.3	12.6	V
Voltage at digital pins	-0.3	2.1	V
Current at VBAT	-	TBD	A

NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

6.2. Power Supply Ratings

Table 42: Module's Power Supply Ratings

Parameters	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltage must be within this range	3.55	4	4.4	V
I _{VBAT}	Peak supply current	Maximum power control level	TBD	TBD	TBD	A

USB_VBUS	USB connection detection	3.7	5.0	12.6	V
VRTC	Supply voltage of the backup battery	2.0	3.0	3.25	V

6.3. Power Consumption

Table 43: SG555D-AP Power Consumption

Test Item	Condition	Typ.	Unit
Turn off	Turn off	203	μA
Sleep (USB disconnected)		4.15	mA

Table 44: SG555D-WF Power Consumption

Test Item	Condition	Typ.	Unit
Turn off	Turn off	199	μA
Sleep (USB disconnected)		TBD	mA
Wi-Fi 802.11b Tx	@ 11 Mbps, 2.4 GHz	TBD	mA
Wi-Fi 802.11g Tx	@ 54 Mbps, 2.4 GHz	TBD	mA
Wi-Fi 802.11n Tx	@ HT20 MCS7, 2.4 GHz	TBD	mA
	@ HT20 MCS7, 5 GHz	TBD	mA
	@ HT40 MCS7, 5 GHz	TBD	mA
Wi-Fi 802.11a Tx	@ 54 Mbps, 5 GHz	TBD	mA
Wi-Fi 802.11ac Tx	@ VHT20 MCS8, 5 GHz	TBD	mA
	@ VHT40 MCS9, 5 GHz	TBD	mA
	@ VHT80 MCS9, 5 GHz	TBD	mA
Bluetooth BR (DH5)	@ Max. power	TBD	mA

Bluetooth EDR (3DH5)	@ Max. power	TBD	mA
BLE	4.2	TBD	mA

Table 45: SG565D-AP Power Consumption

Test Item	Condition	Typ.	Unit
Turn off	Turn off	177	μA
Sleep (USB disconnected)		TBD	mA

Table 46: SG565D-WF Power Consumption

Test Item	Condition	Typ.	Unit
Turn off	Turn off	TBD	μA
Sleep (USB disconnected)		TBD	mA
Wi-Fi 802.11b Tx	@ 11 Mbps, 2.4 GHz	TBD	mA
Wi-Fi 802.11g Tx	@ 54 Mbps, 2.4 GHz	TBD	mA
Wi-Fi 802.11n Tx	@ HT20 MCS7, 2.4 GHz	TBD	mA
	@ HT20 MCS7, 5 GHz	TBD	mA
	@ HT40 MCS7, 5 GHz	TBD	mA
Wi-Fi 802.11a Tx	@ 54 Mbps, 5 GHz	TBD	mA
Wi-Fi 802.11ac Tx	@ VHT20 MCS8, 5 GHz	TBD	mA
	@ VHT40 MCS9, 5 GHz	TBD	mA
	@ VHT80 MCS9, 5 GHz	TBD	mA
Bluetooth BR (DH5)	@ Max. power	TBD	mA
Bluetooth EDR (3DH5)	@ Max. power	TBD	mA
BLE	4.2	TBD	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 47: LDO18B_1V8 I/O Characteristics

Parameters	Description	Min.	Max.	Unit
V_{IH}	High-level Input Voltage	1.17	2.1	V
V_{IL}	Low-level Input Voltage	-0.3	0.63	V
V_{OH}	High-level Output Voltage	1.35	1.8	V
V_{OL}	Low-level Output Voltage	0	0.45	V

Table 48: SD Card High-Voltage I/O Characteristics

Parameters	Description	Min.	Max.	Unit
V_{IH}	High-level Input Voltage	1.7	3.84	V
V_{IL}	Low-level Input Voltage	-0.3	0.89	V
V_{OH}	High-level Output Voltage	2.04	3.54	V
V_{OL}	Low-level Output Voltage	0	0.44	V

Table 49: SD Card Low-Voltage I/O Characteristics

Parameters	Description	Min.	Max.	Unit
V_{IH}	High-level Input Voltage	1.27	2	V
V_{IL}	Low-level Input Voltage	-0.3	0.58	V

V _{OH}	High-level Output Voltage	1.4	-	V
V _{OL}	Low-level Output Voltage	-	0.45	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 50: ESD Characteristics (Temperature: 25 °C–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
All antenna interfaces	±5	±10
Other Interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 51: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature ⁷	-35	+25	+75
Storage Temperature	-40	-	+90

⁷ Within this range, the module's related indicators can meet IEEE specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

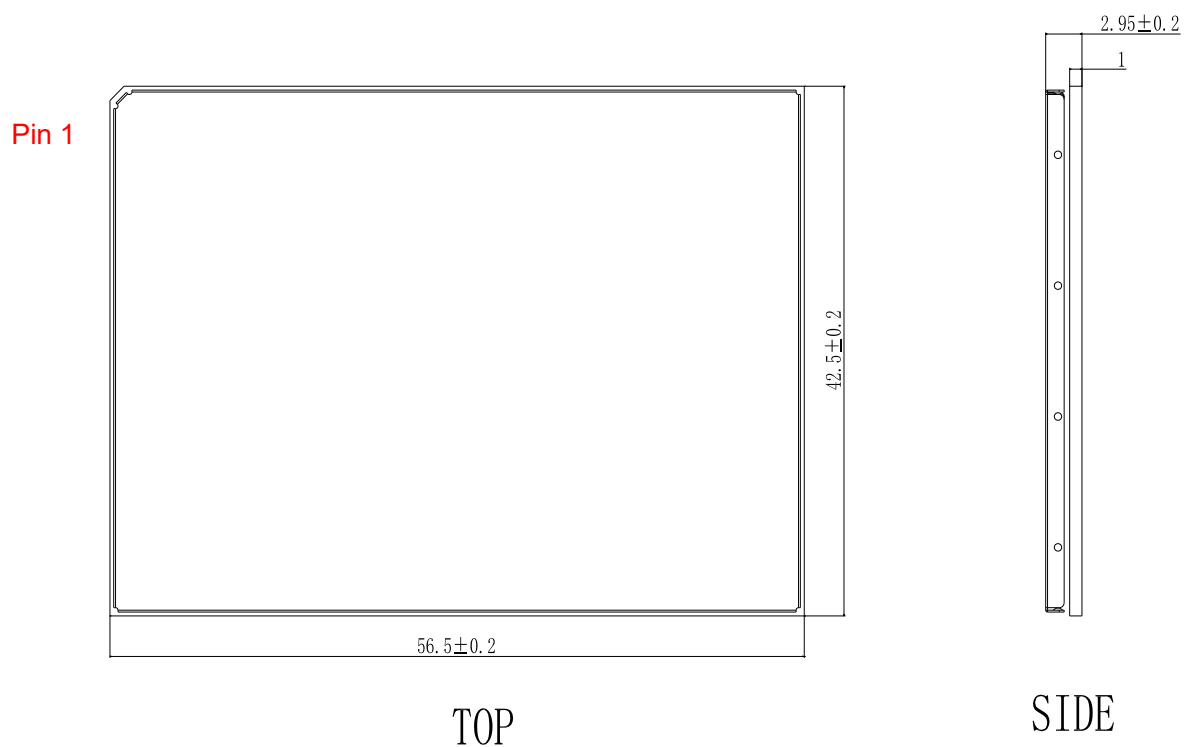


Figure 32: Top and Side Dimensions

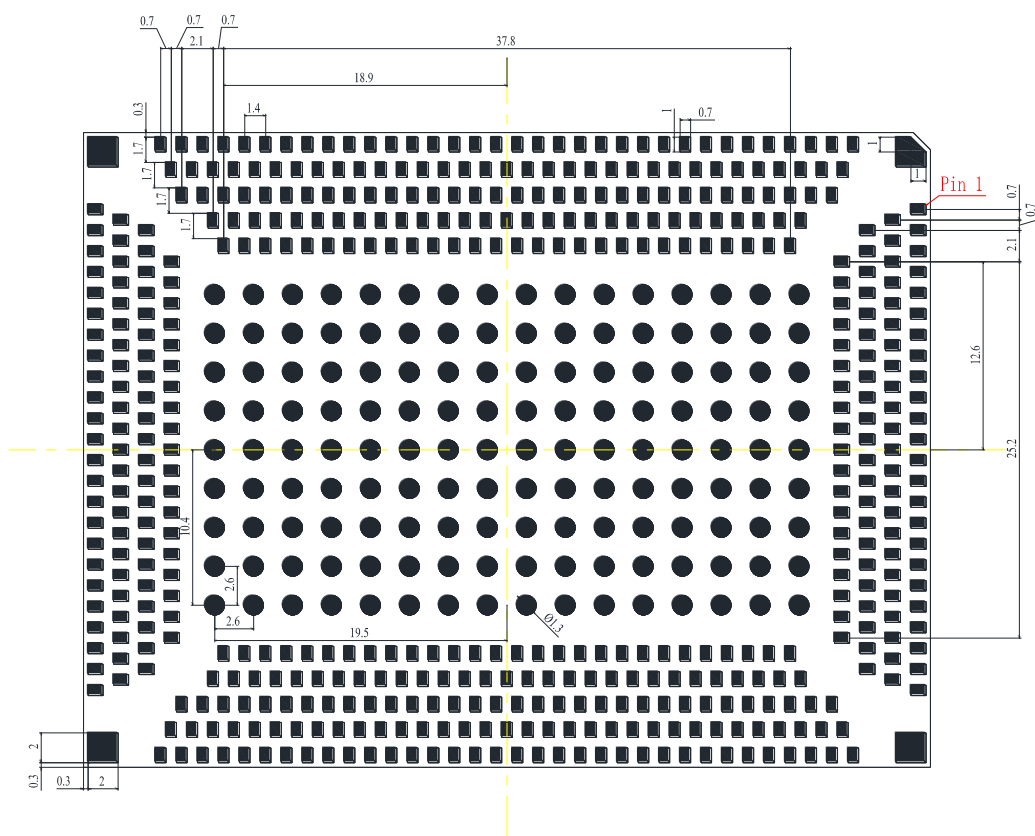


Figure 33: Bottom Dimension

NOTE

The module's coplanarity standard: ≤ 0.16 mm.

7.2. Recommended Footprint

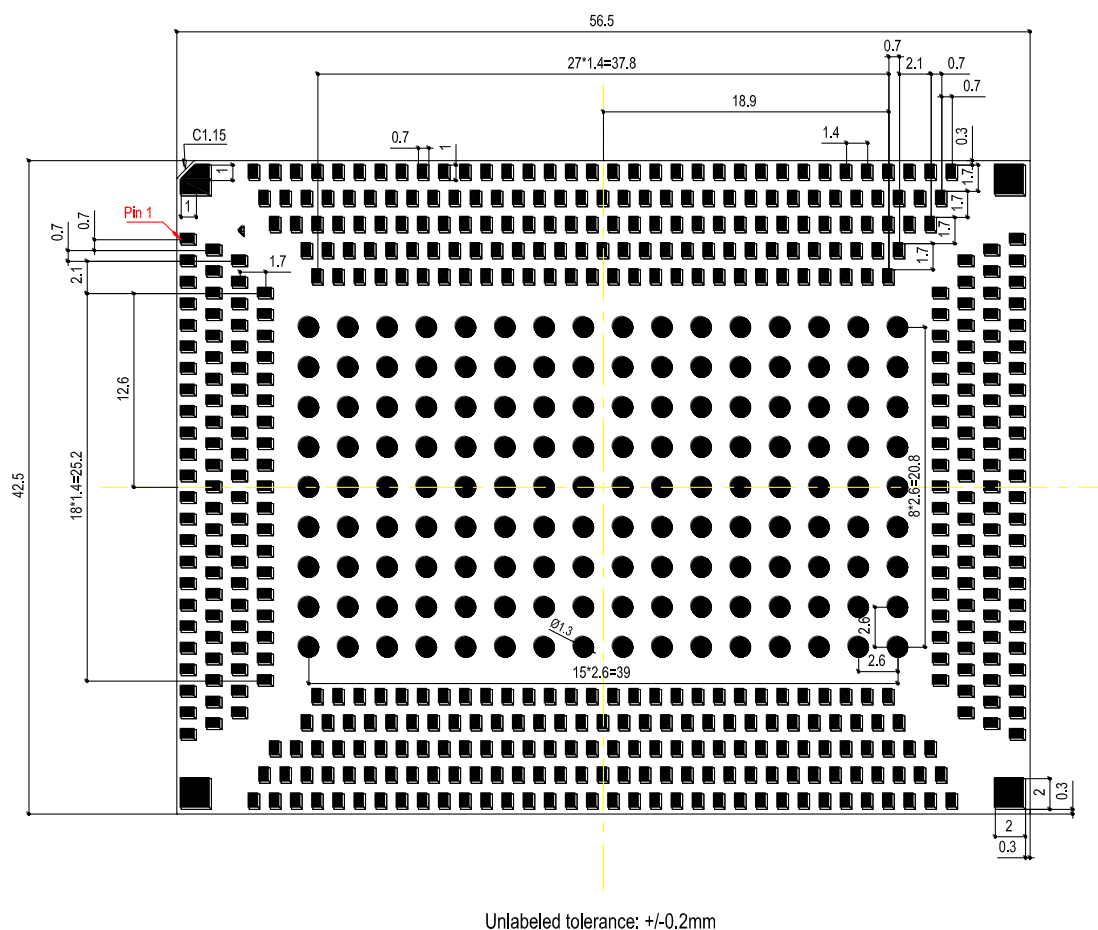


Figure 34: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

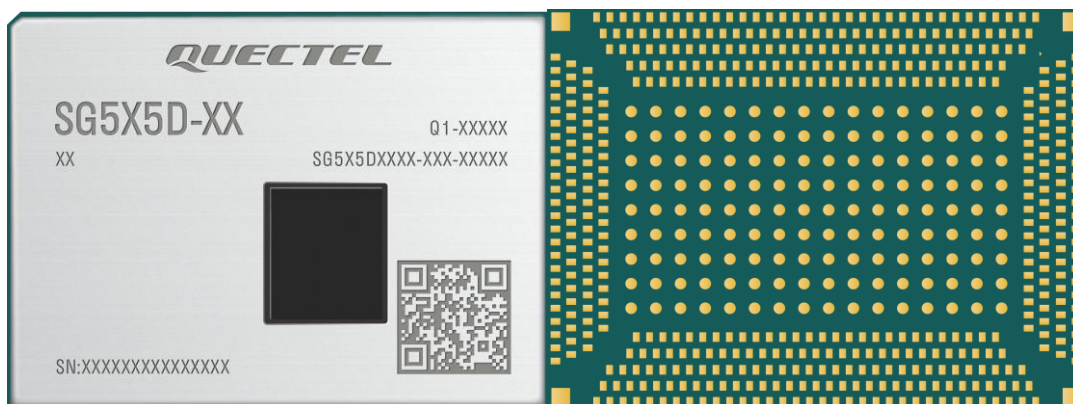


Figure 35: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage, Manufacturing & Packaging

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours ⁸ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 24 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

⁸ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.1. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see **document [4]**.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

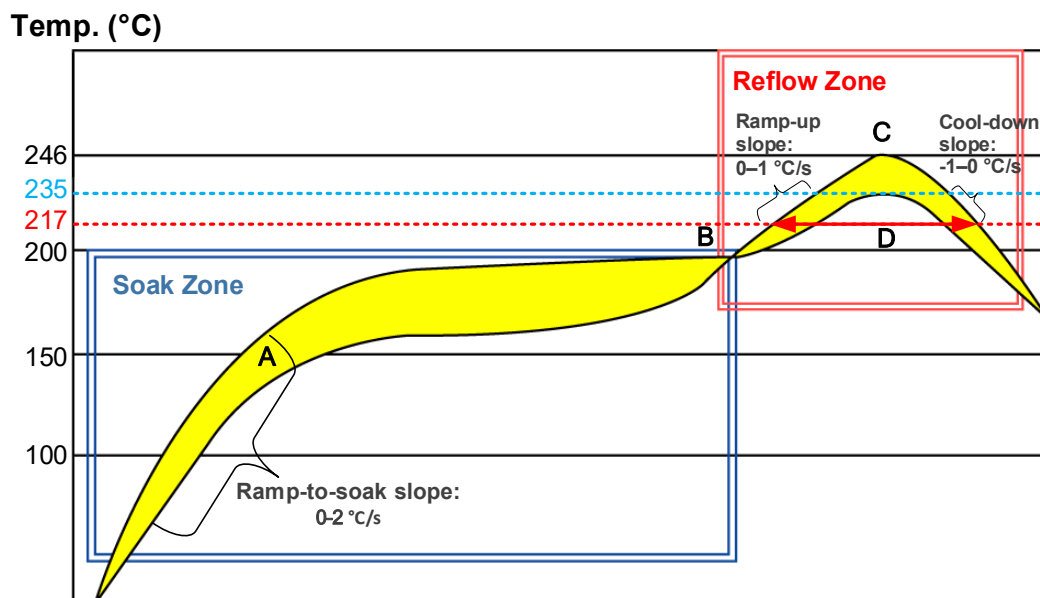


Figure 36: Recommended Reflow Soldering Thermal Profile

Table 52: Recommended Thermal Profile Parameters

Factor	Requirements
Soak Zone	
Ramp-to-soak Slope	0–2 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C Ramp-up Slope	0–1 °C/s
Reflow Time (D: over 217°C)	40–65 s
Max Temperature	235–246 °C
235–217 °C Cool-down Slope	-1–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Thus, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in **document [5]**.

8.2. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in an injection tray packaging as specified in the sub-chapters below.

8.2.1. Injection Tray

Injection tray dimensions are illustrated in the following figure:

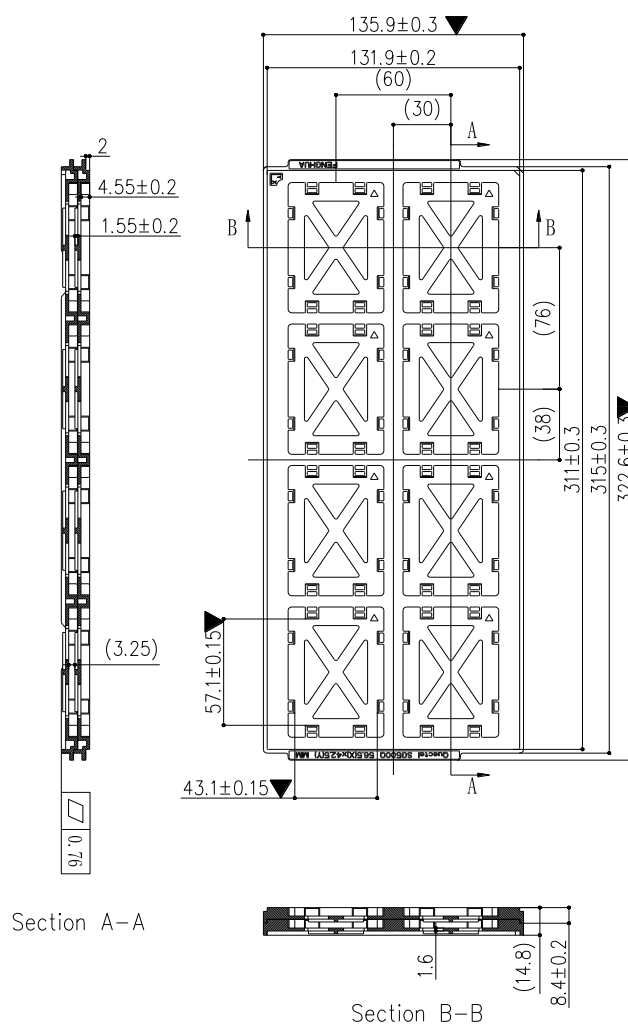
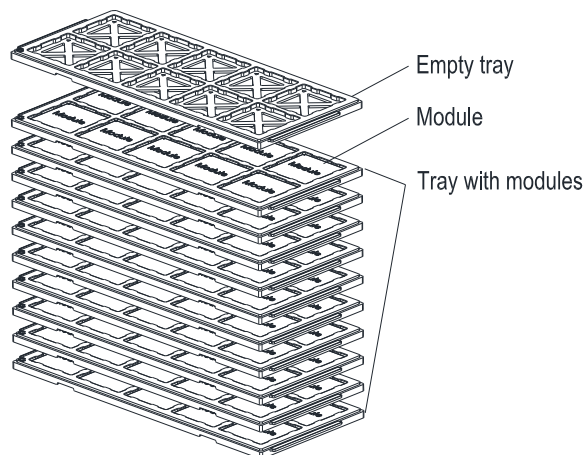


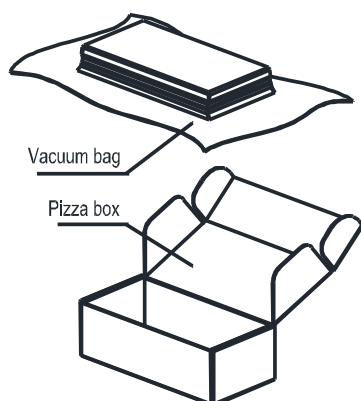
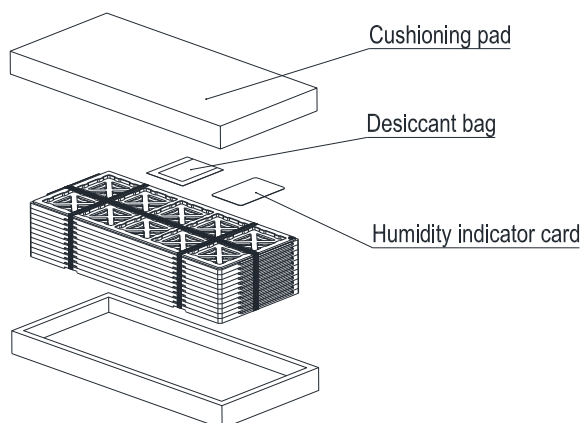
Figure 37: Injection Tray Dimension Drawing (Unit: mm)

8.2.2. Packaging Process



Each injection tray houses 8 modules. Stack 10 trays filled with modules, topping it off with 1 empty tray.

Fasten the 11 trays. Place the humidity indicator card and desiccant bag on top, and sandwich the trays with 2 cushioning pads on the top and bottom.



Place the injection trays, cushioned with pads, into a vacuum bag and seal it. Subsequently, place the vacuum-sealed trays into a pizza box. Each pizza box can accommodate 80 modules.

Place the 2 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 160 modules.

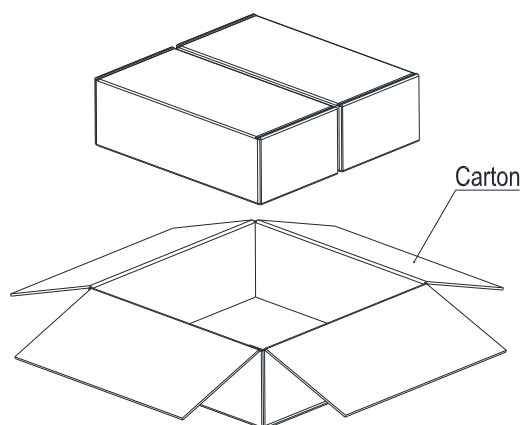


Figure 38: Packaging Process

9 Appendix References

Table 53: Related Documents

Document Name
[1] Quectel_Smart_5G_EVB_User_Guide
[2] Quectel_SG555D&SG565D_Series_GPIO_Configuration
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Stencil_Design_Requirements
[5] Quectel_Module_SMT_Application_Note

Table 54: Terms and Abbreviations

Abbreviation	Description
ADSP	Audio Digital Signal Processor
ADC	Analog-to-Digital Converter
AP	Access Point
ARM	Advanced RISC Machine
AMR-NB	Adaptive Multi Rate-Narrow Band Speech Codec
AMR-WB	Adaptive Multi-Rate Wideband
BLE	Bluetooth Low Energy
bps	Bytes per second
BR	Basic Rate
CPU	Central Processing Unit

CSI	Camera Serial Interface
CTS	Clear to Send
DC	Direct Current
DMIC	Digital Microphone
DP	DisplayPort
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Reference Phase Shift Keying
DSI	Display Serial Interface
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FHD	Full High Definition
FR	Full Rate
FP	Feature Pack
GFSK	Gaussian Frequency Shift Keying
GND	GND
GPIO	General Purpose Input/Output
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
HR	Half Rate
HT	High Throughput
I2S	Inter-IC Sound

IEEE	Institute of Electrical and Electronics Engineers
ISP	Image Signal Processor
LCD	Liquid Crystal Display
LCM	Liquid Crystal Monitor
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LPDDR	Low-Power Double Data Rate
MCS	Modulation and Coding Scheme
MIPI	Mobile Industry Processor Interface
NFC	Near Field Communication
NPU	Neural Network Processing Unit
OTA	Over-the-air programming
OTG	On-The-Go
PC	Personal Computer
PCB	Printed Circuit Board
PMU	Power Management Unit
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTC	Real-Time Clock
RTS	Request to Send
SAW	Surface Acoustic Wave
SCO	Synchronous Connection Oriented
SD	Secure Digital

SDIO	Secure Digital Input and Output Card
SDR	Single Data Rate
SIM	Subscriber Identity Module
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
STA	Station
TP	Touch Panel
TVS	Transient Voltage Suppressor
ZSL	Zero Shutter Lag
UART	Universal Asynchronous Receiver/Transmitter
UFS	Universal Flash Storage
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V _{max}	Maximum Voltage Value
V _{nom}	Nominal Voltage
V _{min}	Minimum Voltage
V _{IH}	High-level Input Voltage
V _{IL}	Low-level Input Voltage
V _{OH}	High-level Output Voltage
V _{OL}	Low-level Output Voltage
VHT	Very High Throughput
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Wide Area Network

FCC Statement

FCC ID: XMR2025SG555DWF

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

The device must not be co-located or operating in conjunction with any other antenna or transmitter. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement

This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Does not comply with the use restrictions of the product:

Portable devices used close with human's body (within 20cm), Like Cell phone, Notebook etc.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.247 & 15.209 & 15.407.

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 0.2dBi antenna. The host manufacturer installing this module into their product must ensure that the final product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

2.4 Limited module procedures

Not applicable. The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable The module has its own antenna, and doesn't need a hosts printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users' body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application The FCC ID of the module cannot be used on the final product In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: External Antenna

Gain: 2.4G: 0.47dBi;5G:1.28dBi;

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a "unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2025SG555DWF" with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15.209 & 15.407 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Federal Communication Commission Statement (FCC, U S)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications However, there is no guarantee that interference will not occur in a particular installation If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

This device complies with Part 15 of the FCC Rules Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

IMPORTANT NOTES**Co-location warning:**

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

OEM integration instructions:

This device is intended only for OEM integrators under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.

As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End product labeling:

The final end product must be labeled in a visible area with the following: "Contains Transmitter Module **FCC ID: XMR2025SG555DWF** "

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IC: 10224A-025SG555DWF

This device complies with Innovation, Science and Economic Development Canada's license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

The device is compliance with RF field strength limits, users can obtain Canadian information on RF exposure and compliance.

IC Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d' exposition aux radiations:

Cet équipement est conforme aux limites d' exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

The user manual for local area network devices shall contain instructions related to the restrictions mentioned in the above sections, namely that:

- (i) the device for operation in the band 5150-5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
- (ii) the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall comply with the e.i.r.p. limit; and
- (iii) the maximum antenna gain permitted for devices in the band 5725-5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

(i) Les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux.

(ii) le gain d'antenne maximal autorisé pour les appareils dans les bandes 5250-5350 MHz et 5470-5725 MHz doivent respecter le pire limiter; et

(iii) le gain d'antenne maximal autorisé pour les appareils dans la bande 5725-5825 MHz doivent respecter le pire limites spécifiées pour le point-à-point et l'exploitation non point à point, le cas échéant.

Users should also be advised that high-power radars are allocated as primary users (i.e. priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

Les utilisateurs de radars de haute puissance sont désignés utilisateurs principaux (c.-à-d., qu'ils ont la priorité) pour les bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer du brouillage et/ou des dommages aux dispositifs LAN-EL.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC:10224A-025SG555DWF".

Étiquetage du produit final

Ce module émetteur n'est autorisé que pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte que 20 cm puissent être maintenus entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans une zone visible avec la mention suivante: "contient IC: 10224A-025SG555DWF".

