SC200R Series

Hardware Design

Smart Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236 Email: info@quectel.com

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About the Document

Revision History

Version	Date	Author	Description
1.0	2019-12-30	Arsene TONG	Initial
1.1	2020-09-09	Jasper LAI/ Jamie SHI	1. Updated SC200R-EM frequency bands (Chapter 2.1/6.1): Added B4 in LTE-FDD Deleted B39 in LTE-TDD Added B4 in WCDMA 2. Added Galileo in supported GNSS (Chapter 2.1/2.2/5/6.3). 3. Added a note for the wakeup of LDO6_1V8 during sleep mode (Chapter 3.3). 4. Updated Wi-Fi output power and added Wi-Fi receiving sensitivity (Chapter 4.1.1). 5. Added BT transmitting and receiving performance (Chapter 4.2.1). 6. Added GNSS performance data (Chapter 5.1). 7. Added current consumption of SC200R-CE/-NA (Chapter 7.4). 8. Added RF output power of SC200R-NA (Chapter 7.5). 9. Added RF receiving sensitivity of SC200R-CE/-NA (Chapter 7.6). 10. Updated the maintenance clearance between the module and other components to at least 5 mm (Chapter 8.2). 11. Updated general description of storage, manufacturing and soldering (Chapter 9.1/9.2). 12. Added package weight of the module (Chapter 9.3).

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1 Introduction

This document, describing SC200R-WF module and its air and hardware interfaces connected to your applications, informs you of the interface specifications, electrical and mechanical details, as well as other related information of the module.
With the application notes and user guides provided separately, you can easily use SC200R-WF to design and set up mobile applications.

Federal Communications Commission (FCC) Declaration of Conformity FCC Caution:
Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This device complies with Part 15 of the FCC Rules.Operation is subject to the following two conditions:
1. This device may not cause harmful interference, and
2. this device must accept any interference received, including interference that may cause un-desired operation. Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules.These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equip-ment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
—Reorient or relocate the receiving antenna.
—Increase the separation between the equipment and receiver.
—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
—Consult the dealer or an experienced radio/TV technician for help. Radiation Exposure Statement This equipment complies with FCC radiation exposure limits set forth for an uncontrolled rolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Important Note: This radio module must not installed to co-locate and operating simultaneously with other radios in host system except in accordance with FCC multi-transmitter product procedures. Additional testing and equipment authorization may be required to operating simultaneously with other ra-dio. The availability of some specific channels and/or operational frequency bands are country dependent and are firmware programmed at the factory to match the intended destination. The firmware setting is not accessible by the end user. The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the mod-ular transmitter installed. The end user manual shall include all required regulatory information/warning as shown in this manual,

including: This product must be in-stalled and operated with a minimum distance of 20 cm between the radiator and user body. This device have got a FCC ID: XMR20SC200RWF.The final end product must be labeled in a visible area with the following: “Contains Transmitter Mod-ule FCC ID: XMR20SC200RWF” This device is intended only for OEM integrators under the following conditions: 1) The antenna must be installed such that 20cm is main-tained between the antenna and users, and 2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance require-ments required with this module installed.
Declaration of Conformity European notice.

Canada Regulations:

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.
Le présentappareilestconforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence. L’exploitationestautorisée aux deux conditions suivantes :
(1) l’appareil ne doit pas produire de brouillage;
(2) l’utilisateur de l’appareildoit accepter tout brouillageradioélectriquesubi, mêmesi le brouillageest susceptible d’encompromettre le fonctionnement. Caution：

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body.

Cet émetteur ne doit pas être Co-placé ou ne fonctionnant en même temps qu’aucune autre antenne ou émetteur. Cet équipement devrait être installé et actionné avec une distance minimum de 20 centimètres entre le radiateur et votre corps.

A label with the following statements must be attached to the host end product: This device contains IC: 10224A-20SC200RWF.
The manual provides guidance to the host manufacturer will be included in the documentation that will be provided to the OEM. The module is limited to installation in mobile or fixed applications.
The separate approval is required for all other operating configurations, including portable configurations and different antenna configurations. The OEM integrators are responsible for ensuring that the end-user has no manual or instructions to remove or install module.
The module is limited to OEM installation ONLY.
Une étiquette avec les instructions suivantes doit être attachée au produit final hôte:
Cet appareil contient IC: 10224A-20SC200RWF.
Le manuel fournit des conseils au fabricant hôte sera inclus dans la documentation qui sera fournie à l'OEM. Le module est limité à l'installation dans des applications mobiles ou fixes.
L'approbation distincte est requise pour toutes les autres configurations de fonctionnement, y compris les configurations portables et différentes configurations d'antenne.
Les intégrateurs OEM sont responsables de s'assurer que l'utilisateur n'a pas de manuel ou d'instructions pour retirer ou installer le module.
Le module est limité à l'installation OEM SEULEMENT.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

SC200R is a series of 4G Smart LTE module based on Qualcomm platform and Android operating system, and provides industrial grade performance. Its general features are listed below:

- Supports worldwide LTE-FDD, LTE-TDD, DC-HSPA+, HSPA+, HSDPA, HSUPA, WCDMA, EVDO/CDMA, EDGE and GPRS coverage.
- Supports short-range wireless communication via Wi-Fi 802.11a/b/g/n and BT 4.2 LE.
- Integrates GPS/GLONASS/BeiDou or GPS/Galileo/Beidou satellite positioning systems.
- Supports multiple audio and video codecs.
- Built-in high performance Adreno™ 308 graphics processing unit.
- Provides multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

SC200R series module is available in five variants: SC200R-CE, SC200R-EM*, SC200R-NA, SC200R-JP*, SC200R-WF*. The following tables show the supported frequency bands and network standards of SC200R series modules.

Table 1: SC200R-CE Frequency Bands

Mode	Frequency
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
WCDMA	B1/B8
EVDO/CDMA	BC0
GSM	900/1800 MHz
Wi-Fi 802.11a/b/g/n	2402–2482 MHz 5180–5825 MHz
BT 4.2 LE	2402–2480 MHz

GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz Galileo: 1575.42 ±1.023 MHz

Table 2: SC200R-EM* Frequency Bands

Mode	Frequency
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28
LTE-TDD	B38/B40/B41
WCDMA	B1/B2/B4/B5/B8
GSM	850/900/1800/1900 MHz
Wi-Fi 802.11a/b/g/n	2402–2482 MHz 5180–5825 MHz
BT 4.2 LE	2402–2480 MHz
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz Galileo: 1575.42 ±1.023 MHz

Table 3: SC200R-NA Frequency Bands

Mode	Frequency
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41
WCDMA	B2/B4/B5
Wi-Fi 802.11a/b/g/n	2402–2482 MHz 5180–5825 MHz
BT 4.2 LE	2402–2480 MHz
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz Galileo: 1575.42 ±1.023 MHz

Table 4: SC200R-JP* Frequency Bands

Mode	Frequency
LTE-FDD	B1/B3/B5/B8/B11/B18/B19/B21/B26/B28
LTE-TDD	B41
WCDMA	B1/B6/B8/B19
Wi-Fi 802.11a/b/g/n	2402–2482 MHz 5180–5825 MHz
BT 4.2 LE	2402–2480 MHz
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz Galileo: 1575.42 ±1.023 MHz

Table 5: SC200R-WF* Frequency Bands

Mode	Frequency
Wi-Fi 802.11a/b/g/n	2402–2482 MHz 5180–5825 MHz
BT 4.2 LE	2402–2480 MHz
GNSS	/

NOTES

1. "*" means under development.
2. SC200R-JP supports 802.11b channel 14.

SC200R is a series of SMD type modules, which can be embedded into applications through its 274 pins, including 146 LCC pins and 128 LGA pins. With a compact profile of 40.5 mm × 40.5 mm × 2.8 mm, the module can meet almost all requirements for M2M applications such as edge device, edge computing, CPE, wireless POS, smart metering, router, data card, automotive, smart phone, digital signage, alarm panel, security and industry PDA, etc.

2.2. Key Features

The following table describes the detailed features of SC200R series module.

Table 6: Key Features

Feature	Details
Application Processor	64-bit quad-core ARM Cortex-A53 microprocessor, up to 1.3 GHz 512 KB L2 cache
Modem DSP	Hexagon DSP v56 core, up to 691 MHz 768 KB L2 cache
GPU	Adreno™ 308 GPU with 64-bit addressing, up to 485 MHz
Memory	8 GB eMMC + 1 GB LPDDR3 (default) 16 GB eMMC + 2 GB LPDDR3 (optional)
Operating System	Android 10.0
Power Supply	Supply voltage: 3.55–4.2 V Typical supply voltage: 3.8 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for GSM850 Class 4 (33 dBm ±2 dB) for EGSM900 Class 1 (30 dBm ±2 dB) for DCS1800 Class 1 (30 dBm ±2 dB) for PCS1900 Class E2 (27 dBm ±3 dB) for GSM850 8-PSK Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK Class 3 (24 dBm +1/-3 dB) for WCDMA bands Class 3 (24 dBm +3/-1 dB) for EVDO/CDMA BC0 Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	Supports 3GPP R10 Cat 4 FDD and TDD Supports 1.4 to 20 MHz RF bandwidth ● FDD: Max. 150 Mbps (DL)/Max. 50 Mbps (UL) ● TDD: Max. 130 Mbps (DL)/Max. 30 Mbps (UL)
UMTS Features	Supports 3GPP R9 DC-HSDPA/DC-HSUPA/HSPA+/HSDPA/HSUPA/WCDMA Supports 16-QAM, 64-QAM and QPSK modulations ● DC-HSDPA: Max. 42 Mbps (DL) ● DC-HSUPA: Max. 11.2 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/Max. 384 kbps (UL)

CDMA2000 Features	Supports 3GPP2 CDMA2000 1X Advanced, CDMA2000 1xEV-DO Rev.A ● EVDO: Max. 3.1 Mbps (DL)/Max. 1.8 Mbps (UL) ● 1X Advanced: Max. 307.2 kbps (DL)/Max. 307.2 kbps (UL)
GSM Features	**R99:** CSD: 9.6 kbps, 14.4 kbps **GPRS:** Supports GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max. 107 kbps (DL)/Max. 85.6 kbps (UL) **EDGE:** Supports EDGE multi-slot class 33 (33 by default) Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: MCS 1-9 Uplink coding schemes: MCS 1-9 Max. 296 kbps (DL)/Max. 236.8 kbps (UL)
WLAN Features	Support AP and STA mode 2.4/5 GHz, 802.11a/b/g/n, up to 150 Mbps
Bluetooth Feature	BT 4.2 LE
GNSS Features[1)]	GPS/GLONASS/BeiDou or GPS/Galileo/BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast
LCM Interface	Supports one 4-lane MIPI_DSI Supports HD+ (1440 × 720) @ 60 fps
Camera Interfaces	Supports two 4-lane MIPI_CSI, up to 2.1 Gbps/lane Supports two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane) Up to 13 MP
Video Codec	Video encoding + decoding: 720P @ 30 fps + 1080P @ 30 fps Encoding up to 1080P @ 30 fps, decoding up to 1080P @ 30 fps
Audio Interfaces	**Audio inputs:** Three single-ended microphone inputs **Audio outputs:** Class AB stereo headphone output Class AB earpiece differential output Class D speaker differential amplifier output
Audio Codec	EVRC, EVRC-B, EVRC-WB; G.711, G.729A, and G.729AB; GSM-FR, GSM-EFR, GSM-HR; AMR-NB, AMR-WB, eAMR, BeAMR

USB Interface	Compliant with USB 2.0 specification Supports up to 480 Mbps Supports USB OTG Used for AT command communication, data transmission, software debugging and firmware upgrade
UART Interfaces	Three UART interfaces: UART5, UART2 (debug UART) and UART1, baud rate up to 4 Mbps ● UART5: 4-wire UART interface, hardware flow control supported ● UART2 (debug UART): 2-wire UART interface, used for debugging by default ● UART1: 2-wire UART interface
SD Card Interface	Supports SD 3.0 Supports SD card hot-plug
(U)SIM Interfaces	Two (U)SIM interfaces Supports USIM/SIM card: 1.8 V or 2.95 V Supports Dual SIM Dual Standby (supported by default)
I2C Interfaces	Four I2C interfaces Used for peripherals such as camera, sensor, touch panel, etc.
ADC Interfaces	One generic ADC interface up to 15-bit resolution
Real Time Clock	Supported
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS[1)] antenna and Wi-Fi/BT antenna
Physical Characteristics	Size: (40.5 ±0.15) mm × (40.5 ±0.15) mm × (2.8 ±0.2) mm Package: LCC + LGA Weight: Approx. 10.2 g
Temperature Range	Operating temperature range: -35 °C to +75 °C [2)] Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Over USB interface
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] SC200R-WF does not support GNSS.
2. [2)] Within the operating temperature range, the module is 3GPP compliant.

2.3. Functional Diagram

The following figure shows a block diagram of SC200R series module and illustrates the major functional parts.

- Power management
- Radio frequency
- Baseband
- LPDDR3 + eMMC flash
- Peripheral interfaces
  -- USB interface
  -- UART interfaces
  -- (U)SIM interfaces
  -- SD card interface
  -- GPIO interfaces
  -- I2C interfaces
  -- SPI interfaces
  -- ADC interface
  -- Motor drive interface
  -- LCM interface
  -- Touch panel interface
  -- Camera interfaces
  -- Audio interfaces

2.4. Evaluation Board

To help you design and test applications with the module, Quectel supplies an evaluation kit, which includes an evaluation board, a USB to RS-232 converter cable, a USB data cable, a power adapter, an earphone and antennas. For details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

SC200R is a series of SMD type modules with 146 LCC pins and 128 LGA pins. The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- VRTC interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- SPI interfaces
- ADC interface
- Motor drive interface
- LCM interface
- Touch panel interface
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SC200R series module.

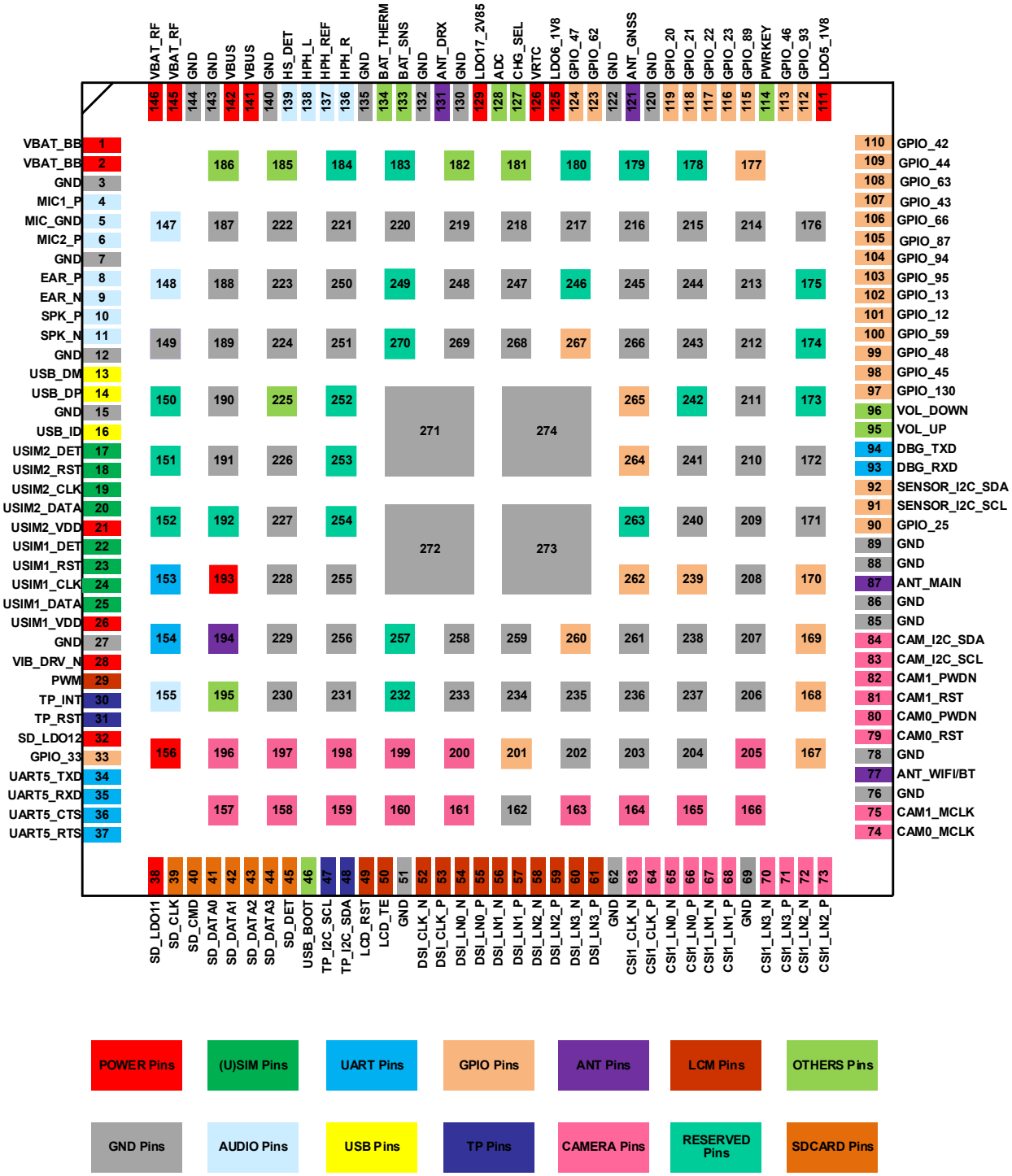


Figure 1: Pin Assignment (Top View)

3.3. Pin Description

Table 7: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
OD	Open drain
PI	Power input
PO	Power output

The following table shows the pin definition and electrical characteristics of the module.

Table 8: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	1, 2	PI/ PO	Power supply for the module's baseband part	Vmax = 4.2 V Vmin = 3.55 V Vnorm = 3.8 V	You must provide them with sufficient current of up to 3.0 A. It is suggested to add a TVS for surge protection.
VBAT_RF	145, 146	PI	Power supply for the module's RF part	Vmax = 4.2 V Vmin = 3.55 V Vnorm = 3.8 V	
VRTC	126	PI/ PO	Power supply for internal RTC circuit	$V_O$max = 3.2 V V_I = 2.0–3.25 V	If it is not used, keep this pin open.
LDO5_1V8	111	PO	1.8 V output power supply	Vnorm = 1.8 V $I_O$max = 20 mA	Power supply for external GPIO's pull-up and level shift circuits.

LDO6_1V8[1)]	125	PO	1.8 V output power supply	Vnorm = 1.8 V $I_O$max = 150 mA	Power supply for sensors, cameras, and I2C pull-up circuit. If it is used, connect an external 1.0–4.7 μF capacitor to this pin in parallel. If it is not used, keep it open.
LDO10_2V85	156	PO	2.85 V output power supply	Vnorm = 2.85 V $I_O$max = 150 mA	Reserved power supply. If it is used, add a 1.0–2.2 μF bypass capacitor. If it is not used, keep it open.
LDO17_2V85	129	PO	2.85 V output power supply	Vnorm = 2.85 V $I_O$max = 450 mA	Power supply for AVDD of LCM, TP, sensors and cameras. If it is used, connect an external 2.2–4.7 μF capacitor to this pin in parallel. If it is not used, keep it open.
LDO16_2V8	193	PO	2.8 V output power supply	Vnorm = 2.8 V $I_O$max = 55 mA	Reserved power supply. If it is used, add a 1.0–2.2 μF bypass capacitor. If it is not used, keep it open.

GND

Pin Name	Pin No.
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 149, 162, 171, 172, 176, 187–191, 202–204, 206–224, 226–231, 233–238, 240, 241, 243–245, 247, 248, 250, 251, 255, 256, 258, 259, 261, 266, 268, 269, 271–274

Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC1_P	4	AI	Main microphone input (+)		
MIC_GND	5	AI	Microphone reference ground		If it is not used, connect it to the ground.
MIC2_P	6	AI	Microphone input for headset (+)		
EAR_P	8	AO	Earpiece output (+)		
EAR_N	9	AO	Earpiece output (-)		
SPK_P	10	AO	Speaker output (+)		
SPK_N	11	AO	Speaker output (-)		
HPH_R	136	AO	Headphone right channel output		
HPH_REF	137	AO	Headphone reference ground		
HPH_L	138	AO	Headphone left channel output		
HS_DET	139	AI	Headset insertion detect		High level by default.
MIC_BIAS1	147	AO	Microphone bias voltage 1	V_O = 1.6–2.85 V	
MIC3_P	148	AI	Secondary microphone input (+)		
MIC_BIAS2	155	AO	Microphone bias voltage 2	V_O = 1.6–2.85 V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	141, 142	PI	USB 5 V power input and USB connection detect	Vmax = 6.2 V Vmin = 4.35 V Vnorm = 5.0 V	
USB_DM	13	AI/AO	USB 2.0 differential data (-)		USB 2.0 standard compliant. 90 Ω differential impedance.
USB_DP	14	AI/AO	USB 2.0 differential data (+)		

USB_ID	16	DI	USB ID detect		High level by default.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Externally pull it up to 1.8 V. If it is not used, keep it open. This function is disabled by default via software. Cannot be multiplexed into a generic GPIO.
USIM2_RST	18	DO	(U)SIM2 card reset	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	Cannot be multiplexed into generic GPIOs.
USIM2_CLK	19	DO	(U)SIM2 card clock		
USIM2_DATA	20	IO	(U)SIM2 card data	V_{IL}max = 0.2 × USIM2_VDD V_{IH}min = 0.7 × USIM2_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	
USIM2_VDD	21	PO	(U)SIM2 card power supply	**For 1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **For 2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V	Either 1.8 V or 2.95 V (U)SIM card is supported.

USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Externally pull it up to 1.8 V. If it is not used, keep it open. This function is disabled by default via software. Cannot be multiplexed into a generic GPIO.
USIM1_RST	23	DO	(U)SIM1 card reset	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	Cannot be multiplexed into generic GPIOs.
USIM1_CLK	24	DO	(U)SIM1 card clock		
USIM1_DATA	25	IO	(U)SIM1 card data	V_{IL}max = 0.2 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	
USIM1_VDD	26	PO	(U)SIM1 card power supply	**For 1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **For 2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART5_TXD	34	DO	UART5 transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If not used, keep these pins open.
UART5_RXD	35	DI	UART5 receive data	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART5_CTS	36	DI	UART5 clear to send	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART5_RTS	37	DO	UART5 request to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
DBG_RXD	93	DI	UART2 (debug UART) receive data	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	

DBG_TXD	94	DO	UART2 (debug UART) transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART1_RXD	153	DI	UART1 receive data	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART1_TXD	154	DO	UART1 transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_LDO11	38	PO	2.95 V output power supply	Vnorm = 2.95 V $I_O$max = 800 mA	Power supply for SD card.
SD_LDO12	32	PO	1.8/2.95 V output power supply	Vnorm = 1.8/2.95 V $I_O$max = 50 mA	Power supply for SD card pull-up circuits.
SD_CLK	39	DO	High speed digital clock signal of SD card	**1.8 V SD card:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{OL}max = 0.37 V V_{OH}min = 2.2 V	50 Ω characteristic impedance.
SD_CMD	40	IO	Command signal of SD card	**1.8 V SD card:** V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{IL}max = 0.73 V V_{IH}min = 1.84 V V_{OL}max = 0.37 V V_{OH}min = 2.2 V	
SD_DATA0	41	IO	High speed bidirectional digital signals of SD card		
SD_DATA1	42	IO			
SD_DATA2	43	IO			
SD_DATA3	44	IO			
SD_DET	45	DI	SD card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low.
Touch Panel Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_INT	30	DI	Interrupt signal of TP	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
TP_RST	31	DO	Reset signal of TP	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active low.

TP_I2C_SCL	47	OD	I2C clock signal of TP		Externally pull them up to 1.8 V. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	I2C data signal of TP		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWM	29	DO	PWM output which adjusts the backlight brightness	V_{OL}max = 0.45 V V_{OH}max = VBAT_BB	
LCD_RST	49	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
LCD_TE	50	DI	LCD tearing effect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
DSI_CLK_N	52	AO	LCD MIPI clock (-)		
DSI_CLK_P	53	AO	LCD MIPI clock (+)		
DSI_LN0_N	54	AO	LCD MIPI data 0 (-)		
DSI_LN0_P	55	AO	LCD MIPI data 0 (+)		
DSI_LN1_N	56	AO	LCD MIPI data 1 (-)		
DSI_LN1_P	57	AO	LCD MIPI data 1 (+)		
DSI_LN2_N	58	AO	LCD MIPI data 2 (-)		
DSI_LN2_P	59	AO	LCD MIPI data 2 (+)		
DSI_LN3_N	60	AO	LCD MIPI data 3 (-)		
DSI_LN3_P	61	AO	LCD MIPI data 3 (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI1_CLK_N	63	AI	Camera MIPI clock signal (-)		
CSI1_CLK_P	64	AI	Camera MIPI clock signal (+)		

CSI1_LN0_N	65	AI	Camera MIPI data 0 signal (-)		
CSI1_LN0_P	66	AI	Camera MIPI data 0 signal (+)		
CSI1_LN1_N	67	AI	Camera MIPI data 1 signal (-)		
CSI1_LN1_P	68	AI	Camera MIPI data 1 signal (+)		
CSI1_LN3_N	70	AI	Camera MIPI data 3 signal (-)		
CSI1_LN3_P	71	AI	Camera MIPI data 3 signal (+)		
CSI1_LN2_N	72	AI	Camera MIPI data 2 signal (-)		
CSI1_LN2_P	73	AI	Camera MIPI data 2 signal (+)		
CSI0_CLK_N	157	AI	Camera MIPI clock signal (-)		
CSI0_CLK_P	196	AI	Camera MIPI clock signal (+)		
CSI0_LN0_N	158	AI	Camera MIPI data 0 signal (-)		
CSI0_LN0_P	197	AI	Camera MIPI data 0 signal (+)		
CSI0_LN1_N	159	AI	Camera MIPI data 1 signal (-)		
CSI0_LN1_P	198	AI	Camera MIPI data 1 signal (+)		
CSI0_LN2_N	160	AI	Camera MIPI data 2 signal (-)		
CSI0_LN2_P	199	AI	Camera MIPI data 2 signal (+)		
CSI0_LN3_N	161	AI	Camera MIPI data 3 signal (-)		
CSI0_LN3_P	200	AI	Camera MIPI data 3 signal (+)		
CAM0_MCLK	74	DO	Clock signal of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM1_MCLK	75	DO	Clock signal of camera		
CAM0_RST	79	DO	Reset signal of camera		

CAM0_PWDN	80	DO	Power down signal of camera		
CAM1_RST	81	DO	Reset signal of camera		
CAM1_PWDN	82	DO	Power down signal of camera		
CAM_I2C_SCL	83	OD	I2C clock signal of camera		Externally pull them up to 1.8 V.
CAM_I2C_SDA	84	OD	I2C data signal of camera		
CAM2_MCLK	165	DO	Clock signal of camera	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM2_RST	164	DO	Reset signal of camera		
CAM2_PWDN	163	DO	Power down signal of camera		
DCAM_I2C_SCL	166	OD	I2C clock signal of camera		Externally pull them up to 1.8 V.
DCAM_I2C_SDA	205	OD	I2C data signal of camera		
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	114	DI	Turns on/off the module	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Pulled up to 1.8 V internally. Active low.
RESET_N	225	DI	Resets the module		Disabled by default and can be enabled via software configuration.
VOL_UP	95	DI	Volume up	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	If it is not used, keep it open. Do not pull it up. 1.8 V power domain.
VOL_DOWN	96	DI	Volume down	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	If it is not used, keep it open. Do not pull it up. 1.8 V power domain.
SENSOR_I2C Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor		Dedicated for external sensors. Cannot be used for touch panel, NFC, I2C keyboard, etc. Externally pull them up to 1.8 V.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor		
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_SNS	133	AI	Battery voltage detect		The maximum input voltage is 4.2 V.
BAT_THERM	134	AI	Battery temperature detect		Internally pulled up. Externally connect it to the 47 kΩ NTC thermistor. If it is not used, connect it to GND with a 47 kΩ resistor.
BAT_ID	185	AI	Battery type detect	V_{OL}min = 0.1 V V_{OH}max = 1.7 V	Internal pulled down with a 100 kΩ resistor. If it is not used, keep it open.
CHG_SEL	127	DI	Charger select		If you use an internal charging chip, keep this pin open. If you use an external charging chip, connect it to GND.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	128	AI	Generic ADC		The maximum input voltage is 1.7 V.
Antenna Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_MAIN	87	AI/ AO	Main antenna interface		
ANT_DRX	131	AI	Rx-diversity antenna interface		50 Ω impedance.
ANT_GNSS[2)]	121	AI	GNSS antenna interface		
ANT_WIFI/BT	77	AI/ AO	Wi-Fi/BT antenna interface		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_33	33	IO	GPIO		
GPIO_25	90	IO	GPIO		
GPIO_130	97	IO	GPIO		
GPIO_45	98	IO	GPIO		
GPIO_48	99	IO	GPIO		
GPIO_59	100	IO	GPIO		
GPIO_12	101	IO	GPIO		
GPIO_13	102	IO	GPIO	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V	1.8 V power domain.
GPIO_95	103	IO	GPIO		
GPIO_94	104	IO	GPIO		
GPIO_87	105	IO	GPIO		
GPIO_66	106	IO	GPIO		
GPIO_43	107	IO	GPIO		
GPIO_63	108	IO	GPIO		
GPIO_44	109	IO	GPIO		
GPIO_42	110	IO	GPIO		
GPIO_93	112	IO	GPIO		

GPIO_46	113	IO	GPIO		
GPIO_89	115	IO	GPIO		
GPIO_23	116	IO	GPIO		
GPIO_22	117	IO	GPIO		
GPIO_21	118	IO	GPIO		
GPIO_20	119	IO	GPIO		
GPIO_62	123	IO	GPIO		
GPIO_47	124	IO	GPIO		
GPIO_6	167	IO	GPIO		
GPIO_7	168	IO	GPIO		
GPIO_127	169	IO	GPIO		
GPIO_34	170	IO	GPIO		
GPIO_90	177	IO	GPIO		
GPIO_39	201	IO	GPIO		
GPIO_86	239	IO	GPIO		
GPIO_88	264	IO	GPIO		Do not pull up this GPIO when turning on the module. 1.8 V power domain.
GPIO_85	265	IO	GPIO		1.8 V power domain.
GPIO_61	267	IO	GPIO		
GNSS LNA Enable Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_LNA_EN	194	IO	External GNSS LNA enable		Cannot be multiplexed into a generic GPIO.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

RFFE3_CLK	260	IO	GRFC used for RF tuner control		Cannot be multiplexed into generic GPIOs.
RFFE3_DATA	262	IO	GRFC used for RF tuner control		
Emergency Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	46	DI	Forces the module to enter emergency download mode		You can force the module to enter emergency download mode by pulling it up to LDO5_1V8 during power-up.
Motor Drive Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV_N	28	PO	Motor drive	V_O = 1.2–3.1 V $I_O$max = 175 mA	Connect it to the negative pole of the motor.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CHG_LED	195	AO	Indicates the module's charging status	$I_O$max = 5 mA	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NFC_CLK	181	DO	NFC clock		
NFC_CLK_REQ	182	DI	NFC clock request		
CBL_PWR_N	186	DI	Initiates power-on when pulled down		The module cannot be turned off when this pin is pulled down. If it is not used, keep it open.
Reserved Pins					
Pin Name	**Pin No.**				**Comment**

RESERVED	150–152, 173–175, 178–180, 183, 184, 192, 232, 242, 246, 249, 252–254, 257, 263, 270	Keep these pins open.

NOTE

1. [1] When the module is in sleep mode, LDO6_1V8 wakes up periodically or randomly. Considering the actual requirement for power consumption during sleep mode, you can use either LDO6_1V8 or an external LDO for power supply. For lower power consumption, use an external LDO instead.
2. [2] SC200R-WF does not support GNSS.

3.4. Power Supply

3.4.1. Power Supply Pins

SC200R series module provides two VBAT_RF pins and two VBAT_BB pins for connection with the external power supply. The VBAT_RF pins are used for the RF part of the module and the VBAT_BB pins are used for the baseband part of the module.

3.4.2. Decrease Voltage Drop

The power supply range of the module is 3.55–4.2 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the transient peak current of the module may surge up to 3 A. If the supply voltage is not enough, there will be voltage drops, and if the voltage drops below 3.1 V, the module will be turned off automatically. Therefore, make sure the input voltage never drops below 3.1 V.

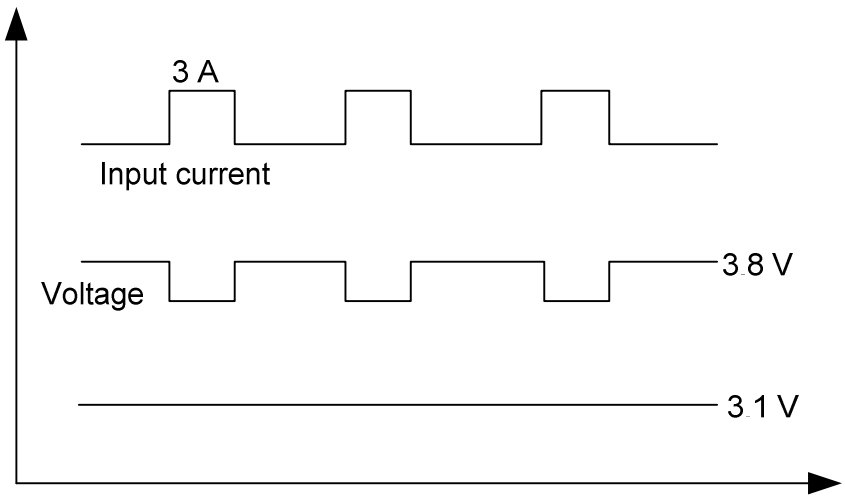


Figure 2: Voltage Drop Sample

To decrease voltage drop, use a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array and place these capacitors close to VBAT_BB/VBAT_RF pins. Additionally, add a 4.7 μF capacitor in parallel. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is suggested to use a TVS and place it as close to the VBAT_BB/VBAT_RF pins as possible to enhance surge protection. The following figure shows the star structure of the power supply.

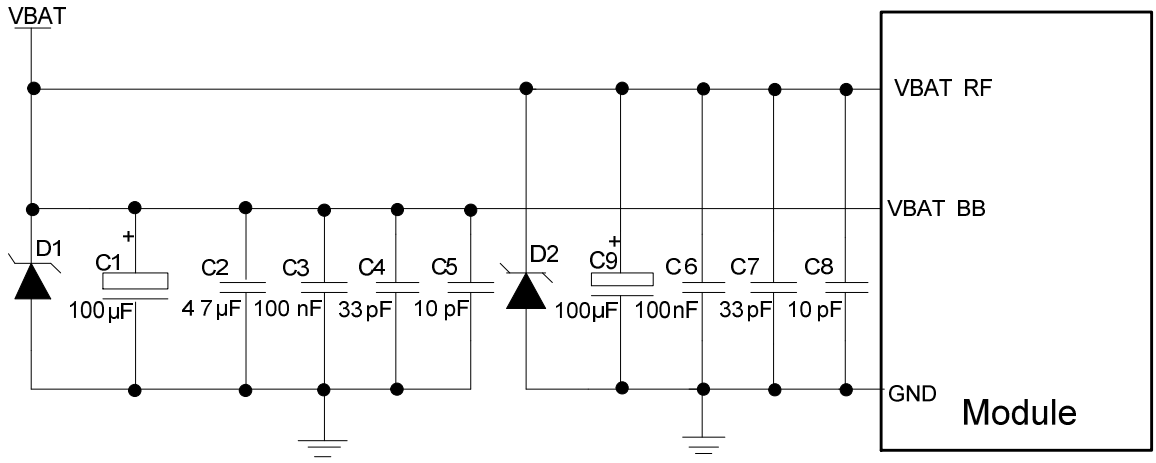


Figure 3: Star Structure of the Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of SC200R series module should be able to provide sufficient current of at least 3 A. If the voltage drop between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5 V input power source. The typical output voltage is 3.8 V and the maximum load current is 5.0 A.

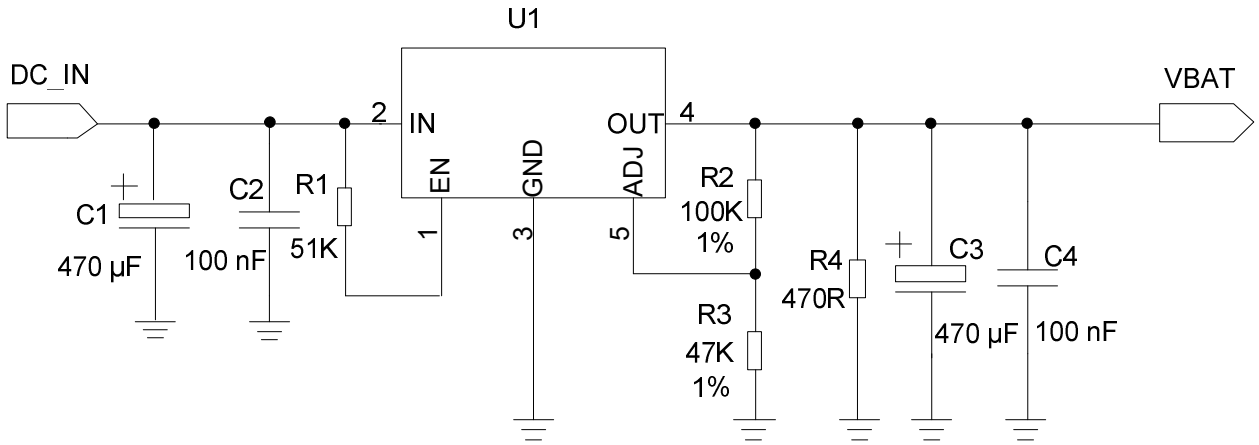


Figure 4: Reference Circuit of Power Supply

NOTES

1. It is recommended to switch off the power supply when the module is in abnormal state, and then switch on the power to restart the module.
2. The module supports battery charging by default. If the above power supply design is adopted, make sure the charging function is disabled by software, or connect VBAT to a Schottky diode in series to avoid the reverse current to the power supply chip.

3.5. Turn on and off Scenarios

3.5.1. Turn on the Module Using PWRKEY

The module can be turned on by driving the PWRKEY pin low for at least 1.6 s. The PWRKEY pin is pulled up to 1.8 V internally. It is recommended to use an open drain/collector driver to control PWRKEY. A simple reference circuit is illustrated in the following figure.

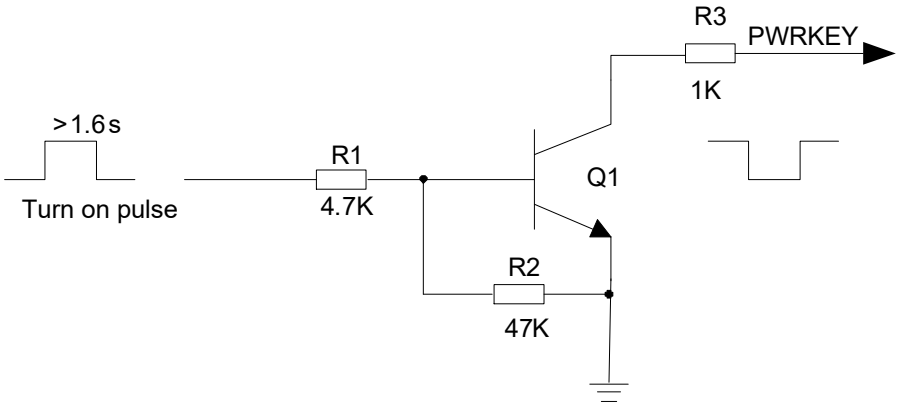


Figure 5: Turn on the Module Using Driving Circuit

The other way to control PWRKEY is by using a button directly. You must place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

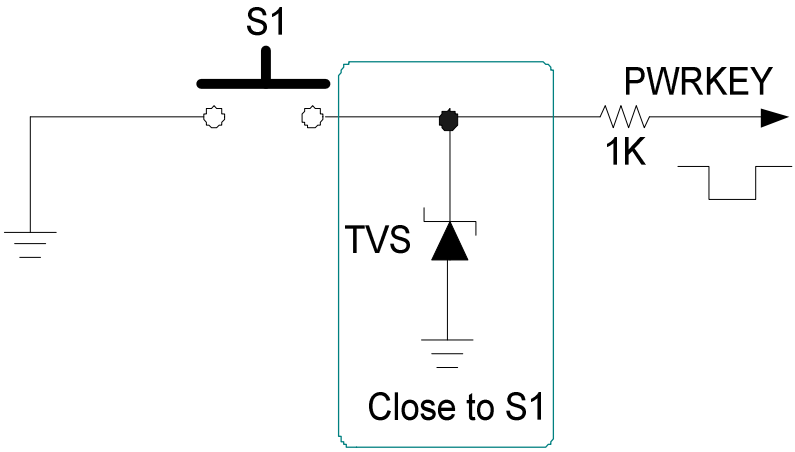


Figure 6: Turn on the Module Using Keystroke

The turning on scenario is illustrated in the following figure.

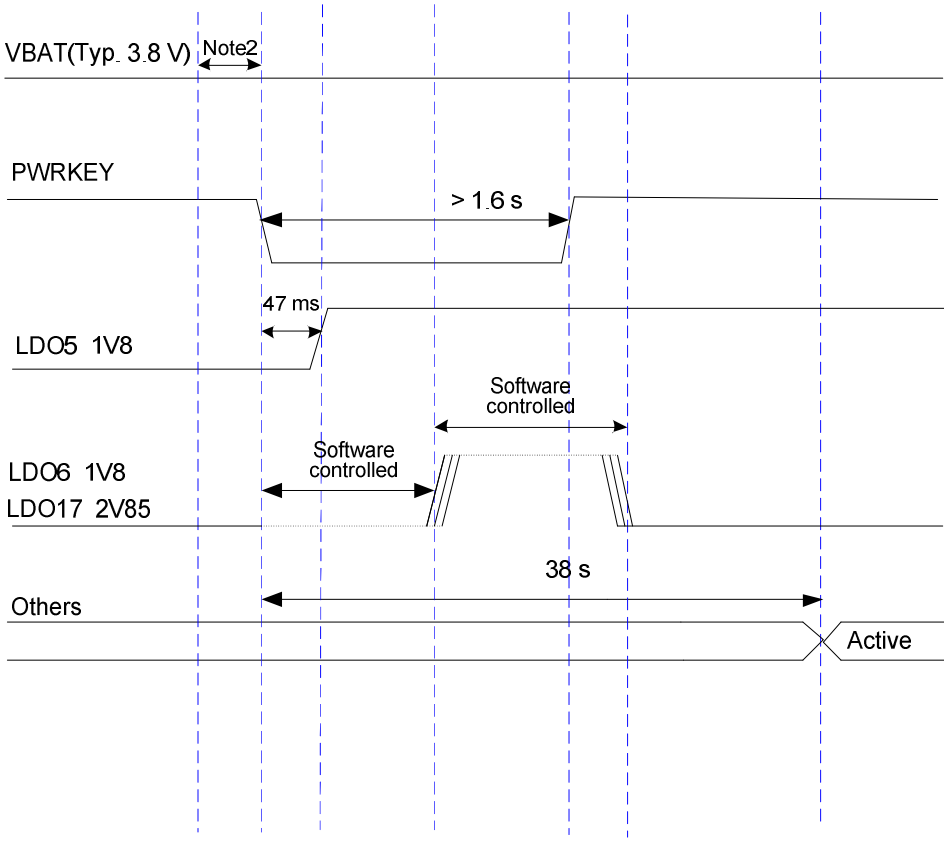


Figure 7: Timing of Turning on the Module

NOTES

1. When the module is powered on for the first time, its timing of turning on may be different from that shown above.
2. Make sure that VBAT is stable before pulling down PWRKEY. It is recommended to wait until VBAT to be stable at 4.0 V for at least 30 ms before pulling down PWRKEY. Additionally, PWRKEY cannot be pulled down all the time.

3.5.2. Turn off the Module

Drive the PWRKEY pin low for at least 1 s, and then choose to turn off the module when the prompt window comes up.

You can also force the module to power off by driving PWRKEY low for at least 8 s. The forced power-down scenario is illustrated in the following figure.

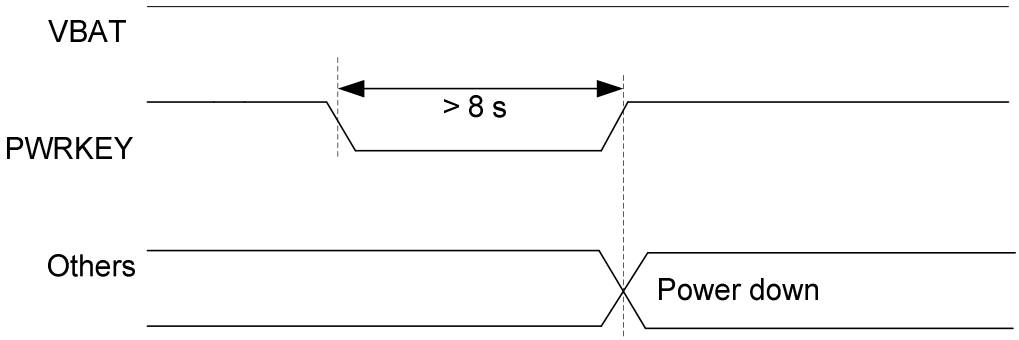


Figure 8: Timing of Turning off the Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for VBAT. The external power source can be a rechargeable battery (such as a coin cell) according to application demands. A reference circuit design is shown below.

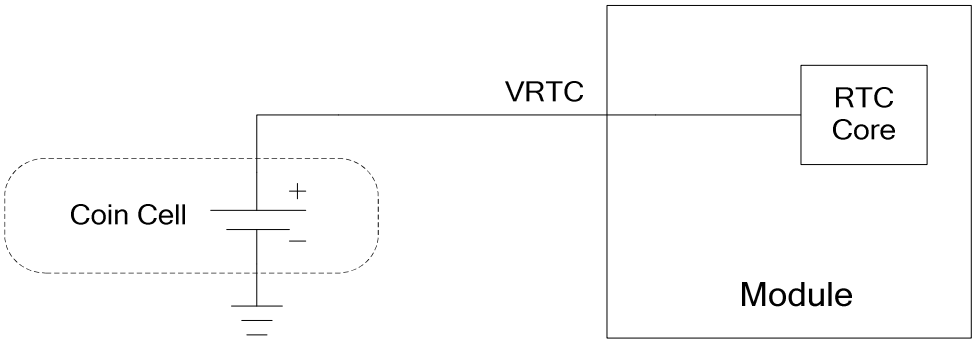


Figure 9: RTC Powered by Coin Cell

If RTC is ineffective, it can be synchronized through the network after the module is powered on. The recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3.0 V.

3.7. Power Output

SC200R series module supports output of regulated voltages for peripheral circuits. During application, it is recommended to connect a 33 pF and a 10 pF capacitor in parallel in the circuit to suppress high-frequency noise.

Table 9: Power Description

Pin Name	Default Voltage (V)	Driving Current (mA)	Idle
LDO5_1V8	1.8	20	Keep
LDO6_1V8[1)]	1.8	150	/
LDO10_2V85	2.85	150	/
LDO17_2V85	2.85	450	/
LDO16_2V8	2.8	55	/
SD_LDO12	1.8/2.95	50	/
SD_LDO11	2.95	800	/
USIM1_VDD	1.8/2.95	55	/
USIM2_VDD	1.8/2.95	55	/

NOTE

[1)] When the module is in sleep mode, LDO6_1V8 wakes up periodically or randomly. Considering the actual requirement for power consumption during sleep mode, you can use either LDO6_1V8 or an external LDO for power supply. If you require lower power consumption during sleep mode, use an external LDO for power supply.

3.8. Battery Charging and Management

SC200R series module supports battery charging. The battery charger in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** There are two steps in this mode. When the battery voltage is below 2.8 V, a 90 mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.8 V and 3.2 V, the charging current can be set to 450 mA maximally.
- **Constant current mode (CC mode):** When the battery is increased to between 3.2 V and 4.2 V, the system will switch to CC mode. The maximum charging current is 1.44 A when an adapter is used for battery charging, and the maximum charging current is 450 mA for USB charging.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.2 V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, charging is completed.

Table 10: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_SNS	133	AI	Battery voltage detect	The maximum input voltage is 4.2 V.
BAT_THERM	134	AI	Battery temperature detect	Internally pulled up. Externally connect it to the 47 kΩ NTC thermistor. If it is not used, connect it to GND with a 47 kΩ resistor.
BAT_ID	185	AI	Battery type detect	Internal pulled down with a 100 kΩ resistor. If it is not used, keep it open.
CHG_SEL	127	DI	Charger select	If you use an internal charging chip, keep this pin open. If you use an external charging chip, connect it to GND.

SC200R series module supports battery temperature detection in the condition that the battery integrates a thermistor (47 kΩ 1 % NTC thermistor with a B-constant of 4050 K by default) and the thermistor is connected to BAT_THERM pin. If the BAT_THERM pin is not connected, there will be malfunctions such as battery charging failure, battery level display error, etc. The default battery temperature range is -3.0 °C to 48.5 °C.

A reference design for the battery charging circuit is shown below.

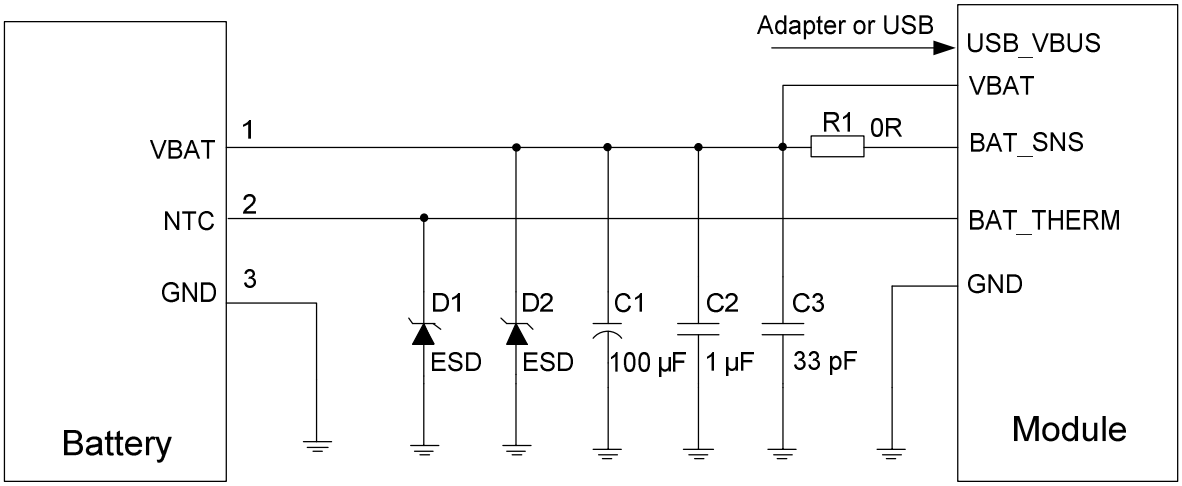


Figure 10: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones or handheld POS systems are powered by batteries. For different batteries, you should modify the charging and discharging curve correspondingly to achieve the best performance.

If the thermistor is not available in the battery, or an adapter is utilized to power the module, you must connect BAT_THERM to GND via a 47 kΩ resistor. Otherwise, the system may mistakenly judge that the battery temperature is abnormal, and therefore cause battery charging failure.

BAT_SNS must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as associated problems with power-on/off and battery charging/discharging.

3.9. USB Interface

SC200R series module provides one integrated Universal Serial Bus (USB) interface which complies with USB 2.0 specification and supports high speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface supports USB OTG and is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PI	USB 5 V power input and USB connection detect	Vmax = 6.2 V Vmin = 4.35 V Vnorm = 5.0 V
USB_DM	13	AI/AO	USB 2.0 differential data (-)	USB 2.0 standard compliant. 90 Ω differential impedance.
USB_DP	14	AI/AO	USB 2.0 differential data (+)	
USB_ID	16	AI	USB ID detect	High level by default.

For the design of USB 2.0 interface, it is recommended to connect USB_ID directly to the USB_ID pin of the external USB port for USB ID detection. When you insert a device into the external USB port, the USB_ID pin of the module will be pulled down to make the module enter host mode.

You can choose either to support USB OTG or not. The following figures show the reference designs.

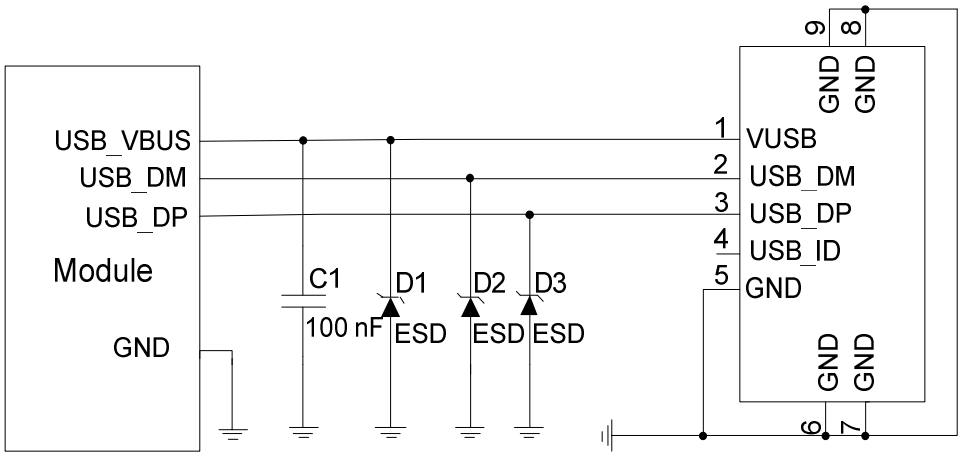


Figure 11: USB Interface Reference Design (OTG Not Supported)

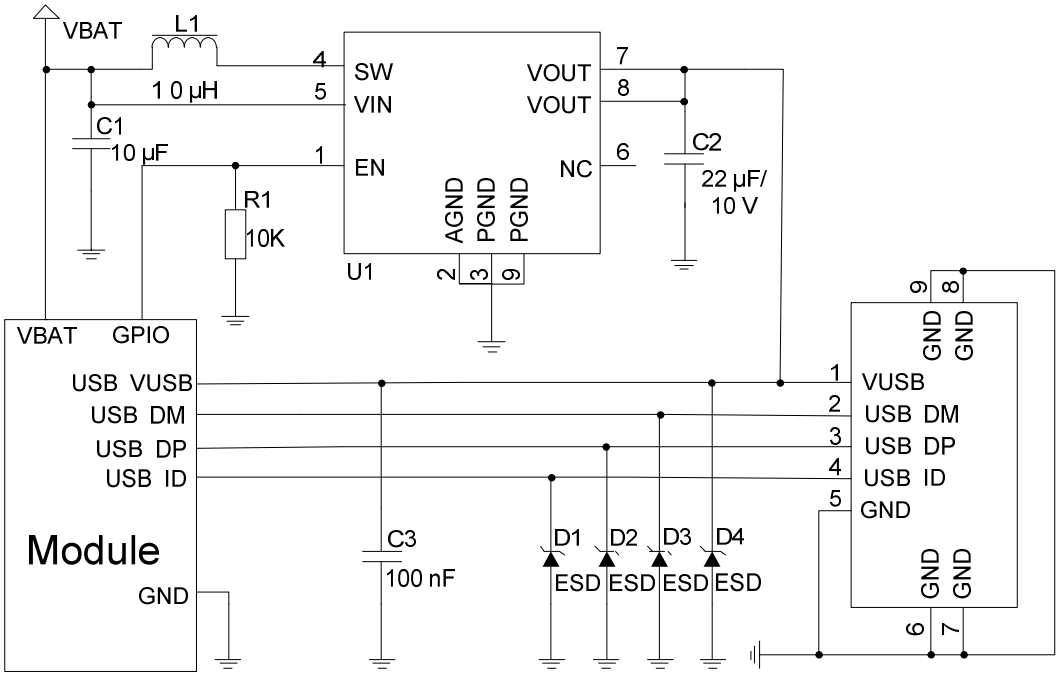


Figure 12: USB Interface Reference Design (OTG Supported)

In order to ensure USB performance, comply with the following principles when designing the USB interface.

- Route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace should be 90 Ω.
- Keep the ESD protection devices as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2 pF.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. Route the USB differential traces in inner-layer with ground shielding on not only the upper and lower layers but also the right and left sides.
- Make sure the trace length difference between USB 2.0 differential data signals is less than 0.7 mm.

Table 12: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (DP-DM)
13	USB_DM	32.25	-0.10
14	USB_DP	32.15	

3.10. UART Interfaces

SC200R series module provides three UART interfaces and supports up to 4 Mbps:

- **UART5:** 4-wire UART interface, hardware flow control supported
- **UART2 (debug UART):** 2-wire UART interface, used for debugging by default
- **UART1:** 2-wire UART interface

Table 13: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART5_TXD	34	DO	UART5 transmit data	1.8 V power domain. If not used, keep these pins open.
UART5_RXD	35	DI	UART5 receive data	
UART5_CTS	36	DI	UART5 clear to send	
UART5_RTS	37	DO	UART5 request to send	
DBG_RXD	93	DI	UART2 (debug UART) receive data	
DBG_TXD	94	DO	UART2 (debug UART) transmit data	
UART1_RXD	153	DI	UART1 receive data	
UART1_TXD	154	DO	UART1 transmit data	

UART5 is a 4-wire UART interface with 1.8 V power domain. You should use a level translator if your application is equipped with a 3.3 V UART interface. The following figure shows the reference design.

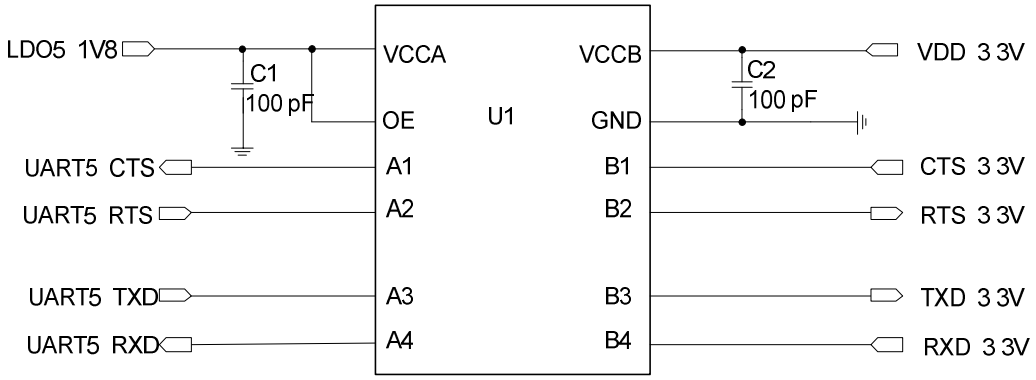


Figure 13: Reference Circuit with Level Translator Chip (for UART5)

The following figure is an example of connection between the module and PC. It is recommended to add a level translator and an RS-232 level translator chip between the module and PC. The following figure shows the reference design.

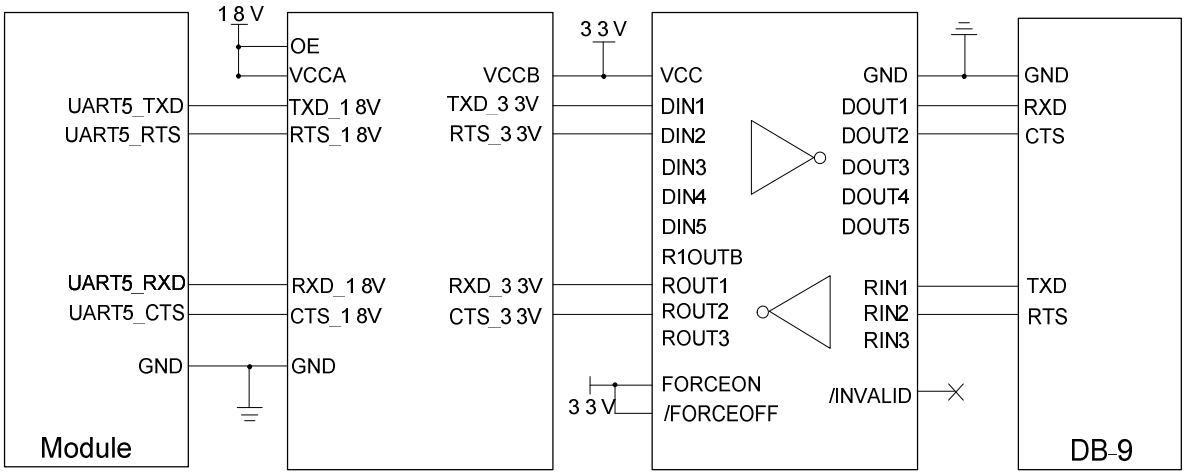


Figure 14: RS-232 Level Match Circuit (for UART5)

NOTE

UART2 and UART1 are similar to UART5. For the reference design, refer to that of UART5.

3.11. (U)SIM Interfaces

SC200R series module provides two (U)SIM interfaces that meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM card is powered by the internal power supply of the module.

Table 14: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	Active low. Externally pull it up to 1.8 V. If it is not used, keep it open. This function is disabled by default via software. Cannot be multiplexed into a generic GPIO.

USIM2_RST	18	DO	(U)SIM2 card reset	Cannot be multiplexed into generic GPIOs.
USIM2_CLK	19	DO	(U)SIM2 card clock	
USIM2_DATA	20	IO	(U)SIM2 card data	
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	Active low. Externally pull it up to 1.8 V. If it is not used, keep it open. This function is disabled by default via software. Cannot be multiplexed into a generic GPIO.
USIM1_RST	23	DO	(U)SIM1 card reset	Cannot be multiplexed into generic GPIOs.
USIM1_CLK	24	DO	(U)SIM1 card clock	
USIM1_DATA	25	IO	(U)SIM1 card data	
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.

SC200R series module supports (U)SIM card hot-plug via the USIM_DET pin. (This function is disabled by default via software. To enable it, contact Quectel Technical Supports to change the software configuration.) A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

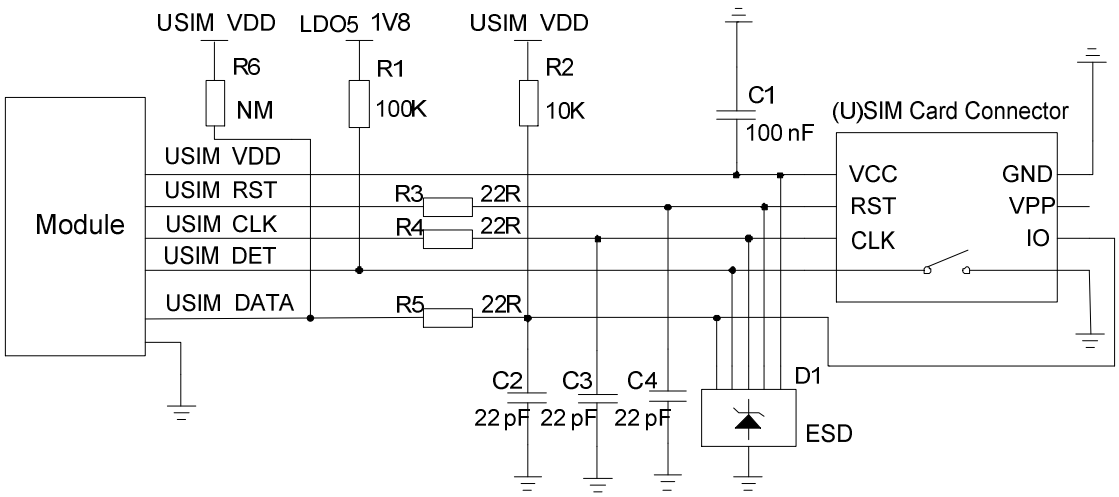


Figure 15: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If you do not need to use USIM_DET, keep this pin open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

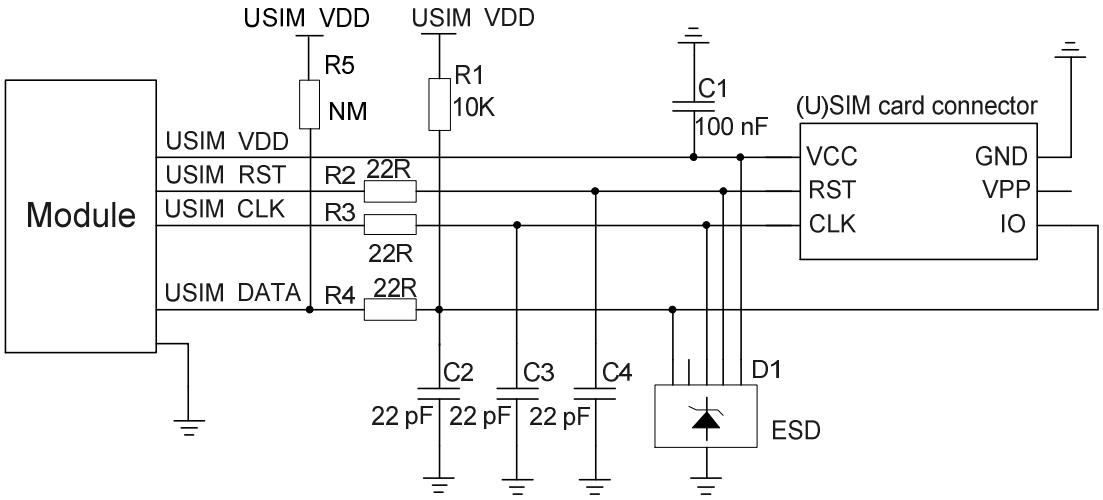


Figure 16: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to ensure good performance and avoid damage of (U)SIM cards, follow the criteria listed below during (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Reserve a filter capacitor for USIM_VDD, and its maximum capacitance should not exceed 1 μF. Additionally, place the capacitor near the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.
- In order to ensure good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50 pF. Add 22 Ω resistors in series between the module and (U)SIM card to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- Add 22 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST signal lines to filter RF interference, and place them as close to the (U)SIM card connector as possible.
- Place the reserved pull-up resistors R6 and R5 in ***Figure 16*** and ***17*** close to the module.

3.12. SD Card Interface

SD Card interface of SC200R series module supports SD 3.0 protocol. The pin definition of SD card interface is shown below.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	39	DO	High-speed digital clock signal of SD card	50 Ω characteristic impedance.
SD_CMD	40	IO	Command signal of SD card	
SD_DATA0	41	IO	High-speed bidirectional digital signals of SD card	
SD_DATA1	42	IO		
SD_DATA2	43	IO		
SD_DATA3	44	IO		
SD_DET	45	DI	SD card hot-plug detect	Active low.
SD_LDO11	38	PO	2.95 V output power supply	Power supply for SD card.
SD_LDO12	32	PO	1.8/2.95 V output power supply	Power supply for SD card pull-up circuits.

A reference circuit for the SD card interface is shown below.

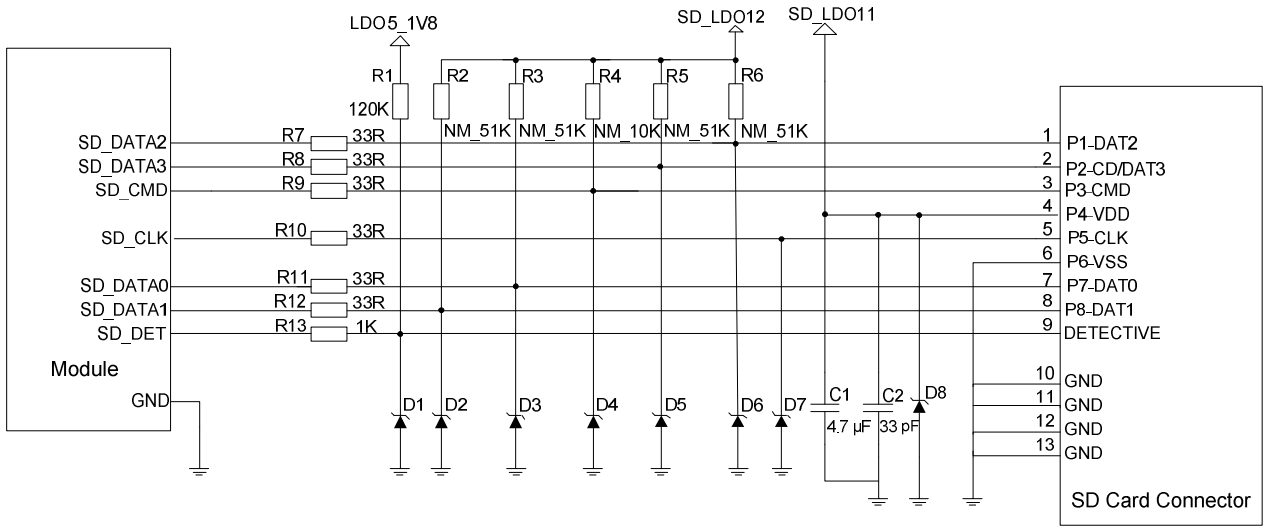


Figure 17: Reference Circuit for SD Card Interface

SD_LDO11 is the power supply for the SD card and can provide up to 800 mA output current. Due to the high output current, it is recommended that the trace width should be at least 0.8 mm. In order to ensure stability of output current, add a 4.7 μF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2, and SD_DATA3 are all high-speed signal lines. In PCB design, control the characteristic impedance of them to 50 Ω, and do not cross them with other traces. It is recommended to route the traces on the inner layer of PCB and keep them of the same length. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control the impedance to 50 Ω ±10 % and add ground shielding.
- The total trace length difference between SD_CLK and other signal traces like SD_CMD and SD_DATA should not exceed 1 mm.

Table 16: SD Card Trace Length Inside the Module

Pin No.	Signal	Length (mm)
39	SD_CLK	21.50
40	SD_CMD	21.40
41	SD_DATA0	21.45
42	SD_DATA1	21.60
43	SD_DATA2	21.40
44	SD_DATA3	21.35

3.13. GPIO Interfaces

SC200R series module has abundant GPIO interfaces with a power domain of 1.8 V. The pin definition is listed below.

Table 17: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	GPIO No.	Default State	Comment
GPIO_6	167	GPIO_6	B-PD:nppukp[1)]	
GPIO_7	168	GPIO_7	B-PD:nppukp	
GPIO_12	101	GPIO_12	B-PD:nppukp	Wakeup[2)]
GPIO_13	102	GPIO_13	B-PD:nppukp	Wakeup
GPIO_20	119	GPIO_20	B-PD:nppukp	
GPIO_21	118	GPIO_21	B-PD:nppukp	Wakeup
GPIO_22	117	GPIO_22	B-PD:nppukp	
GPIO_23	116	GPIO_23	B-PD:nppukp	
GPIO_25	90	GPIO_25	B-PD:nppukp	Wakeup
GPIO_33	33	GPIO_33	B-PD:nppukp	
GPIO_34	170	GPIO_34	B-PD:nppukp	Wakeup
GPIO_39	201	GPIO_39	B-PD:nppukp	
GPIO_42	110	GPIO_42	B-PD:nppukp	Wakeup
GPIO_43	107	GPIO_43	B-PD:nppukp	Wakeup
GPIO_44	109	GPIO_44	B-PD:nppukp	Wakeup
GPIO_45	98	GPIO_45	B-PD:nppukp	Wakeup
GPIO_46	113	GPIO_46	B-PD:nppukp	Wakeup
GPIO_47	124	GPIO_47	B-PD:nppukp	
GPIO_48	99	GPIO_48	B-PD:nppukp	Wakeup

GPIO_59	100	GPIO_59	B-PD:nppukp	Wakeup
GPIO_61	267	GPIO_61	B-PD:nppukp	Wakeup
GPIO_62	123	GPIO_62	B-PD:nppukp	Wakeup
GPIO_63	108	GPIO_63	B-PD:nppukp	Wakeup
GPIO_66	106	GPIO_66	B-PD:nppukp	
GPIO_85	265	GPIO_85	B-PD:nppukp	
GPIO_86	239	GPIO_86	B-PD:nppukp	Wakeup
GPIO_87	105	GPIO_87	B-PD:nppukp	
GPIO_88	264	GPIO_88	B-PD:nppukp	
GPIO_89	115	GPIO_89	B-PD:nppukp	
GPIO_90	177	GPIO_90	B-PD:nppukp	Wakeup
GPIO_93	112	GPIO_93	B-PD:nppukp	Wakeup
GPIO_94	104	GPIO_94	B-PD:nppukp	
GPIO_95	103	GPIO_95	B-PD:nppukp	
GPIO_127	169	GPIO_127	B-PD:nppukp	Wakeup
GPIO_130	97	GPIO_130	B-PD:nppukp	Wakeup
SD_DET	45	GPIO_67	B-PD:nppukp	Wakeup
TP_INT	30	GPIO_65	B-PD:nppukp	Wakeup
TP_RST	31	GPIO_64	B-PD:nppukp	
TP_I2C_SCL	47	GPIO_11	B-PD:nppukp	
TP_I2C_SDA	48	GPIO_10	B-PD:nppukp	
LCD_RST	49	GPIO_60	B-PD:nppukp	
LCD_TE	50	GPIO_24	B-PD:nppukp	
CAM0_MCLK	74	GPIO_26	B-PD:nppukp	
CAM1_MCLK	75	GPIO_28	B-PD:nppukp	Wakeup

CAM0_RST	79	GPIO_128	B-PD:nppukp	Wakeup
CAM0_PWDN	80	GPIO_126	B-PD:nppukp	Wakeup
CAM1_RST	81	GPIO_129	B-PD:nppukp	
CAM1_PWDN	82	GPIO_125	B-PD:nppukp	
CAM2_MCLK	165	GPIO_27	B-PD:nppukp	
CAM2_RST	164	GPIO_38	B-PD:nppukp	Wakeup
CAM2_PWDN	163	GPIO_41	B-PD:nppukp	Wakeup
VOL_UP	95	GPIO_91	B-PD:nppukp	Wakeup
VOL_DOWN	96	GPIO_50	B-PD:nppukp	Wakeup
UART5_TXD	34	GPIO_16	B-PD:nppukp	
UART5_RXD	35	GPIO_17	B-PD:nppukp	Wakeup
UART5_CTS	36	GPIO_18	B-PD:nppukp	
UART5_RTS	37	GPIO_19	B-PD:nppukp	
UART1_TXD	154	GPIO_0	B-PD:nppukp	
UART1_RXD	153	GPIO_1	B-PD:nppukp	Wakeup

NOTES

1. [1] B: Bidirectional digital with CMOS input; PD:nppukp = default pull-down with programmable options following the colon (:).
2. [2] Wakeup: Interrupt pins that can wake up the system.
3. For more details about GPIO configuration, see ***document [2]***.

3.14. I2C Interfaces

SC200R series module provides four I2C interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. The SENSOR_I2C interface only supports sensors of aDSP architecture. CAM_I2C and DCAM_I2C signals are controlled by Linux Kernel code and support connection with devices related to video output.

Table 18: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	47	OD	I2C clock signal of touch panel	Used for touch panel
TP_I2C_SDA	48	OD	I2C data signal of touch panel	
CAM_I2C_SCL	83	OD	I2C clock signal of camera	Used for camera
CAM_I2C_SDA	84	OD	I2C data signal of camera	
DCAM_I2C_SCL	166	OD	I2C clock signal of camera	Used for camera
DCAM_I2C_SDA	205	OD	I2C data signal of camera	
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor	Used for external sensor
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor	

3.15. SPI Interfaces

SC200R series module provides three SPI interfaces, which are multiplexed from UART and GPIO interfaces. These interfaces can only support master mode and can be used for fingerprint recognition.

Table 19: Pin Definition of SPI Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART5_RXD	35	DI	SPI5 data input	Can be multiplexed into SPI5_MISO
UART5_TXD	34	DO	SPI5 data output	Can be multiplexed into SPI5_MOSI
UART5_RTS	37	DO	SPI5 clock	Can be multiplexed into SPI5_CLK

UART5_CTS	36	DO	SPI5 chip select	Can be multiplexed into SPI5_CS
GPIO_22	117	DO	SPI6 chip select	Can be multiplexed into SPI6_CS
GPIO_23	116	DO	SPI6 clock	Can be multiplexed into SPI6_CLK
GPIO_20	119	DO	SPI6 data output	Can be multiplexed into SPI6_MOSI
GPIO_21	118	DI	SPI6 data input	Can be multiplexed into SPI6_MISO
GPIO_87	105	DO	SPI7 chip select	Can be multiplexed into SPI7_CS
GPIO_85	265	DO	SPI7 data output	Can be multiplexed into SPI7_MOSI
GPIO_88	264	DO	SPI7 clock	Can be multiplexed into SPI7_CLK
GPIO_86	239	DI	SPI7 data input	Can be multiplexed into SPI7_MISO

3.16. ADC Interface

SC200R series module supports one analog-to-digital converter (ADC) interface. The ADC interface supports resolution of up to 15 bits. The pin definition is shown below.

Table 20: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC	128	AI	Generic ADC	The maximum input voltage is 1.7 V.

3.17. Motor Drive Interface

The pin definition of the motor drive interface is listed below.

Table 21: Pin Definition of Motor Drive Interface

Pin Name	Pin No.	I/O	Description	Comment
VIB_DRV_N	28	PO	Motor drive	Connect it to the negative pole of the motor.

The motor is driven by an exclusive circuit, and a reference circuit is shown below.

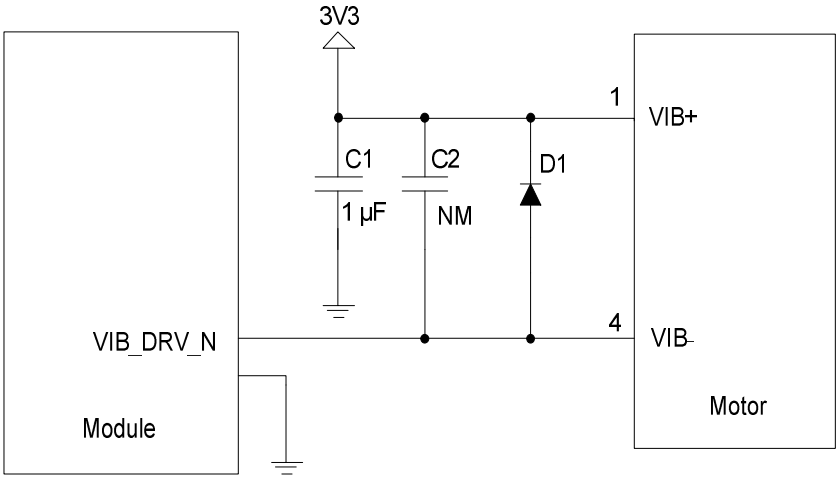


Figure 18: Reference Circuit for Motor Connection

When the motor stops working and the VIB_DRV_N is disconnected, the redundant electricity on the motor can be discharged from the circuit loop formed by diodes, thus avoiding damage to components.

3.18. LCM Interface

SC200R series module provides one LCM interface, which is MIPI_DSI standard compliant. The interface supports high-speed differential data transmission and supports HD+ display (1440 × 720 @ 60 fps). The pin definition of the LCM interface is shown below.

Table 22: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LDO17_2V85	129	PO	2.85 V output power supply for LCM VCC	
PWM	29	DO	PWM output which adjusts the backlight brightness	
LCD_RST	49	DO	LCD reset	1.8 V power domain
LCD_TE	50	DI	LCD tearing effect	
DSI_CLK_N	52	AO	LCD MIPI clock (-)	
DSI_CLK_P	53	AO	LCD MIPI clock (+)	

DSI_LN0_N	54	AO	LCD MIPI data 0 (-)
DSI_LN0_P	55	AO	LCD MIPI data 0 (+)
DSI_LN1_N	56	AO	LCD MIPI data 1 (-)
DSI_LN1_P	57	AO	LCD MIPI data 1 (+)
DSI_LN2_N	58	AO	LCD MIPI data 2 (-)
DSI_LN2_P	59	AO	LCD MIPI data 2 (+)
DSI_LN3_N	60	AO	LCD MIPI data 3 (-)
DSI_LN3_P	61	AO	LCD MIPI data 3 (+)

A reference circuit for the LCM interface is shown below.

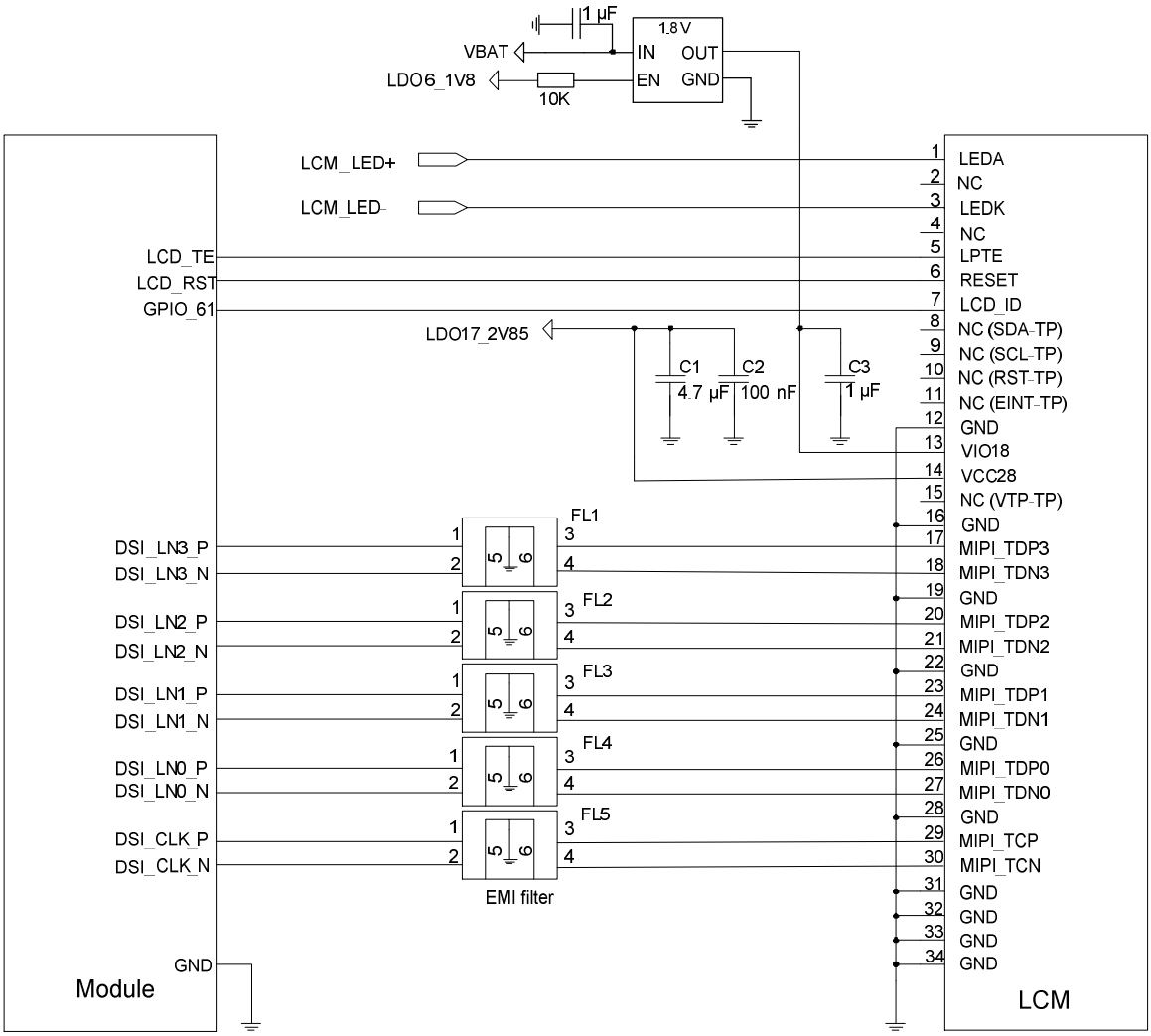


Figure 19: Reference Circuit Design for LCM Interface

MIPI are high-speed signal lines. It is recommended to add common-mode filters in series near the LCM connector, to improve protection against electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that the LCM factory should burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pin of the module, but you need to make sure that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

You can design the external backlight driving circuit for LCM according to actual requirements. A reference circuit design is shown in the following figure, in which the PWM pin is used to adjust the backlight brightness.

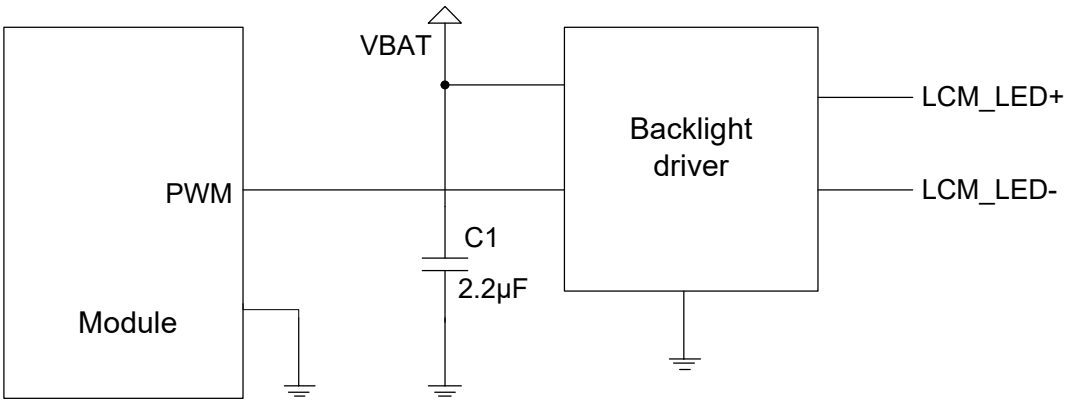


Figure 20: Reference Design for External Backlight Driving Circuit

3.19. Touch Panel Interface

SC200R series module provides one I2C interface for connection with Touch Panel (TP), and also provides the corresponding power supply and interrupt pins. The definitions of TP interface pins are illustrated below.

Table 23: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
LDO17_2V85	129	PO	2.85 V output power supply for TP VDD	Vnorm = 2.85 V $I_O$max = 450 mA
LDO6_1V8	125	PO	1.8 V output power supply for TP I/O power domain and I2C pull-up circuit	Vnorm = 1.8 V $I_O$max = 150 mA

TP_INT	30	DI	Interrupt signal of TP	1.8 V voltage domain.
TP_RST	31	DO	Reset signal of TP	1.8 V voltage domain. Active low.
TP_I2C_SCL	47	OD	I2C clock signal of TP	Externally pull them up to 1.8 V. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	I2C data signal of TP	

A reference circuit for the TP interface is shown below.

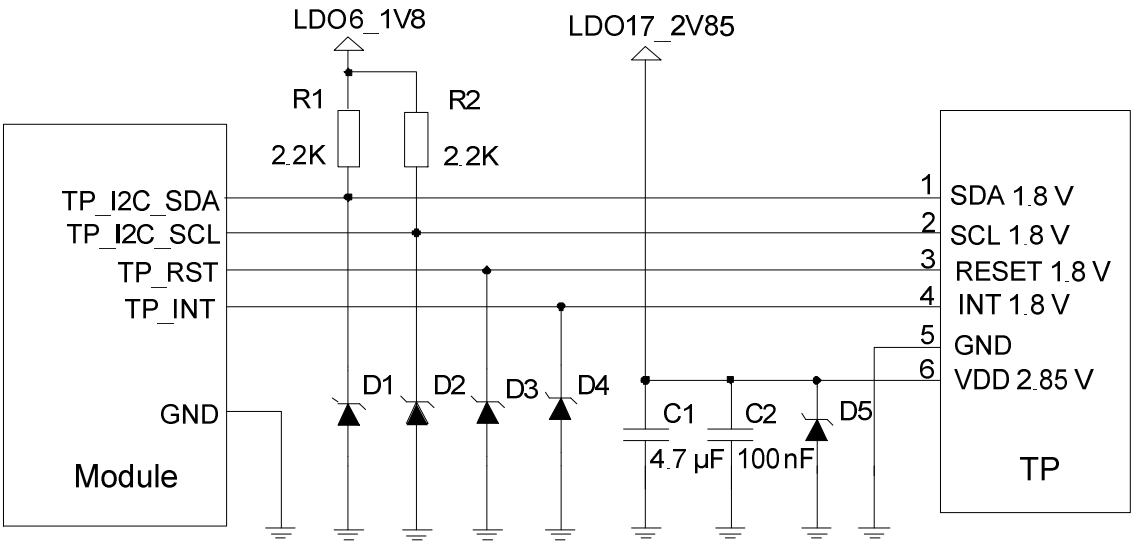


Figure 21: Reference Circuit Design for TP Interface

3.20. Camera Interfaces

Based on MIPI_CSI standard, SC200R series module supports two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane), and the maximum pixel of the camera can be up to 13 MP. The video and photo quality is determined by various factors such as the camera sensor, camera lens quality, etc.

Table 24: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
LDO6_1V8	125	PO	1.8 V output power supply for DOVDD of camera	Vnorm = 1.8 V $I_O$max = 150 mA
LDO17_2V85	129	PO	2.85 V output power supply for AVDD of camera	Vnorm = 2.85 V $I_O$max = 450 mA
CSI1_CLK_N	63	AI	Camera MIPI clock signal (-)	
CSI1_CLK_P	64	AI	Camera MIPI clock signal (+)	
CSI1_LN0_N	65	AI	Camera MIPI data 0 signal (-)	
CSI1_LN0_P	66	AI	Camera MIPI data 0 signal (+)	
CSI1_LN1_N	67	AI	Camera MIPI data 1 signal (-)	
CSI1_LN1_P	68	AI	Camera MIPI data 1 signal (+)	
CSI1_LN3_N	70	AI	Camera MIPI data 3 signal (-)	
CSI1_LN3_P	71	AI	Camera MIPI data 3 signal (+)	
CSI1_LN2_N	72	AI	Camera MIPI data 2 signal (-)	
CSI1_LN2_P	73	AI	Camera MIPI data 2 signal (+)	
CSI0_CLK_N	157	AI	Camera MIPI clock signal (-)	
CSI0_CLK_P	196	AI	Camera MIPI clock signal (+)	
CSI0_LN0_N	158	AI	Camera MIPI data 0 signal (-)	
CSI0_LN0_P	197	AI	Camera MIPI data 0 signal (+)	
CSI0_LN1_N	159	AI	Camera MIPI data 1 signal (-)	
CSI0_LN1_P	198	AI	Camera MIPI data 1 signal (+)	

CSI0_LN2_N	160	AI	Camera MIPI data 2 signal (-)	
CSI0_LN2_P	199	AI	Camera MIPI data 2 signal (+)	
CSI0_LN3_N	161	AI	Camera MIPI data 3 signal (-)	
CSI0_LN3_P	200	AI	Camera MIPI data 3 signal (+)	
CAM0_MCLK	74	DO	Clock signal of camera	1.8 V power domain.
CAM1_MCLK	75	DO	Clock signal of camera	
CAM0_RST	79	DO	Reset signal of camera	
CAM0_PWDN	80	DO	Power down signal of camera	
CAM1_RST	81	DO	Reset signal of camera	
CAM1_PWDN	82	DO	Power down signal of camera	
CAM_I2C_SCL	83	OD	I2C clock signal of camera	Externally pull them up to 1.8 V.
CAM_I2C_SDA	84	OD	I2C data signal of camera	
CAM2_MCLK	165	DO	Clock signal of camera	1.8 V power domain.
CAM2_RST	164	DO	Reset signal of camera	
CAM2_PWDN	163	DO	Power down signal of camera	
DCAM_I2C_SDA	205	OD	I2C data signal of camera	Externally pull them up to 1.8 V.
DCAM_I2C_SCL	166	OD	I2C clock signal of camera	

The following is a reference circuit design for 3-camera applications.

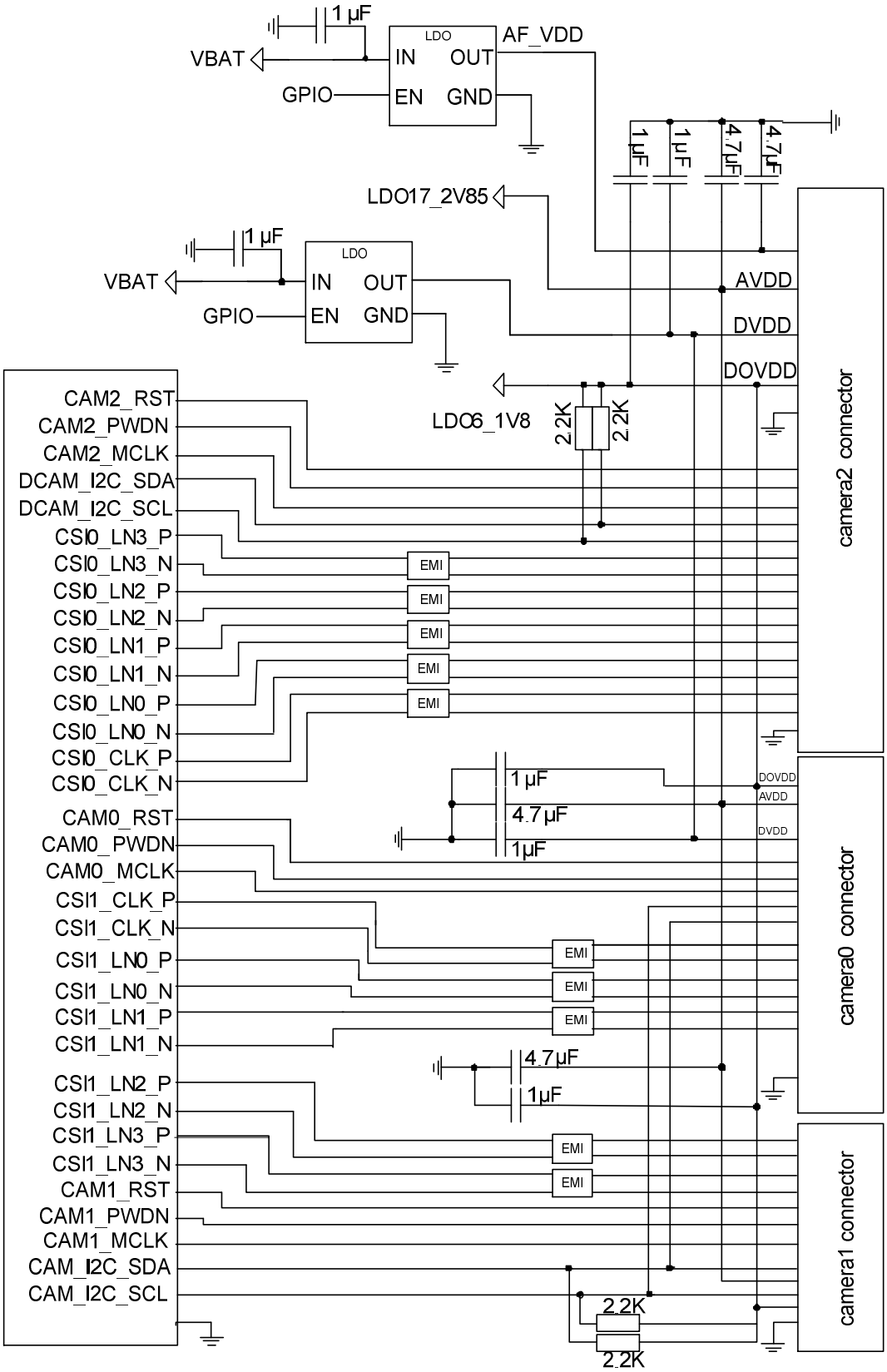


Figure 22: Reference Circuit Design for 3-Camera Applications

NOTE

In 3-camera applications, CSI1_LN3_P and CSI1_LN3_N are used as CLK_P and CLK_N of camera1, CSI1_LN2_P and CSI1_LN2_N are used as the LN_P and LN_N of the camera1.

3.20.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Make sure the module and the connectors are correctly connected .
- MIPI are high speed signal lines, supporting maximum data rate of up to 2.1 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, keep all the MIPI traces of the same length. In order to avoid crosstalk, keep a distance of 1.5 times the trace width among MIPI signal lines. During impedance matching, do not connect GND on different planes to ensure impedance consistency.
- It is recommended to select a low-capacitance TVS for ESD protection and the recommended parasitic capacitance should be below 1 pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 305 mm;
  b) Control the differential impedance to 100 Ω ±10 %;
  c) Control intra-lane length difference within 0.67 mm;
  d) Control inter-lane length difference within 1.3 mm.

Table 25: MIPI Trace Length Inside the Module

Pin Name	Pin No.	Length (mm)	Length Difference (P-N)
52	DSI_CLK_N	12.40	0.00
53	DSI_CLK_P	12.40	
54	DSI_LN0_N	11.75	-0.10
55	DSI_LN0_P	11.65	
56	DSI_LN1_N	9.40	-0.10
57	DSI_LN1_P	9.30	
58	DSI_LN2_N	9.60	0.00
59	DSI_LN2_P	9.60	
60	DSI_LN3_N	12.35	0.00

61	DSI_LN3_P	12.35	
63	CSI1_CLK_N	18.10	-0.05
64	CSI1_CLK_P	18.05	
65	CSI1_LN0_N	18.05	0.05
66	CSI1_LN0_P	18.10	
67	CSI1_LN1_N	18.15	0.05
68	CSI1_LN1_P	18.20	
70	CSI1_LN3_N	18.10	0.10
71	CSI1_LN3_P	18.20	
72	CSI1_LN2_N	18.05	0.05
73	CSI1_LN2_P	18.10	
157	CSI0_CLK_N	22.60	-0.05
196	CSI0_CLK_P	22.55	
158	CSI0_LN0_N	22.55	-0.05
197	CSI0_LN0_P	22.50	
159	CSI0_LN1_N	20.25	0.05
198	CSI0_LN1_P	20.30	
160	CSI0_LN2_N	20.50	0.00
199	CSI0_LN2_P	20.50	
161	CSI0_LN3_N	12.95	0.00
200	CSI0_LN3_P	12.95	

3.21. Sensor Interfaces

SC200R series module supports communication with sensors via I2C interfaces, and it supports ALS/PS, compass, accelerometer, gyroscope, etc.

Table 26: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	Dedicated for external sensors. Cannot be used for touch panel, NFC, I2C keyboard, etc. Externally pull them up to 1.8 V.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	
GPIO_43	107	DI	Light sensor interrupt	
GPIO_44	109	DI	Compass sensor interrupt	
GPIO_42	110	DI	Accelerometer sensor interrupt	
GPIO_63	108	DI	Gyroscope sensor interrupt	

3.22. Audio Interfaces

SC200R series module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 27: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	4	AI	Main microphone input (+)	
MIC_GND	5	AI	Microphone reference ground	If it is not used, connect it to the ground.
MIC2_P	6	AI	Microphone input for headset (+)	
MIC_BIAS2	155	AO	Microphone bias voltage 2	V_O = 1.6–2.85 V

MIC3_P	148	AI	Secondary microphone input (+)	
MIC_BIAS1	147	AO	Microphone bias voltage 1	V_O = 1.6–2.85 V
EAR_P	8	AO	Earpiece output (+)	
EAR_N	9	AO	Earpiece output (-)	
SPK_P	10	AO	Speaker output (+)	
SPK_N	11	AO	Speaker output (-)	
HPH_R	136	AO	Headphone right channel output	
HPH_REF	137	AO	Headphone reference ground	
HPH_L	138	AO	Headphone left channel output	
HS_DET	139	AI	Headset insertion detect	High level by default.

- The module offers three audio input channels, including three single-ended channels.
- The output voltage range of the two MIC_BIAS is programmable between 1.6 V and 2.85 V, and the maximum output current is 3 mA.
- The earpiece interface uses differential output.
- The loudspeaker interface uses differential output as well. The output channel is available with a Class-D amplifier whose output power is 1362 mW when the load is 8 Ω.
- The headphone interface features stereo left and right channel output, and supports headphone insertion detect.

3.22.1. Reference Circuit Design for Microphone Interfaces

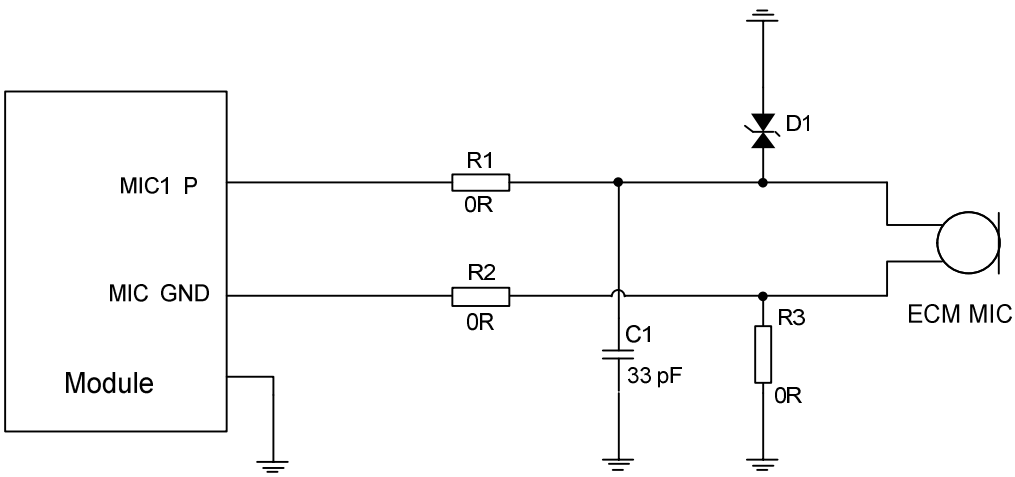


Figure 23: Reference Circuit Design for ECM Microphone Interface

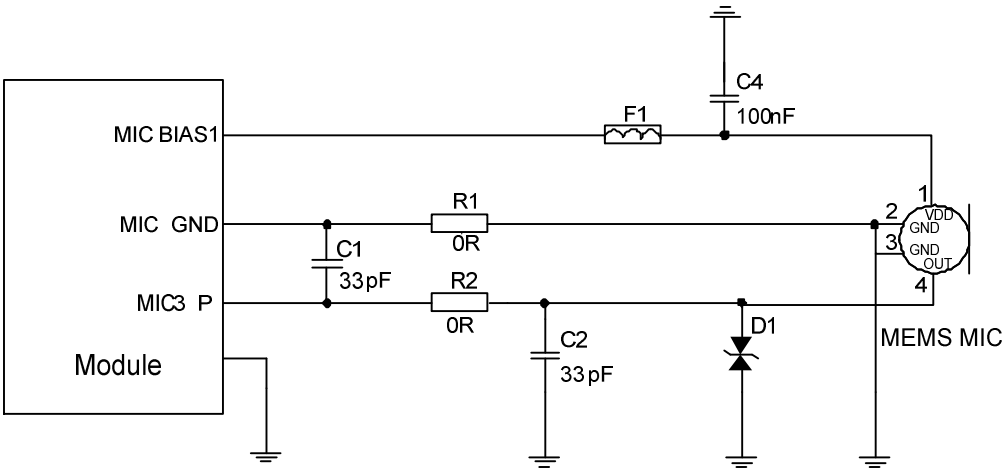


Figure 24: Reference Circuit Design for MEMS Microphone Interface

3.22.2. Reference Circuit Design for Earpiece Interface

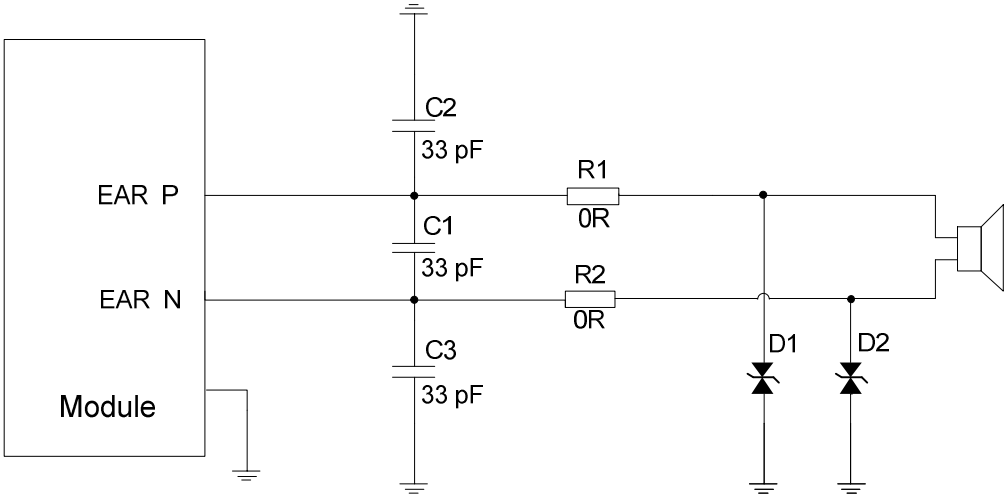


Figure 25: Reference Circuit Design for Earpiece Interface

3.22.3. Reference Circuit Design for Headphone Interface

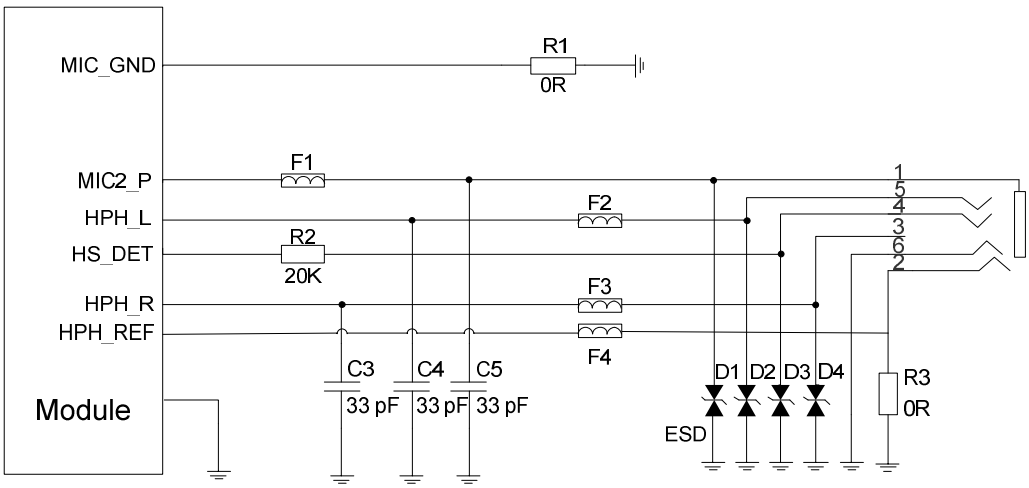


Figure 26: Reference Circuit Design for Headphone Interface

3.22.4. Reference Circuit Design for Loudspeaker Interface

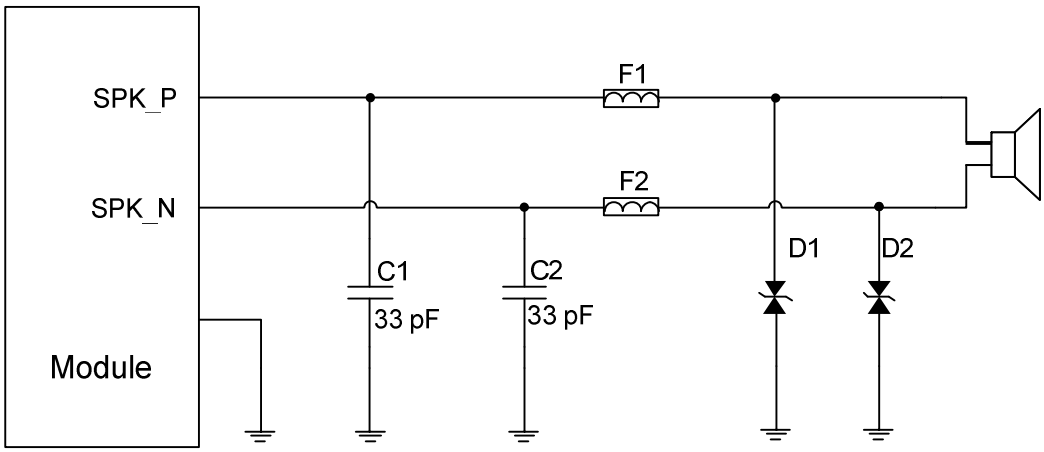


Figure 27: Reference Circuit Design for Loudspeaker Interface

3.22.5. Design Considerations for Audio Interfaces

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied to filter out RF interference when the module is transmitting at EGSM900. Without this capacitor, TDD noise could be heard during voice calls. The 10 pF capacitor is used to filter out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on its material and manufacturing

technique. Therefore, you should consult the capacitor vendors to choose the most suitable capacitor to filter out the high-frequency noises.

The severity of RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, you should select a suitable capacitor accroding to the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, place RF antennas away from audio interfaces and audio traces. Additionally, keep power traces far away from the audio traces and do not route them in parallel.

Route the differential audio traces according to the differential signal layout rule.

3.23. Emergency Download Interface

USB_BOOT is an emergency download interface. You can force the module to enter emergency download mode by pulling it up to LDO5_1V8 during power-up. This is an emergency option when failures such as abnormal start-up or running occur. For firmware upgrade and debugging in the future, reserve the following reference design.

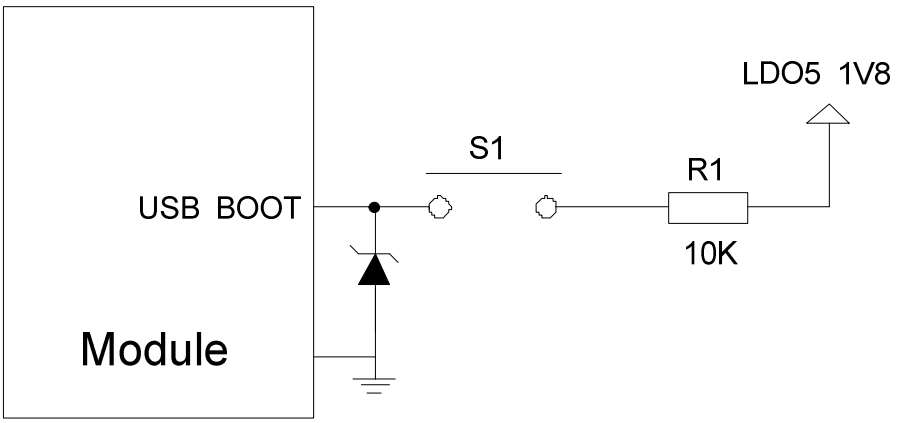


Figure 28: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SC200R series module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth (BT) functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna, and ceramic antenna to the module via the interface to achieve Wi-Fi and BT functions.

4.1. Wi-Fi Overview

SC200R series module supports 2.4/5 GHz dual-band WLAN based on IEEE 802.11a/b/g/n standard protocols. The maximum data rate is up to 150 Mbps. The features are as below:

- Supports Wake-on-WLAN (WoWLAN)
- Supports ad hoc mode
- Supports WAPI SMS4 hardware encryption
- Supports AP mode
- Supports Wi-Fi Direct
- Supports MCS 0-7 for HT20 and HT40

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 28: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	16 dBm ±2.5 dB
	802.11b	11 Mbps	16 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB
	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB

	802.11n HT40	MCS0	14 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	15 dBm ±2.5 dB
	802.11a	54 Mbps	13 dBm ±2.5 dB
	802.11n HT20	MCS0	14 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
	802.11n HT40	MCS0	14 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB

Table 29: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-96
	802.11b	11 Mbps	-87
	802.11g	6 Mbps	-90
	802.11g	54 Mbps	-73
	802.11n HT20	MCS0	-89
	802.11n HT20	MCS7	-71
	802.11n HT40	MCS0	-89
	802.11n HT40	MCS7	-69
5 GHz	802.11a	6 Mbps	-90
	802.11a	54 Mbps	-72
	802.11n HT20	MCS0	-88
	802.11n HT20	MCS7	-69
	802.11n HT40	MCS0	-86
	802.11n HT40	MCS7	-66

Reference specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11a, IEEE Std 802.11b, IEEE Std 802.11g: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.2. BT Overview

SC200R series module supports BT 4.2 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally supports up to 7 wireless connections.
- Maximally supports up to 3.5 piconets at the same time.
- Support one SCO (Synchronous Connection Oriented) or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 30: BT Data Rate and Version

Version	Data Rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0 + EDR	3 Mbit/s	> 80 kbit/s
3.0 + HS	24 Mbit/s	Reference 3.0 + HS
4.0	24 Mbit/s	Reference 4.0 LE

Reference specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009

4.2.1. BT Performance

The following table lists the BT transmitting and receiving performance of SC200R series module.

Table 31: BT Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	10.0	10.0	9.9
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-91	-90	-90

5 GNSS

SC200R series module integrates a Qualcomm IZat™ GNSS engine (GEN 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, Galileo and BeiDou. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.1. GNSS Performance

The following table lists the GNSS performance of the module in conduction mode.

Table 32: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Cold start	-146	dBm
	Reacquisition	-158	dBm
	Tracking	-158	dBm
TTFF	Cold start	30.8	s
	Warm start	21	s
	Hot start	3.3	s
Static Drift	CEP-50	< 2.5	m

NOTE

SC200R-WF does not support GNSS.

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid this, follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, place GNSS RF signal lines and RF components far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protective diodes for the antenna interface. The junction capacitance of the diodes should be less than 0.5 pF. Otherwise, it will influence the impedance characteristic of RF circuit loop, or cause attenuation of bypass RF signals.
- Control the impedance of feeder lines and PCB traces to 50 Ω, and keep the trace as short as possible.
- See ***Chapter 6.3*** for reference circuit designs of GNSS antenna.

6 Antenna Interfaces

SC200R series module provides four antenna interfaces for the main antenna, Rx-diversity antenna, Wi-Fi/BT antenna and GNSS antenna respectively. The antenna ports have an impedance of 50 Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 33: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	AI/AO	Main antenna interface	50 Ω impedance
ANT_DRX	131	AI	Rx-diversity antenna interface	

The operating frequencies of SC200R series modules are listed in the following tables.

Table 34: SC200R-CE Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925–960	880–915	MHz
DCS1800	1805–1880	1710–1785	MHz
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B8	925–960	880–915	MHz
EVDO/CDMA BC0	869–894	824–849	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz

LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B8	925–960	880–915	MHz
LTE-TDD B34	2010 – 2025	2010 – 2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2555–2655	2555–2655	MHz

Table 35: SC200R-EM* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869–894	824–849	MHz
EGSM900	925–960	880–915	MHz
DCS1800	1805–1880	1710–1785	MHz
PCS1900	1930–1990	1850–1910	MHz
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B2	1930–1990	1850–1910	MHz
WCDMA B4	2110 – 2155	1710 – 1755	MHz
WCDMA B5	869–894	824–849	MHz
WCDMA B8	925–960	880–915	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B2	1930–1990	1850–1910	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz
LTE-FDD B4	2110 – 2155	1710 – 1755	MHz
LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz

LTE-FDD B8	925–960	880–915	MHz
LTE-FDD B20	791–821	832–862	MHz
LTE-FDD B28(A + B)	758–803	703–748	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2555–2655	2555–2655	MHz

Table 36: SC200R-NA Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B2	1930–1990	1850–1910	MHz
WCDMA B4	2110 – 2155	1710 – 1755	MHz
WCDMA B5	869–894	824–849	MHz
LTE-FDD B2	1930–1990	1850–1910	MHz
LTE-FDD B4	2110 – 2155	1710 – 1755	MHz
LTE-FDD B5	869 – 894	824 – 849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz
LTE-FDD B12	729 – 746	699 – 716	MHz
LTE-FDD B13	746 – 756	777 – 787	MHz
LTE-FDD B14	758 – 768	788 – 798	MHz
LTE-FDD B17	734 – 746	704 – 716	MHz
LTE-FDD B25	1930 – 1995	1850 – 1915	MHz
LTE-FDD B26	859 – 894	814 – 849	MHz
LTE-FDD B66	2100 – 2200	1710 – 1780	MHz
LTE-FDD B71	663 – 698	617 – 652	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 37: SC200R-JP* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B1	2110–2170	1920–1980	MHz
WCDMA B6	875–885	830–840	MHz
WCDMA B8	925–960	880–915	MHz
WCDAM B19	875–890	830–845	MHz
LTE-FDD B1	2110–2170	1920–1980	MHz
LTE-FDD B3	1805–1880	1710–1785	MHz
LTE-FDD B5	869 – 894	824 – 849	MHz
LTE-FDD B8	925–960	880–915	MHz
LTE-FDD B11	1428–1447	1475–1495	MHz
LTE-FDD B18	860–875	815–830	MHz
LTE-FDD B19	875–890	830–845	MHz
LTE-FDD B21	1496~1511	1448~1463	MHz
LTE-FDD B26	859–894	814–849	MHz
LTE-FDD B28	758–803	703–748	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

NOTE

"*" means under development.

6.1.1. Reference Design for Main and Rx-diversity Antenna Interfaces

A reference circuit design for main and Rx-diversity antenna interfaces is shown below. Reserve a π-type matching circuit for each antenna to achieve better RF performance, and place the π-type matching components (R1/C1/C2, R2/C3/C4) as close to the antennas as possible. The capacitors are not mounted by default and the resistors are 0 Ω.

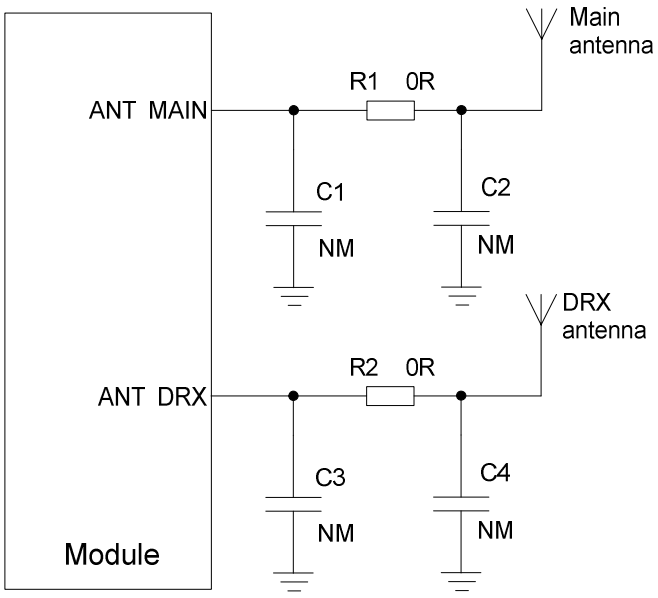


Figure 29: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.2. Wi-Fi/BT Antenna Interface

The following tables show the pin definition and frequency specification of the Wi-Fi/BT antenna interface.

Table 38: Pin Definition of Wi-Fi/BT Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	AI/AO	Wi-Fi/BT antenna interface	50 Ω impedance

Table 39: Wi-Fi/BT Frequency

Type	Frequency	Unit
Wi-Fi (2.4 GHz)	2402–2482	MHz
Wi-Fi (5 GHz)	5180–5825	MHz
BT 4.2 LE	2402–2480	MHz

A reference circuit design for Wi-Fi/BT antenna interface is shown as below. C1 and C2 are not mounted by default and the resistor is 0 Ω.

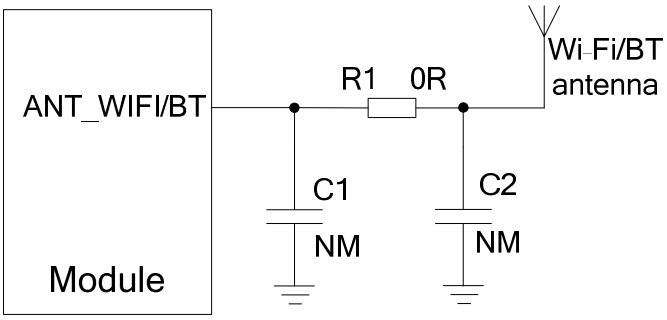


Figure 30: Reference Circuit Design for Wi-Fi/BT Antenna

6.3. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 40: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	121	AI	GNSS antenna interface	50 Ω impedance

Table 41: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
BeiDou	1561.098 ±2.046	MHz
Galileo	1575.42 ±1.023	MHz

NOTE

SC200R-WF does not support GNSS.

6.3.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

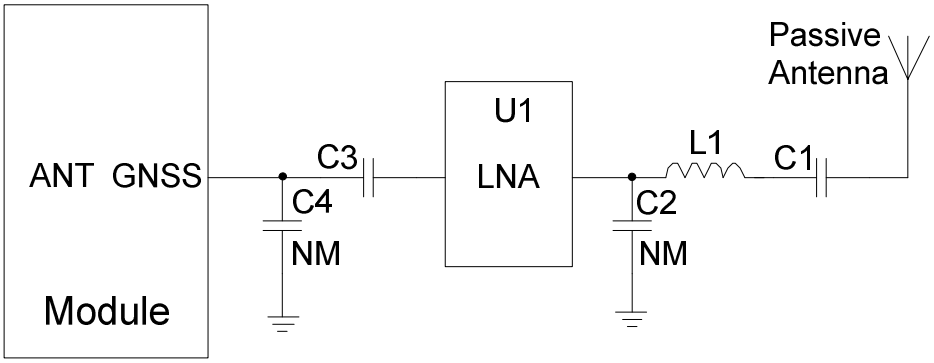


Figure 31: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long) and the external loss is more than 2 dB, it is recommended to add an external LNA circuit for better GNSS receiving performance, and place the LNA close to the antenna.

6.3.2. Recommended Circuit for Active Antenna

The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Despite its low power consumption, the active antenna still requires stable and clean power supplies. Therefore, it is recommended to use high-performance LDO as the power supply. A reference design for GNSS active antenna is shown below.

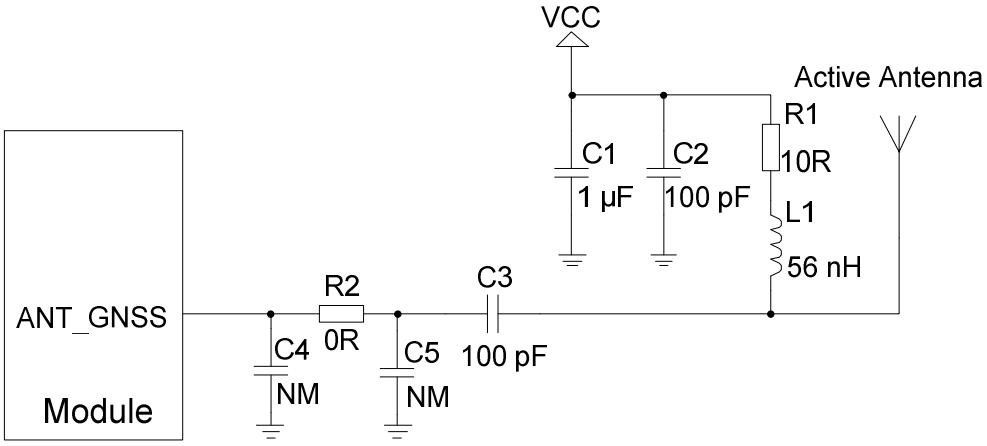


Figure 32: Reference Circuit Design for GNSS Active Antenna

6.4. Reference Design for RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

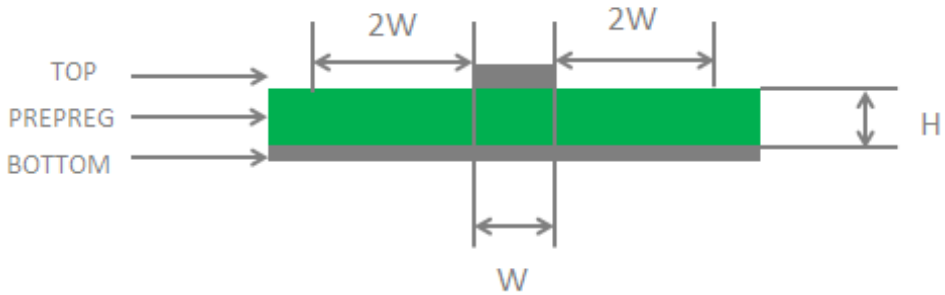


Figure 33: Microstrip Design on a 2-layer PCB

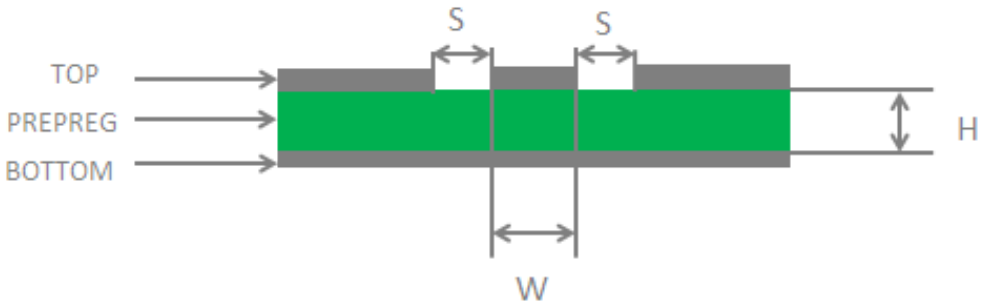


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

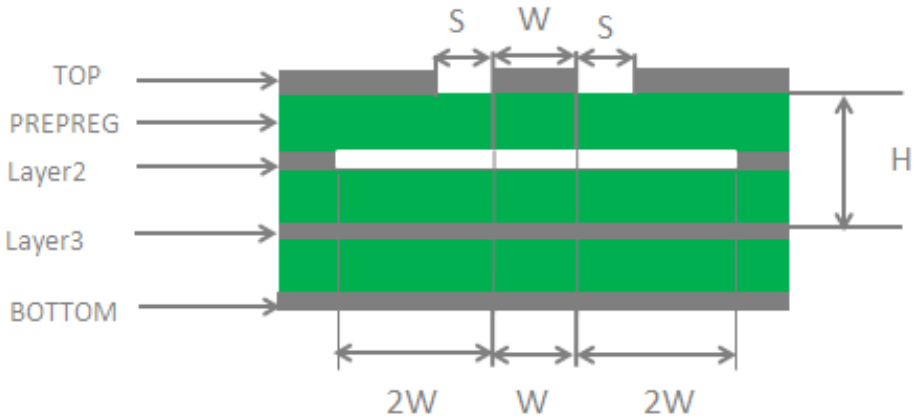


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

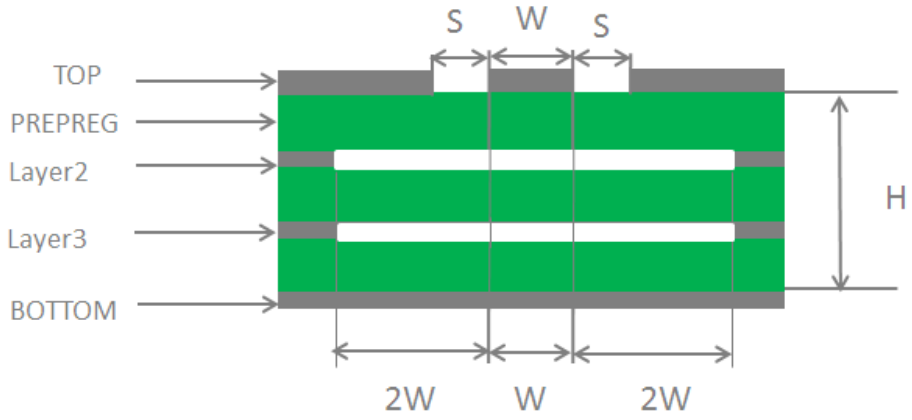


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- Design the GND pins adjacent to RF pins as thermal relief pads, and fully connect them to ground.
- Keep the distance between the RF pins and the RF connector as short as possible. Change all the right-angle traces to curved ones and the recommended trace angle is 135°.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- Keep the reference ground of RF traces complete. Meanwhile, add some ground vias around RF traces and the reference ground to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

6.5. Antenna Installation

6.5.1. Antenna Requirements

The following table shows the requirement on the main antenna, Rx-diversity antenna, Wi-Fi/BT antenna and GNSS antenna.

Table 42: Antenna Requirements

Type	Requirements
GSM/WCDMA/LTE	VSWR: ≤ 2 Gain: 1 dBi Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Cable Insertion Loss: < 1 dB (GSM850, EGSM900, WCDMA B5/B6/B8/B19, EVDO/CDMA BC0, LTE B5/B8/B12/B13/B14/B17/B18/B19/B20/B26/B28A/B28B/B71) Cable Insertion Loss: < 1.5 dB (DCS1800, PCS1900, WCDMA B1/B2/B4, LTE B1/B2/B3/B4/B11/B21/B25/B34/B39/B66) Cable Insertion Loss: < 2 dB (LTE-FDD B7, LTE-TDD B38/B40/B41)
Wi-Fi/BT	VSWR: ≤ 2 Gain: 1 dBi

	Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Cable Insertion Loss: < 1 dB
GNSS[1)]	Frequency range: 1559 MHz–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0 dBi Active Antenna Noise Figure: < 1.5 dB (Typ.) Active Antenna Gain: > -2 dBi Active Antenna Embedded LNA Gain: < 17 dB (Typ.) Active Antenna Total Gain: < 17 dBi (Typ.)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.5.2. Recommended RF Connector for Antenna Installation

If you use an RF connector for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

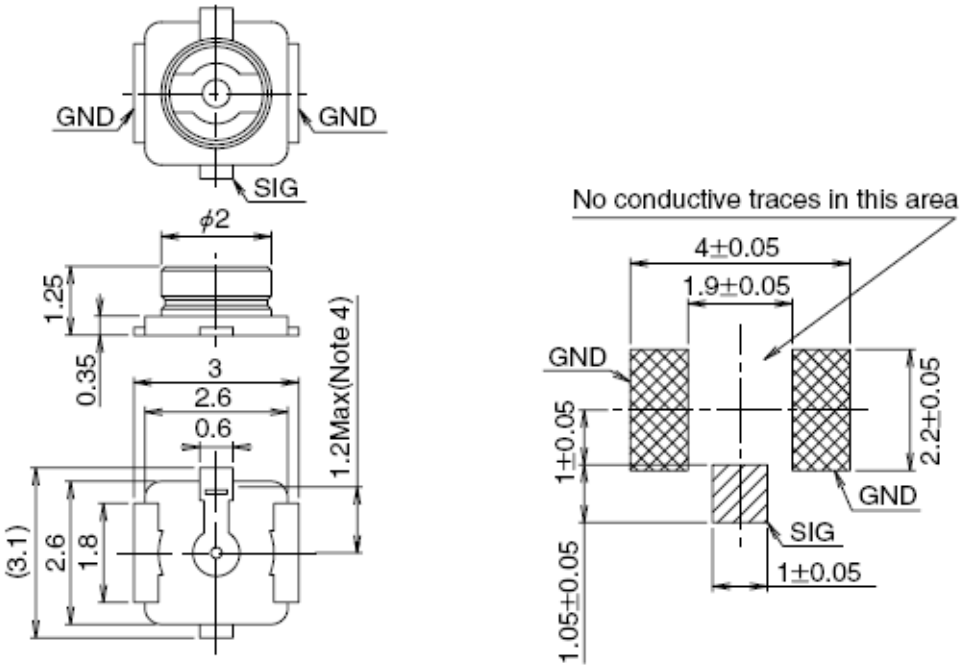


Figure 37: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

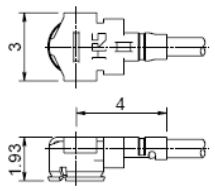
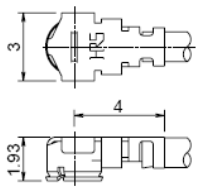
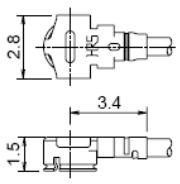
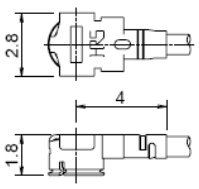
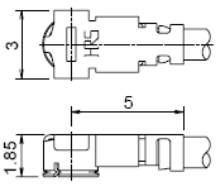
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connectors.

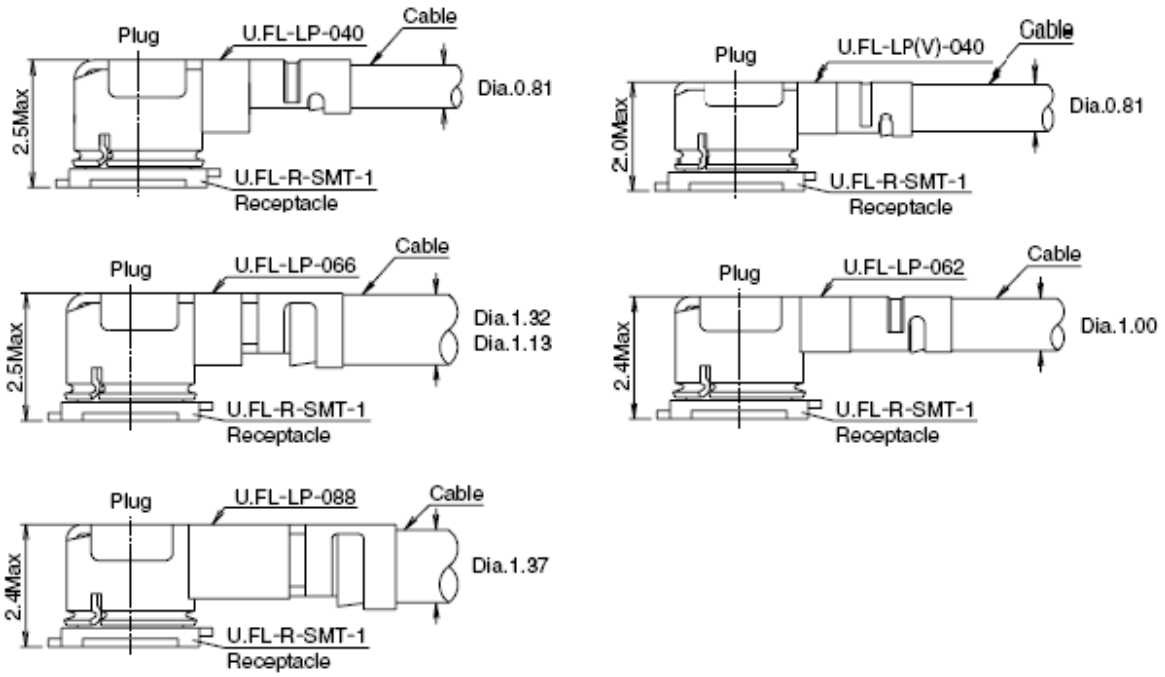


Figure 39: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

7 Electrical, Reliability and Radio Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 43: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.5	16	V
Peak Current of VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.16	V

7.2. Power Supply Ratings

Table 44: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values	3.55	3.8	4.2	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900			400	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900		1.8	3.0	A
USB_VBUS	USB power supply		4.35	5.0	6.2	V
VRTC	Power supply voltage of the backup battery		2.0	3.0	3.25	V

7.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 45: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range[1)]	-35	+25	+75	ºC
Storage Temperature Range	-40		+90	ºC

NOTE

[1)] Within the operating temperature range, the module is 3GPP compliant.

7.4. Current Consumption

The values of current consumption are shown below.

Table 46: SC200R-CE Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	13	μA
	GSM/GPRS supply current	Sleep (USB disconnected) @ DRX = 2	5.26	mA
		Sleep (USB disconnected) @ DRX = 5	4.82	mA
		Sleep (USB disconnected) @ DRX = 9	4.55	mA
	WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	4.60	mA
		Sleep (USB disconnected) @ DRX = 7	4.55	mA
		Sleep (USB disconnected) @ DRX = 8	3.70	mA
		Sleep (USB disconnected) @ DRX = 9	3.60	mA
	CDMA supply current	BC0 CH283 @ Slot Cycle Index = 1	4.80	mA
		BC0 CH283 @ Slot Cycle Index = 7	5.80	mA
	LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 5	7.03	mA
		Sleep (USB disconnected) @ DRX = 6	4.95	mA
		Sleep (USB disconnected) @ DRX = 7	4.20	mA
		Sleep (USB disconnected) @ DRX = 9	3.90	mA
	LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 5	6.78	mA
		Sleep (USB disconnected) @ DRX = 6	5.11	mA
		Sleep (USB disconnected) @ DRX = 7	4.34	mA
		Sleep (USB disconnected) @ DRX = 9	3.93	mA
	GSM voice call	EGSM900 @ PCL 5	255.7	mA
		EGSM900 @ PCL 12	113.9	mA

		EGSM900 @ PCL 19	98.68	mA
		DCS1800 @ PCL 0	185.8	mA
		DCS1800 @ PCL 7	103.2	mA
		DCS1800 @ PCL 15	97.06	mA
	WCDMA voice call	B1 @ max power	534.1	mA
		B8 @ max power	529.6	mA
	GPRS data transfer	EGSM900 (1UL/4DL) @ PCL 5	246.2	mA
		EGSM900 (2UL/3DL) @ PCL 5	394.1	mA
		EGSM900 (3UL/2DL) @ PCL 5	487.9	mA
		EGSM900 (4UL/1DL) @ PCL 5	576.6	mA
		DCS1800 (1UL/4DL) @ PCL 0	170.8	mA
		DCS1800 (2UL/3DL) @ PCL 0	266.2	mA
		DCS1800 (3UL/2DL) @ PCL0	368.4	mA
		DCS1800 (4UL/1DL) @ PCL 0	442.5	mA
	EDGE data transfer	EGSM900 (1UL/4DL) @ PCL 8	188.3	mA
		EGSM900 (2UL/3DL) @ PCL 8	321.6	mA
		EGSM900 (3UL/2DL) @ PCL 8	441.3	mA
		EGSM900 (4UL/1DL) @ PCL 8	562.5	mA
		DCS1800 (1UL/4DL) @ PCL 2	163.2	mA
		DCS1800 (2UL/3DL) @ PCL 2	274.4	mA
		DCS1800 (3UL/2DL) @ PCL 2	386.4	mA
		DCS1800 (4UL/1DL) @ PCL 2	496.5	mA
	WCDMA data transfer	B1 (HSDPA) @ max power	476.4	mA
		B8 (HSDPA) @ max power	461.5	mA
		B1 (HSUPA) @ max power	505.4	mA

		B8 (HSUPA) @ max power	493.5	mA
	EVDO/CDMA data transfer	BC0 @ max power	495.0	mA
	LTE data transfer	LTE-FDD B1 @ max power	709.5	mA
		LTE-FDD B3 @ max power	677.4	mA
		LTE-FDD B5 @ max power	559.2	mA
		LTE-FDD B8 @ max power	631.9	mA
		LTE-TDD B34 @ max power	374.3	mA
		LTE-TDD B38 @ max power	412.6	mA
		LTE-TDD B39 @ max power	379.9	mA
		LTE-TDD B40 @ max power	411.3	mA
		LTE-TDD B41 @ max power	413.5	mA

Table 47: SC200R-EM* Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	μA
	GSM/GPRS supply current	Sleep (USB disconnected) @ DRX = 2	TBD	mA
		Sleep (USB disconnected) @ DRX = 5	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
		Sleep (USB disconnected) @ DRX = 8	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
		Sleep (USB disconnected) @ DRX = 8	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	LTE-TDD	Sleep (USB disconnected) @ DRX = 6	TBD	mA

	supply current	Sleep (USB disconnected) @ DRX = 8	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	GSM voice call	GSM850 @ PCL 5	TBD	mA
		GSM850 @ PCL 12	TBD	mA
		GSM850 @ PCL 19	TBD	mA
		EGSM900 @ PCL 5	TBD	mA
		EGSM900 @ PCL 12	TBD	mA
		EGSM900 @ PCL 19	TBD	mA
		DCS1800 @ PCL 0	TBD	mA
		DCS1800 @ PCL 7	TBD	mA
		DCS1800 @ PCL 15	TBD	mA
		PCS1900 @ PCL 0	TBD	mA
		PCS1900 @ PCL 7	TBD	mA
		PCS1900 @ PCL 15	TBD	mA
	WCDMA voice call	B1 @ max power	TBD	mA
		B2 @ max power	TBD	mA
		B4 @ max power	TBD	mA
		B5 @ max power	TBD	mA
		B8 @ max power	TBD	mA
	GPRS data transfer	GSM850(1UL/4DL) @ PCL 5	TBD	mA
		GSM850 (2UL/3DL) @ PCL 5	TBD	mA
		GSM850 (3UL/2DL) @ PCL 5	TBD	mA
		GSM850 (4UL/1DL) @ PCL 5	TBD	mA
		EGSM900 (1UL/4DL) @ PCL 5	TBD	mA
		EGSM900 (2UL/3DL) @ PCL 5	TBD	mA

	EGSM900 (3UL/2DL) @ PCL 5	TBD	mA
	EGSM900 (4UL/1DL) @ PCL 5	TBD	mA
	DCS1800 (1UL/4DL) @ PCL 0	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 0	TBD	mA
	DCS1800 (3UL/2DL) @ PCL0	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 0	TBD	mA
	PCS1900 (1UL/4DL) @ PCL 0	TBD	mA
	PCS1900 (2UL/3DL) @ PCL 0	TBD	mA
	PCS1900 (3UL/2DL) @ PCL0	TBD	mA
	PCS1900 (4UL/1DL) @ PCL 0	TBD	mA
	GSM850(1UL/4DL) @ PCL 8	TBD	mA
	GSM850 (2UL/3DL) @ PCL 8	TBD	mA
	GSM850 (3UL/2DL) @ PCL 8	TBD	mA
	GSM850 (4UL/1DL) @ PCL 8	TBD	mA
	EGSM900 (1UL/4DL) @ PCL 8	TBD	mA
	EGSM900 (2UL/3DL) @ PCL 8	TBD	mA
	EGSM900 (3UL/2DL) @ PCL 8	TBD	mA
EDGE data transfer	DCS1800 (1UL/4DL) @ PCL 2	TBD	mA
	DCS1800 (2UL/3DL) @ PCL 2	TBD	mA
	DCS1800 (3UL/2DL) @ PCL 2	TBD	mA
	DCS1800 (4UL/1DL) @ PCL 2	TBD	mA
	PCS1900 (1UL/4DL) @ PCL 2	TBD	mA
	PCS1900 (2UL/3DL) @ PCL 2	TBD	mA
	PCS1900 (3UL/2DL) @ PCL 2	TBD	mA
	PCS1900 (4UL/1DL) @ PCL 2	TBD	mA

	WCDMA data transfer	B1 (HSDPA) @ max power	TBD	mA
		B2 (HSDPA) @ max power	TBD	mA
		B4 (HSDPA) @ max power	TBD	mA
		B5 (HSDPA) @ max power	TBD	mA
		B8 (HSDPA) @ max power	TBD	mA
		B1 (HSUPA) @ max power	TBD	mA
		B2 (HSUPA) @ max power	TBD	mA
		B4 (HSUPA) @ max power	TBD	mA
		B5 (HSUPA) @ max power	TBD	mA
		B8 (HSUPA) @ max power	TBD	mA
	LTE data transfer	LTE-FDD B1 @ max power	TBD	mA
		LTE-FDD B2 @ max power	TBD	mA
		LTE-FDD B3 @ max power	TBD	mA
		LTE-FDD B4 @ max power	TBD	mA
		LTE-FDD B5 @ max power	TBD	mA
		LTE-FDD B7 @ max power	TBD	mA
		LTE-FDD B8 @ max power	TBD	mA
		LTE-FDD B20 @ max power	TBD	mA
		LTE-FDD B28 @ max power	TBD	mA
		LTE-TDD B38 @ max power	TBD	mA
		LTE-TDD B40 @ max power	TBD	mA
		LTE-TDD B41 @ max power	TBD	mA

Table 48: SC200R-NA Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	13	μA
	WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	3.922	mA
		Sleep (USB disconnected) @ DRX = 8	3.041	mA
		Sleep (USB disconnected) @ DRX = 9	2.795	mA
	LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 6	6.748	mA
		Sleep (USB disconnected) @ DRX = 8	3.689	mA
		Sleep (USB disconnected) @ DRX = 9	3.133	mA
	LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 6	6.935	mA
		Sleep (USB disconnected) @ DRX = 8	3.788	mA
		Sleep (USB disconnected) @ DRX = 9	3.145	mA
	WCDMA voice call	B2 @ max power	643.7	mA
		B4 @ max power	554.5	mA
		B5 @ max power	475.5	mA
	WCDMA data transfer	B2 (HSDPA) @ max power	592.1	mA
		B4 (HSDPA) @ max power	554.9	mA
		B5 (HSDPA) @ max power	445.0	mA
		B2 (HSUPA) @ max power	522.7	mA
		B4 (HSUPA) @ max power	526.9	mA
		B5 (HSUPA) @ max power	444.5	mA
	LTE data transfer	LTE-FDD B2 @ max power	791	mA
		LTE-FDD B4 @ max power	761	mA
		LTE-FDD B5 @ max power	590	mA
		LTE-FDD B7 @ max power	861	mA

		LTE-FDD B12 @ max power	636	mA
		LTE-FDD B13 @ max power	650	mA
		LTE-FDD B14 @ max power	648	mA
		LTE-FDD B17@ max power	617	mA
		LTE-FDD B25 @ max power	812	mA
		LTE-FDD B26 @ max power	672	mA
		LTE-FDD B66 @ max power	782	mA
		LTE-FDD B71 @ max power	803	mA
		LTE-TDD B41 @ max power	491	mA

Table 49: SC200R-JP* Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	μA
	WCDMA supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
		Sleep (USB disconnected) @ DRX = 8	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
		Sleep (USB disconnected) @ DRX = 8	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	LTE-TDD supply current	Sleep (USB disconnected) @ DRX = 6	TBD	mA
		Sleep (USB disconnected) @ DRX = 8	TBD	mA
		Sleep (USB disconnected) @ DRX = 9	TBD	mA
	WCDMA voice call	B1 @ max power	TBD	mA
		B6 @ max power	TBD	mA
		B8 @ max power	TBD	mA

		B19 @ max power	TBD	mA
	WCDMA data transfer	B1 (HSDPA) @ max power	TBD	mA
		B6 (HSDPA) @ max power	TBD	mA
		B8 (HSDPA) @ max power	TBD	mA
		B19 (HSDPA) @ max power	TBD	mA
		B1 (HSUPA) @ max power	TBD	mA
		B6 (HSUPA) @ max power	TBD	mA
		B8 (HSUPA) @ max power	TBD	mA
		B19 (HSUPA) @ max power	TBD	mA
	LTE data transfer	LTE-FDD B1 @ max power	TBD	mA
		LTE-FDD B3 @ max power	TBD	mA
		LTE-FDD B5 @ max power	TBD	mA
		LTE-FDD B8 @ max power	TBD	mA
		LTE-FDD B11 @ max power	TBD	mA
		LTE-FDD B18 @ max power	TBD	mA
		LTE-FDD B19 @ max power	TBD	mA
		LTE-FDD B21 @ max power	TBD	mA
		LTE-FDD B26 @ max power	TBD	mA
		LTE-FDD B28 @ max power	TBD	mA
		LTE-TDD B41 @ max power	TBD	mA

NOTE

"*" means under development.

7.5. RF Output Power

The following tables show the RF output power of SC200R series modules.

Table 50: SC200R-CE RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
WCDMA B1	24 dBm +1/-3 dB	< -49 dBm
WCDMA B8	24 dBm +1/-3 dB	< -49 dBm
EVDO/CDMA BC0	24 dBm +3/-1 dB	< -49 dBm
LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38	23 dBm ±2 dB	< -39 dBm
LTE-TDD B39	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

Table 51: SC200R-EM* RF Output Power

Frequency	Max.	Min.
GSM850	TBD	TBD
EGSM900	TBD	TBD
DCS1800	TBD	TBD

PCS1900	TBD	TBD
WCDMA B1	TBD	TBD
WCDMA B2	TBD	TBD
WCDMA B4	TBD	TBD
WCDMA B5	TBD	TBD
WCDMA B8	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B2	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B4	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B7	TBD	TBD
LTE-FDD B8	TBD	TBD
LTE-FDD B20	TBD	TBD
LTE-FDD B28	TBD	TBD
LTE-TDD B38	TBD	TBD
LTE-TDD B40	TBD	TBD
LTE-TDD B41	TBD	TBD

Table 52: SC200R-NA RF Output Power

Frequency	Max.	Min.
WCDMA B2	24 dBm +1/-3 dB	< -49 dBm
WCDMA B4	24 dBm +1/-3 dB	< -49 dBm
WCDMA B5	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B2	23 dBm ±2 dB	< -39 dBm

LTE-FDD B4	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B12	23 dBm ±2 dB	< -39 dBm
LTE-FDD B13	23 dBm ±2 dB	< -39 dBm
LTE-FDD B14	23 dBm ±2 dB	< -39 dBm
LTE-FDD B17	23 dBm ±2 dB	< -39 dBm
LTE-FDD B25	23 dBm ±2 dB	< -39 dBm
LTE-FDD B26	23 dBm ±2 dB	< -39 dBm
LTE-FDD B66	23 dBm ±2 dB	< -39 dBm
LTE-FDD B71	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

Table 53: SC200R-JP* RF Output Power

Frequency	Max.	Min.
WCDMA B1	TBD	TBD
WCDMA B6	TBD	TBD
WCDMA B8	TBD	TBD
WCDMA B19	TBD	TBD
LTE-FDD B1	TBD	TBD
LTE-FDD B3	TBD	TBD
LTE-FDD B5	TBD	TBD
LTE-FDD B8	TBD	TBD
LTE-FDD B11	TBD	TBD
LTE-FDD B18	TBD	TBD

LTE-FDD B19	TBD	TBD
LTE-FDD B21	TBD	TBD
LTE-FDD B26	TBD	TBD
LTE-FDD B28	TBD	TBD
LTE-TDD B41	TBD	TBD

NOTES

1. In GPRS 4-slot Tx mode, the maximum output power is reduced by 3 dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. "*" means under development.

7.6. RF Receiving Sensitivity

The following table shows the RF receiving sensitivity of SC200R series modules.

Table 54: SC200R-CE RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109.5	/	/	-102.4 dBm
DCS1800	-109.6	/	/	-102.4 dBm
WCDMA B1	-109.5	-110.5	TBD	-106.7 dBm
WCDMA B8	-110.5	-110.5	TBD	-103.7 dBm
EVDO/CDMA BC0	-109.5	/	/	-104 dBm
LTE-FDD B1 (10 MHz)	-98.1	-97.6	-100.2	-96.3 dBm
LTE-FDD B3 (10 MHz)	-97.9	-97.3	-99.2	-93.3 dBm
LTE-FDD B5 (10 MHz)	-100.1	-99.6	-102.8	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.3	-98.1	-102.3	-93.3 dBm

LTE-TDD B34 (10 MHz)	-98.4	-98.3	-101.5	-96.3 dBm
LTE-TDD B38 (10 MHz)	-98.8	-98.7	-101.8	-96.3 dBm
LTE-TDD B39 (10 MHz)	-98.5	-98	-101.3	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.9	-99	-102.4	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98.2	-97.9	-101.3	-94.3 dBm

Table 55: SC200R-EM* RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	TBD	/	/	-102.4 dBm
EGSM900	TBD	/	/	-102.4 dBm
DCS1800	TBD	/	/	-102.4 dBm
PCS1900	TBD	/	/	-102.4 dBm
WCDMA B1	TBD	TBD	TBD	-106.7 dBm
WCDMA B2	TBD	TBD	TBD	-104.7 dBm
WCDMA B4	TBD	TBD	TBD	-106.7 dBm
WCDMA B5	TBD	TBD	TBD	-104.7 dBm
WCDMA B8	TBD	TBD	TBD	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm

LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8 dBm
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3 dBm

Table 56: SC200R-NA RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-109.5	-110	-110.5	-104.7 dBm
WCDMA B4	-110.5	-110.5	-111	-106.7 dBm
WCDMA B5	-111	-111.5	-112	-104.7 dBm
LTE-FDD B2 (10 MHz)	-97.4	-98.2	-99.6	-94.3 dBm
LTE-FDD B4 (10 MHz)	-98	-98.2	-100.5	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99	-100.6	-102.7	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.8	-97.4	-99.7	-93.3 dBm
LTE-FDD B12 (10 MHz)	-96.4	-96.8	-100.2	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.1	-96.4	-101.1	-93.3 dBm
LTE-FDD B14 (10 MHz)	-98.2	-96.3	-100.3	-93.3 dBm
LTE-FDD B17 (10 MHz)	-96.5	-96.7	-100.1	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.2	-98.2	-99.5	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.3	-100.6	-102.4	-93.8 dBm
LTE-FDD B66 (10 MHz)	-98.3	-98.7	-100.7	-96.3 dBm
LTE-FDD B71 (10 MHz)	-96.3	-97.3	-99.8	-93.5 dBm
LTE-TDD B41 (10 MHz)	-97.9	-97.9	-100.1	-94.3 dBm

Table 57: SC200R-JP* RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	TBD	TBD	TBD	-102.4 dBm
WCDMA B6	TBD	TBD	TBD	-102.4 dBm
WCDMA B8	TBD	TBD	TBD	-106.7 dBm
WCDAM B19	TBD	TBD	TBD	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B11 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B21 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8 dBm
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8 dBm
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3 dBm

NOTE

"*" means under development.

7.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SC200R series module.

Table 58: ESD Characteristics (Temperature: 25 ºC, Humidity: 45 %)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	kV
All Antenna Interfaces	+/-5	+/-10	kV
Other Interfaces	+/-0.5	+/-1	kV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the tolerances for dimensions without tolerance values are ±0.05 mm.

8.1. Mechanical Dimensions of the Module

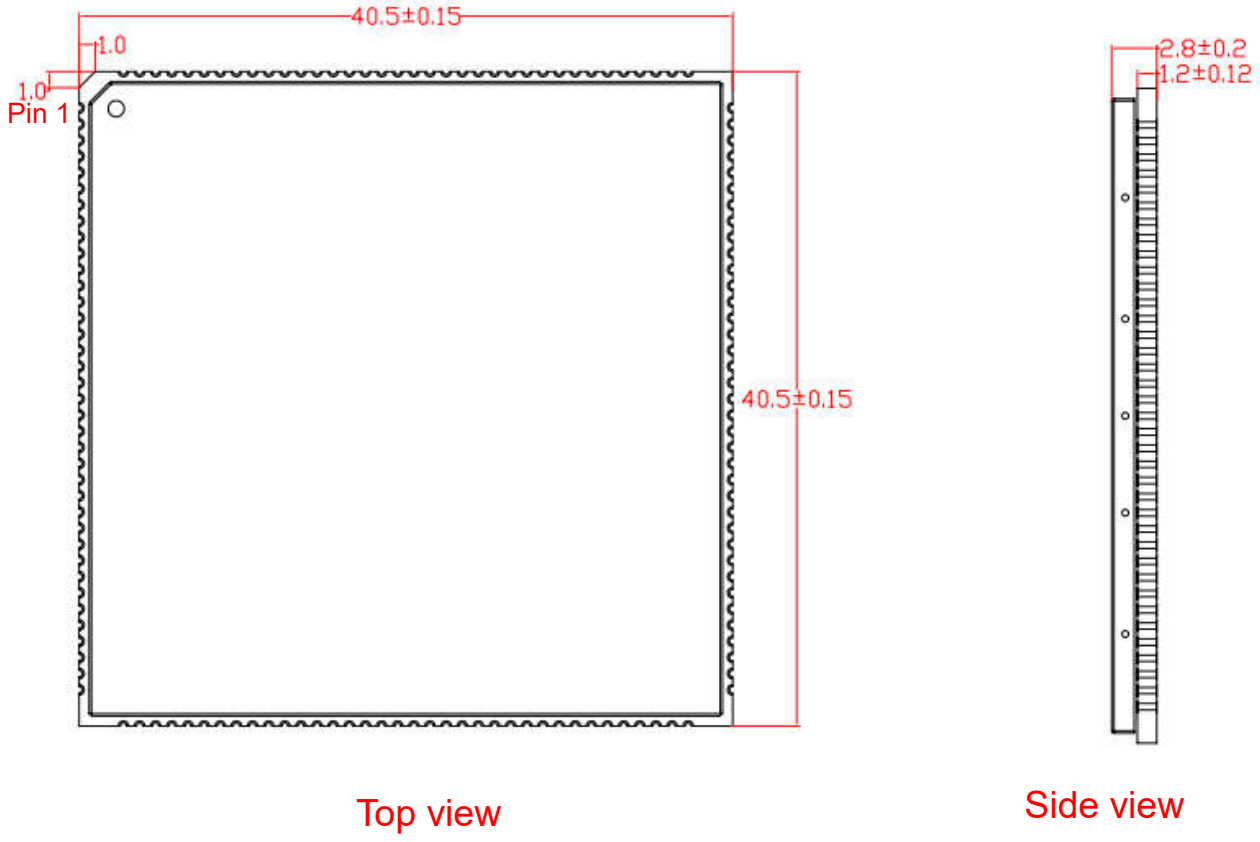


Figure 40: Top and Side Dimensions

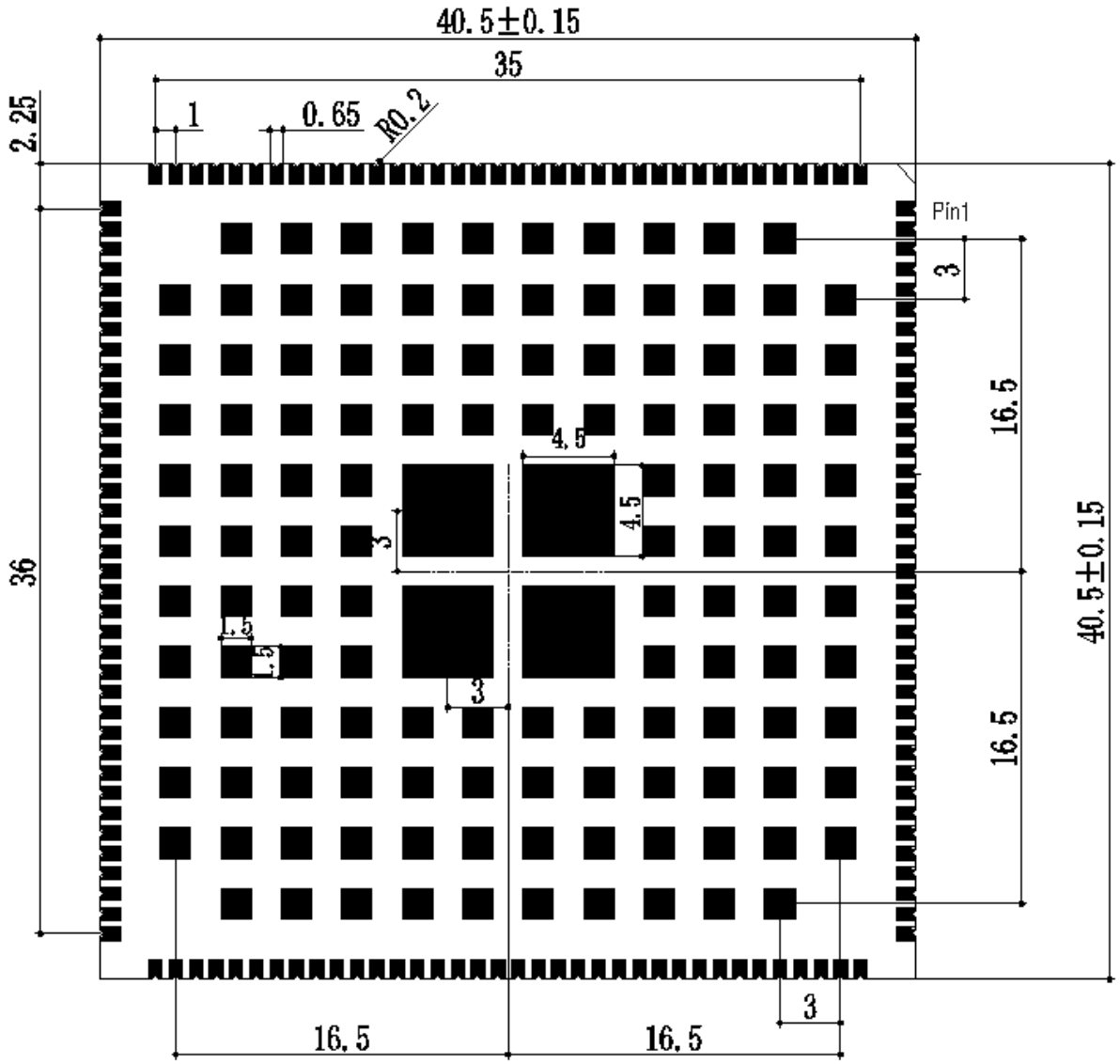


Figure 41: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

8.2. Recommended Footprint

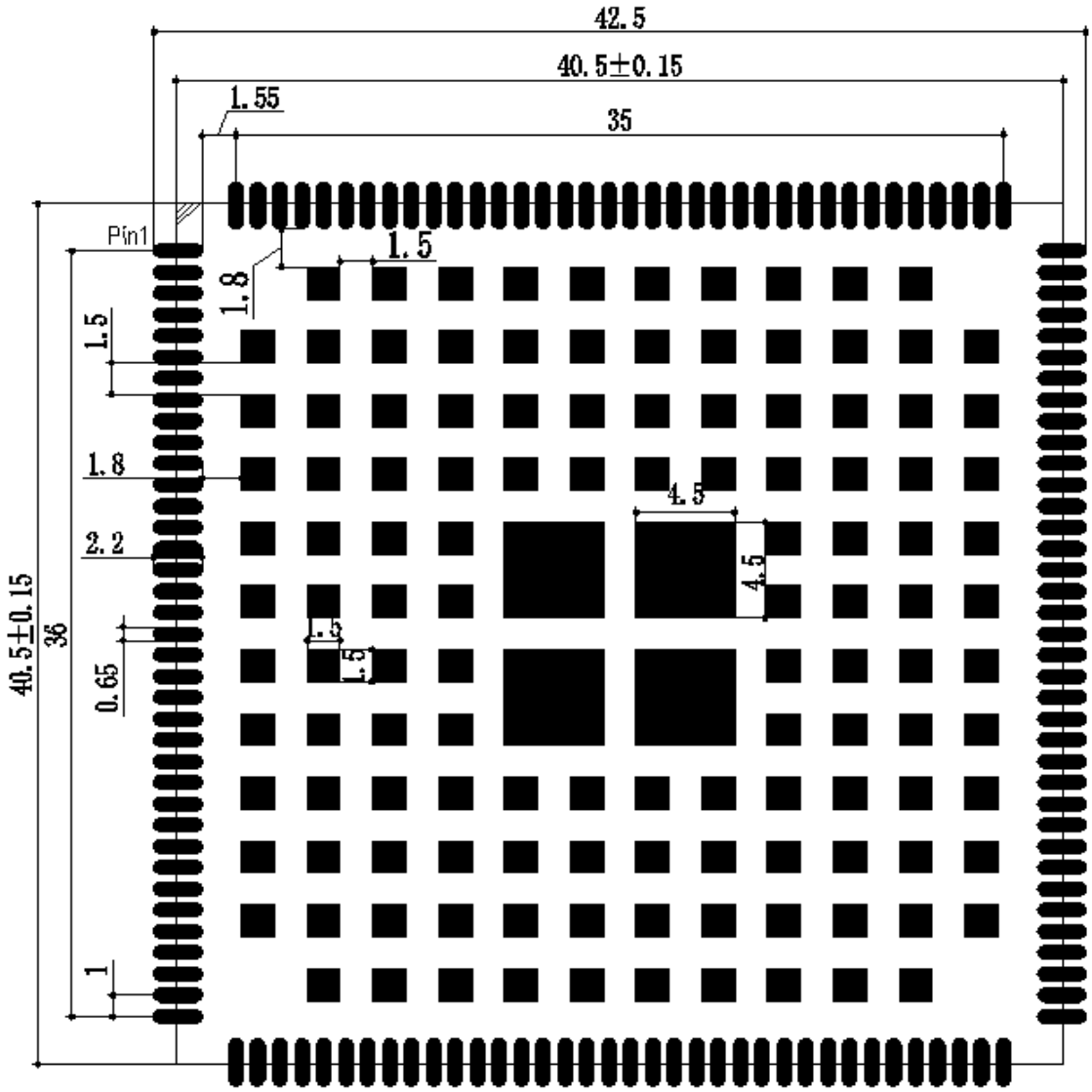


Figure 42: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep at least 5 mm between the module and other components on the host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom Views of the Module

Figure 43: Top View of the Module

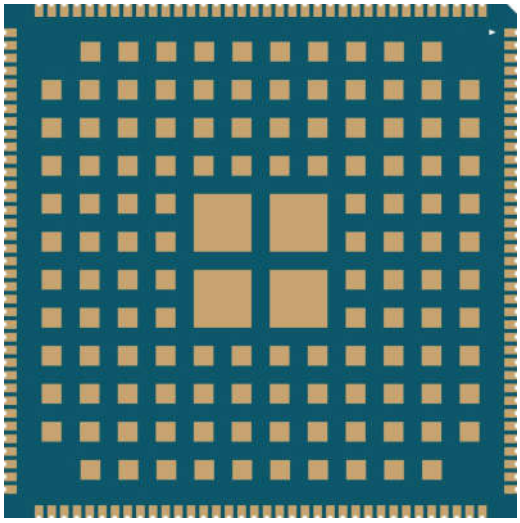


Figure 44: Bottom View of the Module

NOTE

These are renderings of SC200R series module. For authentic dimension and appearance, refer to the module that you receive from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35 %–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, It is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for baking procedure.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [4]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

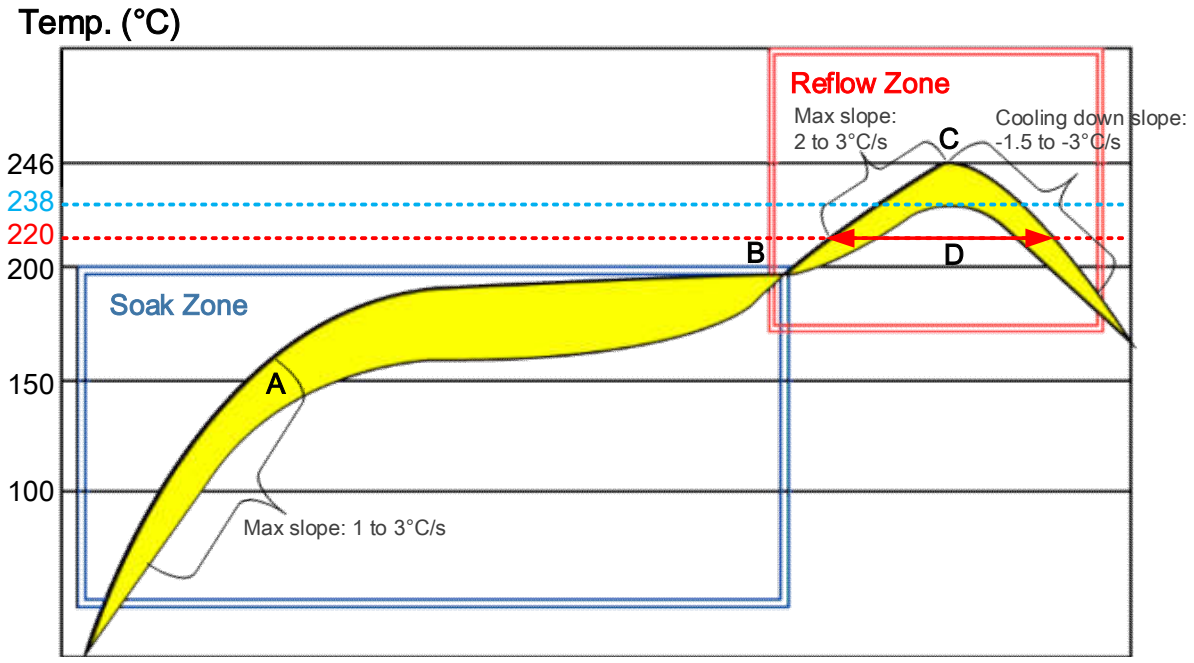


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 59: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220°C)	45–70 s
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

9.3. Packaging

SC200R series module is packaged in tape and reel carriers, and sealed in the vacuum-sealed bag. It is not recommended to open the vacuum package before using the module for actual production. Each reel is 380 mm in diameter and contains 200 modules. The following figures show the package details, measured in mm.

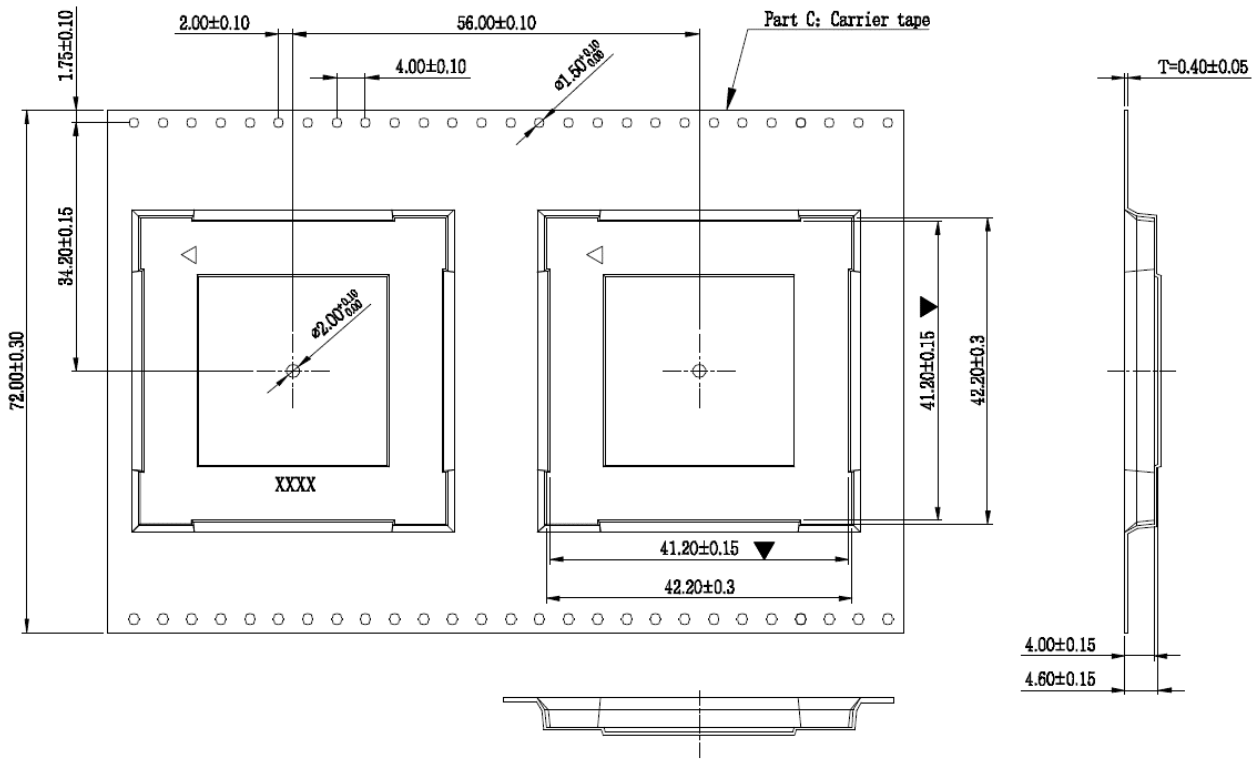


Figure 46: Tape Dimensions (Unit: mm)

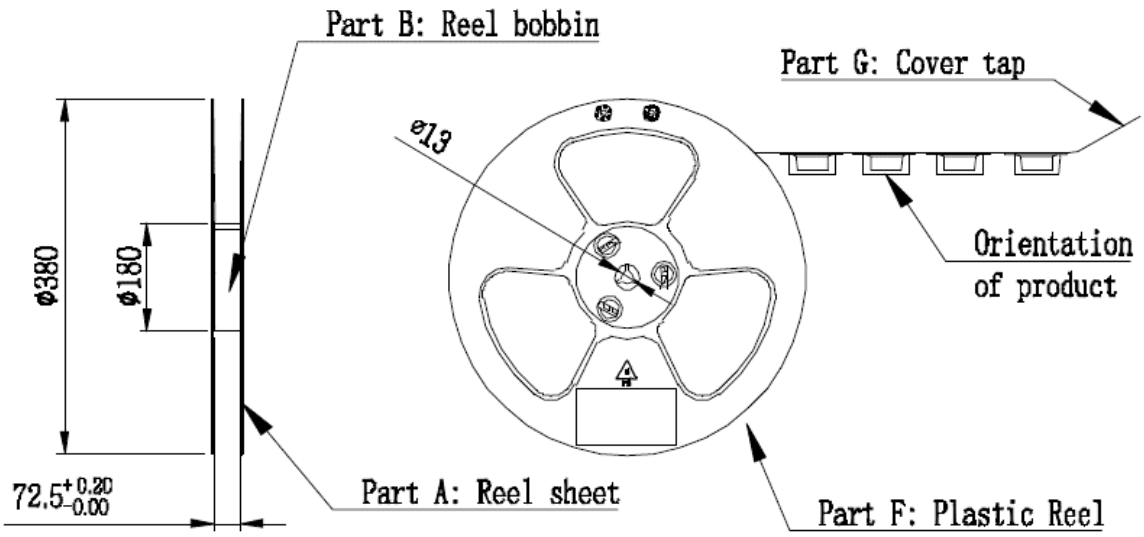


Figure 47: Reel Dimensions (Unit: mm)

Table 60: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 200 pcs	Minimum Package × 4 = 800 pcs
SC200R	200 pcs	Size: 405 mm × 390 mm × 83 mm N.W: 1.9 kg G.W: 3.7 kg	Size: 425 mm × 358 mm × 410 mm N.W: 7.6 kg G.W: 15.2 kg

10 Appendix A References

Table 61: Related Documents

SN	Document Name	Remark
[1]	Quectel_Smart_EVB_G2_User_Guide	Smart EVB G2 User Guide
[2]	Quectel_SC200R_Series_Pin_Description_and_GPIO_Configuration	SC200R Series Pin Description and GPIO Configuration
[3]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[4]	Quectel_Module_Secondary_SMT_Application_Note	Module Secondary SMT Application Note
[5]	Quectel_SC200R_Series_Reference_Design	SC200R Series Reference Design

Table 62: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ALS	Ambient Light Sensor
AMR	Adaptive Multi-rate
AP	Access Point
bps	Bits per Second
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera Serial Interface

CTS	Clear to Send
DC	Dual Carrier
DRX	Discontinuous Reception
DSI	Display Serial Interface
DSP	Digital Signal Processor
ECM	Electret Condenser Microphone
EDGE	Enhanced Data Rate for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EV-DO/EVDO	Evolution-Data Optimized
FDD	Frequency Division Duplex
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GPU	Graphics Processing Unit
GRFC	Generic RF control
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access

HSPA+	High-Speed Packet Access+
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I/O	Input/Output
I2C	Inter-Integrated Circuit
Imax	Maximum Load Current
Inorm	Normal Current
LCC	Leadless Chip Carrier
LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low Dropout Regulator
LE	Low Energy
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long-Term Evolution
MEMS	Micro-Electro-Mechanical System
MIPI	Mobile Industry Processor Interface
NFC	Near Field Communication
NTC	Negative Temperature Coefficient
OTG	On-The-Go
OTP	One Time Programable
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PWM	Pulse Width Modulation

PS	Proximity Sensor
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFFE	RF Front End
RTC	Real Time Clock
RTS	Request to Send
Rx	Receive
SAW	Surface Acoustic Wave
SD Card	Secure Digital Card
SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time-Division Duplex
TP	Touch Panel
TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Teleco mmunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value

V_I	Voltage Input
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
V_Imax	Absolute Maximum Input Voltage Value
V_Imin	Absolute Minimum Input Voltage Value
V_O	Voltage Output
$V_{OH}max$	Maximum Output High Level Voltage Value
$V_{OH}min$	Minimum Output High Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
$V_{OL}min$	Minimum Output Low Level Voltage Value
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

11 Appendix B GPRS Coding Schemes

Table 63: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate kbit/s	9.05	13.4	15.6	21.4

12 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3 + 1 or 2 + 2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 64: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

13 Appendix D EDGE Modulation and Coding Schemes

Table 65: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslots	4 Timeslots
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps