

## DA14870MOD-SF01, DA14870MOD-DF01

SmartBond Multi-Core Dual Mode Bluetooth/Bluetooth LE 6.0 Module

### General Description

The DA14870 module based on DA14870 of integrated BR/EDR/Bluetooth® Low Energy (LE) 6.0 system on chip (SoC), the DA9098 highly integrated, configurable, ultra-low quiescent current charger PMIC and DA7414 high-performance, ultra-low-power, Hi-Fi codec. The DA14870 module brings out all the hardware features and capabilities of the system. The DA14870 Module targets broad market use and is certified across regions providing significant reductions in development cost and risks, and time-to-market.

The DA14870 integrates an Arm® Cortex® M33F application processor, a Tensilica® Fusion F1 DSP, a hardware Voice Activity Detector and Hot-Word detector, Configurable MAC engine with a Bluetooth 6.0 BR/EDR/Bluetooth LE compliant Radio, a rich set of peripherals and communication interfaces including USB 2.0 HS/FS Device mode.

The DA9098 PMIC integrates a 500 mA linear battery charger with power-path manager (PPM), a 4-output SIMO capable of delivering 400 mA of total current, four LDOs and a 3-channel LED driver. In addition to this highly integrated functionality, the DA9098 features a complete set of robust protection features, watchdog and I2C control.

With high-performance playback and record paths, the DA7414 is designed for high dynamic range and minimum latency. Two integrated, programmable, digital signal processors are provided. The first, running at 192 kHz, is dedicated to noise cancellation applications, whilst the second, running at 48 kHz or 192 kHz, can perform music and voice processing such as equalization, limiting, mixing, beamforming, and gain control. A dedicated fast equalization (FEQ) path, operating at the DAC clock rate, delivers improved high-frequency noise cancellation when compared to alternative solutions for both analog and digital microphones.

### Key Features

- Compliant with Bluetooth 6.0, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- Processing Power
  - 160 MHz 32-bit Arm Cortex-M33F with FPU with 16 kB, four-way associative cache with lowest delay LRU algorithm
- Configurable MAC engine with 40/80 MHz Arm M0+ and Automatic Register Programming (ARP) engine
- 320 MHz Tensilica Fusion F1 DSP
- Low-power Voice Activation Detection (VAD) and Hot-Word Detector (HWD) engine with up-to 12 programmable wake words and 2 s pre-roll buffer in Always On state
- On-Chip Memory
  - 256 kB CPU RAM
  - 512 kB CMAC RAM
  - 1024 kB DSP RAM
  - 256 kB Shared RAM
  - 16 kB M33 Cache SRAM with retention capabilities
  - 8 kB PSRAM Data cache
  - 4 kB One-Time-Programmable (OTP) memory for production parameters, crypto keys and configuration scripts
  - 64 kB ROM, including boot ROM and PKI routines for Flash image authentication and RMA field return states
- Memory Interfaces
  - 80 MHz Quad SPI Flash controller with On-the-fly M33 XIP AES256 Decryption
  - 80 MHz Quad SPI PSRAM/Flash Controller with 8 kB cache and Write Back buffer
  - RAM based Entropy for software based True Random Number Generator (TRNG) and FIPS 140-3 compliant DRBG
  - Hidden DMA Security Layers towards OTP and Quad SPI AES256 engine
  - Device locking and Returned Material Authorization (RMA) secure unlocking capabilities
- Clocking
  - RCX32 kHz for start-up and standby (wake-up timer) with Real Time Clock (option for 32 kHz crystal)
  - 40 MHz crystal with 80 MHz Low Power mode
    - Large trimming range
    - Low Power 32 kHz mode
  - 320 MHz SYS-PLL
  - 98.304/90.3168 MHz Fractional PLL for the audio clock domain with automatic ISOC packet Rate Matching (IRM)

- Radio interface
  - TX power consumption:
    - 7.2mW TX 0dBm GFSK
    - 80 mW Tx +12 dBm GFSK
    - 49.0 mW TX +9 dBm EDR
  - RX power consumption: 4.8 mW
  - RX Receiver sensitivity
    - Bluetooth LE 1 Mbit: -99 dBm
    - Bluetooth LE 2 Mbit: -97 dBm
    - BLT BR: -96 dBm
    - BLT EDR 2 Mb: -94 dBm
    - BLT EDR 3 Mb: -88 dBm
    - MIPI RFFE 3-wire interface for single wire antenna matching
    - Internal RX/TX switch
    - CMAC controlled external RF antenna diversity for AoA and AoD applications
    - 2.4 GHz BT/Wi-Fi® Coexistence support
- Security
  - Cryptographic engine with AES-128/192/256, SHA-224/256
  - RAM based Entropy for software based True Random Number Generator (TRNG) and FIPS 140-3 compliant DRBG
  - Hidden DMA Security Layers towards OTP and Quad SPI AES256 engine
  - Device locking and Returned Material Authorization (RMA) secure unlocking capabilities
- Timers
  - 5x General purpose timers, 24/32-bit up/down timers with PWM, 1x dedicated for Coex, 1x MAC timer
  - 3x Watchdog timers
  - Clock calibration circuit
  - 3x Phase counters
- Debug Support
  - Arm CoreSight SoC-400 with single SWD interface for debugging Fusion F1, M33 and CMAC M0+
  - M33F External Trace Module (ETM)
  - M0+ and M33F on-chip Micro Trace Buffer (MTB)
  - Breakpoints triggered freeze logic for all processors
- Power management
  - 0.65-0.8 V Digital core voltage
  - Adaptive Bode Biasing (ABB) for optimal power consumption
  - Dual rail 1.2 V and 1.8 V VDDIO supply voltage per pin selectable
  - Power-On Reset and VDDD and VCS brownout detection with programmable thresholds
  - Charger and Power Path Management
    - Fast charge: 500 mA (max) programmable charge current
    - Programmable pre-charge, fast charge, and termination conditions
    - Dynamic power path
    - Supports adaptive power source voltage to minimize power dissipation
  - Five Power Outputs
    - VSYS V<sub>OUT</sub>: 3.2 V to 4.8 V, programmable in 100 mV steps, I<sub>OUT</sub>: 100 mA (max), programmable in 25 mA steps
    - SIMO1\_1V05 V<sub>OUT</sub>: 1.05 V, I<sub>OUT</sub>: 100 mA
    - SIMO3\_1V8 V<sub>OUT</sub>: 1.8 V, I<sub>OUT</sub>: 100 mA
    - SIMO4\_1V2 V<sub>OUT</sub>: 1.2 V, I<sub>OUT</sub>: 100 mA
    - LDO4\_3V3 V<sub>OUT</sub>: 3.3 V, I<sub>OUT</sub>: 100 mA
  - Protection features
    - Over-voltage protection
    - Thermal shutdown protection
    - Over-discharge protection
  - LED driver current sinks
  - High integration and configurability
    - I2C enabled battery monitors
    - Charging status monitors
- Digital interfaces
  - General Purpose I/Os with programmable pin assignment 42x for SF01 variant, 43x for DF01 variant of the module
  - 3x UARTs up-to 3 Mbps
  - 2x SPI+™ Master/Slave
  - 2x I2C Master/slave 100 kHz, 400 kHz, or 3.4 MHz
  - MIPI I3C controller up-to 12.5 MHz
  - 4x PDM DMIC interface 768 kHz-4 MHz with hardware down sampler
  - Stereo PDM output for external CLASSD amplifier
  - 3x LED timers with load balancing PWM
  - 2x Digital Audio interface (DAI) with I2S, PCM, TDM format master/slave interface up to 8x32 bits channels, 8-192 kHz, 11.025-88.4 kHz
  - 6x Sample Rate Converters for internal DSP rate adaption and DAI slave mode
  - 8x channel DMA for peripherals 16x DSPDMA channels for audio, with dual sample transfer

- USB
  - USB 2.0 HS/FS Device only
  - 1x IN/OUT Control Endpoint 0, 64 B
  - 11x IN/OUT Control, ISOC, Bulk, INT endpoints with Dynamical FIFOs, 64 kB
  - 2x 12 DMA channels
  - LPM L1 (ADC3), LPM L2
- Analog interfaces
  - 12-bit SAR ADC, 1.5 Msamples/s, for 6x external inputs 1.8 V and on-chip supplies and temp sensor measurements
  - Voltage and current based Fuel Gauge accessible through GPADC pins from PMIC
  - On-chip Temperature sensor
  - BC1.2 Battery Charging Detection circuit
- Active Noise Cancellation
  - Support Hybrid, Feedforward, and Feedback topologies
  - 40 dB cancellation at 200 Hz
  - 5.2  $\mu$ s microphone input to headphone output latency through FEQ
  - 25  $\mu$ s microphone input to headphone output latency through DSP
  - Automated calibration and tuning tools
- Digital Audio Interfaces
  - Up to 32-bit 384 kHz sample rate support
  - Three stereo PDM inputs for digital microphones and/or low latency connection from host processors
- Stereo differential headphone path
  - 115 dB dynamic range
  - Output power 2 x 30 mW into 32  $\Omega$
- Input paths
  - Four single-ended or two differential microphone/line-inputs
  - 110 dB dynamic range
  - Integrated dual low-noise microphone
  - Bias
- Digital Signal Processor
  - Dual 98 MHz DSPs
  - 192 kHz, low delay Active Noise canceller (ANC) DSP
  - Dedicated 6 MHz Fast equalization FEQ path
  - 48 kHz/192 kHz, music and voice DSPs
  - Fully-flexible digital mixing with independent gains
- By passable asynchronous sample rate converters

- Clocking
  - Fract-N Phase-locked loop
  - Sample rate tracking

## Applications

- BR/EDR/Bluetooth LE Classic Audio True Wireless Stereo Headset with ANC
  - LE Audio Headset with ANC
  - Bluetooth Audio (Classic and LE) speakers
  - LE Audio Hearing aid
  - LE Audio broadcast TV
  - Proprietary 2.4 GHz ISM band protocols
  - Angle of Arrival (AoA) and Angle of Departure (AoD) IoT applications
  - USB Bluetooth Dongle
  - Wearable devices - Wireless headphones, fitness trackers, smart watches
  - Home automation devices - Smoke detectors, Smart thermostats, Smart door locks
  - Health monitoring medical accessories
  - Rechargeable toys
- 
- Standards conformance
    - ☐ Europe (CE/RED)
    - ☐ UK (UKCA)
    - ☐ US (FCC)
    - ☐ Canada (ISED/ IC)
    - ☐ Japan (MIC)
    - ☐ South Korea (KC)
    - ☐ Taiwan (NCC)
    - ☐ South Africa (ICASA)
    - ☐ Brazil (ANATEL)
    - ☐ China (SRRC)
    - ☐ Australia / New Zealand (ACMA)

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## 1. Terms and Definitions

|      |                           |
|------|---------------------------|
| I-PD | Input Pull-Down           |
| I-PU | Input Pull-Up             |
| DIO  | Digital input-output      |
| GND  | Ground                    |
| ANC  | Active Noise Cancellation |

## 2. References

- [1] DA14870, Datasheet, Renesas Electronics.
- [2] DA9098, Datasheet, Renesas Electronics.
- [3] DA7414, Datasheet, Renesas Electronics.

**Note 1** References are for the latest published version, unless otherwise indicated.

### 3. Block Diagram

#### 3.1 DA14870MOD-SF01 Variant

The DA14870MOD-SF01 variant of the Module, is shown in Figure 1 and consists of:

- DA14870 Multi-Core Dual Mode Bluetooth/Bluetooth LE 6.0 SoC with USB
- DA9098 Ultra-Low IQ Charger PMIC with 4-Output SIMO
- DA7414 High-Performance, Ultra-low power, Hi-Fi Codec with ANC
- 64 Mbit QSPI Flash (XiP)
- RF Switch for Antenna diversity

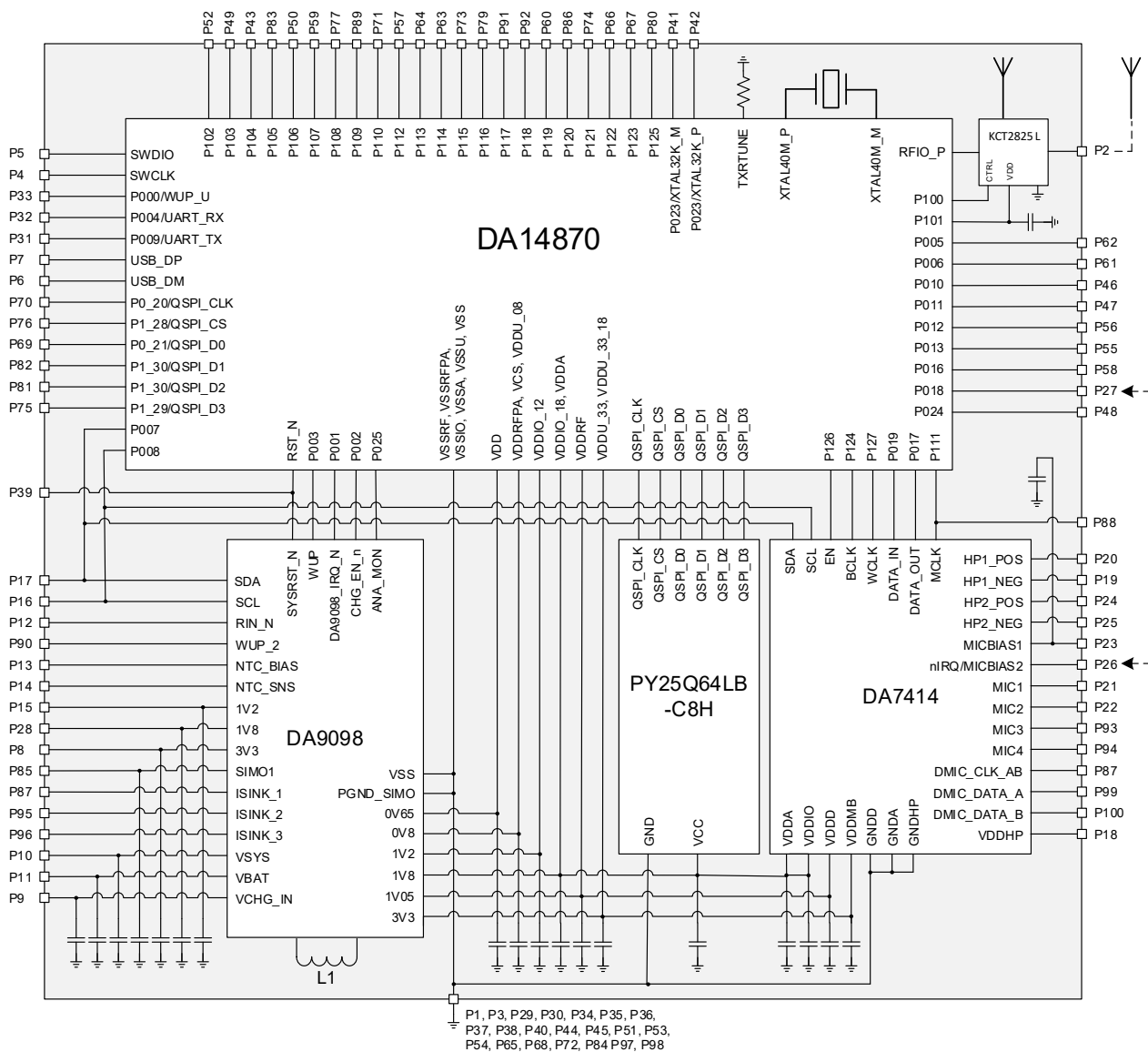


Figure 1. Block diagram of the DA14870 Module (SF01 variant)

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**Figure 2. Block diagram of the DA14870 Module (DF01 variant)**

### 3.3 DA14870 Module Variants

Table 1 shows the differences between the variants of the DA14870 Module.

Table 1: DA14870 Module Variants

| Features                      | DA14870MOD-SF01   | DA14870MOD-DF01   |
|-------------------------------|-------------------|-------------------|
| GPIOs                         | 42                | 43                |
| QSPI Flash                    | 64 Mbit           | 64 Mbit           |
| QSPI Flash/PSRAM Interface    | ✓                 | ✓                 |
| Antenna Diversity (RF Switch) | ✓                 | ✓                 |
| DA7414 Audio Codec            | ✓                 | x                 |
| Package (mm)                  | 21.5 x 14.1 x 2.7 | 21.5 x 14.1 x 2.7 |

**Note 1** The DA7414 Audio Codec exists in SF01 variant of the DA14870 Module.  
The DA7414 Audio Codec does not exist in DF01 variant of the DA14870 Module.

### 3.4 Typical Application

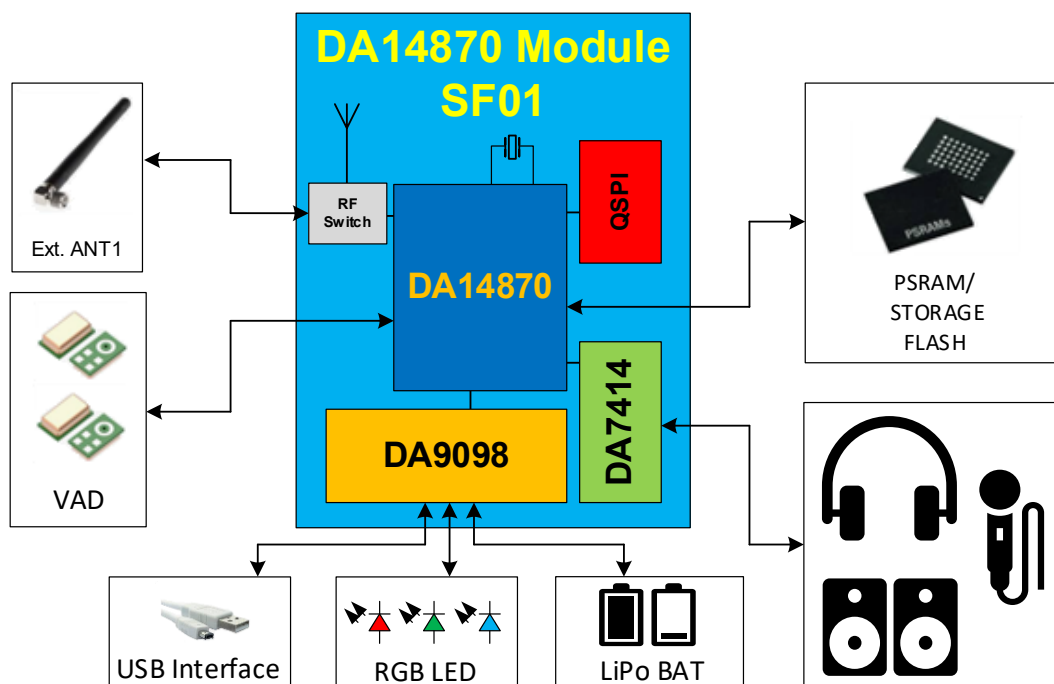


Figure 3. Typical application example of the DA14870 Module (SF01)

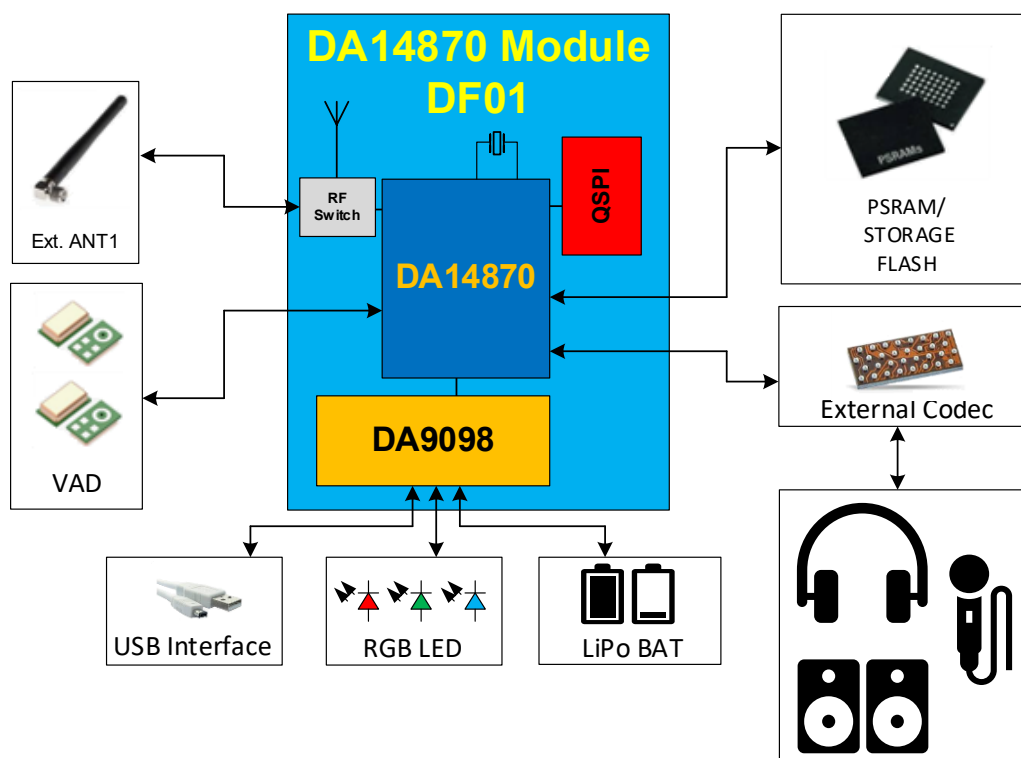


Figure 4. Typical application example of the DA14870 Module (DF01)

## 4. Pinout

### 4.1 Pin Assignments

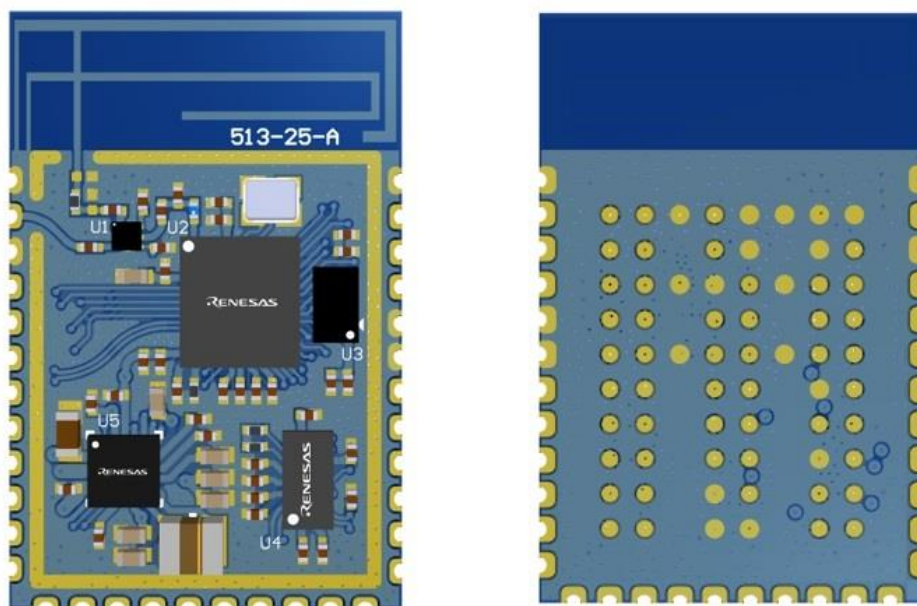


Figure 5. DA14870 Module top and bottom view

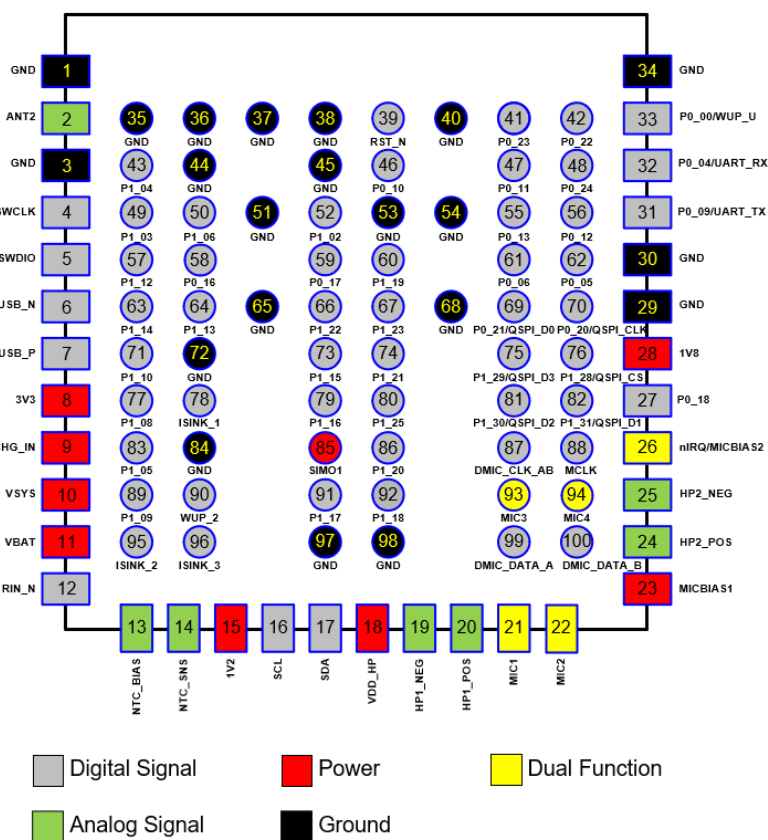


Figure 6. DA14870MOD-SF01 variant pin assignment (top view)

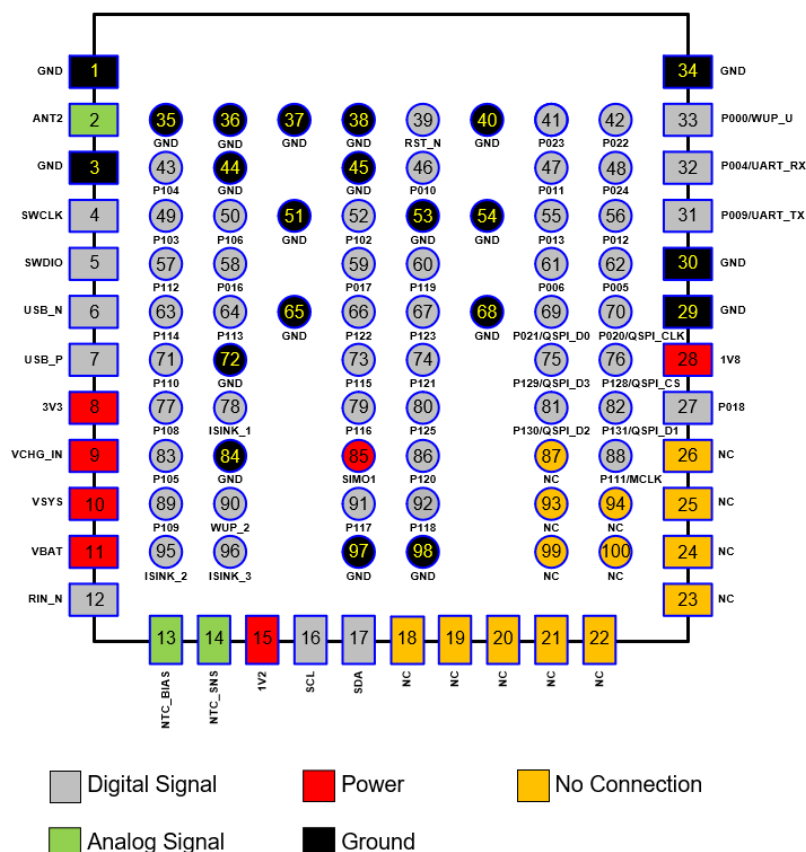


Figure 7. DA14870MOD-DF01 variant pin assignment (top view)

## 4.2 Pin Descriptions

Table 2. Pin description

| Pin number                                                                                                       | Pin name    | Type<br><a href="#">Note 1</a> | Reset state | Description                                                                            |
|------------------------------------------------------------------------------------------------------------------|-------------|--------------------------------|-------------|----------------------------------------------------------------------------------------|
| <b>General Purpose I/Os and fixed pin assignment; additional functions are programmable through Pxy_MODE_REG</b> |             |                                |             |                                                                                        |
| P1                                                                                                               | GND         | Ground                         |             | Ground                                                                                 |
| P2                                                                                                               | ANT2        | RFIO                           |             | INPUT/OUTPUT. External antenna connection point                                        |
| P3                                                                                                               | GND         | Ground                         |             | Ground                                                                                 |
| P4                                                                                                               | SWCLK       | DI                             | I-PD        | INPUT. Serial Wire Debug clock. <a href="#">Note 2</a>                                 |
| P5                                                                                                               | SWDIO       | DIO                            | I-PU        | INPUT/OUTPUT. Serial Wire Debug data I/O. <a href="#">Note 2</a>                       |
| P6                                                                                                               | USB_DM/ADC4 | AIO                            |             | INPUT/OUTPUT. USB- terminal.<br>INPUT. ADC channel 4 (through scaler in BC1.2 circuit) |
| P7                                                                                                               | USB_DP/ADC3 | AIO                            |             | INPUT/OUTPUT. USB+ terminal.<br>INPUT. ADC channel 3 (through scaler in BC1.2 circuit) |
| P8                                                                                                               | 3V3         | PWR                            |             | PMIC LDO4 output                                                                       |
| P9                                                                                                               | VCHG_IN     | PWR                            |             | Input power supply                                                                     |
| P10                                                                                                              | VSYS        | PWR                            |             | Intermediate supply of power rails                                                     |
| P11                                                                                                              | VBAT        | PWR                            |             | Battery connection                                                                     |
| P12                                                                                                              | RIN_N       | DI                             |             | Manual reset input and wake from SHIP mode                                             |
| P13                                                                                                              | NTC_BIAS    | AIO                            |             | External temperature monitoring bias                                                   |
| P14                                                                                                              | NTC_SNS     | AIO                            |             | External temperature monitoring sense pin                                              |
| P15                                                                                                              | 1V2         | PWR                            |             | PMIC SIMO4 output                                                                      |
| P16                                                                                                              | SCL         | DO                             |             | OUTPUT. I2C bus clock. Fixed at 1.8 V.                                                 |

## SmartBond Multi-Core Dual Mode Bluetooth/Bluetooth LE 6.0 Module

| Pin number | Pin name                   | Type<br><a href="#">Note 1</a> | Reset<br>state         | Description                                                                                                                               |
|------------|----------------------------|--------------------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| P17        | SDA                        | DIO                            |                        | INPUT/OUTPUT. I2C bus data. Fixed at 1.8 V.                                                                                               |
| P18        | VDDHP                      | PWR                            |                        | SF01 Variant: DA7414 Codec Headphone supply input.<br>Configurable at 1.2 V or 1.8 V.<br>DF01 Variant: NC                                 |
| P19        | HP1_NEG                    | AO                             |                        | SF01 Variant: DA7414 Headphone channel one negative output<br>DF01 Variant: NC                                                            |
| P20        | HP1_POS                    | AO                             |                        | SF01 Variant: DA7414 Headphone channel one positive output<br>DF01 Variant: NC                                                            |
| P21        | MIC1/MIC1_P                | AI                             |                        | SF01 Variant: Microphone 1 input/Microphone 1 positive input<br>DF01 Variant: NC                                                          |
| P22        | MIC2/MIC2_P                | AI                             |                        | SF01 Variant: Microphone 2 input/Microphone 2 positive input<br>DF01 Variant: NC                                                          |
| P23        | MICBIAS1                   | AO                             |                        | SF01 Variant: MICBIAS output<br>DF01 Variant: NC                                                                                          |
| P24        | HP2_POS                    | AO                             |                        | SF01 Variant: DA7414 Headphone channel two positive output<br>DF01 Variant: NC                                                            |
| P25        | HP2_NEG                    | AO                             |                        | SF01 Variant: DA7414 Headphone channel two negative output<br>DF01 Variant: NC                                                            |
| P26        | nIRQ/MICBIAS2              | DO/AO                          |                        | SF01 Variant: Default active-low, open-drain interrupt (external pullup)/<br>MICBIAS2 output<br>DF01 Variant: NC                          |
| P27        | P0_18                      | DIO                            | I-PD                   | INPUT/OUTPUT with pull-up/down resistor.                                                                                                  |
| P28        | 1V8                        | PWR                            |                        | PMIC SIMO3 output                                                                                                                         |
| P29        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P30        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P31        | P0_09<br>UART_TX<br>(boot) | DIO                            | I-PD                   | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT. UART Transmit data output during boot.                                                |
| P32        | P0_04<br>UART_RX<br>(Boot) | DIO                            | I-PD                   | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT UART RX Receive data input during boot.                                                 |
| P33        | P0_00/WUP_U                | DIO                            | I-PU                   | INPUT/OUTPUT with pull-up/down resistor. <a href="#">Note 3</a><br>INPUT Wake-up signal from User, Active LOW                             |
| P34        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P35        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P36        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P37        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P38        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P39        | RST_N                      | DI                             | I-PU<br>(Fixed<br>25k) | INPUT. Device reset (active LOW). <a href="#">Note 3</a>                                                                                  |
| P40        | GND                        | Ground                         |                        | Ground                                                                                                                                    |
| P41        | P0_23<br>XTAL32K_M         | DIO                            | I-PD                   | INPUT/OUTPUT with pull-up/down resistor. <a href="#">Note 3</a><br>INPUT. Crystal 32 kHz oscillator.<br>External source bypass mode input |

## SmartBond Multi-Core Dual Mode Bluetooth/Bluetooth LE 6.0 Module

| Pin number | Pin name           | Type<br>Note 1 | Reset<br>state | Description                                                                                          |
|------------|--------------------|----------------|----------------|------------------------------------------------------------------------------------------------------|
| P42        | P0_22<br>XTAL32K_P | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/ Crystal 32 kHz oscillator. <a href="#">Note 3</a> |
| P43        | P1_04              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P44        | GND                | Ground         |                | Ground                                                                                               |
| P45        | GND                | Ground         |                | Ground                                                                                               |
| P46        | P0_10              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P47        | P0_11              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P48        | P0_24<br>ADC0      | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT. ADC channel 0.                                    |
| P49        | P1_03<br>TRACE_D0  | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT. ETM Data bit 0.                                  |
| P50        | P1_06<br>TRACE_D2  | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT. ETM Data bit 2.                                  |
| P51        | GND                | Ground         |                | Ground                                                                                               |
| P52        | P1_03<br>TRACE_CLK | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT. ETM Trace clock.                                 |
| P53        | GND                | Ground         |                | Ground                                                                                               |
| P54        | GND                | Ground         |                | Ground                                                                                               |
| P55        | P0_13              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P56        | P0_12              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P57        | P1_12              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P58        | P0_16              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P59        | P1_07<br>TRACE_D3  | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT. ETM Data bit 3.                                  |
| P60        | P1_19              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P61        | P0_06              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P62        | P0_05              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P63        | P1_14              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P64        | P1_13              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P65        | GND                | Ground         |                | Ground                                                                                               |
| P66        | P1_22              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P67        | P1_23              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P68        | GND                | Ground         |                | Ground                                                                                               |
| P69        | P0_21<br>QSPI_D0   | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/OUTPUT. QSPI D0. <a href="#">Note 2</a>            |
| P70        | P0_20<br>QSPI_CLK  | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/OUTPUT. QSPI Clock. <a href="#">Note 2</a>         |
| P71        | P1_10              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P72        | GND                | Ground         |                | Ground                                                                                               |
| P73        | P1_15              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P74        | P1_21              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P75        | P1_29<br>QSPI_D3   | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/OUTPUT. QSPI D3. <a href="#">Note 2</a>            |
| P76        | P1_28<br>QSPI_CS   | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/OUTPUT. QSPI Chip select. <a href="#">Note 2</a>   |
| P77        | P1_08              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P78        | ISINK1             | AO             |                | LED driver Output 1                                                                                  |
| P79        | P1_16              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P80        | P1_25              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                             |
| P81        | P1_30<br>QSPI_D2   | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/OUTPUT. QSPI D2. <a href="#">Note 2</a>            |

| Pin number | Pin name                   | Type<br>Note 1 | Reset<br>state | Description                                                                                                         |
|------------|----------------------------|----------------|----------------|---------------------------------------------------------------------------------------------------------------------|
| P82        | P1_30<br>QSPI_D1           | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>INPUT/OUTPUT. QSPI D1. Note 2                                           |
| P83        | P1_05<br>TRACE_D1          | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT. ETM Data bit 1.                                                 |
| P84        | GND                        | Ground         |                | Ground                                                                                                              |
| P85        | 1V05                       | PWR            |                | SIMO1 output (Adjustable)                                                                                           |
| P86        | P1_20                      | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                                            |
| P87        | DMIC_CLK_AB                | DO             |                | SF01 Variant: DMIC clock for DMIC_DATA_A and<br>DMIC_DATA_B<br>DF01 Variant: NC                                     |
| P88        | P1_11<br>MCLK              | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.<br>OUTPUT Recommended pin for MCLK.                                        |
| P89        | P1_09                      | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                                            |
| P90        | WUP_2                      | DI             |                | Additional pin for wake-up from deep sleep mode                                                                     |
| P91        | P1_17                      | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                                            |
| P92        | P1_18                      | DIO            | I-PD           | INPUT/OUTPUT with pull-up/down resistor.                                                                            |
| P93        | MIC3/MIC1_N<br>DMIC_CLK_C  | AI/DO          |                | SF01 Variant: Microphone 3 input/<br>Microphone 1 negative input/<br>DMIC clock for DMIC_DATA_C<br>DF01 Variant: NC |
| P94        | MIC4/MIC2_N<br>DMIC_DATA_C | AI/DI          |                | SF01 Variant: Microphone 4 input/<br>Microphone 2 negative input/<br>DMIC data input C<br>DF01 Variant: NC          |
| P95        | ISINK2                     | AO             |                | LED driver Output 2                                                                                                 |
| P96        | ISINK3                     | AO             |                | LED driver Output 3                                                                                                 |
| P97        | GND                        | Ground         |                | Ground                                                                                                              |
| P98        | GND                        | Ground         |                | Ground                                                                                                              |
| P99        | DMIC_DATA_A                | DI             |                | SF01 Variant: DMIC data input A<br>DF01 Variant: NC                                                                 |
| P100       | DMIC_DATA_B                | DI             |                | SF01 Variant: DMIC data input B<br>DF01 Variant: NC                                                                 |

**Note 1** This pin is only supplied from the VDDA\_18 rail in all modes

**Note 2** PU = Pull-up resistor enabled, PD = Pull-down resistor enabled, I = input, O = output, Hi-Z = high impedance, DIO = Digital I/O, DIOD = Digital I/O with open drain, 1 = logic HIGH level, 0 = logic LOW level. See Pxy\_MODE\_REG[PUPD] for INPUT/OUTPUT and Pull-up/Pull-down configurations.

**Note 3** During and after reset all I/Os are set to input, and all pull-up and pull-down resistors are enabled unless otherwise specified.

**Table 3. Pin type definition**

| Pin type | Description                     | Pin type | Description                   |
|----------|---------------------------------|----------|-------------------------------|
| DI       | Digital input                   | AI       | Analog input                  |
| DO       | Digital output                  | AO       | Analog output                 |
| DIO      | Digital input/output            | AIO      | Analog input/output           |
| DIOD     | Digital input/output open drain | BP       | Back drive protection         |
| PU       | Pull-up resistor (fixed)        | SPU      | Switchable pull-up resistor   |
| PD       | Pull-down resistor (fixed)      | SPD      | Switchable pull-down resistor |
| PWR      | Power                           | GND      | Ground                        |

## 5. Specifications

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only. Default measurement conditions (unless otherwise specified): VDDA\_18 = 1.8 V, VDDRF = 1.05 V, VDDRFPA = 0.8 V, VCS = 0.8 V, VDDD = 0.8 V, TA = 25 °C. All radio measurements are performed with standard RF measurement equipment providing a source/load impedance of 50 Ω.

The specified MIN and MAX capacitor values define the range of the effective capacitance, which may vary over the applied voltage due to voltage derating. Refer to the component manufacturer for the capacitor specifications.

### 5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

| Parameter                     | Description                               | Conditions        | Min  | Max  | Unit |
|-------------------------------|-------------------------------------------|-------------------|------|------|------|
| T <sub>STG</sub>              | Storage temperature                       |                   | -40  | 150  | °C   |
| V <sub>PIN_LIM</sub>          | Limiting voltage on all pins except below |                   | 0    | 1.98 | V    |
| V <sub>PIN_LIM_ANT2</sub>     | Limiting voltage on ANT2                  |                   | 0    | 0.88 | V    |
| V <sub>PIN_LIM_USB_DM</sub>   | Limiting voltage pin USB_DM               |                   | 0    | 4.6  | V    |
| V <sub>PIN_LIM_USB_DP</sub>   | Limiting voltage pin USB_DP               |                   | 0    | 4.6  | V    |
| V <sub>PIN_LIM_XTAL_32K</sub> | Limiting voltage on XTAL32K               |                   | 0    | 0.9  | V    |
| V <sub>PIN_LIM_VDD_HP</sub>   | Limiting voltage pin VDD_HP               | SF01 variant only | 1.14 | 1.89 | V    |
| V <sub>PIN_LIM_CHG_IN</sub>   | Limiting voltage on input power supply    |                   | -0.3 | 22   | V    |
| V <sub>PIN_LIM_VBAT</sub>     | Limiting voltage on battery connection    |                   | -0.3 | 6    | V    |
| V <sub>PIN_LIM_ISINK1</sub>   | Limiting voltage for pins ISINK1          |                   | -0.3 | 6    | V    |
| V <sub>PIN_LIM_ISINK2</sub>   | Limiting voltage for pins ISINK2          |                   | -0.3 | 6    | V    |
| V <sub>PIN_LIM_ISINK3</sub>   | Limiting voltage for pins ISINK3          |                   | -0.3 | 6    | V    |
| V <sub>PIN_LIM_NTC_BIAS</sub> | Limiting voltage for pins NTC_BIAS        |                   | -0.3 | 6    | V    |
| V <sub>PIN_LIM_NTC_SNS</sub>  | Limiting voltage for pins NTC_SNS         |                   | -0.3 | 6    | V    |

|                                                                                                                                                                                                         |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
|                                                                                                                      | <b>CAUTION</b> |
| Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty. |                |

### 5.2 Electrostatic Discharge Ratings

Table 5. Electrostatic discharge ratings

| Parameter            | Description            | Conditions                 | Rating | Unit |
|----------------------|------------------------|----------------------------|--------|------|
| V <sub>ESD_HBM</sub> | Maximum ESD protection | Human body model (HBM)     | 2000   | V    |
| V <sub>ESD_CDM</sub> | Maximum ESD protection | Charged device model (CDM) | 400    | V    |

### 5.3 Recommended Operating Conditions

Table 6. Recommended operating conditions

| Parameter             | Description                                           | Conditions                                           | Min  | Typ  | Max  | Unit |
|-----------------------|-------------------------------------------------------|------------------------------------------------------|------|------|------|------|
| T <sub>A</sub>        | Operating ambient temperature                         |                                                      | -30  |      | 85   | °C   |
| V <sub>CHG_IN</sub>   | Charger input supply                                  |                                                      | 3.6  | 5    | 5.5  | V    |
| I <sub>CHG_IN</sub>   |                                                       |                                                      |      |      |      |      |
| V <sub>BAT</sub>      | Battery voltage                                       | Active battery                                       | 2.5  | 3.6  | 4.7  | V    |
| I <sub>BAT</sub>      |                                                       |                                                      |      |      |      |      |
| V <sub>GPIO</sub>     | General purpose I/O                                   | Exclude I2C pins (P16, P17) which are constant 1.8 V | 1.2  | 1.8  | 1.89 | V    |
| V <sub>DDHP</sub>     | Headphone Supply                                      | SF01 variant only                                    | 1.14 | 1.8  | 1.89 | V    |
| V <sub>AMIC</sub>     | Analog MIC Supply                                     | SF01 variant only                                    | 1.71 | 1.8  | 1.89 | V    |
| V <sub>DMIC</sub>     | Digital MIC Supply                                    | SF01 variant only                                    | 1.71 | 1.8  | 1.89 | V    |
| V <sub>105</sub>      | VDDRF, VDDD supply, VIN_LDO1, VIN_LDO2 voltage supply |                                                      | 1    | 1.05 | 1.1  | V    |
| V <sub>12</sub>       | IO supply voltage 1.2V                                |                                                      | 1.14 | 1.2  | 1.89 | V    |
| V <sub>18</sub>       | IO supply voltage 1.18V                               |                                                      | 1.71 | 1.8  | 1.89 | V    |
| V <sub>33</sub>       | VDDU_18_33, VDDU_33, VDD_MB power supply              |                                                      | 3.1  | 3.3  | 3.6  | V    |
| V <sub>SYS</sub>      | VSYS output voltage                                   |                                                      | 3.2  |      | 4.8  | V    |
| V <sub>MICBIAS1</sub> | MICBIAS1 supply voltage                               | SF01 variant only                                    | 1.71 | 1.8  | 1.89 | V    |
| V <sub>MICBIAS2</sub> | MICBIAS2 supply voltage                               | SF01 variant only (multiplexed with nIRQ)            | 1.71 | 1.8  | 1.89 | V    |

### 5.4 Thermal Specifications

Table 7. &lt;Package&gt; ratings

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|-------------|------------|-----|-----|-----|------|
|           |             |            |     |     |     |      |

### 5.5 Electrical Specifications

Electrical characteristics table limits are guaranteed by production testing, design, or correlation using standard statistical quality control methods unless otherwise stated. Typical (Typ) specifications are mean or average values at T<sub>A</sub> = 25°C and are not guaranteed.

Recommended operating conditions unless otherwise noted. V<sub>IN</sub> = 4.5 V to 80 V, or V<sub>DD</sub> = 8 V ±10%, C<sub>VCC5V</sub> = 4.7 μF, T<sub>A</sub> = -40°C to +125°C, Typical values are at T<sub>A</sub> = +25°C, unless otherwise specified.

Table 8. DC specifications

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|-----------|--------|-----------------|-----|-----|-----|------|
|           |        |                 |     |     |     |      |

Table 9. AC specifications

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|-----------|--------|-----------------|-----|-----|-----|------|
|           |        |                 |     |     |     |      |

Table 10. Electrical specifications

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|-----------|--------|-----------------|-----|-----|-----|------|
|           |        |                 |     |     |     |      |

## 5.6 ISINK - LED Driver Characteristics

Table 11: ISINK Electrical Characteristics

| Parameter                      | Description                                             | Conditions                                                                        | Min   | Typ | Max  | Unit |
|--------------------------------|---------------------------------------------------------|-----------------------------------------------------------------------------------|-------|-----|------|------|
| <b>Programmable Conditions</b> |                                                         |                                                                                   |       |     |      |      |
| I <sub>OUT</sub>               | Programmable output current range per sink              |                                                                                   | 0.05  |     | 12.8 | mA   |
| F <sub>PWM</sub>               | PWM frequency                                           |                                                                                   | 0.001 |     | 1    | kHz  |
| <b>Electrical Performance</b>  |                                                         |                                                                                   |       |     |      |      |
| I <sub>OUT_ACC</sub>           | Absolute output current accuracy                        | T <sub>A</sub> = 25 °C<br>V <sub>SINK</sub> = 0.2 V<br>I <sub>SINK</sub> = 3.3 mA | -2    |     | 2    | %    |
| V <sub>OUT</sub>               | Absolute operating voltage of the sink                  |                                                                                   | 0     |     | 5.5  | V    |
| V <sub>DROPOUT</sub>           | Dropout voltage above which sink operates in regulation |                                                                                   | 0.2   |     |      | V    |
| I <sub>Q</sub>                 | Quiescent current per active current sink               |                                                                                   |       | 5   | 15   | μA   |

## 5.7 Battery Charger Electrical Characteristics

Table 12: Battery Charger Electrical Characteristics

| Parameter                      | Description                                         | Conditions                                                                             | Min   | Typ | Max  | Unit |
|--------------------------------|-----------------------------------------------------|----------------------------------------------------------------------------------------|-------|-----|------|------|
| <b>Programmable Conditions</b> |                                                     |                                                                                        |       |     |      |      |
| I <sub>BAT_DCHG_RNG</sub>      | Discharge current limit setting range               | Programmable                                                                           | 0.15  |     | 2    | A    |
| V <sub>BAT_CHG</sub>           | Charge voltage range                                | Operating in voltage regulation, programmable in 10 mV steps                           | 3.6   |     | 4.65 | V    |
| I <sub>CHG</sub>               | Fast charge current range                           |                                                                                        | 2.5   |     | 500  | mA   |
| I <sub>TER_5%</sub>            | Termination charge current 5 % of I <sub>CHG</sub>  |                                                                                        | 0.125 |     | 25   | mA   |
| I <sub>TER_10%</sub>           | Termination charge current 10 % of I <sub>CHG</sub> |                                                                                        | 0.25  |     | 50   | mA   |
| I <sub>TER_20%</sub>           | Termination charge current 20 % of I <sub>CHG</sub> |                                                                                        | 0.5   |     | 100  | mA   |
| I <sub>TER_35%</sub>           | Termination charge current 35 % of I <sub>CHG</sub> |                                                                                        | 0.875 |     | 175  | mA   |
| I <sub>PRE_CHG_RNG</sub>       | Pre-charge current range                            | Note 1                                                                                 | 0.5   |     | 64   | mA   |
| V <sub>RCHG</sub>              | Recharge threshold voltage range                    | V <sub>BAT</sub> below V <sub>BAT_CHG</sub> - 2 programmable thresholds                | 140   |     | 300  | mV   |
| V <sub>VSYS_DPPM_THR</sub>     | V <sub>VSYS</sub> DPPM voltage threshold            | V <sub>VSYS</sub> falling, relative to V <sub>BAT</sub><br>Programmable in 50 mV steps | 100   |     | 250  | mV   |

| Parameter                        | Description                                       | Conditions                                                    | Min  | Typ         | Max | Unit |
|----------------------------------|---------------------------------------------------|---------------------------------------------------------------|------|-------------|-----|------|
| V <sub>PRE_TO_FAST_CHG_THR</sub> | Pre charge to fast charge threshold voltage range | VBAT rising<br>Programmable in 100 mV steps                   | 2.7  |             | 3.4 | V    |
| <b>Electrical Performance</b>    |                                                   |                                                               |      |             |     |      |
| R <sub>ON_CHG_INT</sub>          | Battery charger MOSFET on-resistance              | Measured from VBAT to VSYS<br>VBAT = 4.35 V,<br>IBAT = 100 mA |      |             | 175 | mΩ   |
| V <sub>VBAT_SM_THR</sub>         | Threshold to enter the battery supplement mode    | VVBAT > VVBAT_UVLO                                            |      | VSYS < VBAT |     | V    |
| V <sub>BAT_CHG_ACC</sub>         | Charge voltage accuracy                           | 0 °C < T <sub>J</sub> < 85 °C                                 | -0.5 |             | 0.5 | %    |
| I <sub>CHG_ACC</sub>             | Fast charge current accuracy                      | ICHG > 5 mA                                                   | -5   |             | 5   | %    |
| I <sub>PRE_CHG_ACC</sub>         | Pre-charge current accuracy                       | VBAT > 2 V                                                    | -10  |             | 10  | %    |
| I <sub>TER_ACC</sub>             | Termination charge current accuracy               | ITER = 10 mA                                                  | -10  |             | 10  | %    |

**Note 1** See CHG\_IPRECHG\_CFG in register map

## 5.8 Battery Temperature Sensor Characteristics

Table 13: Battery Temperature Sensor Characteristics

| Parameter                      | Description                | Conditions                      | Min  | Typ  | Max  | Unit |
|--------------------------------|----------------------------|---------------------------------|------|------|------|------|
| <b>Electrical Performance</b>  |                            |                                 |      |      |      |      |
| V <sub>TEMP_HOT</sub>          | Hot temperature threshold  | % of VSYS,<br>NTC_SNS falling   | 14.5 | 15   | 15.2 | %    |
| V <sub>TEMP_WARM</sub>         | Warm threshold             | % of VSYS<br>,NTC_SNS falling   | 20.1 | 20.5 | 20.8 | %    |
| V <sub>TEMP_COOL</sub>         | Cool threshold             | % of VSYS<br>,NTC_SNS rising    | 34.4 | 35   | 35.4 | %    |
| V <sub>TEMP_COLD</sub>         | Cold temperature threshold | % of VSYS<br>,NTC_SNS rising    | 39.3 | 39.8 | 40.2 | %    |
| V <sub>OFF_TEMP_SNS</sub>      | NTC_SNS disable threshold  | % of VSYS for rising<br>NTC_SNS | 55   |      | 60   | %    |
| t <sub>TEMP_SNS DEGLITCH</sub> | NTC_SNS deglitch time      | NTS_SNS at any threshold        |      | 10   |      | ms   |

## 5.9 Protection Electrical Characteristics for PMIC

Table 14: Protection Electrical Characteristics

| Parameter                      | Description                                                              | Conditions                                                                       | Min | Typ | Max  | Unit |
|--------------------------------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----|-----|------|------|
| <b>Programmable Conditions</b> |                                                                          |                                                                                  |     |     |      |      |
| T <sub>WARN_RNG</sub>          | Warning temperature                                                      | T <sub>J</sub> ,<br>Programmable in<br>10 °C steps                               | 70  |     | 100  | °C   |
| <b>Electrical Performance</b>  |                                                                          |                                                                                  |     |     |      |      |
| V <sub>BAT_SHRT_THR</sub>      | Battery voltage short<br>detection threshold                             | V <sub>BAT</sub> falling,<br>V <sub>CHG_IN</sub> = 5 V<br><a href="#">Note 2</a> |     | 2   |      | V    |
| V <sub>BAT_SHRT_HYS</sub>      | Battery voltage short<br>detection hysteresis                            |                                                                                  |     | 100 |      | mV   |
| V <sub>BAT_UVLO_THR</sub>      | Battery under-voltage<br>lockout threshold<br>range                      | Programmable<br>range<br>100 mV steps<br>V <sub>BAT</sub> falling                | 2.5 |     | 3    | V    |
| V <sub>BAT_UVLO_ACC</sub>      | Default battery under-<br>voltage lockout<br>accuracy                    | V <sub>BAT_UVLO</sub> = 2.5<br>V                                                 | -3  |     | 3    | %    |
| V <sub>BAT_UVLO_HYS</sub>      | Battery under-voltage<br>lockout threshold<br>hysteresis                 |                                                                                  |     | 200 |      | mV   |
| V <sub>CHG_IN_OV</sub>         | V <sub>CHG_IN</sub> over-voltage<br>protection threshold<br>voltage      | V <sub>CHG_IN</sub> rising                                                       | 5.5 |     | 5.85 | V    |
| V <sub>CHG_IN_OV_HYS</sub>     | Over-voltage<br>protection<br>hysteresis                                 |                                                                                  |     | 100 |      | mV   |
| V <sub>SLP</sub>               | Sleep entry threshold                                                    | V <sub>CHG_IN</sub> - V <sub>BAT</sub><br>V <sub>CHG_IN</sub> falling            |     | 85  | 145  | mV   |
| V <sub>SLP_HYS</sub>           | Sleep mode hysteresis                                                    | V <sub>CHG_IN</sub> rising                                                       | 80  | 130 | 200  | mV   |
| V <sub>SYS_UVLO_THR</sub>      | V <sub>SYS</sub> under-voltage<br>lockout threshold                      | V <sub>SYS</sub> falling                                                         |     | 2.5 |      | V    |
| V <sub>CHG_IN_UVLO_THR</sub>   | V <sub>CHG_IN</sub> under-<br>voltage<br>lockout threshold               | V <sub>CHG_IN</sub> rising                                                       | 3.3 |     | 3.6  | V    |
| V <sub>CHG_IN_UVLO_HYS</sub>   | V <sub>CHG_IN</sub> under-<br>voltage<br>lockout threshold<br>hysteresis | V <sub>CHG_IN</sub> falling                                                      |     | 150 |      | mV   |
| T <sub>SHDN</sub>              | Thermal shutdown                                                         | T <sub>J</sub>                                                                   |     | 125 |      | °C   |
| T <sub>HYS</sub>               | Thermal shutdown<br>hysteresis                                           | T <sub>J</sub>                                                                   |     | 20  |      | °C   |

**Note 2** Charge current is reduced to IPRE\_CHG



## 5.10 Radio

### 5.10.1 LPA, HPA DC Radio Characteristics

Table 15. RADIO\_CURRENTS - DC characteristics

| Parameter                        | Symbol                            | Test conditions                             | Min | Typ  | Max | Unit |
|----------------------------------|-----------------------------------|---------------------------------------------|-----|------|-----|------|
| I <sub>RF_RX_VDDA_18</sub>       | Supply current from VDDA_18 1.8 V | Radio Receiver LDOs and Bias                |     | 0.13 |     | mA   |
| I <sub>RF_RX_VDDD</sub>          | Supply current from VDDD 0.8 V    | Radio Receiver Demodulator                  |     | 1.1  |     | mA   |
| I <sub>RF_RX_VDDRF</sub>         | Supply current from VDDRF 1.05 V  | Radio Receiver excl. XTAL40MHz              |     | 3.5  |     | mA   |
| I <sub>RF_TX_VDDA_18</sub>       | Supply current from VDDA_18 1.8 V | Radio Transmitter LDOs and Bias             |     | 0.04 |     | mA   |
| I <sub>RF_TX_VDDRFPA_12dBm</sub> | Supply current from VDDRFPA 0.8 V | Radio Transmitter HPA; +12 dBm              |     | 75   |     | mA   |
| I <sub>RF_TX_VDDRFPA_9dBm</sub>  | Supply current from VDDRFPA 0.8 V | Radio Transmitter HPA; +9 dBm               |     | 45   |     | mA   |
| I <sub>RF_TX_VDDRFPA_6dBm</sub>  | Supply current from VDDRFPA 0.8 V | Radio Transmitter HPA; +6 dBm               |     | 31   |     | mA   |
| I <sub>RF_TX_VDDRFPA_4dBm</sub>  | Supply current from VDDRFPA 0.8 V | Radio Transmitter LPA; +4 dBm               |     | 9.5  |     | mA   |
| I <sub>RF_TX_VDDRFPA_0dBm</sub>  | Supply current from VDDRFPA 0.8 V | Radio Transmitter LPA; 0 dBm                |     | 5.5  |     | mA   |
| I <sub>RF_TX_VDDRF_LPA</sub>     | Supply current from VDDRF 1.05 V  | Radio Transmitter using LPA excl. XTAL40MHz |     | 1.2  |     | mA   |
| I <sub>RF_TX_VDDRF_HPA</sub>     | Supply current from VDDRF 1.05 V  | Radio Transmitter using HPA excl. XTAL40MHz |     | 1.5  |     | mA   |

### 5.10.2 LE 1M AC Characteristics

Table 16. BLE\_1M - Recommended operating conditions

| Parameter       | Symbol             | Test conditions | Min  | Typ | Max  | Unit |
|-----------------|--------------------|-----------------|------|-----|------|------|
| f <sub>CH</sub> | Channel frequency  | In 2 MHz steps  | 2402 |     | 2480 | MHz  |
| N <sub>CH</sub> | Number of channels |                 |      | 40  |      | 1    |

Table 17. BLE\_1M - AC characteristics

| Parameter               | Symbol            | Test conditions                                                                                                              | Min | Typ | Max | Unit |
|-------------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| P <sub>SENS_CLEAN</sub> | Sensitivity level | Dirty Transmitter disabled;<br>clean power supply; PER = 30.8%<br><a href="#">Note 1</a><br><a href="#">Note 2</a>           |     | -99 |     | dBm  |
| P <sub>SENS</sub>       | Sensitivity level | Normal Operating Conditions;<br>DC-DC converter disabled;<br>PER = 30.8%<br><a href="#">Note 1</a><br><a href="#">Note 2</a> |     | -97 |     | dBm  |
| P <sub>SENS_EPKT</sub>  | Sensitivity level | Extended packet size (255 octets)                                                                                            |     | -94 |     | dBm  |

| Parameter              | Symbol                               | Test conditions                                                                            | Min | Typ | Max | Unit |
|------------------------|--------------------------------------|--------------------------------------------------------------------------------------------|-----|-----|-----|------|
|                        |                                      | Note 1<br>Note 2                                                                           |     |     |     |      |
| P <sub>O_MAX_HPA</sub> | Maximum output power level using HPA |                                                                                            |     | 12  |     | dBm  |
| P <sub>O_MAX_LPA</sub> | Maximum output power level using LPA |                                                                                            |     | 4   |     | dBm  |
| P <sub>O_STP_HPA</sub> | Output power step size for HPA       | Output power level in +4 dBm to +12 dBm range                                              |     | 0.5 |     | dB   |
| P <sub>O_STP_LPA</sub> | Output power step size for LPA       | Output power level in -20 dBm to +4 dBm range;<br>1 dB step size in -4 dBm to +4 dBm range |     | 1   | 6   | dB   |
| P <sub>O_MIN</sub>     | Minimum output power level           |                                                                                            |     | -54 |     | dBm  |

**Note 1** Up to 5 dB degradation when f<sub>CH</sub> is XTAL40M harmonic.

**Note 2** Measured according to Bluetooth Low Energy Test Specification RFPHY.TS.

### 5.10.3 LE 2M AC Characteristics

Table 18. BLE\_2M - Recommended operating conditions

| Parameter       | Symbol             | Test conditions | Min  | Typ | Max  | Unit |
|-----------------|--------------------|-----------------|------|-----|------|------|
| f <sub>CH</sub> | Channel frequency  | In 2 MHz steps  | 2402 |     | 2480 | MHz  |
| N <sub>CH</sub> | Number of channels |                 |      | 40  |      | 1    |

Table 19. BLE\_2M - AC characteristics

| Parameter               | Symbol                               | Test conditions                                                                              | Min | Typ | Max | Unit |
|-------------------------|--------------------------------------|----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| P <sub>SENS_CLEAN</sub> | Sensitivity level                    | Dirty Transmitter disabled;<br>clean power supply; PER = 30.8%<br>Note 1<br>Note 2           |     | -97 |     | dBm  |
| P <sub>SENS</sub>       | Sensitivity level                    | Normal Operating Conditions;<br>DC-DC converter disabled;<br>PER = 30.8%<br>Note 1<br>Note 2 |     | -96 |     | dBm  |
| P <sub>SENS_EPKT</sub>  | Sensitivity level                    | Extended packet size (255 octets)<br>Note 1<br>Note 2                                        |     | -94 |     | dBm  |
| P <sub>O_MAX_HPA</sub>  | Maximum output power level using HPA |                                                                                              |     | 12  |     | dBm  |
| P <sub>O_MAX_LPA</sub>  | Maximum output power level using LPA |                                                                                              |     | 4   |     | dBm  |
| P <sub>O_STP_HPA</sub>  | Output power step size for HPA       | Output power level in +4 dBm to +12 dBm range                                                |     | 0.5 |     | dB   |

| Parameter              | Symbol                         | Test conditions                                                                            | Min | Typ | Max | Unit |
|------------------------|--------------------------------|--------------------------------------------------------------------------------------------|-----|-----|-----|------|
| P <sub>O_STP_LPA</sub> | Output power step size for LPA | Output power level in -20 dBm to +4 dBm range;<br>1 dB step size in -4 dBm to +4 dBm range |     | 1   | 6   | dB   |
| P <sub>O_MIN</sub>     | Minimum output power level     |                                                                                            |     | -54 |     | dBm  |

**Note 1** Up to 4 dB degradation when f<sub>CH</sub> is XTAL40M harmonic.

**Note 2** Measured according to Bluetooth Low Energy Test Specification RFPHY.TS.

#### 5.10.4 BR 1M AC Characteristics

Table 20. BT\_BR\_1M - Recommended operating conditions

| Parameter       | Symbol             | Test conditions | Min  | Typ | Max  | Unit |
|-----------------|--------------------|-----------------|------|-----|------|------|
| f <sub>CH</sub> | Channel frequency  | In 1 MHz steps  | 2402 |     | 2480 | MHz  |
| N <sub>CH</sub> | Number of channels |                 |      | 79  |      | 1    |

Table 21. BT\_BR\_1M - AC characteristics

| Parameter               | Symbol                               | Test conditions                                                                                                                                            | Min | Typ | Max | Unit |
|-------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| P <sub>SENS_CLEAN</sub> | Sensitivity level                    | Dirty Transmitter disabled;<br>clean power supply; BER = 0.1%; 1.6M DH1 packets<br><a href="#">Note 1</a><br><a href="#">Note 2</a>                        |     | -96 |     | dBm  |
| P <sub>SENS</sub>       | Sensitivity level                    | Normal Operating Conditions;<br>DC-DC converter disabled;<br>BER = 0.1%; 1.6M DH1 packets<br><a href="#">Note 1</a><br><a href="#">Note 2</a>              |     | -94 |     | dBm  |
| P <sub>SENS_EPKT</sub>  | Sensitivity level                    | Dirty Transmitter disabled; DC-DC converter disabled; BER = 0.1%; Multi-slot packets; 1.6M DH5 packets<br><a href="#">Note 1</a><br><a href="#">Note 2</a> |     | -96 |     | dBm  |
| P <sub>O_MAX_HPA</sub>  | Maximum output power level using HPA |                                                                                                                                                            |     | 12  |     | dBm  |
| P <sub>O_MAX_LPA</sub>  | Maximum output power level using LPA |                                                                                                                                                            |     | 4   |     | dBm  |
| P <sub>O_MIN</sub>      | Minimum output power level           |                                                                                                                                                            |     | -30 |     | dBm  |
| P <sub>O_STP</sub>      | Output power step size               |                                                                                                                                                            | 2   | 3   | 6   | dB   |

**Note 1** Up to 3 dB degradation when f<sub>CH</sub> is XTAL40M harmonic.

**Note 2** Measured according to Bluetooth® Test Specification RF.TS.

#### 5.10.5 EDR 2M AC Characteristics

Table 22. BT\_EDR\_2M - Recommended operating conditions

| Parameter       | Symbol            | Test conditions | Min  | Typ | Max  | Unit |
|-----------------|-------------------|-----------------|------|-----|------|------|
| f <sub>CH</sub> | Channel frequency | In 1 MHz steps  | 2402 |     | 2480 | MHz  |

| Parameter       | Symbol             | Test conditions | Min | Typ | Max | Unit |
|-----------------|--------------------|-----------------|-----|-----|-----|------|
| N <sub>CH</sub> | Number of channels |                 |     | 79  |     | 1    |

Table 23. BT\_EDR\_2M - AC characteristics

| Parameter               | Symbol                               | Test conditions                                                                                                        | Min | Typ   | Max | Unit |
|-------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------|
| P <sub>SENS_CLEAN</sub> | Sensitivity level                    | Dirty Transmitter disabled; DC-DC converter disabled; BER = 0.01%<br><a href="#">Note 1</a><br><a href="#">Note 2</a>  |     | -94   |     | dBm  |
| P <sub>SENS</sub>       | Sensitivity level                    | Normal Operating Conditions; DC-DC converter disabled; BER = 0.01%<br><a href="#">Note 1</a><br><a href="#">Note 2</a> |     | -93.5 |     | dBm  |
| P <sub>O_MAX_HPA</sub>  | Maximum output power level using HPA | <a href="#">Note 3</a>                                                                                                 |     | 9     |     | dBm  |
| P <sub>O_MIN</sub>      | Minimum output power level           |                                                                                                                        |     | -30   |     | dBm  |
| P <sub>O_STP</sub>      | Output power step size               |                                                                                                                        | 2   | 3     | 6   | dB   |

**Note 1** Up to 4 dB degradation when f<sub>CH</sub> is XTAL40M harmonic.

**Note 2** Measured according to Bluetooth® Test Specification RF.TS.

**Note 3** Needs careful board design to minimize impact of cross-talk.

### 5.10.6 EDR 3M AC Characteristics

Table 24. BT\_EDR\_3M - Recommended operating conditions

| Parameter       | Symbol             | Test conditions | Min  | Typ | Max  | Unit |
|-----------------|--------------------|-----------------|------|-----|------|------|
| f <sub>CH</sub> | Channel frequency  | In 1 MHz steps  | 2402 |     | 2480 | MHz  |
| N <sub>CH</sub> | Number of channels |                 |      | 79  |      | 1    |

Table 25. BT\_EDR\_3M - AC characteristics

| Parameter               | Symbol                               | Test conditions                                                                                                        | Min | Typ | Max | Unit |
|-------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| P <sub>SENS_CLEAN</sub> | Sensitivity level                    | Dirty Transmitter disabled; DC-DC converter disabled; BER = 0.01%<br><a href="#">Note 1</a><br><a href="#">Note 2</a>  |     | -87 |     | dBm  |
| P <sub>SENS</sub>       | Sensitivity level                    | Normal Operating Conditions; DC-DC converter disabled; BER = 0.01%<br><a href="#">Note 1</a><br><a href="#">Note 2</a> |     | -85 |     | dBm  |
| P <sub>O_MAX_HPA</sub>  | Maximum output power level using HPA | <a href="#">Note 3</a>                                                                                                 |     | 9   |     | dBm  |
| P <sub>O_MIN</sub>      | Minimum output power level           |                                                                                                                        |     | -30 |     | dBm  |
| P <sub>O_STP</sub>      | Output power step size               |                                                                                                                        | 2   | 3   | 6   | dB   |

**Note 1** Up to 3 dB degradation when f<sub>CH</sub> is XTAL40M harmonic.

**Note 2** Measured according to Bluetooth® Test Specification RF.TS.

**Note 3** Needs careful board design to minimize impact of cross-talk.

## 5.11 XTAL 40M Characteristics

**Table 26. 40M xtal oscillator - Absolute maximum ratings**

| Parameter            | Description            | Conditions                                                                  | Min | Max  | Unit |
|----------------------|------------------------|-----------------------------------------------------------------------------|-----|------|------|
| V <sub>CLK_EXT</sub> | External clock voltage | With external clock source on XTAL40M_P (XTAL40M_N can be connected to VSS) | 0.1 | 0.88 | V    |

**Table 27. 40M xtal oscillator - Absolute maximum ratings**

| Parameter            | Description                                            | Conditions                                                | Min | Max  | Unit |
|----------------------|--------------------------------------------------------|-----------------------------------------------------------|-----|------|------|
| f <sub>XTAL</sub>    | Crystal oscillator frequency                           |                                                           |     | 40   |      |
| C <sub>L</sub>       | Load capacitance                                       | No external capacitors are required                       | 4   | 6    | 7    |
| ESR                  | Equivalent series resistance                           |                                                           |     | 35   | 100  |
| C <sub>0</sub>       | Shunt capacitance                                      |                                                           |     | 0.65 | 3    |
| Δf <sub>XTAL_T</sub> | Crystal frequency variation over temperature and aging | Relative to frequency at 25 °C during production          | -15 |      | 15   |
| Φ <sub>N_EXT</sub>   | Phase noise                                            | f <sub>c</sub> = 50 kHz; in case of external clock source |     |      | -130 |
| f <sub>XTAL</sub>    | Crystal oscillator frequency                           |                                                           |     | 40   |      |

**Table 28. 40M xtal oscillator - DC characteristics**

| Parameter               | Description                                       | Conditions                                                                                                                         | Min | Max | Unit |
|-------------------------|---------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| I <sub>SUP_32kHz</sub>  | VDDRF supply current low power 32 kHz mode        |                                                                                                                                    |     | 50  |      |
| I <sub>SUP_ACTIVE</sub> | VDDRF supply current including part of clock tree | Startup completed, recommended setting, buffer enabled but clock not used (current consumption is including load of clock-buffer). |     | 160 |      |

**Table 29. 40M xtal oscillator - Timing characteristics**

| Parameter                 | Description                                            | Conditions          | Min | Max   | Unit |
|---------------------------|--------------------------------------------------------|---------------------|-----|-------|------|
| t <sub>STA_XTAL+LDO</sub> | Crystal oscillator startup time, including LDO startup | Until OK bit is set |     | 0.015 | 0.06 |

## 5.12 GPIO Pads Characteristics

**Table 30. IO\_pad - Recommended operating conditions**

| Parameter       | Description               | Conditions          | Min                       | Max | Unit                      |
|-----------------|---------------------------|---------------------|---------------------------|-----|---------------------------|
| C <sub>L</sub>  | External load capacitance |                     |                           |     | 15                        |
| V <sub>IH</sub> | High-level input voltage  | VDDIO = 1.2 - 1.8 V | 0.7*V <sub>D</sub><br>DIO |     |                           |
| V <sub>IL</sub> | Low-level input voltage   | VDDIO = 1.2 - 1.8 V |                           |     | 0.3*V <sub>D</sub><br>DIO |

Table 31. IO\_pad - DC characteristics (TBD)

| Parameter              | Description               | Conditions                           | Min                    | Max  | Unit                   |
|------------------------|---------------------------|--------------------------------------|------------------------|------|------------------------|
| V <sub>IH</sub>        | High-level input voltage  | VDDIO=1.8 V                          | 0.7*V <sub>D</sub> DIO |      |                        |
| V <sub>IL</sub>        | Low-level input voltage   | VDDIO=1.8 V                          |                        |      | 0.3*V <sub>D</sub> DIO |
| V <sub>OH</sub>        | High-level output voltage | I <sub>O</sub> =4 mA, VDDIO=1.8 V    | 0.8*V <sub>D</sub> DIO |      |                        |
| V <sub>OL</sub>        | Low-level output voltage  | I <sub>O</sub> =4 mA, VDDIO=1.8 V    |                        |      | 0.2*V <sub>D</sub> DIO |
| V <sub>OH_LOWDRV</sub> | High-level output voltage | I <sub>O</sub> =0.66 mA, VDDIO=1.8 V | 0.8*V <sub>D</sub> DIO |      |                        |
| V <sub>OL_LOWDRV</sub> | Low-level output voltage  | I <sub>O</sub> =0.66 mA, VDDIO=1.8 V |                        |      | 0.2*V <sub>D</sub> DIO |
| C <sub>IN</sub>        | Input capacitance         |                                      |                        | 0.75 |                        |
| R <sub>PD</sub>        | Pull-down resistance      |                                      | 17                     | 25   | 35                     |
| R <sub>PU</sub>        | Pull-up resistance        |                                      | 17                     | 25   | 35                     |

Table 32. QSPI Pads Characteristics

| Parameter | Description | Conditions | Min | Max | Unit |
|-----------|-------------|------------|-----|-----|------|
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |
|           |             |            |     |     |      |

## 6. Codec Section

The DA7414 stereo codec exists only in DA14870SF01 variant of the module.

### 6.1 Input path characteristics

Table 33: System Inputs

| Parameter                     | Description                                                                        | Conditions                                                                         | Min | Typ  | Max | Unit       |
|-------------------------------|------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----|------|-----|------------|
| <b>Electrical performance</b> |                                                                                    |                                                                                    |     |      |     |            |
| <b>Differential Input</b>     |                                                                                    |                                                                                    |     |      |     |            |
| $V_{IN\_DIFF}$                | Full-scale differential input signal on microphone input<br><a href="#">Note 1</a> | Peak-to-peak                                                                       |     | 2.88 |     | V          |
| $DR_{DIFF}$                   | Dynamic range (MUS)<br><a href="#">Note 2</a>                                      | MUS path, differential input, DRE enabled<br><a href="#">Note 3</a>                |     | 110  |     | dB         |
| $DR_{DIFF\_ANC}$              | Dynamic range (ANC)<br><a href="#">Note 2</a>                                      | ANC path, differential input<br><a href="#">Note 3</a>                             |     | 95   |     | dB         |
| $THD+N_{DIFF}$                | Total harmonic distortion plus noise<br><a href="#">Note 4</a>                     | Input signal = -1 dBFS                                                             |     | -85  |     | dB         |
| <b>Single-ended Input</b>     |                                                                                    |                                                                                    |     |      |     |            |
| $V_{IN}$                      |                                                                                    | Peak-to-peak                                                                       |     | 1.44 |     | V          |
| DR                            |                                                                                    | MUS path, single-ended input, DRE enabled<br><a href="#">Note 3</a>                |     | 105  |     | dB         |
| $DR_{ANC}$                    |                                                                                    | ANC path, single-ended input<br><a href="#">Note 3</a>                             |     | 95   |     | dB         |
| THD+N                         |                                                                                    | Input signal = -1 dBFS                                                             |     | -85  |     | dB         |
| <b>Any Input</b>              |                                                                                    |                                                                                    |     |      |     |            |
| XTLK                          | Channel-to-channel crosstalk                                                       | One channel input = -1 dBFS<br>Other channel input = mute<br>Both channels enabled |     | 100  |     | dB         |
| $PSRR_{217Hz}$                | Power supply rejection ratio from VDDA to the ADC outputs                          | Measured at 217 Hz                                                                 |     | 60   |     | dB         |
| $PSRR_{1kHz}$                 | Power supply rejection ratio from VDDA to the ADC outputs                          | Measured at 1 kHz                                                                  |     | 60   |     | dB         |
| $PSRR_{20kHz}$                | Power supply rejection ratio from VDDA to the ADC outputs                          | Measured at 20 kHz                                                                 |     | 50   |     | dB         |
| $V_{N\_IN}$                   | Input referred noise level                                                         | RMS, A-weighted, analog gain = 30 dB                                               |     | 3    | 5   | $\mu V$    |
| $Z_{IN}$                      | Input impedance                                                                    |                                                                                    |     | 10   |     | k $\Omega$ |
| $A_{RNG}$                     | Analog gain range                                                                  |                                                                                    | 0   |      | 30  | dB         |
| $A_{STP}$                     | Analog gain step                                                                   |                                                                                    |     | 6    |     | dB         |

**Note 1**  $V_{IN}$  yields 0 dBFS at the DAI output, when the path gain = 0 dB.

**Note 2** DR is a ratio of the full-scale signal  $V_{IN}$  to the integrated noise in the presence of a -60 dBFS, 997 Hz input signal.

**Note 3** A-weighted, input signal = -60 dBFS, input frequency = 997 Hz, PGA gain = 0 dB.

**Note 4** THD+N is the integrated noise plus distortion level relative to the given reference signal level

**Table 34: Digital Input Filters (Standard)**

| Parameter                     | Description          | Conditions | Min  | Typ    | Max | Unit    |
|-------------------------------|----------------------|------------|------|--------|-----|---------|
| <b>Electrical Performance</b> |                      |            |      |        |     |         |
| $f_{PB\_48kHz}$               | Passband frequency   | SSR=48kHz  |      | 21600  |     | Hz      |
| $f_{PB\_192kHz}$              | Passband frequency   | SSR=192kHz |      | 67200  |     | Hz      |
| $ARPL\_PB$                    | Passband gain ripple |            | -0.1 |        | 0.1 | dB      |
| $f_{SB\_48kHz}$               | Stopband frequency   | SSR=48kHz  |      | 26400  |     | Hz      |
| $f_{SB\_192kHz}$              | Stopband frequency   | SSR=192kHz |      | 134400 |     | Hz      |
| $ASB\_48kHz$                  | Stopband attenuation | SSR=48kHz  |      | 66     |     | dB      |
| $ASB\_192kHz$                 | Stopband attenuation | SSR=192kHz |      | 41     |     | dB      |
| $t_{D\_GRP\_48kHz}$           | Group delay          | SSR=48kHz  |      | 5      |     | Samples |
| $t_{D\_GRP\_192kHz}$          | Group delay          | SSR=192kHz |      | 5      |     | Samples |

Table 35: Digital Input Filters (Low Latency)

| Parameter                     | Description                          | Conditions                                         | Min   | Typ   | Max   | Unit |
|-------------------------------|--------------------------------------|----------------------------------------------------|-------|-------|-------|------|
| <b>Electrical performance</b> |                                      |                                                    |       |       |       |      |
| f <sub>CLK_DMIC</sub>         | DMIC clock frequency                 |                                                    | 0.768 |       | 6.144 | MHz  |
| f <sub>PB</sub>               | Passband frequency                   | -3 dB cut off                                      |       | 108   |       | kHz  |
| ARPL_PB                       | Passband ripple                      |                                                    | -0.5  | 0.1   | 0.5   | dB   |
| f <sub>SB_CUT_OFF</sub>       | Stopband cut-off frequency           |                                                    |       | 163   |       | kHz  |
| A <sub>SB</sub>               | Stopband attenuation                 |                                                    |       | 80    |       | dB   |
| t <sub>D_GRP</sub>            | Group delay                          | f <sub>CLK_DMIC</sub> =3.072MHz                    |       | 6.52  |       | μs   |
| t <sub>D_GRP</sub>            | Group delay                          | f <sub>CLK_DMIC</sub> =2.4576MHz                   |       | 6.88  |       | μs   |
| t <sub>D_GRP</sub>            | Group delay                          | f <sub>CLK_DMIC</sub> =1.536MHz                    |       | 6.03  |       | μs   |
| t <sub>D_GRP</sub>            | Group delay                          | f <sub>CLK_DMIC</sub> =0.768MHz                    |       | 5.05  |       | μs   |
| DR                            | Dynamic range                        | Input=-60dBFS<br>f <sub>CLK_DMIC</sub> = 3.072MHz  |       | 105.7 |       | dB   |
| DR                            | Dynamic range                        | Input=-60dBFS<br>f <sub>CLK_DMIC</sub> = 2.4576MHz |       | 104.7 |       | dB   |
| DR                            | Dynamic range                        | Input=-60dBFS<br>f <sub>CLK_DMIC</sub> = 1.536MHz  |       | 86.5  |       | dB   |
| DR                            | Dynamic range                        | Input=-60dBFS<br>f <sub>CLK_DMIC</sub> = 0.768MHz  |       | 60.3  |       | dB   |
| THD+N                         | Total harmonic distortion plus noise | Input=-7dBFS<br>f <sub>CLK_DMIC</sub> = 3.072MHz   |       | -86.3 |       | dB   |
| THD+N                         | Total harmonic distortion plus noise | Input=-7dBFS<br>f <sub>CLK_DMIC</sub> = 2.4576MHz  |       | -86   |       | dB   |
| THD+N                         | Total harmonic distortion plus noise | Input=-7dBFS<br>f <sub>CLK_DMIC</sub> = 1.536MHz   |       | -74   |       | dB   |
| THD+N                         | Total harmonic distortion plus noise | Input=-7dBFS<br>f <sub>CLK_DMIC</sub> = 0.768MHz   |       | -43.5 |       | dB   |
| FS <sub>IN</sub>              | Full scale input signal              | All except 2.4576 MHz (-6 dB)                      |       | 0     |       | dB   |

## 6.2 Output path characteristics

Table 36: System Outputs

| Parameter                             | Description                                       | Conditions                                                                                                                 | Min | Typ  | Max   | Unit |
|---------------------------------------|---------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-----|------|-------|------|
| <b>External electrical conditions</b> |                                                   |                                                                                                                            |     |      |       |      |
| R <sub>HP_LD</sub>                    | Headphone output load resistance, per output      |                                                                                                                            | 12  | 32   | 10000 | Ω    |
| C <sub>HP_LD</sub>                    | Headphone output load capacitance, per output     |                                                                                                                            | 0   |      | 250   | pF   |
| L <sub>HP_LD</sub>                    | Headphone output load inductance, per output      |                                                                                                                            |     |      | 400   | μH   |
| <b>Electrical performance</b>         |                                                   |                                                                                                                            |     |      |       |      |
| V <sub>OUT</sub>                      | Full-scale differential HP output signal level    | V <sub>DDHP</sub> = 1.8 V<br>RMS                                                                                           |     | 1    |       | V    |
| V <sub>OUT_OFS</sub>                  | Output dc offset                                  | V <sub>DDHP</sub> = 1.8 V                                                                                                  |     | 100  |       | μV   |
| V <sub>N_OUT_24dB</sub>               | Output noise                                      | RMS<br>V <sub>{DDHP}</sub> = 1.8 V<br>HPPGA gain ≤ -24 dB<br>Input < -60 dBFS<br>A-weighted<br>R <sub>{HP_LD}</sub> = 32 Ω |     | 1.7  |       | μV   |
| DR                                    | Dynamic range                                     | V <sub>{DDHP}</sub> = 1.8 V<br>HPPGA gain = -24 dB to 0 dB<br>20 Hz to 20 kHz, A-weighted<br>1 kHz -60 dBFS output         |     | 115  |       | dB   |
| THD+N <sub>1dbFS</sub>                | Total harmonic distortion plus noise              | V <sub>{DDHP}</sub> = 1.8 V<br>HPPGA gain = 0 dB<br>Input 1 kHz @ -1 dBFS                                                  |     | -90  |       | dB   |
| THD+N <sub>20dBFS</sub>               | Total harmonic distortion plus noise              | V <sub>{DDHP}</sub> = 1.8 V<br>HPPGA gain = 0 dB<br>Input 1 kHz at -20 dBFS                                                |     | -100 |       | dB   |
| P <sub>OUT</sub>                      | Headphone driver load power, per output           | V <sub>{DDHP}</sub> = 1.8 V<br>THD+N ≤ 0.1 %                                                                               |     | 30   |       | mW   |
| AR <sub>PL</sub>                      | Output path gain ripple                           | HPPGA gain = -24 dB to 0 dB                                                                                                |     | ±0.5 |       | dB   |
| AR <sub>NG</sub>                      | Output path analog gain range                     |                                                                                                                            | -24 |      | 0     | dB   |
| A <sub>STP</sub>                      | Output path analog gain step                      |                                                                                                                            |     | 6    |       | dB   |
| PSRR <sub>217Hz</sub>                 | Power supply rejection from VDDA to the HP output | V <sub>{DDHP}</sub> = 1.8 V<br>Measured at 217 Hz                                                                          |     | 75   |       | dB   |
| PSRR <sub>1kHz</sub>                  | Power supply rejection from VDDA to the HP output | V <sub>DDHP</sub> = 1.8 V<br>Measured at 1 kHz                                                                             |     | 75   |       | dB   |
| PSRR <sub>20kHz</sub>                 | Power supply rejection from VDDA to the HP output | V <sub>{DDHP}</sub> = 1.8 V<br>Measured at 20 kHz                                                                          |     | 65   |       | dB   |
| XTLK                                  | HP-to-HP channel-to-channel crosstalk             | HPPGA gain = 0 dB<br>-1 dBFS output from aggressor and<br>-120 dBFS output from victim                                     |     | -100 |       | dB   |

Table 37: Digital Output Filters

| Parameter                     | Description                | Conditions                                 | Min   | Typ | Max  | Unit |
|-------------------------------|----------------------------|--------------------------------------------|-------|-----|------|------|
| <b>Electrical performance</b> |                            |                                            |       |     |      |      |
| f <sub>PB_48kHz</sub>         | Passband frequency         | SSR = 48 kHz                               | 20000 |     |      | Hz   |
| AR <sub>PL_PB_48kHz</sub>     | Passband ripple            | SSR = 48 kHz<br>Input = 20 Hz to 0.4166*fs |       |     | 0.11 | dB   |
| f <sub>SB_CUT_OFF_48kHz</sub> | Stopband cut-off frequency | SSR = 48 kHz                               | 27800 |     |      | Hz   |
| A <sub>SB_48kHz</sub>         | Stopband attenuation       | SSR = 48 kHz                               | 87    |     |      | dB   |

|                                |                            |                                             |        |       |      |    |
|--------------------------------|----------------------------|---------------------------------------------|--------|-------|------|----|
| t <sub>D_GRP_48kHz</sub>       | Group delay                | SSR = 48 kHz<br>Input = 1 kHz               |        |       | 58   | μs |
| f <sub>PB_192kHz</sub>         | Passband frequency         | SSR = 192 kHz                               | 55000  |       |      | Hz |
| ARPL_PB_192kHz                 | Passband ripple            | SSR = 192 kHz<br>Input = 20 Hz to 0.2864*fs |        |       | 0.01 | dB |
| f <sub>SB_CUT_OFF_192kHz</sub> | Stopband cut-off frequency | SSR = 192 kHz                               | 168000 |       |      | Hz |
| ASB_192kHz                     | Stopband attenuation       | SSR = 192 kHz                               | 90     |       |      | dB |
| t <sub>D_GRP_192kHz</sub>      | Group delay                | SSR = 192 kHz<br>Input = 1 kHz              |        |       | 6.7  | μs |
| ADIG_RNG                       | Digital gain range         |                                             | -77.25 |       | 18   | dB |
| ADIG_STP                       | Digital gain step          |                                             |        | 0.375 |      | dB |

### 6.3 Microphone bias characteristics

Table 38: Micbias Supply

| Parameter                      | Description                                         | Conditions                                                                   | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------------------------|------------------------------------------------------------------------------|-----|-----|-----|------|
| External electrical conditions |                                                     |                                                                              |     |     |     |      |
| C <sub>LD</sub>                | Load capacitance                                    |                                                                              |     | 1   |     | μF   |
| I <sub>LD</sub>                | Load current                                        |                                                                              |     |     | 2   | mA   |
| Electrical performance         |                                                     |                                                                              |     |     |     |      |
| V <sub>MICBIAS</sub>           | Output voltage                                      | Programmable in eight steps (1.2, 1.4, 1.6, 1.8, 2.16, 2.4, 2.7, 2.98) V     | 1.2 |     | 3   | V    |
| V <sub>N_OUT</sub>             | Noise voltage at MICBIAS1/MICBIAS2                  | RMS, A-weighted (20 Hz – 20 kHz), VDDMB = 3.3 V, VMICBIAS1/VMICBIAS2 = 2.2 V |     | 5   |     | μV   |
| PSRR <sub>VDDMB_217Hz</sub>    | power supply rejection ratio to VDDMB               | At f = 217 Hz, VMICBIAS1 /VMICBIAS2 = 2.2 V, Load = 2 mA                     |     | 75  |     | dB   |
| PSRR <sub>VDDMB_1kHz</sub>     | power supply rejection ratio to V <sub>{DDMB}</sub> | At f = 1kHz, VMICBIAS1 /VMICBIAS2 = 2.2V, Load = 2 mA                        |     | 75  |     | dB   |
| PSRR <sub>VDDMB_20kHz</sub>    | power supply rejection ratio to V <sub>{DDMB}</sub> | At f = 20 kHz, VMICBIAS1 /VMICBIAS2 = 2.2 V, Load = 2 mA                     |     | 60  |     | dB   |

### 6.4 System characteristics

Table 39: System Signal Latencies

| Parameter              | Description                    | Conditions                            | Min | Typ | Max | Unit |
|------------------------|--------------------------------|---------------------------------------|-----|-----|-----|------|
| Timing characteristics |                                |                                       |     |     |     |      |
| t <sub>DMIC_DSP</sub>  | DMIC to HP latency via DSP     | SSR = 192 kHz<br>From DMIC to HP pins |     | 25  |     | μs   |
| t <sub>AMIC_DSP</sub>  | AMIC to HP latency via DSP     | SSR = 192 kHz<br>From AMIC to HP pins |     | 25  |     | μs   |
| t <sub>DMIC_FEQ</sub>  | DMIC to HP latency via FEQ     | From DMIC to HP pins                  |     | 5.2 |     | μs   |
| t <sub>AMIC_FEQ</sub>  | AMIC to HP latency via FEQ     | From AMIC to HP pins                  |     | 5.5 |     | μs   |
| t <sub>DMIC_ANC</sub>  | DMIC to HP latency via ANC DSP | SSR = 192 kHz<br>From MIC to HP pins  |     | 25  |     | μs   |

|                       |                                      |                                                                 |  |    |  |    |
|-----------------------|--------------------------------------|-----------------------------------------------------------------|--|----|--|----|
| t <sub>AMIC_ANC</sub> | AMIC to HP latency via<br>ANC<br>DSP | SSR = 192 kHz<br>f <sub>IN</sub> = 1 kHz<br>From MIC to HP pins |  | 25 |  | μs |
|-----------------------|--------------------------------------|-----------------------------------------------------------------|--|----|--|----|

Table 40: Power Consumption

| Parameter                         | Description                                                           | Conditions                                                                                                    | Min | Typ | Max | Unit |
|-----------------------------------|-----------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| <b>Electrical performance</b>     |                                                                       |                                                                                                               |     |     |     |      |
| P <sub>Q_OFF</sub>                | Quiescent power in OFF                                                | EN pin = GND                                                                                                  |     | 20  |     | μW   |
| P <sub>Q_STANDBY</sub>            | Quiescent power in STANDBY                                            | EN pin = VDDIO                                                                                                |     | 260 |     | μW   |
| P <sub>Q_MONO_REC</sub>           | Mono microphone record power consumption                              | DMIC1 to DAI<br>Passthrough DSP profile<br>SRC disabled<br>LP_MODE_SET<x> = 1                                 |     | 2.9 |     | mW   |
| P <sub>Q_STEREO_REC</sub>         | Stereo microphone record power consumption                            | DMIC1 and DMIC2 to DAI<br>Passthrough DSP profile<br>SRC disabled<br>LP_MODE_SET<x> = 1                       |     | 4.3 |     | mW   |
| P <sub>Q_MONO_PLB</sub>           | Mono headphone playback, standard load, quiescent power consumption   | DAI to HP1, no signal<br>Note 1                                                                               |     | 4.3 |     | mW   |
| P <sub>Q_STEREO_PLB</sub>         | Stereo headphone playback, standard load, quiescent power consumption | DAI to HP1, no signal<br>Note 1                                                                               |     | 6.9 |     | mW   |
| P <sub>MONO_PLB_0.1mW</sub>       | Mono headphone 0.1 mW playback power consumption                      | DAI to HP1<br>P <sub>OUT</sub> = 0.1 mW<br>Note 1                                                             |     | 7   |     | mW   |
| P <sub>MONO_ANC_PLB_0.1mW</sub>   | Mono hybrid ANC 0.1 mW playback power consumption                     | DAI = MUS DSP = 48 kHz,<br>ANC DSP = 192 kHz<br>Hybrid ANC DSP profile<br>P <sub>OUT</sub> = 0.1 mW<br>Note 1 |     | 11  |     | mW   |
| P <sub>STEREO_ANC_PLB_0.1mW</sub> | Stereo hybrid ANC 0.1 mW playback power consumption                   | DAI = MUS DSP = 48 kHz,<br>ANC DSP = 192 kHz<br>Hybrid ANC DSP profile<br>P <sub>OUT</sub> = 0.1 mW<br>Note 1 |     | 18  |     | mW   |
| N <sub>PATH</sub>                 | Internal path width                                                   | All digital paths<br>From MIC to HP pins                                                                      |     | 24  |     | bits |

**Note 1** HP load = 32 Ω, SRC disabled, LP\_MODE\_SET<x> = 1, VDDA = VDDIO = 1.8 V, VDDD = 0.9V, VDDHP = 1.8 V.

## 7. Package Outline Drawings

RENESAS

### Package Outline Drawing

PSC-5180-01

ML0100AA

100-MODULE 14.1 x 21.5 x 2.70 mm Body, 1.27mm Pitch

Rev. 01, Sep 05, 2025

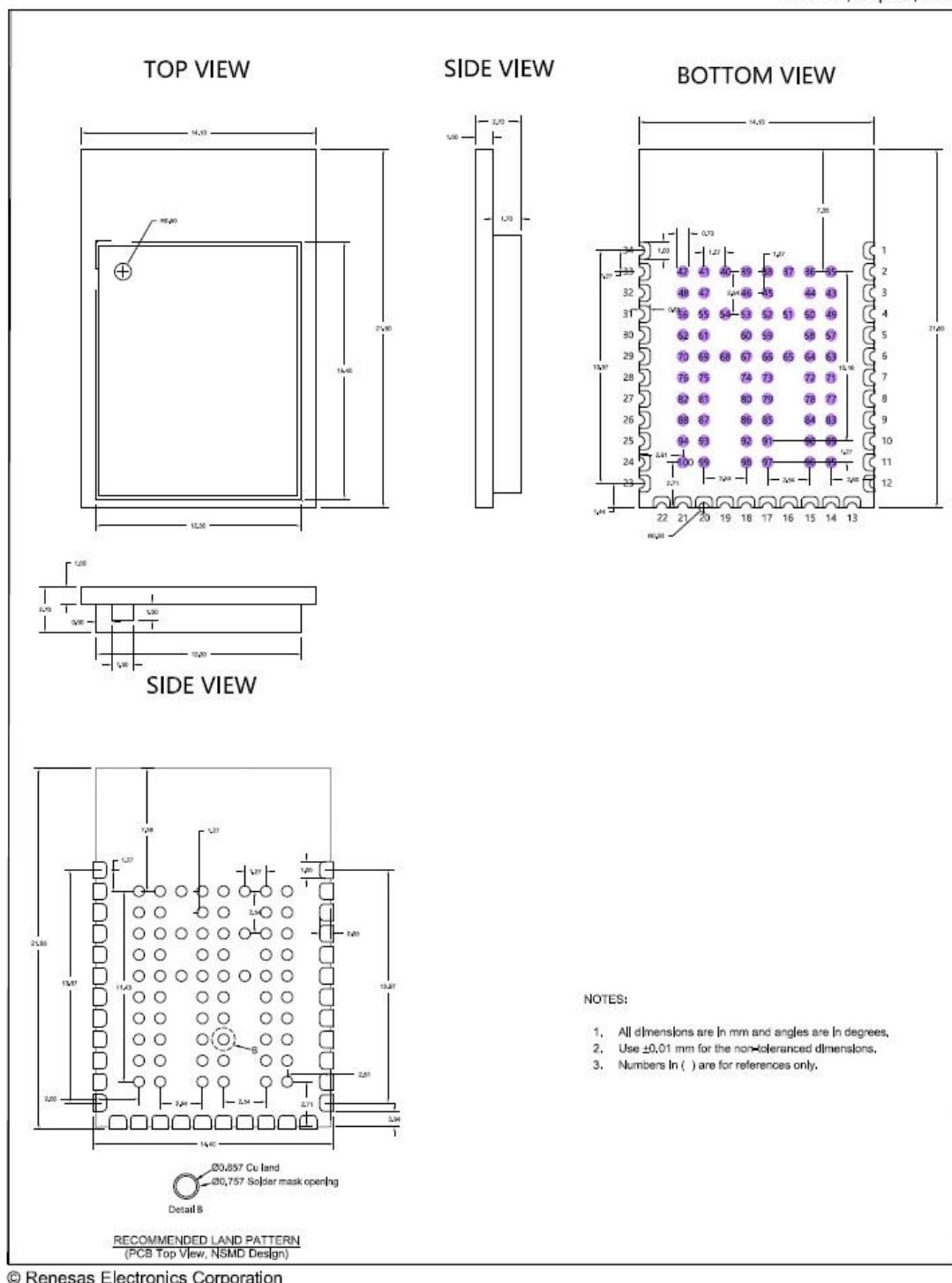


Figure 8. DA14870 Module package outline drawing

## 8. Design Guidelines

The DA14870MOD comes with an integrated PCB trace antenna. The antenna area is 14.1 x 6.1 mm. The antenna's Voltage Standing Wave Ratio (VSWR) and efficiency depend on the installation location. The radiation performance of the PCB trace antenna depends on the host PCB layout. The maximum antenna gain is 1.6 dBi when installed on a 89 x 35 mm reference board, as shown in Figure 8. Antenna Radiation Efficiency is better than -5.33 dB for all mounting positions. The RF front end is optimized to achieve the maximum possible efficiency for various installations positions of the module on a host PCB. To obtain similar performance, follow the guidelines described in the following subsections.

### 8.1 Installation Location

The DA14870MOD printed antenna performance is characterized in terms of Voltage Standing Wave Ratio (VSWR), antenna efficiency and radiation patterns, when the module is positioned at three locations; left, middle, and right on a reference test board with dimensions 89 x 35 mm, Figure 9.

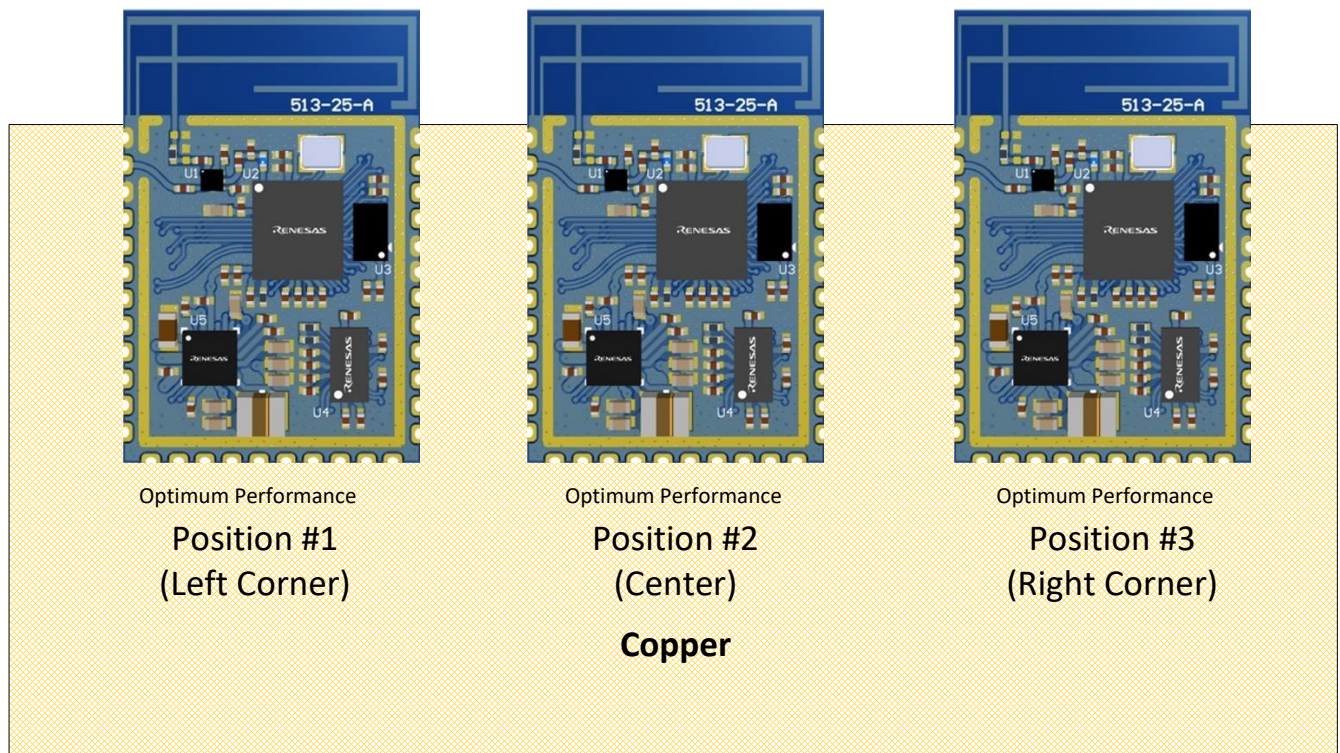


Figure 9: Installation Location

## 8.2 VSWR Measurements

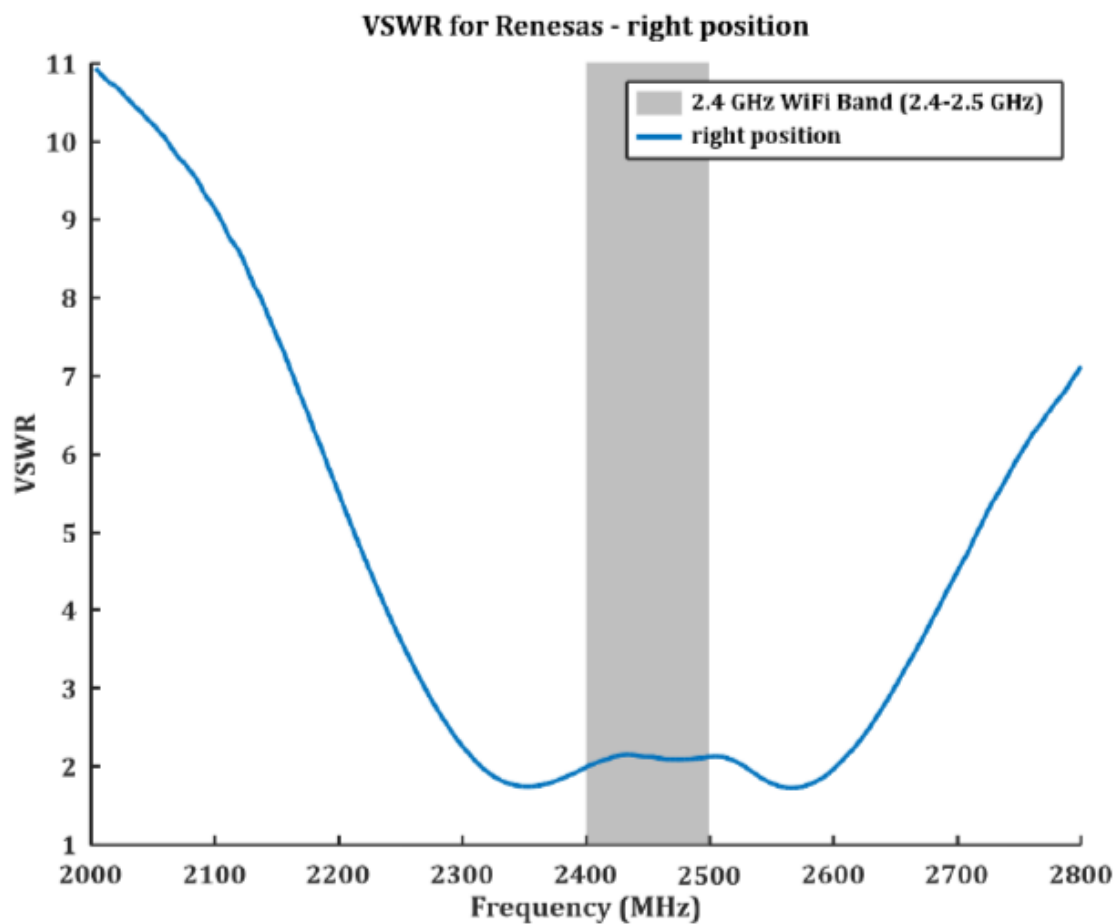


Figure 10: VSWR right position

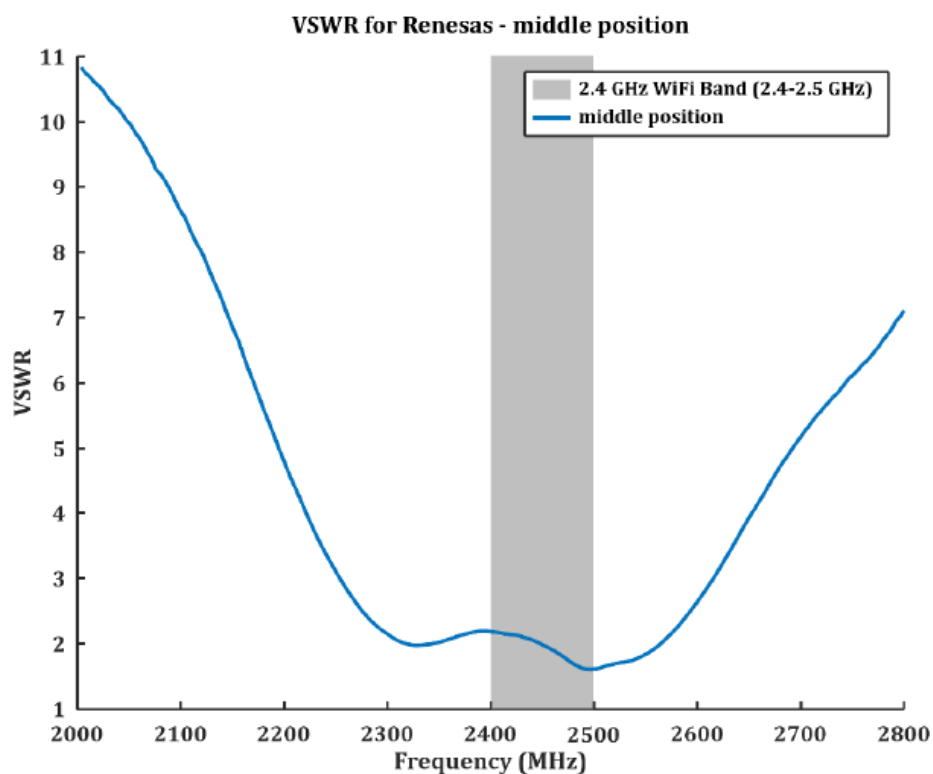


Figure 11: VSWR middle position

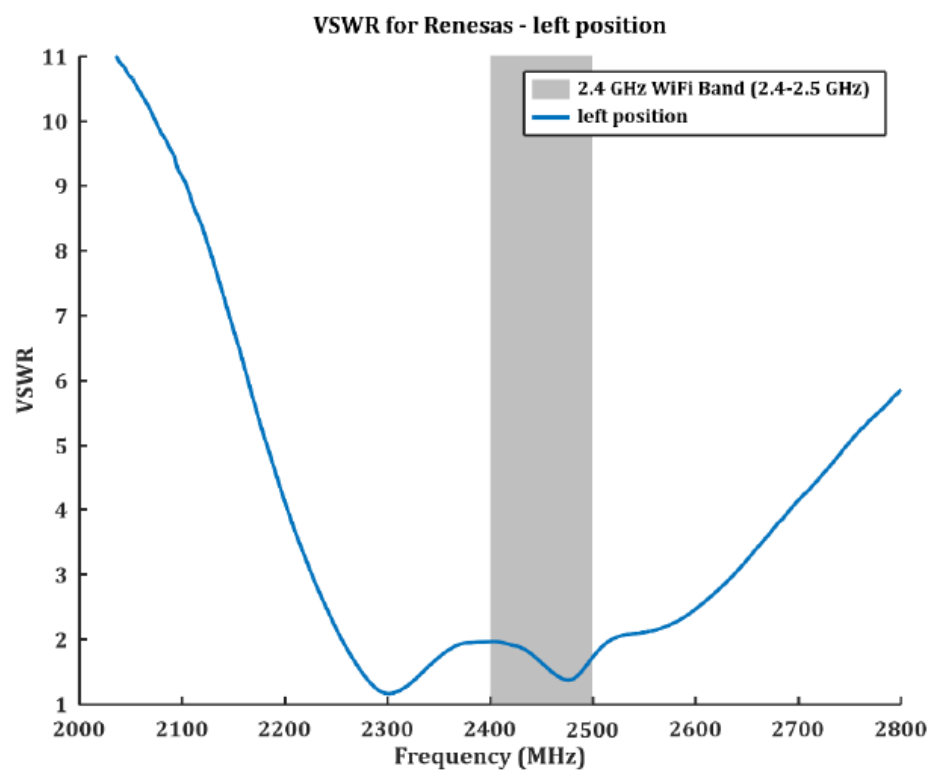


Figure 12: VSWR left position

### 8.3 Antenna Efficiency

| Frequency<br>[MHz] | Right position             | Middle position | Left position |
|--------------------|----------------------------|-----------------|---------------|
|                    | Antenna efficiency<br>[dB] |                 |               |
| 2400.00            | -2.58                      | -4.20           | -3.84         |
| 2405.00            | -2.57                      | -4.21           | -3.85         |
| 2410.00            | -2.65                      | -4.06           | -3.73         |
| 2415.00            | -2.74                      | -3.83           | -3.49         |
| 2420.00            | -2.77                      | -3.80           | -3.43         |
| 2425.00            | -2.78                      | -3.92           | -3.64         |
| 2430.00            | -2.78                      | -3.90           | -3.78         |
| 2435.00            | -2.81                      | -3.79           | -3.77         |
| 2440.00            | -3.04                      | -3.99           | -4.01         |
| 2445.00            | -3.10                      | -4.03           | -4.14         |
| 2450.00            | -3.10                      | -3.88           | -4.05         |
| 2455.00            | -3.09                      | -3.61           | -3.73         |
| 2460.00            | -3.18                      | -3.51           | -3.58         |
| 2465.00            | -3.41                      | -3.60           | -3.71         |
| 2470.00            | -3.80                      | -3.78           | -3.94         |
| 2475.00            | -4.30                      | -4.03           | -4.13         |
| 2480.00            | -4.79                      | -4.30           | -4.33         |
| 2485.00            | -5.33                      | -4.54           | -4.61         |

Figure 13: Antenna Efficiency

## 8.4 Radiation Pattern

The antenna radiation pattern measurements are carried out in a Satimo SG-23 6GHz Stargate Antenna Test Chamber. Radiation patterns are presented for three measurement planes: XY-, XZ- and YZ-planes

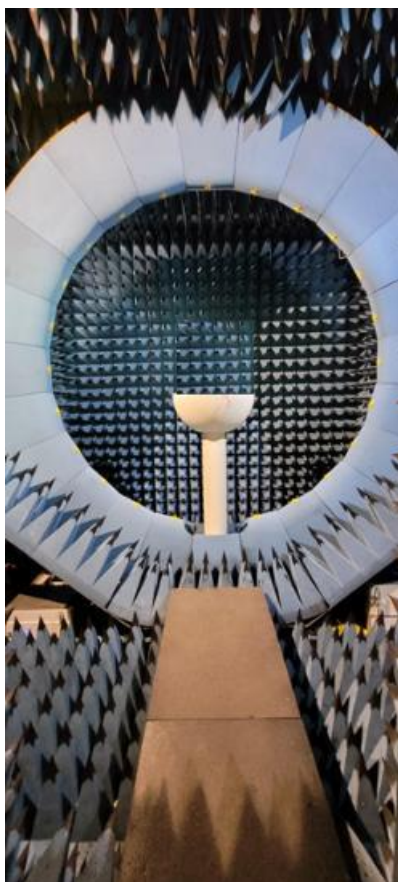


Figure 7. Satimo SG-23 6 GHz Stargate Antenna Test Chamber.

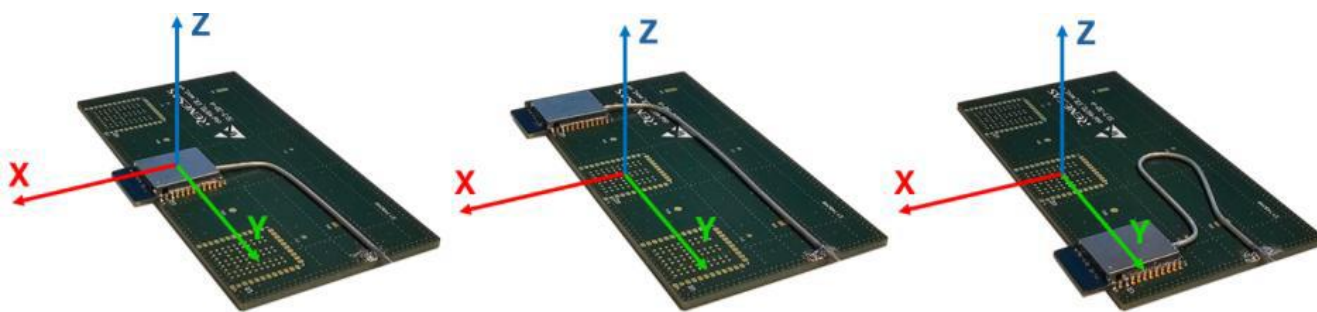
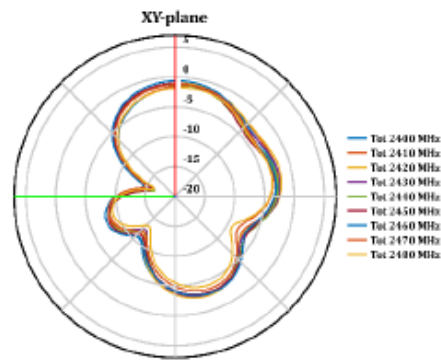


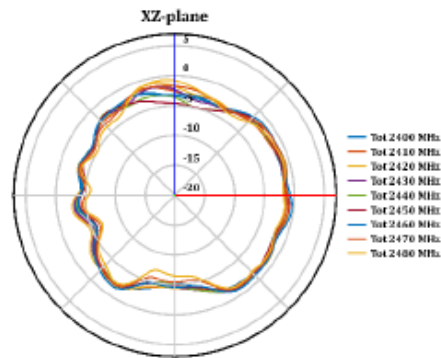
Figure 8. Measurement plane definitions.

## 5.4.1 2.4GHz: Module in right position



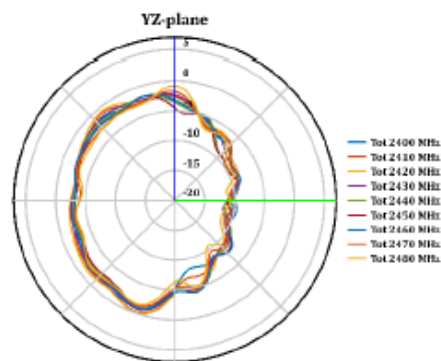
| Freq [MHz] | Peak [dBi] | Avg [dBi] |
|------------|------------|-----------|
| 2400       | -1.2       | -4.5      |
| 2410       | -1.3       | -4.5      |
| 2420       | -1         | -4.1      |
| 2430       | -1.2       | -4.4      |
| 2440       | -1.2       | -4.5      |
| 2450       | -1.1       | -4.5      |
| 2460       | -0.6       | -4.2      |
| 2470       | -1.2       | -4.8      |
| 2480       | -1.7       | -5.3      |

Figure 9. Radiation patterns for Renesas DA14870 BLE module located at right position in XY-plane.



| Freq [MHz] | Peak [dBi] | Avg [dBi] |
|------------|------------|-----------|
| 2410       | -1.3       | -2.7      |
| 2420       | -0.7       | -2.3      |
| 2430       | -0.8       | -2.6      |
| 2440       | -0.8       | -2.9      |
| 2450       | -0.7       | -2.9      |
| 2460       | -0.2       | -2.4      |
| 2470       | -0.8       | -2.7      |
| 2480       | -0.6       | -3        |

Figure 10. Radiation patterns for Renesas DA14870 BLE module located at right position in XZ-plane.

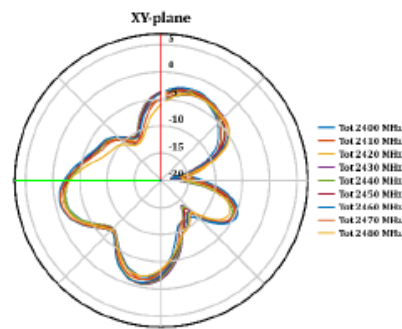


| Freq [MHz] | Peak [dBi] | Avg [dBi] |
|------------|------------|-----------|
| 2400       | -0.9       | -4.3      |
| 2410       | -0.3       | -3.9      |
| 2420       | -0.1       | -3.5      |
| 2430       | -0.8       | -3.9      |
| 2440       | -1.3       | -4.3      |
| 2450       | -1.4       | -4.5      |
| 2460       | -1         | -4.1      |
| 2470       | -1.3       | -4.3      |
| 2480       | -0.8       | -4.6      |

Figure 11. Radiation patterns for Renesas DA14870 BLE module located at right position in YZ-plane.

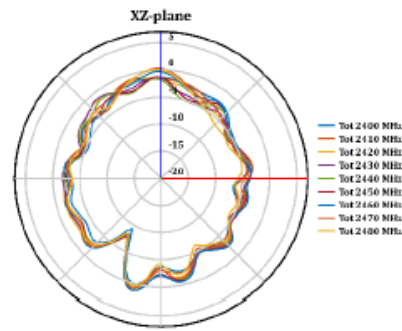
Figure 14: 2D radiation patterns for 2.4 GHz band for DA14870MOD, right position

## 5.4.2 2.4GHz: Module in middle position



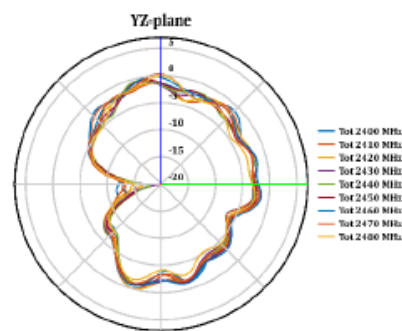
| Freq [MHz] | Peak [dBi] | Avg [dBi] |
|------------|------------|-----------|
| 2400       | -2         | -5.7      |
| 2410       | -1.5       | -5.5      |
| 2420       | -0.7       | -5.1      |
| 2430       | -0.5       | -5.1      |
| 2440       | -0.6       | -5.2      |
| 2450       | -0.7       | -5.1      |
| 2460       | -0.8       | -4.8      |
| 2470       | -1.1       | -5.2      |
| 2480       | -1.7       | -5.8      |

Figure 12. Radiation patterns for Renesas DA14870 BLE module located at middle position in XY-plane.



| Freq [MHz] | Peak [dBi] | Avg [dBi] |
|------------|------------|-----------|
| 2400       | 0.2        | -3.4      |
| 2410       | 0.8        | -3.1      |
| 2420       | 1.3        | -2.8      |
| 2430       | 1.2        | -2.9      |
| 2440       | 1.2        | -3        |
| 2450       | 1.3        | -3        |
| 2460       | 1.2        | -2.7      |
| 2470       | 0.8        | -2.9      |

Figure 13. Radiation patterns for Renesas DA14870 BLE module located at middle position in XZ-plane.



| Freq [MHz] | Peak [dBi] | Avg [dBi] |
|------------|------------|-----------|
| 2400       | -0.8       | -3.4      |
| 2410       | -0.1       | -3.4      |
| 2420       | 0          | -3.4      |
| 2430       | -0.8       | -3.6      |
| 2440       | -0.4       | -3.7      |
| 2450       | -0.5       | -3.5      |
| 2460       | 0          | -3        |
| 2470       | 0.3        | -3.3      |
| 2480       | 0          | -4        |

Figure 14. Radiation patterns for Renesas DA14870 BLE module located at middle position in YZ-plane.

Figure 15: 2D radiation patterns for 2.4 GHz band for DA14870MOD, middle position

## 5.4.2.1 2.4GHz Module in left position

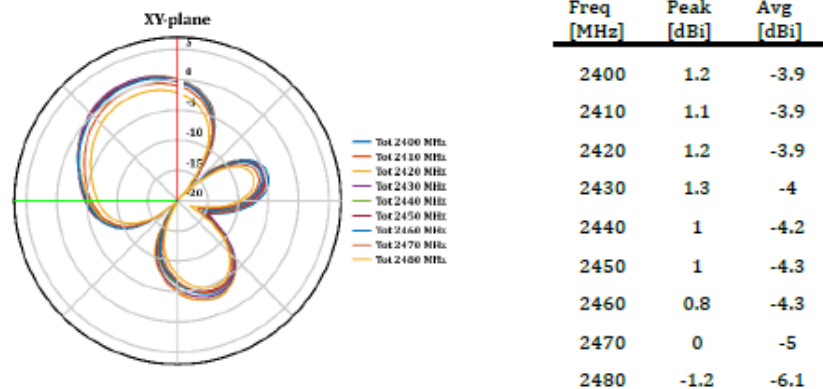


Figure 15. Radiation patterns for Renesas DA14870 BLE module located at left position in XY-plane.

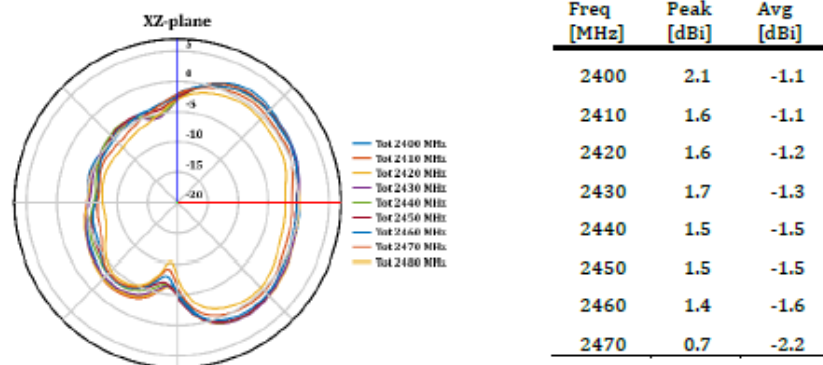


Figure 16. Radiation patterns for Renesas DA14870 BLE module located at left position in XZ-plane.

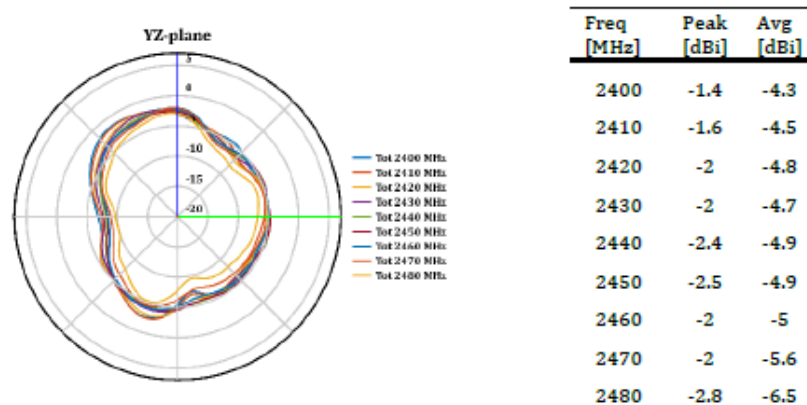


Figure 17. Radiation patterns for Renesas DA14870 BLE module located at left position in YZ-plane.

Figure 16: 2D radiation patterns for 2.4 GHz band for DA14870MOD, left position

## 9. Packaging Information

### 9.1 Tape and Reel

Reel Modules: QTY-100 Modules.

Reel Modules: QTY-700 Modules.

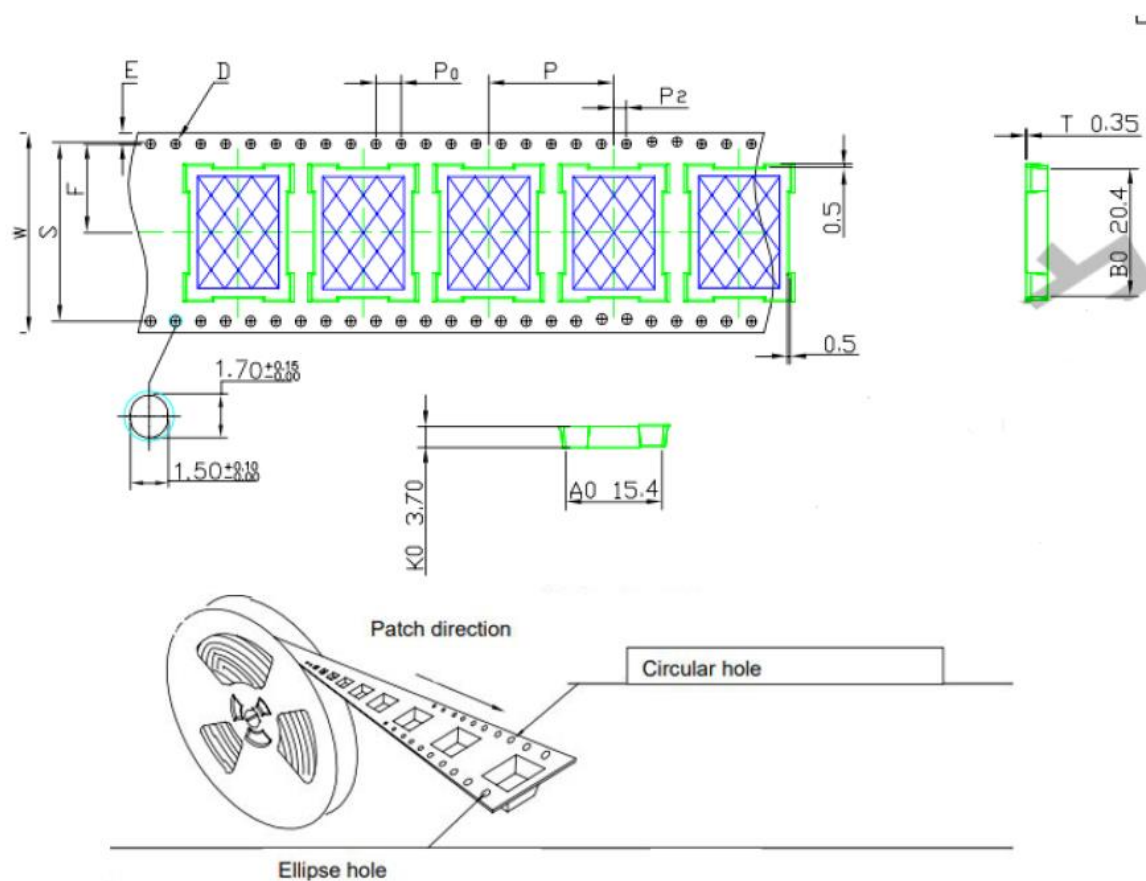


Figure 17: Tape and Reel

## 9.2 Labelling

On each reel, a set of labels are placed. The information label shows information regarding the batch number, date code, reel date and number, quantity (MOQ 100 or MOQ 700), and part number as shown in Figure 18.



Figure 18: Reel part information label (example)

## 10. Soldering

TBD

## 11. Moisture Sensitivity Level

MSL is an indicator for the maximum allowable time period (floor lifetime) in which a moisture-sensitive plastic device, when removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH before the solder reflow process.

The DA14870 Module is qualified for MSL 3.

Table 21: MSL level vs floor lifetime

| MSL Level | Floor Lifetime           |
|-----------|--------------------------|
| MSL 4     | 72 hours                 |
| MSL 3     | 168 hours                |
| MSL 2     | 4 weeks                  |
| MSL 2A    | 1 year                   |
| MSL 1     | Unlimited at 30 °C/85%RH |

## 12. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

**Table 41. Ordering information**

| Part number     | Description                                                      | Carrier type  | Temperature range |
|-----------------|------------------------------------------------------------------|---------------|-------------------|
| DA14870MOD-SF01 | Dual Mode<br>Bluetooth/Bluetooth LE 6.0<br>Module, with codec    | Tape and reel | -30°C to +85°C    |
| DA14870MOD-DF01 | Dual Mode<br>Bluetooth/Bluetooth LE 6.0<br>Module, without codec | Tape and reel | -30°C to +85°C    |

**Part number legend:**

### 13. Regulatory Information

This section outlines the regulatory information for the DA14870-SF01 and DA14870-DF01 Module. The modules are certified for the global market. This facilitates the market entry of the end product. The end product would need to apply for the end product certification, however, the module certification listed below will facilitate that procedure.

When the user sends the end product to those markets, the end product may need to follow additional requirements according to the specific market regulation.

For example, some markets have additional testing and/or certification like Korea EMC and some have the requirement to put on the end product label a modular approval ID or mark that consists of an approved modular ID on host label directly, like Japan, Taiwan, Brazil.

A list of the Conformance Standards that the DA14870-SF01 and DA14870MOD-DF01 Modules meets is shown in [Table 42](#).

**Table 42: Standards conformance**

| Area        | Item     | Service  | Standard                                                                                     | Certification IDs/ Certificate No     |                 |
|-------------|----------|----------|----------------------------------------------------------------------------------------------|---------------------------------------|-----------------|
|             |          |          |                                                                                              | DA14870MOD-SF01                       | DA14870MOD-DF01 |
| Global      | Safety   | CB       | IEC 62368-1:2023                                                                             | DE 2-046602<br><a href="#">Note 1</a> |                 |
| Europe      | Wireless | RED      | EN 300 328 v2.2.2 (2019-07)<br>EN IEC 62311:2020-01                                          | Pending                               |                 |
|             | Safety   | CE       | IEC 62368-1:2023                                                                             |                                       |                 |
|             | EMC      | RED      | EN 301 489-1 v2.2.3<br>EN 301 489-17 v3.3.1<br>DIN EN 55032:2022                             |                                       |                 |
| UK          | Wireless | UKCA-RED | EN 300 328 v2.2.2 (2019-07)<br>EN IEC 62311:2020-01                                          | Pending                               |                 |
|             | Safety   | UKCA-LVD | IEC 62368-1:2023                                                                             |                                       |                 |
|             | EMC      | UKCA-RED | EN 301 489-1 v2.2.3<br>EN 301 489-17 v3.3.1<br>DIN EN 55032:2022                             |                                       |                 |
| US/CA       | Wireless | FCC ID   | FCC - Title 47 CFR Part 15<br>FCC 47 CFR Part 2                                              | Y82-DA14870MOD                        |                 |
|             |          | IC ID    | RSS - 247 Issue 4<br>RSS - Gen Issue 5 incl.<br>Amendment 1 & 2<br>RSS-102:Issue 6 (2023-12) | 9576A-DA14870MOD                      |                 |
| Japan       | Wireless | MIC      | JRL                                                                                          | 202-JWM009                            |                 |
| Taiwan      | Wireless | NCC      | LP0002                                                                                       | Pending                               |                 |
| South Korea | Wireless | KC       | 방송통신표준<br>KS X 3123 "무선 설비 적합성<br>평가 시험 방법"<br>KS X 3124:2024 / KS X<br>3126:2024            | R-R-8DL-DA14870MODSF01                |                 |
| China       | Wireless | SRRC     | 信部无【2002】353                                                                                 | 26J994Z8S870                          |                 |
| Brazil      | Wireless | ANATEL   | ATO No.14448/2017<br>Resolution No.680                                                       | 02180-26-16689                        |                 |

| Area                  | Item     | Service | Standard     | Certification IDs/ Certificate No |                 |
|-----------------------|----------|---------|--------------|-----------------------------------|-----------------|
|                       |          |         |              | DA14870MOD-SF01                   | DA14870MOD-DF01 |
| S.Africa              | Wireless | ICASA   | Based on RED | Pending                           |                 |
| Australia/New Zealand | Wireless | ACMA    | Based on RED |                                   |                 |

**Note 1** Include national differences of EU Group Differences, JP, US, CA, AU/ New Zealand

## 13.1 CE (Radio Equipment Directive 2014/53/EU (RED)) – (Europe)

**Model no. DA14870MOD-SF01**

**Model no. DA14870MOD-DF01**

The DA14870 Module is radio equipment assessed in accordance with Directive 2014/53/EU (RED) and is CE marked. The module has been manufactured and tested for use as a subassembly intended for integration into a final host product. The module has been tested against the applicable essential requirements of Directive 2014/53/EU for Health and Safety (Article 3.1(a)), Electromagnetic Compatibility (Article 3.1(b)), and Radio spectrum usage (Article 3.2).

The applicable standards are:

**Radio: EN 300 328 v2.2.2 (2019-07)**

**EMC: EN 301 489-1 v2.2.3, EN 301 489-17 v3.3.1**

**Health: EN IEC 62311:2020-01**

**Safety: IEC 62368-1:2023**

The final host product may be subject to additional EMC testing. Conducted test results from the module evaluation may be used to support the end-product conformity assessment, provided that integration conditions remain equivalent. It is recommended to repeat EN 300 328 radiated testing with the final end-product assembly.

### Simplified Declaration of Conformity

Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14870 Module is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: [www.renesas.com](http://www.renesas.com)

## 13.2 UKCA (UK)

**Model no. DA14870MOD-SF01**

**Model no. DA14870MOD-DF01**

The module has been tested and found to comply with the standards harmonized with the regulations listed below according to UKCA-Radio Equipment Regulations 2017-CHAPTER 1 6(1)(a) Health and Safety, 6(1)(b) Electromagnetic Compatibility & 6(2) Radio spectrum usage.

The applicable standards are:

**Radio: EN 300 328 v2.2.2 (2019-07)**

**EMC: EN 301 489-1 v2.2.3, EN 301 489-17 v3.3.1**

**Health: EN IEC 62311:2020-01**

**Safety: IEC 62368-1:2023**

The final host product may be subject to additional EMC testing. Conducted test results from the module evaluation may be used to support the end-product conformity assessment, provided that integration conditions remain equivalent. It is recommended to repeat EN 300 328 radiated testing with the final end-product assembly.

| <b>Simplified Declaration of Conformity</b>                                                                                                                                                                                                                                                              |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14870 Module is in compliance with Radio Equipment Regulations 2017. The full text of the UK declaration of conformity is available at the following internet address: <a href="http://www.renesas.com">www.renesas.com</a> |

### 13.3 FCC (USA)

Model no. DA14870MOD-SF01, FCC ID: Y82-DA14870MOD

Model no. DA14870MOD-DF01, FCC ID: Y82-DA14870MOD

#### 13.3.1 List of applicable FCC rules

The module complies with FCC Part 15.247.

#### 13.3.2 Summarize the specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

#### 13.3.3 Limited module procedures

Not applicable.

#### 13.3.4 Trace antenna designs

Not applicable.

#### 13.3.5 RF exposure considerations

This equipment complies with FCC's RF radiation exposure limits set forth for an uncontrolled environment. For body-worn or head applications the minimum distance to the human body has to be at least 15 mm, for limb-worn applications no minimum safety distance to the human body is required. The antenna(s) used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

#### 13.3.6 Antenna Information

| Type        | Brand   | Model Name          | Gain             | Impedance | Application |
|-------------|---------|---------------------|------------------|-----------|-------------|
| PCB Antenna | Renesas | DA14870 BLE Antenna | 2.4GHz: +1.6 dBi | 50Ω       | Fixed       |

In the case of PCB antenna is permanently attached, can't be replaced.

#### 13.3.7 Label and compliance information.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

##### Note

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

##### Warning

Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

##### Note

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency

## Note

energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

The system integrator must place an exterior label on the outside of the final product housing the DA14870 Module. Below are the contents that must be included on this label.

## OEM Labeling Requirements:

### Notice

The OEM must make sure that FCC labeling requirements are met. This includes a clearly visible exterior label on the outside of the final product housing that displays the contents shown below.

Model: **DA14870MOD-SF01**  
Contains FCC ID: **Y82-DA14870MOD**

Model: **DA14870MOD-DF01**  
Contains FCC ID: **Y82-DA14870MOD**

## 13.3.8 Information on test modes and additional testing requirements

When testing host product, the host manufacture should follow FCC KDB Publication 996369 D04 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements. In setting up the configurations, if the pairing and call box options for testing do not work, then the host product manufacturer should coordinate with the module manufacturer for access to test mode software.

## 13.3.9 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247 and 15.407) list on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuitry.

## 13.4 ISED (Canada)

Model no. **DA14870MOD-SF01**, IC: **9576A-DA14870MOD**

Model no. **DA14870MOD-DF01**, IC: **9576A-DA14870MOD**

The DA14870 Module is certified for the IC as a single-modular transmitter. The module meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

The module has been tested according to the following standards:

- Radio: RSS-247, ISSUE 4, July 2025, RSS - Gen Issue 5 incl. Amendment 1 & 2
- Health: RSS-102 Issue 6:2023

This device contains license exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

(1) this device may not cause interference

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

(1) L'appareil ne doit pas produire de brouillage

(2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

### RF Exposure Statement

This device complies with IC radiation exposure limits set forth for an uncontrolled environment and meets RSS-102 of the IC radio frequency (RF) Exposure rules. For body-worn or head applications the minimum distance to the human body has to be at least 20 mm, for limb-worn applications the minimum safety distance to the human body has to be 15 mm. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Le présent appareil est conforme à l'exposition aux radiations IC définies pour un environnement non contrôlé et répond aux RSS-102 de la fréquence radio (RF) IC règles d'exposition. L'intégrateur de module doit intégrer l'appareil à une distance minimale de 20 cm du corps humain, sinon l'intégrateur de module doit effectuer des tests et une certification SAR. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

### OEM Responsibilities to comply with IC Regulations

**OEM integrator is responsible for testing their end product for any additional compliance requirements needed for the module installation** like IC ES003 (EMC). This can be combined with the FCC Part 15B test.

### End product labeling

The DA14870 Module is labeled with its own IC ID. Model no. DA14870MOD-SF01, IC: **9576A-DA14870MOD**

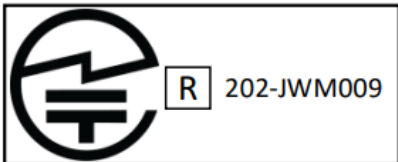
Model no. DA14870MOD-DF01, IC: **9576A-DA14870MOD**. If the IC ID is not visible when the module is installed inside another device, the host product must be labelled to display the ISED certification number for the module, preceded by the word "contains" or similar wording expressing the same meaning, as follows: "Contains IC: **9576A-DA14870MOD**".

## 13.5 MIC (Japan)

**Model no. DA14870MOD-SF01, MIC ID: 202-JWM009**

**Model no. DA14870MOD-SF01, MIC ID: 202-JWM009**

This radio module has been tested and certified in accordance with the Japan Radio Law (電波法), including Article 49-20 and the relevant provisions of the Ordinance Regulating Radio Equipment

| Model                                            | GITEKI mark label                                                                    |
|--------------------------------------------------|--------------------------------------------------------------------------------------|
| <b>DA14870MOD-SF01</b><br><b>DA14870MOD-DF01</b> |  |

### End Product Labeling

When this certified radio module is incorporated into a host product and the module's conformity mark is **not visible externally**, the **MIC (GITEKI) conformity mark and certification number assigned to the module**

**may be displayed on the host product.** This is permitted under the Japan Radio Law following the **2014 revision of the Radio Act**, which allows host products incorporating certified radio modules to bear the same conformity mark.

To indicate the presence of a certified radio module, the following notice may be displayed next to, above, or below the GITEKI mark and certification number on the host product:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

**Translation:**

"This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

### 13.6 NCC (Taiwan)

**Model no. DA14870MOD-SF01**, NCC ID: pending

**Model no. DA14870MOD-DF01**, NCC ID: pending

| Model                  | NCC label |
|------------------------|-----------|
| <b>DA14870MOD-SF01</b> |           |
| <b>DA14870MOD-DF01</b> |           |

DA14870 Modules have received compliance approval in accordance with the Telecommunications Act. The modules have been tested according to the following standards:

- Radio: Low Power Radio Frequency Devices Technical Regulations (LP0002)

End product may need to follow additional requirements according to the regulation EMC.

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。低功率射頻器材之使用不得影響飛航安

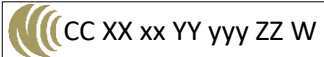
及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

應避免影響附近雷達系統之操作。

高增益指向性天線只得應用於固定式點對點系統。

#### End product labeling

The NCC ID can be applied directly to the end product's label.

| NCC Warning                                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 本模組於取得認證後將依規定於模組本體標示審驗合格標籤，並要求最終產品平台廠商 (OEM Integrator) 於最終產品平台 (End Product) 上標示" 本產品內含射頻模組，其NCC型式認證號碼為：<br> CC XX xx YY yyy ZZ W |

### 13.7 KC (South Korea)

**Model no. DA14870MOD-SF01, MSIP ID: R-R-8DL-DA14870MODSF01**

**Model no. DA14870MOD-DF01, MSIP ID: R-R-8DL-DA14870MODSF01**

DA14870 Module has received certification of conformity in accordance with Radio Waves Act. The module has been tested according to the following standard:

- Radio: Ministry of Science and ICT Notice No. 2019-105

For the end product wireless test, you can refer to Renesas' own certification report so that the lab knows the module itself has passed although it still needs to be tested.

**Additionally, EMC for wireless (KS X 3124:2024 / KS X 3126:2024).**

#### End product labeling

The MSIP ID can be applied directly to the end product's label. The ID should be clearly visible on the final end product. The integrator of the module should refer to the labeling requirements for Korea available on the Korea Communications Commission (KCC) website.

### 13.8 SRRC (China)

**Model no. DA14870MOD-SF01, SRRC ID: 26J994Z8S870**

**Model no. DA14870MOD-DF01, SRRC ID: 26J994Z8D870**

The module has been tested and found to be compliant according to the following standards:

信部无【2002】353号

End product may need to follow additional requirements according to the regulation EMC.

### 13.9 ANATEL (Brazil)

**Model no. DA14870MOD-SF01, ANATEL ID: 02180-26-16689**

**Model no. DA14870MOD-SF01, ANATEL ID: 02180-26-16689**

DA14870 modules have been evaluated for conformity in accordance with ANATEL technical requirements for Restricted Radiation Radiocommunication Equipment, as defined by Resolução N° 680/2017 and applicable ANATEL Acts, including Ato N° 14.448/2017 and Ato N° 4.776/2020.

| Warning                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| "Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados. Para mais informações consulte o site da ANATEL <a href="http://www.anatel.gov.br">www.anatel.gov.br</a> "                  |
| Translation of the text:<br>"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems. For more information, consult the ANATEL website <a href="http://www.anatel.gov.br">www.anatel.gov.br</a> " |

### 13.10 ICASA (South Africa)

South Africa certification is based on RED(CE) approval.

**Model no. DA14870MOD-SF01, Equipment Type Approval Number: PENDING**

Model no. DA14870MOD-DF01, Equipment Type Approval Number: PENDING

Approval is granted to print labels for the products as described below:

- For use as Label on the product size: 80 mm (W) X 40 mm (H). To be printed on the product.
- For use as Label on the package size: 80 mm (W) X 40 mm (H). To be printed on the package.

End product may need to follow additional requirements according to the regulation EMC.

### 13.11 Australia/New Zealand (ACMA)

Certification is based on RED(CE) approval.

### 13.12 WEEE Directive (2012/19/EU)



The Waste Electrical and Electronic Equipment Regulations 2013



#### For Customers in the UK and European Union

The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use, the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled, and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back the end of life equipment. Register for this service at:

<https://www.renesas.com/eu/en/support/regional-customer-support/weee>

## Appendix A Appendix Heading

### A.1 Appendix Subheading

<Insert text here>.

## 14. Revision History

| Revision | Date         | Description                                          |
|----------|--------------|------------------------------------------------------|
| 1.1      | Apr 21, 2026 | Preliminary release. Updated regulatory information. |
| 1.0      | Feb 12, 2026 | Preliminary release.                                 |
| 0.1      | Oct 9, 2025  | First internal release.                              |

### RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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