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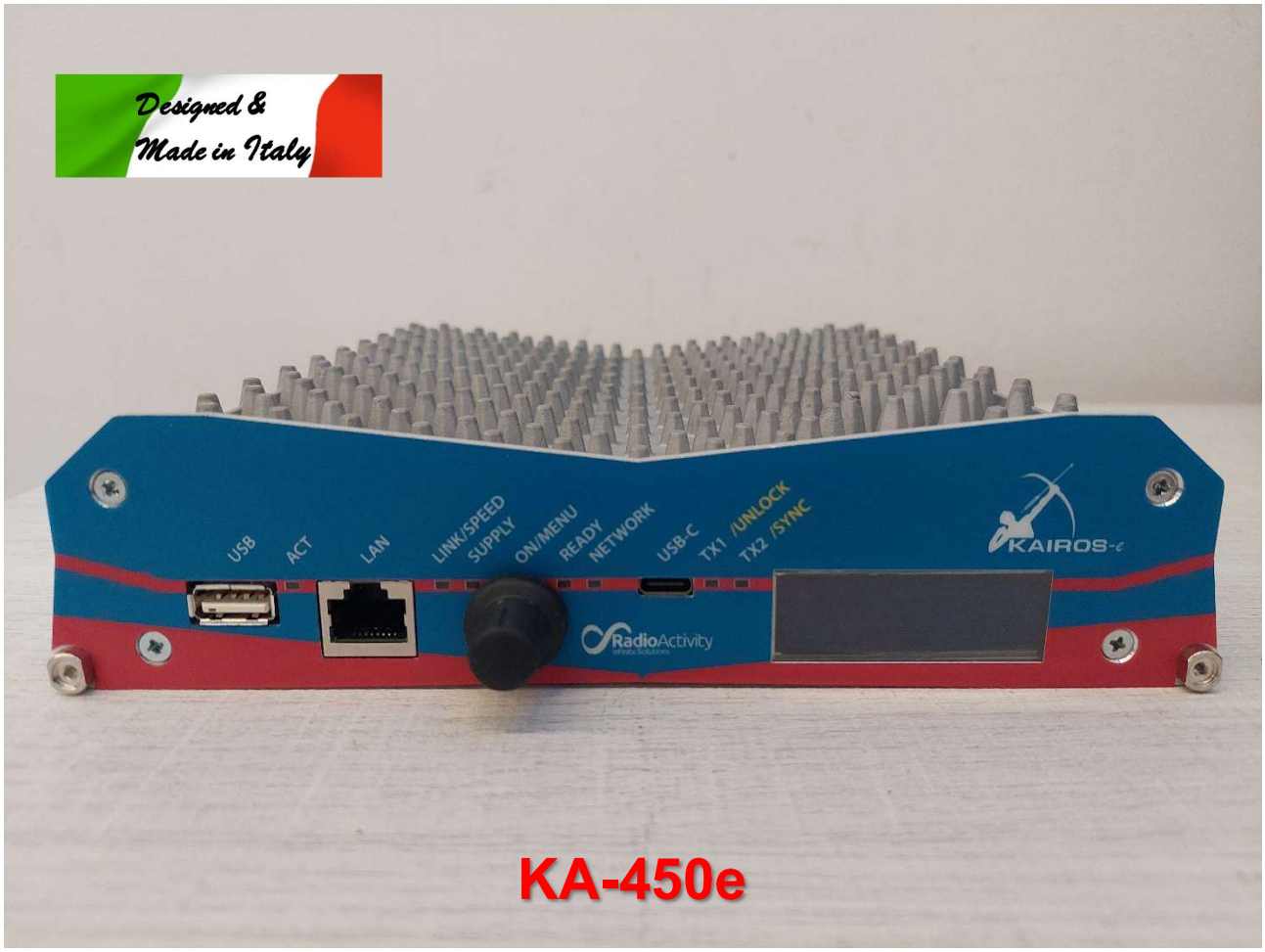
Tel. +39.02.36514205 - FAX/Voicebox +39.1782.242408 - CCIAA Milano N° 1728248 - VAT Id. 04135130963

KA-040e circuit description

Version 1.0 – 04/14/2026



REVISION SUMMARY:

Number	Date	Main modifications to previous version
Ver 1.0	04/14/2026	First edition
…….	…….	…….

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Summary

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1 GENERAL DESCRIPTION

KAIROS enhanced (**KAe**) is an evolution of the **KAIROS** transceiver, which is multi-protocol analog and digital transceiver, intended for both stand-alone and network application. The previous series has been completely renewed, in terms of components, performances and applications and a new look has been designed, keeping the same overall shape of its previous model.

KAe transceiver is a professional software defined radio station, based on a LINUX logic core. It is a building block for a number of applications ranging from a simple standalone repeater to a national wide network system, thanks to its extreme flexibility.

KAe transceiver embeds on a single boards a logic core, including microprocessor, DSP and PLD, a digital transmitter with output power up to 40W, a double receiver, for space diversity reception, a GPS module for synchronization, an audio interface, both digital over IP and analog over 4 wire line.

Main characteristics:

Model	KA-040e		
MHz	39-50		
Channel spacing	25/20/12,5/6,25 kHz		
RF output power	1-40 W / 100% duty cycle / selectable per channel		
Synthesis step	50Hz		
Frequency stability	0,1 p.p.m.		
Synchronization sources	Internal ref., GPS/GLONASS, Ethernet IEE-1588v2, 2 wire, Digital RX, External		
Operating temperature	-30°C ÷ +60°C		
Power supply (negative ground)	Min.	Typ.	Max.
	10,8V	13,2V	15,6V
Power consumption	TX: 100 W @40W RF / RX: 6 W		
Dimensions & weight	160x200x45mm / 1.5kg		
Audio lines	2x 4 wires + E&M, RTP over IP		
LAN port	Ethernet 10/100/1000 (auto MDI/MDI X) on an RJ45 socket		

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IP multisite bandwidth	70 kb/s in analog to/from Master 24 kb/s in DMR to/from Master (both DMR timeslots)
Max tolerable IP delay	1080ms (round trip)
Alarm I/O	2xInput + 1xOutput
Command I/O	2xInput + 2xOutput + 1xAnalog input

2 PRODUCT IDENTIFICATION

- Object of Declaration: PMR digital transceiver/repeater
- Type/Model: KA-040e
- Trade mark:
- Power supply: 13.2Vdc nominal (from 10.8V to 15.6V) negative to GND, 10A max
- Weight: 1.5 kg
- Dimensions: 160mm x 200mm x 45mm
- Type of radio interface: GNSS and PMR
- Embedded chipset: Skyworks SKY72310-11 – PLL
  Peregrine PE4152 – RF mixer
  Analog Devices ADF9864 – IF processor
  NXP AFT09MS015NT1 – RF driver
  NXP AFT05MP075N – RF power amplifier
  Texas Sitara AM5716 – microprocessor
  Analog Devices ADSP2187N – DSP
  Lattice Mac XO3 9400 – PLD
  Marvell 88E1510P – Ethernet physical interface
  Texas TLV320AIC34 – Audio coded
  Quectel L76 – GPS receiver
- Firmware: pkg release: 0.9.3
  GNSS FW L76NR04A01S
- Frequency band: 39-50MHz
  GPS L1 band (1575.42 MHz); Glonass G1 (1602 MHz)
- Maximum RF power (PMR) 46dBm under extreme conditions
- Channel spacing: 12.5kHz/20/25kHz
- Type of modulation: FM/PM 4FSK C4FM; BPSK for GNSS

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- Antenna connector: SMA, 50ohm; not provided external antenna
- Max gain PMR antenna refers to specific authorization for frequency use by Government
- GNSS antenna 50 ohm, 5V, 100mA max, gain typ. 26dB (min 20, max 30), 1575MHz
- RF communication protocols: analog, digital DMR, digital P25 phase 1
- Data communication interface: TCP/IP over Ethernet 10-100-1000M (RJ45 connector)
  Proprietary protocol

3 PRODUCT DESCRIPTION

KAIROS-enhanced (KAe) is a multi-protocol transceiver, designed to operate in the frequency range of 39 to 50MHz (model KA-040e).

KAe is composed by three main blocks:

- A full RF transceiver
- A logic board with additional GPS receiver
- A power supply

The logic board completely manages the **KAe**, in terms of both digital signal processing and connection with other devices. It takes care about synchronization and network management. It embeds a microprocessor, a DSP, a PLD, a GPS receiver, and an Ethernet processor with PTP - IEEE1588.

The RF transceiver includes one transmitter (working in class C) and two receivers. They embed all the needed blocks, including fully digital modulator and demodulator.

The receiver system is composed by two separate and matched receivers to obtain a soft space diversity reception. Main and diversity receiver chains are completely independent and coherent (sharing the same local oscillators). This receiver uses a double conversion heterodyne system, with 70 MHz first IF and 1.5MHz digital conversion to base-band.

The transmit signal frequency is generated by the VCO / PLL and modulated by the signal from the DSP. It is then amplified and fed to the antenna.

The power supply is implemented by discrete components; it provides all the internal supplies of the board, including the set of supplies for microprocessor and it is equipped with input protections against over/under-voltages, over-current, polarity inversion, short circuit.

The overall block diagram is the following:

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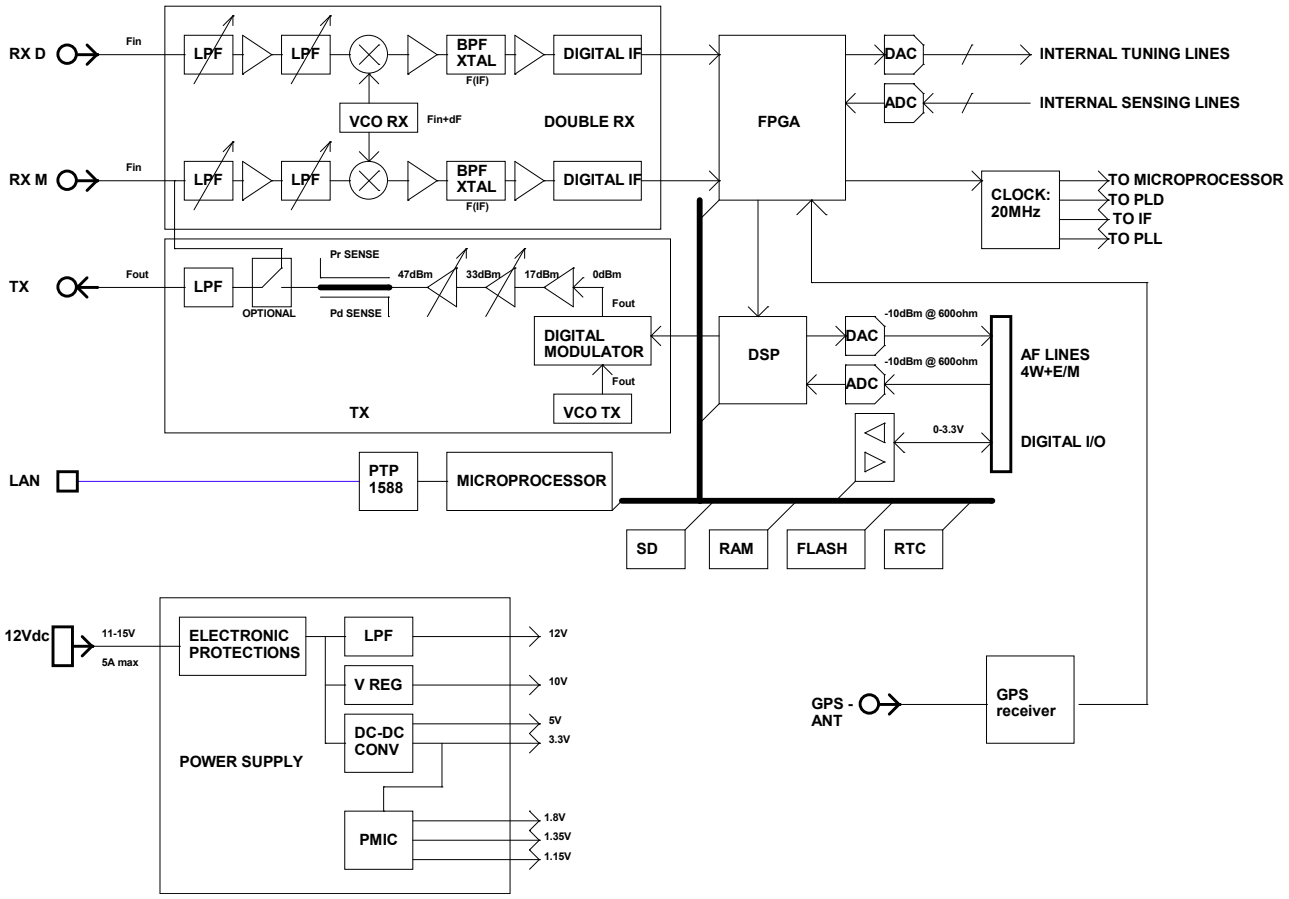

Different models of **KAe**, differs each other for the RF front-end only; the logic block and the power supply are exactly the same. From mechanical point of view also, the models are all identical.

3.1 RECEIVER SYSTEM

3.1.1 FRONT-END

The front-end circuit consist of a former tunable band pass filter, RF Low Noise Amplifier (PL08) and latter tunable band pass filter. The BPF covers the frequency range from 39 to 50MHz, for the KA-040e model.

The double BPF attenuates the unwanted signals and send only the necessary signal to the first mixer (PE4152).

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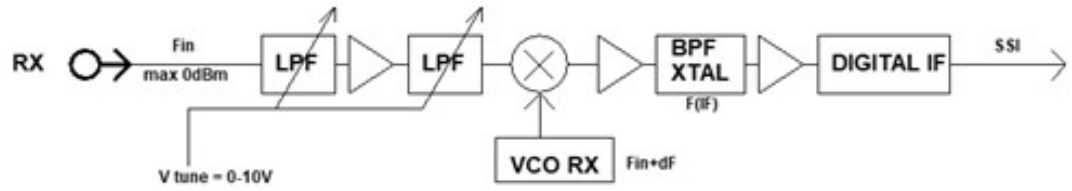

3.1.2 FIRST MIXER

The filtered signal from the front-end circuit is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (PE4152) to become a 70 MHz first intermediate frequency (IF) signal.

3.1.3 IF CIRCUIT

The first IF signal is amplified by the IF LNA amplifier (GRF2013) and passed through a monolithic crystal filter (4 poles, fundamental) to reject adjacent channel signal. The filtered first IF signal is amplified by the IF amplifier (BFU550W), which acts as a compressor also, in order to limit the maximum signal level at the input port of the following digital IF.

The IF signal is then fed into a Digitizing Subsystem IC (AD9864), that digitizes with a signal bandwidth ranging from 6.8kHz to 270kHz. This IC consists of a low noise amplifier, a mixer, a band-pass sigma-delta analog-to-digital converter, and a decimation filter with programmable decimation factor. The signals from the receivers are sent in digital vector format (I&Q) to the DSP. These vectors represent the electromagnetic field vectors, as received from antennas, before any demodulation. By this way the DSP can sum, with the appropriate phases, the received signals to obtain a “soft diversity” reception. This corresponds to an electronic antennas alignment in order to receive the maximum available information along the incoming signal detection.

3.2 TRANSMITTER SYSTEM

3.2.1 DRIVER AND FINAL AMPLIFIER

The signal from TX VCO circuit is amplified by pre-drive amplifier (GRF2013) up to 50mW. The output of the pre-drive amplifier is amplified by the drive amplifier (AFT09MS015NT1 MOS FET) to 2W and by the final amplifier (AFT05MP075NR1: LDMOS) to 40W. The power amplifier works in C class and ensures a very high efficiency, lowering the needed power from supply system and lowering the thermal dissipation.

The output of the final amplifier is the passed through the harmonic filter (LPF), the coupled micro-strips circuit (CM), and filter circuit to lower spurious emissions under required levels by existing regulations.

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An internal TX/ RX switch can be enabled for simplex/ half duplex applications. This switch is optional, normally not mounted, due to isolation reasons; it cannot be enabled/disabled by SW commands.

3.2.2 CM COUPLER CIRCUIT

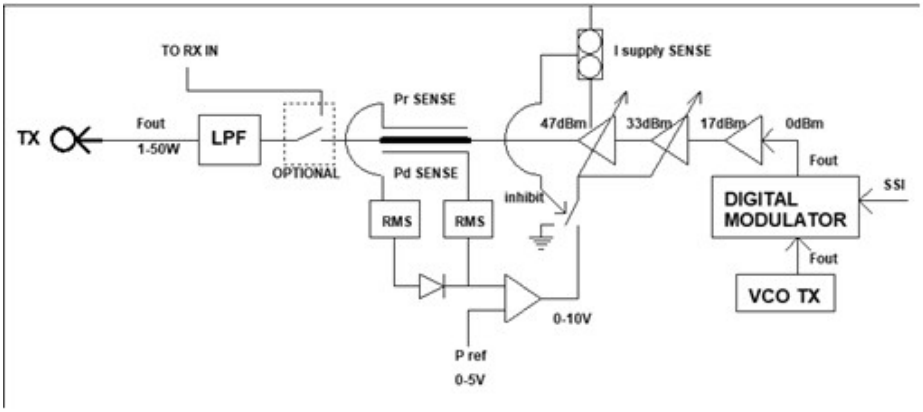
The CM coupler circuit is a line for detecting forward wave and reflected wave. Forward wave is detected and is converted into DC voltage by the direct detector IC (AD8361). If an abnormal antenna load is connected, reflected wave is detected and converted into DC voltage by the reflected detector IC (AD8361). A HW loop provides fast reduction of MOSFET biasing, in order to protect the stages against reverse power.

3.2.3 CURRENT CONTROL CIRCUIT

A current sensor keeps monitoring the current flowing through the RF power amplifier (AFT05MP075NR1). The circuit acts in a closed loop and keeps constant the total power at MOSFET drain. To protect it against any possible short circuit or overdrive.

3.2.4 HIGH TEMPERATURE DETECTOR CIRCUIT

To prevent thermal destruction of drive amplifier (AFT09MS015NT1) and final amplifier (AFT05MP075NR1), this circuit reduces the GATE control voltage when the temperature of drive amplifier and final amplifier rises over a threshold of 90 degrees centigrade. A thermal sensor is hosted in the near proximity of the final MOS stage for temperature monitoring. If the reflected power or the MOSFET temperature exceeds protection threshold, regulation circuit will lower output power up to safe levels for transmitter.



3.3 PLL SYSTEM

3.3.1 RECEIVER PLL CIRCUIT

The receiver PLL circuit consists of a VCO (based on BFU550W BJT) and a fractional PLL (SKY72310-11).

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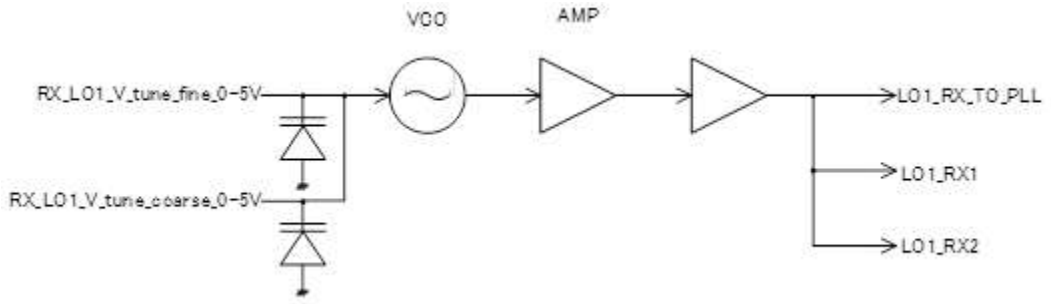
The RX VCO generates the signal for converting the input signal to the first IF frequency; the first local oscillator works at the frequency range from 109MHz to 120MHz, for the KA-040e model. The VCO oscillation frequency is determined by the combination of two control voltages, named "RX_Lo1_V_tune_fine_0-5V" and "RX_LO1_V_tune_coarse_0-10V".

The voltage control terminals, "RX_Lo1_V_tune_fine_0-5V" is controlled by the PLL IC (SKY72310-11).

The voltage control terminals, "RX_LO1_V_tune_coarse_0-10V" is controlled by the PLD(LCMXO3L/LF-9400-BG256) through DAC(TLV320AIC34) circuit. The output frequency changes continuously according to the applied voltage. The "coarse" voltage moves the tuning sub-range inside the total tuning range; the "fine" voltage locks the frequency of the oscillator to the exact desired value.

The first local circuit consists of the VCO, the buffer amplifier(PL08), the RF buffer (BFU550W), the PLL IC(SKY72310-11) and the active loop filters.



PLL IC compares the differences in phase of the VCO oscillation frequency (LO1_RX_TO_PLL) and the reference frequency (20MHz_TO_PLL), returns the difference to the VCO "RX_Lo1_V_tune_fine_0-5V" terminal and realizes the "Phase Locked Loop" for the return control. This allows the VCO oscillation frequency to accurately match (lock) the desired frequency.

3.3.2 TRANSMITTER PLL CIRCUIT

The transmitter PLL circuit consists of the VCO (based on BFU550W BJT) and a fractional PLL (SKY72310-11). The circuit synthesizes the frequency signal to transmit.

TX VCO produces transmitter frequencies from 39 to 50MHz, for the KA-040e model. The VCO oscillation frequencies is determined by two systems of voltage control terminals.

The voltage control terminals, "TX_LO_V_tune_fine_0-5V" and "TX_LO_V_tune_coarse_0-10V", are controlled by the PLL IC(SKY72310-11) and MCU respectively. The output frequency changes continuously according to applied voltage. The input terminal "TX_LO_V_tune_coarse_0-10V" is used to set tune the oscillation sub-band in a continuous mode inside the full frequency range; the exact frequency is set by the input terminal "TX_LO_V_tune_fine_0-5V", which is driven by the PLL. The modulation of the output frequency is performed by the same PLL, acting on the "TX_LO_V_tune_fine_0-5V" signal: the DSP adjusts

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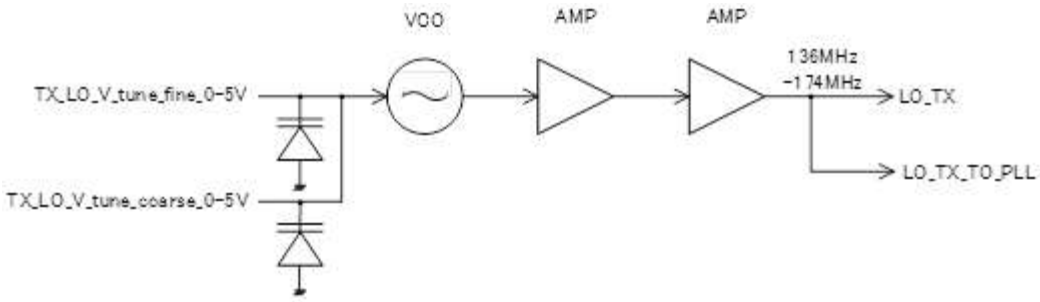
the fractional index of the divisor of the PLL, in order to change the output frequency, as a function of the modulation signal along the time.



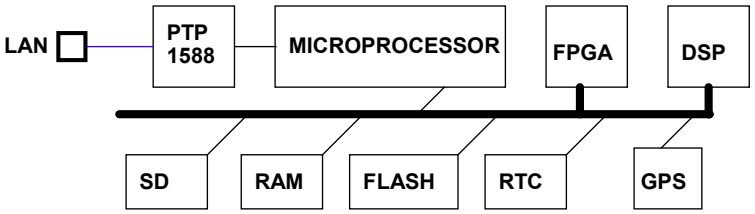
The PLL IC compares the differences in phases of the VCO oscillation frequency and the transmitter PLL reference signal (20MHz), returns the difference to the VCO "TX_LO_V_tune_fine_0-5V" terminal and realizes the "Phase Locked Loop" for the return control. This allows the VCO oscillation frequency to accurately match (lock) the desired frequency.

The desired frequency is set for the PLL IC by the MCU through the 3-line serial bus. Whether the PLL IC is locked or not is monitored by the MCU through the "TX_PLL_LOCK" signal line.

3.4 LOGIC BOARD: CONTROL SYSTEM

3.4.1 MCU

The control system is based on a powerful microprocessor, with LINUX operative system, a Sitara AM5716, which consists of an ARM15 processor, a C66 DSP and an M4 real time processor. It includes all the calculation logic that is needed by the board, anyway an external DSP and FPGA are present for keeping the same signal processing FW as for the previous equipment and for managing the peripheral modules and power supply of the board, respectively.



The processor is connected through a BUS to a set of modules:

- 1Gbyte low power DDR3 RAM memory
- 8Gbyte EMMC flash memory
- Serial NOR flash for booting only
- SD card, as booting memory, program memory or expansion memory

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The processor is equipped also with a real time clock for correlating alarms with date and time only, not for synchronization purposes. The main source for total board synchronization is the embedded GPS receiver of the boards.

It manages an autosensing LAN Ethernet 10/100/1000 interface, supporting the Precision Time Protocol over IP (standard 1588v2).

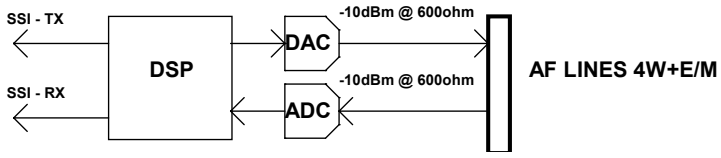
The processor is equipped with a parallel bus to interface with a FPGA and a DSP:

- FPGA is responsible for managing the power supply, board reset and local alarms, when the microprocessor if offline;
- DSP performs the full signal processing, takes care about board synchronization, signal modulation and demodulation.

3.4.2 DSP

The core of system is this the DSP unit which via software performs every function of signal processing into radio station.

The DSP(ADSP2187) is a low power / high performances fixed point 80MIPS device, that can process contemporary 2 digital receivers, one digital synthesizer and 2 audio lines.



DSP is equipped with a fast SPI to interface with the FPGA, which in turns interfaces with microprocessor.

The Sitara processor already includes a C66 DSP; the reason why to mount an external DSP is for keeping the same FW as the one of the previous equipment by Radio Activity, without porting it to a new device.

3.4.3 FPGA

FPGA (really a CPLD by Lattice, series MACXo3) embeds many functionalities:

- it interfaces the inter-processors bus with the peripheral modules, like PLLs, RX IF processors;
- it manages the power supply and the reset commands of the board, when the processor is offline;
- it embeds some PLLs for synchronizing the boards, implements some A-to-D and D-to-A converters, performs a watchdog functions towards other processors.

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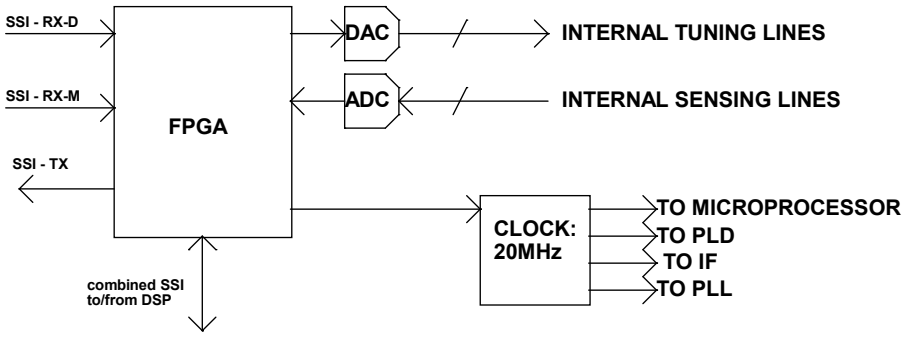
The FPGA is very important because it is independent from any other logic device and it can perform emergency actions.



3.5 RADIO MODULES

The equipment embeds a GNSS receiver module (model L76 by Quectel) in order to provide the1PPS clock to synchronize every other clock, VCO and digital processing of the board and to provide date and time information to the microprocessor for high level logging options. The module is a SOM (System ON Module), which need just power supply and external GNSS antenna, to provide 1PPS signal and NMEA information protocol over a serial interface. It is equipped with an external circuit for providing power supply to external antenna, superimposed to the RF signal. The module has been partially tested according to ETSI EN 303 413 V1.2.1 standard.

3.6 POWER SUPPLY

The equipment is powered through Main connector (2 poles 5.08mm pitch) by nominal 13.2V DC from battery with negative shorted to ground and with a maximum current absorption of 10A.

The on/off switch is managed by the FPGA device that surveys the power supply events. The FPGA memorize the last state and automatically powers on/off KAIROS according with the last state.

An I/O contact, placed in the back of the equipment, allows to switch off KAIROS from an external push-button.

The Power Supply subsystem protects the equipment (by a hot-swap controller, model LT4363-2 by Linear Technologies) from:

- Polarity inversion
- Over voltage: the equipment switches off when the power supply exceeds 15.6V. This may be useful in solar panel powered applications or in mobile applications.

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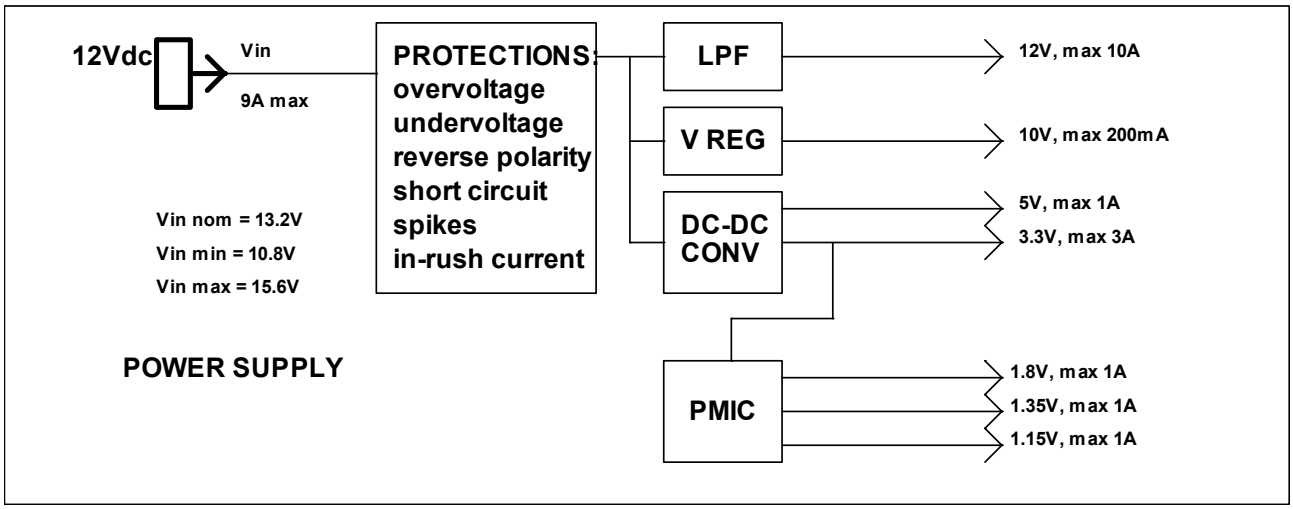
- Under Voltage: equipment switches off when the power supply drops 10.8V. This saves an external lead acid battery that could be damaged from an excessive discarding.
- Over Current: an internal short circuit does not destroy the equipment of fuse the power supply cable.
- Transient voltage: a double protection, one fast and resettable combined with another one relatively slow but able to absorb more energy, automatically stops transient in the power supply.
- Soft start/inrush current: when the equipment is connected to the power supply, this circuit limit the maximum current during the charging of the internal capacitors.

The Power Supply subsystem is made by a set of stages which provide all the internally needed voltages.

A dual output, ultra-low noise DC-DC converter (TPS65917), provides the following secondary voltages:

- 5V switching regulated for low noise amplifier, PLL and some logics
- 3.3V switching regulated for DSP, FPGA, Risk processor, IF, Ethernet device and other logics



Then a power supply processor (PMIC) provides all the voltages that the microprocessor needs, with the correct time sequence. It generates the 1.8V also to feed the DSP.

A separate linear regulator (LT3042) is used to supply the VOCs at 10V, providing very low noise and high rejection of input ripples. It ensures a clean power supply to the oscillators, which are responsible for the good spectral emission of the TX and a good signal selection of the RX.

The RF power amplifier is instead directly connected to the input voltage, by a simple noise filter, in order to optimize the efficiency of the overall device.