

WB10

Datasheet



Revisions History

Date	Version Number	Document Changes
2018/03/05	0.0	Initial Draft
2018/04/18	0.1	Correct typo
2018/08/14	0.2	Update connector SPEC and link

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1 Overview

1.1 General Information

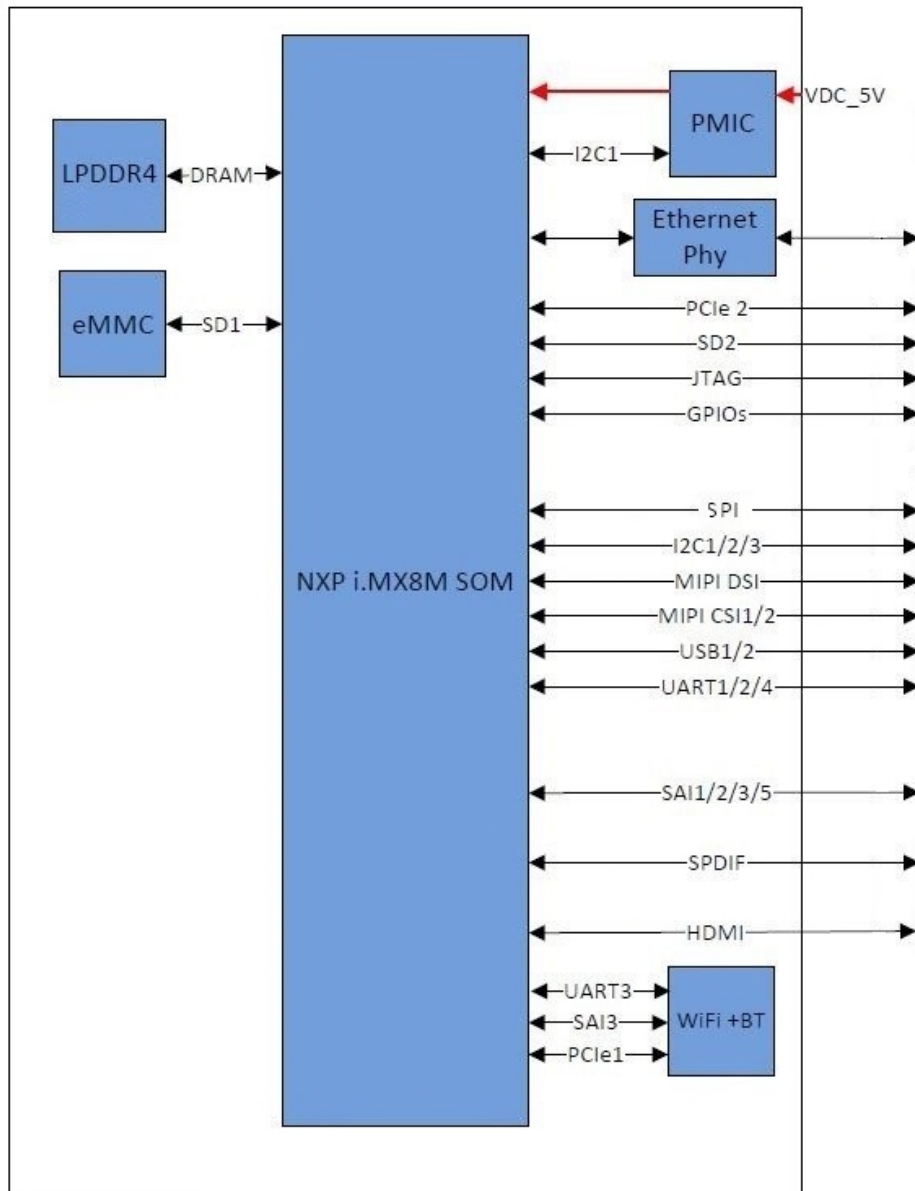
WB10 is a high performance System on Module(SOM) which is designed based on NXP®i.MX8MQuad processor. The i.MX8MQuad integrate fourARM® Cortex-A53up to 1.5GHz and oneCortex-M4 cores to provide industry-leading audio voice and video processing for applications that scale from consumer home audio to home&building automation, voice assistance&machine vision, healthcare industry, etc.It supports video quality with full 4K Ultra HD resolution and supports the highest levels of pro audio fidelity with more than 20 audio channels each @384KHz as well.

WB10 module offers a wide range of interfaces - GPIOs, PWM, I2C, SPI, CSI, DSI, HDMI, UART, USB 3.0 and synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. Moreover, this module features anEthernet PHY on the module to support Giga bitsEthernet Transceiver with HP Auto-MDIX.

It targets a wide range of embedded products such as medical devices, industrial automation, HMLs, data acquisition, and much more.

1.2 Architecture and Block Diagram

Figure 1-1 WB10 SOM Block Diagram



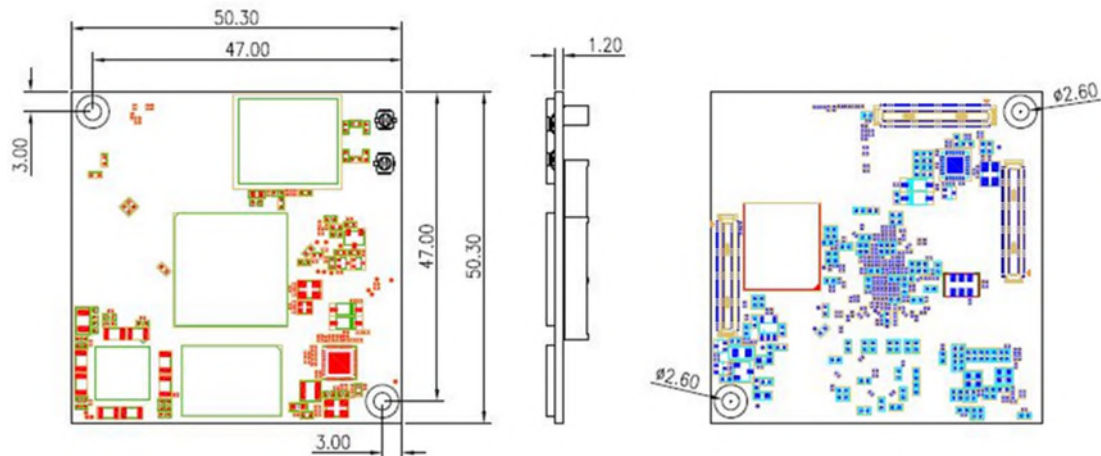
1.3 Feature Summary

- NXP i.MX8M Quad
- 1GB/2GB LPDDR4 RAM
- 4GB/8GB eMMC
- HDMI2.0a output

- 1 x MIPI DSI
- 2 x MIPI CSI
- Wi-Fi 802.11 a/b/g/n/ac, 2x2 MIMO
- Bluetooth 4.2
- 1 x USB 2.0 OTG
- 1 x USB 3.0 Host
- 1x Ethernet Gigabits
- 1 x SD/MMC
- Serial interfaces (3 x I2C, 3 x UART, 1 x SPI, 4 x SAI)
- 2 x PWM/GPIOs
- 1x PCIe2.0

1.4 Dimension

Figure 1-5 WB10 Dimension



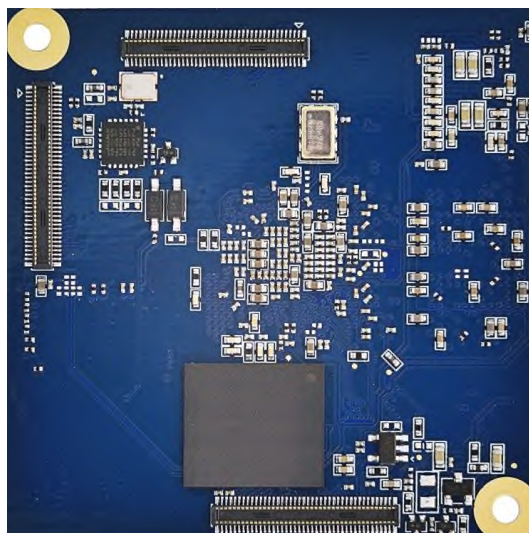
2 Main Hardware Components

WB10 has three [Hirose DF40C-80DP-0.4V\(51\)](#) 80in headers to connect with another carrier board. It integrates the NXP® i.MX8M, LPDDR4 Memory, eMMC, Power Manage IC (PMIC), and Wi-Fi/Bluetooth on the module.

Figure 2-1 – Top side of WB10



Figure 2-2 – Bottom side of WB10



2.1 CPU

The i.MX 8MQuad integrates four ARM® Cortex-A53 up to 1.5GHz and one Cortex-M4 core to provide industry-leading audio, voice and video processing for applications.

The features of the i.MX 8MQuad of processors include the following:

- 4xARM Cortex-A53 plus ARM Cortex-M4
- L1 Instruction Cache
 - 32 KB L1 Instruction Cache for A53
 - 16 KB L1 Instruction Cache for M4
- L1 Data Cache (each core)
 - 32 KB L1 Data Cache (A7)
 - 16 KB L1 Data Cache (M4)
- The ARM Cortex-A53 Core complex shares
 - General interrupt controller (GIC)
 - Global timer
 - Snoop control unit (SCU)
 - Unified instruction and data (1MB)

2.2 Memory

WB10 is available with up to 3GB of LPDDR4 memory. The default configuration is 1GB/2GB LPDDR4.

2.3 Power Management IC

WB10 features Rohm BD71837MWV power management IC. BD71837MWV is a programmable power management IC integrates 8 buck regulators and 7 LDOs to provide all power rails required by SoC and peripherals.

For system management, it provides the following features,

- Support software shutdown or hardware power off
- External wakeup source
- Output monitor
- PWROK signal for reset or power off
- OVP, UVLO, TSD

2.4 eMMC Storage

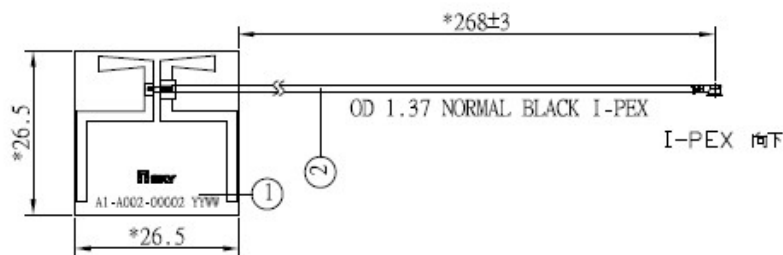
The onboard eMMC device is connected on the SD1 pins of the i.MX 8M processor in an 8 bit width configuration.

2.5 Wi-Fi/Bluetooth Module

The WB10 adopts Fn-Link 8274B combo module that integrates wireless local area network 802.11 a/b/g/n/ac 2x2 MIMO and Bluetooth 4.2.

2.6 Antenna

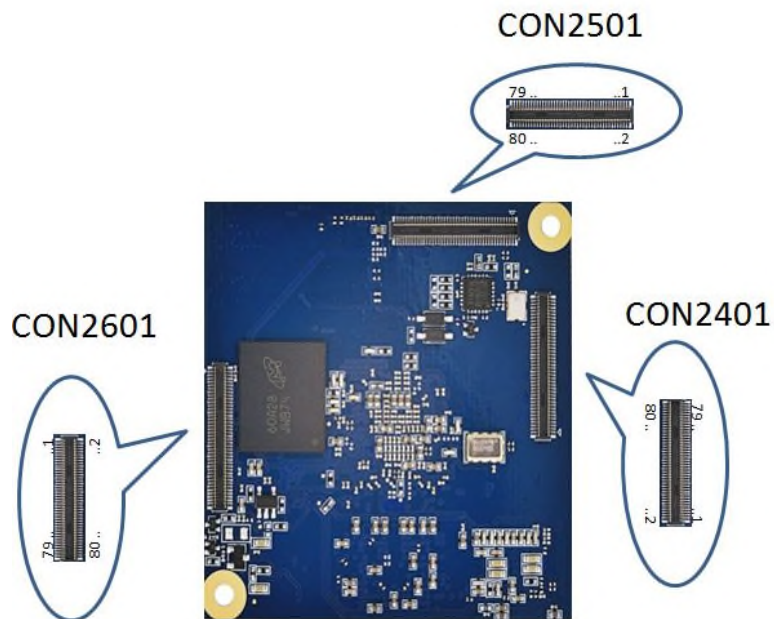
The module is shipped with an Embedded Wi-Fi Dual Band Antenna, only the antenna supplied with the module may be used. It is PCB type, using IPEX connector to connect with module.



Frequency (MHz)	2400	2450	2500	5150	5550	5850
Directivity (dBi)	4.95	5.17	5.36	7.26	6.68	7.38
Efficiency (dB)	-1.68	-1.62	-1.67	-1.63	-1.54	-1.63
Efficiency (%)	68.40	69.21	68.70	68.84	70.58	68.89
Peak Gain (dBi)	3.27	3.55	3.69	5.63	5.14	5.75

3 WB10 Interfaces and Connectors

WB10 is equipped with three [Hirose DF40C-80DP-0.4V\(51\)](#) connectors- CON2401, CON2501 and CON2601. The tables below detail the pin assignment and functionality of these connectors.



3.1 CON2601 Connector

Table 3-1 CON2601 Connector

CON2601 Pin#	Signal Name	i.MX8 Pin #	i.MX8 Ball Name	CON2601 Pin#	Signal Name	i.MX8 Pin #	i.MX8 Ball Name
1	PWRON_B	.		2	VDD_SD2	.	
3	BTB_GPIO5_IO7	A4	ECSPI1_MOSI	4	VDD_ETH_3V3	.	
5	BTB_GPIO5_IO6	D5	ECSPI1_SCLK	6	GND	.	
7	GND	.		8	GPIO3_IO6	G20	
9	PCIE2_RXM	D24		10	GPIO3_IO12	L19	
11	PCIE2_RXP	D25		12	GPIO3_IO15	K19	
13	GND	.		14	GPIO3_IO7	J20	
15	PCIE2_TXM	E24		16	GPIO3_IO16	K20	
17	PCIE2_TXP	E25		18	GPIO3_IO10	L20	
19	GND	.		20	GPIO3_IO8	H22	
21	PCIE2_REF_CLKM	F24		22	GPIO3_IO11	J22	
23	PCIE2_REF_CLKP	F25		24	GPIO3_IO9	J21	
25	GND	.		26	GPIO3_IO18	K21	
27	GPIO3_IO17	K22		28	GND	.	
29	SD2_CLK	L22		30	SD2_WP	M21	
31	GPIO3_IO14	M20		32	SD2_CMD	M22	

33	GPIO3_IO13	M19		34	SD2_DATA0	N22	
35	SD2_DATA3	P21		36	SD2_DATA1	N21	
37	SD2_nRST	R22		38	SD2_DATA2	P22	
39	SD2_nSDCD	L21		40	GND	.	
41	JTAG_TCK	T5		42	JTAG_TMS	V5	
43	JTAG_nTRST	U6		44	JTAG_TDO	U5	
45	GND	.		46	BOOT_MODE1	V6	
47	ETHER_TRXN3	.		48	BOOT_MODE0	W6	
49	ETHER_TRXP3	.		50	JTAG_TDI	W5	
51	GND	.		52	ONOFF	W21	ONOFF
53	ETHER_TRXN2	.		54	GND	.	
55	ETHER_TRXP2	.		56	LED_1000	.	
57	GND	.		58	LED_ACT	.	
59	ETHER_TRXN1	.		60	SYS_nRST	.	
61	ETHER_TRXP1	.		62	VDD_1V8	.	
63	GND	.		64	VDD_1V8	.	
65	ETHER_TRXN0	.		66	VDD_SNV5_3V3	.	
67	ETHER_TRXP0	.		68	PORn	W20	POR_B
69	GND	.		70	GND	.	
71	VDC_5V	.		72	VDC_5V	.	
73	VDC_5V	.		74	VDC_5V	.	
75	VDC_5V	.		76	VDC_5V	.	
77	VDC_5V	.		78	VDC_5V	.	
79	VDC_5V	.		80	VDC_5V	.	

3.2 CON2401 Connector

Table 3-2CON2401 Connector

CON2401 Pin#	Signal Name	i.Mx8 Pin #	i.MX8 Ball Name	CON2401 Pin#	Signal Name	i.Mx8 Pin #	i.MX8 Ball Name
1	HDMI_AUXM	V2		2	HDMI_CEC	P1	
3	HDMI_AUXP	V1		4	HDMI_DDC_SDA	P3	
5	GND	.		6	HDMI_DDC_SCL	R3	
7	HDMI_D0M	T2		8	HDMI_HPD	W2	
9	HDMI_D0P	T1		10	GND	.	
11	GND	.		12	HDMI_D1P	U2	
13	HDMI_D2P	N2		14	HDMI_D1M	U1	
15	HDMI_D2M	N1		16	GND	.	
17	GND	.		18	HDMI_D3M	M2	
19	SAI1_RXC	K1		20	HDMI_D3P	M1	

21	SAI1_RXD0	K2		22	GND	.	
23	SAI1_RXD3	J2		24	SAI1_RXD1	L2	
25	SAI1_RXD4	J1		26	SAI1_RXFS	L1	
27	SAI2_RXFS	J4		28	SAI1_RXD2	H2	
29	BTB_GPIO1_IO3	P4	GPIO1_IO03	30	SAI1_TXFS	H1	
31	BTB_GPIO1_IO1	T7	GPIO1_IO01	32	SAI2_RXC	H3	
33	SAI5_RXFS	N4		34	SAI2_TXFS	H4	
35	SAI5_RXD2	M4		36	SAI1_RXD7	G1	
37	BTB_GPIO1_IO5	P7	GPIO1_IO05	38	GND	.	
39	BTB_GPIO1_IO12	L7	GPIO1_IO12	40	SAI1_RXD6	G2	
41	GND	.		42	BTB_GPIO1_IO6	N5	GPIO1_IO06
43	SAI5_MCLK	K4		44	SAI5_RXD0	M5	
45	SAI5_RXD3	K5		46	BTB_GPIO1_IO8	N7	GPIO1_IO08
47	BTB_GPIO1_IO13	K6	GPIO1_IO13	48	GND	.	
49	BTB_GPIO1_IO15	J6	GPIO1_IO15	50	SAI5_RXD1	L4	
51	SAI2_MCLK	H5		52	SAI5_RXC	L5	
53	SAI2_RXD	H6		54	SAI2_TXC	J5	
55	SPDIF_RX	G6		56	SAI2_TXD	G5	
57	SPDIF_EXT_CLK	E6		58	SPDIF_TX	F6	
59	SAI1_TXD0	F2		60	SAI3_TXFS	G3	
61	GND	.		62	SAI1_RXD5	F1	
63	SAI3_RXD	F3		64	GND	.	
65	SAI1_TXC	E1		66	SAI3_RXFS	G4	
67	SAI1_TXD1	E2		68	SAI1_TXD3	D1	
69	SAI3_RXC	F4		70	SAI1_TXD4	D2	
71	SAI1_TXD7	C1		72	SAI3_TXD	C3	
73	SAI1_TXD5	C2		74	SAI3_MCLK	D3	
75	GND	.		76	GND	.	
77	SAI1_TXD2	B2		78	SAI1_TXD6	B3	
79	SAI1_MCLK	A3		80	SAI3_TXC	C4	

3.3 CON2501 Connector

Table 3-3CON2501 Connector

CON2501 Pin#	Signal Name	i.Mx8 Pin #	i.MX8 Ball Name	CON2501 Pin#	Signal Name	i.Mx8 Pin #	i.MX8 Ball Name
1	ECSP12_MOSI	E5		2	USB1_VBUS	D14	
3	ECSP12_MISO	B5		4	USB1_ID	C14	
5	I2C3_SDA	E9		6	UART2_TXD	D6	
7	I2C3_SCL	G8		8	UART2_RXD	B6	
9	USB2_VBUS	D9		10	ECSP12_SCLK	C5	
11	USB2_ID	C9		12	ECSP12_SS0	A5	
13	PCIE2_NCLKREQ	F9	I2C4_SDA	14	UART4_TXD (UART2_RTS)	D7	
15	I2C2_SCL	G7		16	UART4_RXD (UART2_CTS)	C6	
17	I2C2_SDA	F7		18	UART1_TXD	A7	
19	I2C1_SDA	E8		20	UART1_RXD	C7	
21	I2C1_SCL	E7		22	GND	.	
23	GND	.		24	DSI_D3P	B15	
25	DSI_CLKP	D16		26	DSI_D3M	A15	
27	DSI_CLKM	C16		28	DSI_D1P	B16	
29	DSI_D0P	B17		30	DSI_D1M	A16	
31	DSI_D0M	A17		32	GND	.	
33	GND	.		34	CSI2_CLKP	B19	
35	DSI_D2P	B18		36	CSI2_CLKM	A19	
37	DSI_D2M	A18		38	GND	.	
39	GND	.		40	CSI2_D2P	B21	
41	CSI2_D1P	B20		42	CSI2_D2M	A21	
43	CSI2_D1M	A20		44	GND	.	
45	GND	.		46	CSI1_CLKP	B22	
47	CSI2_D3P	D19		48	CSI1_CLKM	A22	
49	CSI2_D3M	C19		50	GND	.	
51	GND	.		52	CSI1_D0P	B23	
53	CSI2_D0P	D20		54	CSI1_D0M	A23	
55	CSI2_D0M	C20		56	GND	.	
57	GND	.		58	CSI1_D3P	D21	
59	CSI1_D1M	C22		60	CSI1_D3M	C21	
61	CSI1_D1P	D22		62	GND	.	
63	GND	.		64	USB2_RXP	A8	
65	CSI1_D2M	B24		66	USB2_RXN	B8	
67	CSI1_D2P	C23		68	USB2_TXP	A9	
69	GND	.		70	USB2_TXN	B9	
71	USB2_DP	A10		72	USB1_RXP	A12	
73	USB2_DN	B10		74	USB1_RXN	B12	
75	USB1_DP	A14		76	USB1_TXP	A13	
77	USB1_DN	B14		78	USB1_TXN	B13	
79	VDDIO_3V3	.		80	VDDIO_3V3	.	

4 WB10Interfaces

4.1 Power Signals

Table 4-1 Power Signal Pins

Connector PIN#	WB10Function	I/O	Description
CON2601 71, 72, 73, 74, 75, 76, 77, 78, 79, 80	VDC_5V	I	Input power 5V
CON2601 62, 64	VDD_1V8	O	1.8V power
CON2601 66	VDD_SNV5_3V3	O	RTC power
CON2601 4	VDD_ETH_3V3	O	Ethernet indicationLED power
CON2601 2	VDD_SD2	O	SD card power
CON2601 60	SYS_nRST	I	SOM Reset
CON2601 1	PWRON_B	I	Power On-Off Key
CON2501 79, 80	VDDIO_3V3	O	3.3V IO power
CON2501 2	USB1_VBUS	I	USB1 VBUS input power
CON2501 9	USB2_VBUS	I	USB2 VBUS input power

4.2 GPIO

WB10 SOM has 15 dedicate pins for GPIO purpose, moreover the pins are not used in other function (SDIO, SPI, UART, SAI..) can be configured as GPIO as well. The power domain of WB10 SOM IOs is VDDIO_3V3.

Table 4-2 GPIO Signal Pins

Connector PIN#	WB10 Function	I/O	Description
CON2601 3, 5, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 27, 31, 33,	GPIO	I/O	GPIO (3.3V)

** Unused pins in other function (SDIO, SPI, UART, SAI) can be configured as GPIO.*

4.3 Ethernet

One Gigabit Ethernet interface is supported.

Table 4-3 Ethernet Signal Pins

Connector PIN#	WB10Function	I/O	Description
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CON2601 56	LED1000	O	Ethernet LED1 control
CON2601 58	LED_ACT	O	Ethernet LED2 control
CON2601 67	ETHER_TRXP0	IO	Ethernet_TRXP
CON2601 65	ETHER_TRXN0	IO	Ethernet_TRXN
CON2601 61	ETHER_TRXP1	IO	Ethernet_TRXP
CON2601 59	ETHER_TRXN1	IO	Ethernet_TRXN
CON2601 55	ETHER_TRXP2	IO	Ethernet_TRXP
CON2601 53	ETHER_TRXN2	IO	Ethernet_TRXN
CON2601 49	ETHER_TRXP3	IO	Ethernet_TRXP
CON2601 47	ETHER_TRXN3	IO	Ethernet_TRXN

4.4 USB

The USB interface which provides high speed USB functionality conforms to the USB3.0. The OTG controller conforms to OTG2.0 specification.

Table 4-4 USB Signal Pins

Connector PIN#	WB10Function	I/O	Description
CON2501 2	USB1_VBUS	I	USB1_VBUS
CON2501 4	USB1_ID	I	USB1_ID
CON2501 9	USB2_VBUS	I	USB2_VBUS
CON2501 11	USB2_ID	I	USB2_ID
CON2501 75	USB1_DP	IO	USB1_DP
CON2501 77	USB1_DN	IO	USB1_DN
CON2501 71	USB2_DP	IO	USB2_DP
CON2501 73	USB2_DN	IO	USB2_DN
CON2501 72	USB1_RXP	IO	USB1_RXP
CON2501 74	USB1_RXN	IO	USB1_RXN
CON2501 76	USB1_TXP	IO	USB1_TXP
CON2601 78	USB1_TXN	IO	USB1_TXN
CON2501 64	USB2_RXP	IO	USB2_RXP
CON2501 66	USB2_RXN	IO	USB2_RXN

CON2501 68	USB2_TXP	IO	USB2_TXP
CON2501 70	USB2_TXN	IO	USB2_TXN

4.5 UARTs

Each of the UART interface support the following serial data transmit/receive protocols and configurations:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 4-5 UART Signal Pins

Connector PIN#	WB10 Function	I/O	Description
CON2501 6	UART2_TXD	O	UART2_TXD
CON2501 8	UART2_RXD	I	UART2_RXD
CON2501 14	UART4_TXD	O	UART4_TXD
CON2501 16	UART4_RXD	I	UART4_RXD
CON2501 18	UART1_TXD	O	UART1_TXD
CON2501 20	UART1_RXD	I	UART1_RXD

4.6 I2Cs

WB10SOM has three I2C interfaces which provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 4-6 I2C Signal Pins

Connector PIN#	WB10 Function	I/O	Description
CON2501 5	I2C3_SDA	IO	I2C3_SDA
CON2501 7	I2C3_SCL	IO	I2C3_SCL

CON2501 15	I2C2_SCL	IO	I2C2_SCL
CON2501 17	I2C2_SDA	IO	I2C2_SDA
CON2501 19	I2C1_SDA	IO	I2C1_SDA
CON2501 21	I2C1_SCL	IO	I2C1_SCL

4.7 eCSPI

WB10 SOM supports one full-duplex Enhanced Configurable Serial Peripheral Interface (ECSPI).

The ECSPI contain a 64x32 receive buffer and a 64x32 transmit buffer.

Table 4-7eSPI Signal Pins

Connector PIN#	WB10 Function	I/O	Description
CON2501 1	ECSPI2_MOSI	O	ECSPI2_MOSI
CON2501 3	ECSPI2_MISO	I	ECSPI2_MISO
CON2501 10	ECSPI2_SCLK	O	ECSPI2_SCLK
CON2501 12	ECSPI2_SS0	O	ECSPI2_SS0

4.8 DSI Interface

WB10SOM provides a 4-lanes MIPI display interface operating up to 1080p60 resolution.

Table 4-8 DSI Signal Pins

Connector PIN#	WB10 Function	I/O	Description
CON2501 25	DSI_CLKP	O	DSI_CLKP
CON2501 27	DSI_CLKM	O	DSI_CLKM
CON2501 29	DSI_D0P	O	DSI_D0P
CON2501 31	DSI_D0M	O	DSI_D0M
CON2501 28	DSI_D1P	O	DSI_D1P
CON2501 30	DSI_D1M	O	DSI_D1M
CON2501 35	DSI_D2P	O	DSI_D2P

CON2501 37	DSI_D2M	O	DSI_D2M
CON2501 24	DSI_D3P	O	DSI_D3P
CON2501 26	DSI_D3M	O	DSI_D3M

4.9 MIPI CSI interface

This module provides a two 4-lanes MIPI camera interface operating up to a maximum bit rate of 1.5 Gbps per lane, providing 4K@30fps capability for the 4 lanes.

Table 4-9 CSI Signal Pins

Connector PIN#	WB10 Function	I/O	Description
CON2501 34	CSI2_CLKP	I	CSI2_CLKP
CON2501 36	CSI2_CLKM	I	CSI2_CLKM
CON2501 53	CSI2_D0P	I	CSI2_D0P
CON2501 55	CSI2_D0M	I	CSI2_D0M
CON2501 41	CSI2_D1P	I	CSI2_D1P
CON2501 43	CSI2_D1M	I	CSI2_D1M
CON2501 40	CSI2_D2P	I	CSI2_D2P
CON2501 42	CSI2_D2M	I	CSI2_D2M
CON2501 47	CSI2_D3P	I	CSI2_D3P
CON2501 49	CSI2_D3M	I	CSI2_D3M
CON2501 46	CSI1_CLKP	I	CSI1_CLKP
CON2501 48	CSI1_CLKM	I	CSI1_CLKM
CON2501 52	CSI1_D0P	I	CSI1_D0P
CON2501 54	CSI1_D0M	I	CSI1_D0M
CON2501 61	CSI1_D1P	I	CSI1_D1P
CON2501 59	CSI1_D1M	I	CSI1_D1M
CON2501 65	CSI1_D2P	I	CSI1_D2P
CON2501 67	CSI1_D2M	I	CSI1_D2M
CON2501 58	CSI1_D3P	I	CSI1_D3P
CON2501 60	CSI1_D3M	I	CSI1_D3M

4.10 PWM

The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO.

Table 4-10 PWN Signal Pins

Connector PIN#	WB10Function	I/O	Description
CON2401 29	BTB_GPIO1_IO3	IO	PWM1
CON2401 31	BTB_GPIO1_IO1	IO	PWM2

4.11 SD/MMC

Fully compatible with MMC command/response set and Physical Layer as defined in the MultimediaCard System Specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.

- Fully compatible with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications v 3.0 including high-capacity SDXC cards up to 2 TB.
- Fully compatible with SDIO command/response sets and interrupt/Read-Wait mode as defined in the SDIO Card Specification, Part E1, v. 3.0

Table 4-11 SD/MMC Signal Pins

Connector PIN#	WB10Function	I/O	Description
CON2601 30	SD2_WP	O	SD2 Write Protection
CON2601 37	SD2_nRST	O	SD2 Rest
CON2601 32	SD2_CMD	O	SD2_CMD
CON2601 39	SD2_nSDCD	I	SD2 Card detection
CON2601 34	SD2_DATA0	IO	SD2_DATA0
CON2601 36	SD2_DATA1	IO	SD2_DATA1
CON2601 38	SD2_DATA2	IO	SD2_DATA2
CON2601 35	SD2_DATA3	IO	SD2_DATA3

4.12 SAIs

The SAI interface provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM and codec/DSP interfaces.

Table 4-12 SAI1 Signal Pins

CON2401 PIN#	WB10 Function	I/O	Description
79	SAI1_MCLK	O	SAI1_MCLK
19	SAI1_RXC	I	SAI1_RXC
26	SAI1_RXFS	I	SAI1_RXFS
21	SAI1_RXD0	I	SAI1_RXD0
24	SAI1_RXD1	I	SAI1_RXD1
28	SAI1_RXD2	I	SAI1_RXD2
23	SAI1_RXD3	I	SAI1_RXD3
25	SAI1_RXD4	I	SAI1_RXD4
62	SAI1_RXD5	I	SAI1_RXD5
40	SAI1_RXD6	I	SAI1_RXD6
36	SAI1_RXD7	I	SAI1_RXD7
30	SAI1_TXFS	O	SAI1_TXFS
65	SAI1_TXC	O	SAI1_TXC
59	SAI1_TXD0	O	SAI1_TXD0
67	SAI1_TXD1	O	SAI1_TXD1
77	SAI1_TXD2	O	SAI1_TXD2
68	SAI1_TXD3	O	SAI1_TXD3
70	SAI1_TXD4	O	SAI1_TXD4
73	SAI1_TXD5	O	SAI1_TXD5
78	SAI1_TXD6	O	SAI1_TXD6
71	SAI1_TXD7	O	SAI1_TXD7

Table 4-13 SAI2,3,5 Signal Pins

CON2401 PIN#	WB10 Function	I/O	Description
51	SAI2_MCLK	O	SAI2_MCLK
32	SAI2_RXC	I	SAI2_RXC
27	SAI2_RXFS	I	SAI2_RXFS
53	SAI2_RXD	I	SAI2_RXD
54	SAI2_TXC	O	SAI2_TXC
34	SAI2_TXFS	O	SAI2_TXFS
56	SAI2_TXD	O	SAI2_TXD
74	SAI3_MCLK	O	SAI3_MCLK
69	SAI3_RXC	I	SAI3_RXC
66	SAI3_RXFS	I	SAI3_RXFS
63	SAI3_RXD	I	SAI3_RXD

80	SAI3_TXC	O	SAI3_TXC
60	SAI3_TXFS	O	SAI3_TXFS
72	SAI3_TXD	O	SAI3_TXD
43	SAI5_MCLK	O	SAI5_MCLK
52	SAI5_RXC	I	SAI5_RXC
33	SAI5_RXFS	I	SAI5_RXFS
44	SAI5_RXD0	I	SAI5_RXD0
50	SAI5_RXD1	I	SAI5_RXD1
35	SAI5_RXD2	I	SAI5_RXD2
45	SAI5_RXD3	I	SAI5_RXD3

4.13 HDMI

WB10SOM support HDMI TX port with HDMI 2.0a specification.

Table 4-14 HDMI Signal Pins

CON2401 PIN#	WB10 Function	I/O	Description
1	HDMI_AUXM	I	HDMI_AUXM
3	HDMI_AUXP	I	HDMI_AUXP
2	HDMI_CEC	IO	HDMI_CEC
4	HDMI_DDC_SDA	IO	HDMI_DDC_SDA
6	HDMI_DDC_SCL	O	HDMI_DDC_SCL
7	HDMI_D0M	O	HDMI_D0M
9	HDMI_D0P	O	HDMI_D0P
12	HDMI_D1P	O	HDMI_D1P
14	HDMI_D1M	O	HDMI_D1M
15	HDMI_D2M	O	HDMI_D2M
13	HDMI_D2P	O	HDMI_D2P
18	HDMI_D3M	O	HDMI_D3M
20	HDMI_D3P	O	HDMI_D3P
8	HDMI_HPD	I	HDMI_HPD

4.14 SPDIF

WB10SOM supports Sony/Philips Digital Interface with 24-bit data width.

Table 4-15 SPDIF Signal Pins

CON2401 PIN#	WB10Function	I/O	Description
55	SPDIF_RX	I	SPDIF_RX
57	SPDIF_EXT_CLK	I	SPDIF_EXT_CLK
58	SPDIF_TX	O	SPDIF_TX

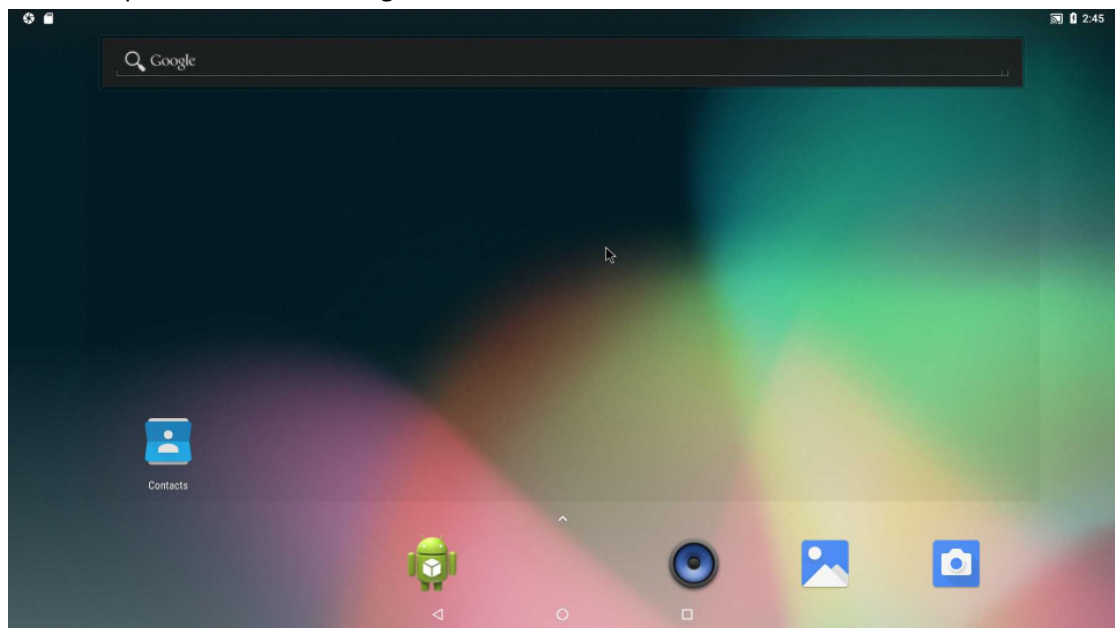
4.15 PCIe

Table 4-16 PCIe Signal Pins

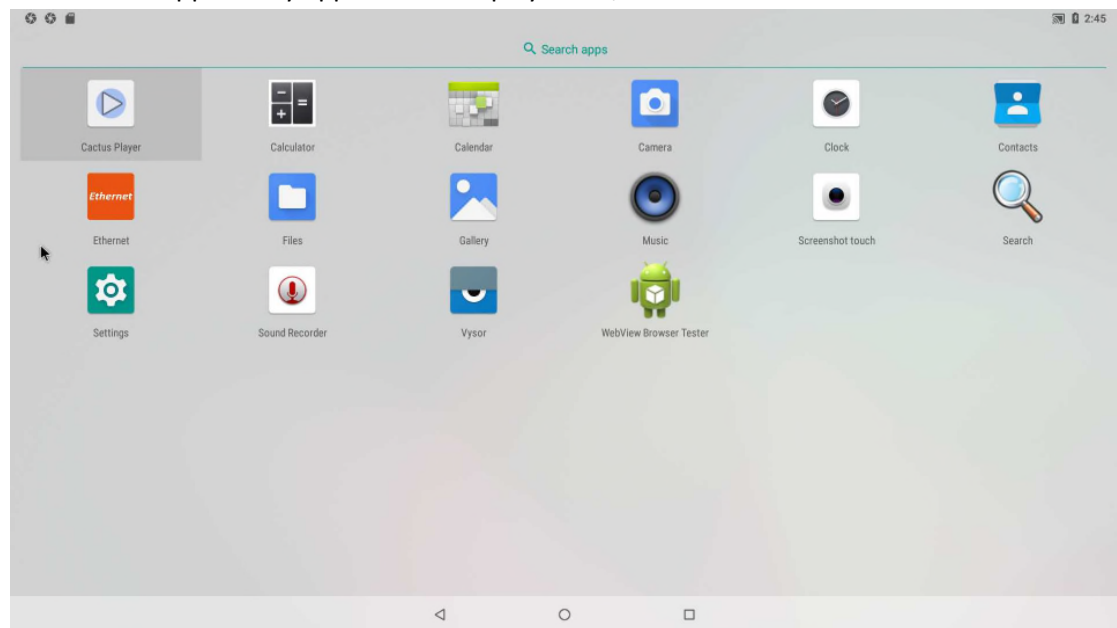
CON2601 PIN#	WB10Function	I/O	Description
9	PCIE2_RXM	I	Rx Data_M
11	PCIE2_RXP	I	Rx Data_P
15	PCIE2_TXM	O	Tx Data_M
17	PCIE2_TXP	O	Tx Data_P
21	PCIE2_REF_CLKM	O	CLK_M
23	PCIE2_REF_CLKP	O	CLK_P

5 Getting start

1. The SoM can function power on 5V DC input, once system start, WB10 can use EVB HDMI output or use USB sharing to external monitor for control.



2. You can use App for any application like play video, music etc.



6 Reference Documents

3. i.MX 8M Family of Applications Processors Datasheet
4. i.MX 8M Family of Applications Processor Reference Manual
5. BD71837MWV Data sheet
6. Fn-Link 8274B Combo Wi-Fi Module Datasheet
7. LAN AR8035 Datasheet

Federal Communication Commission Interference Statement

15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

15.21

Any changes or modifications not expressly approved by the party responsible for compliance could void the authority to operate equipment.

This device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

End-users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

For product available in the USA/Canada market, only channel 1~11 can be operated. Selection of other channels is not possible

FCC RF Radiation Exposure Statement:

This module is intended for OEM integrator. The OEM integrator is still responsible for the FCC compliance requirement of the end product, which integrates this module. 20cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the FCC radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.



If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: YAIWB10 ". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

MIC Statement

- 5GHz product for indoor use only
- 「5.2GHz 帯を使用する登録局と通信する場合を除き屋外使用禁止」
- 「5.2GHz 帯を使用する登録局と通信する場合を除き屋内においてのみ使用可能」
- 「5.2GHz 帯登録局と通信する場合を除き屋内においてのみ使用可能」