

Schematics

Brand name: InnoComm

Model Name: WB15

Mozart SoM DVT

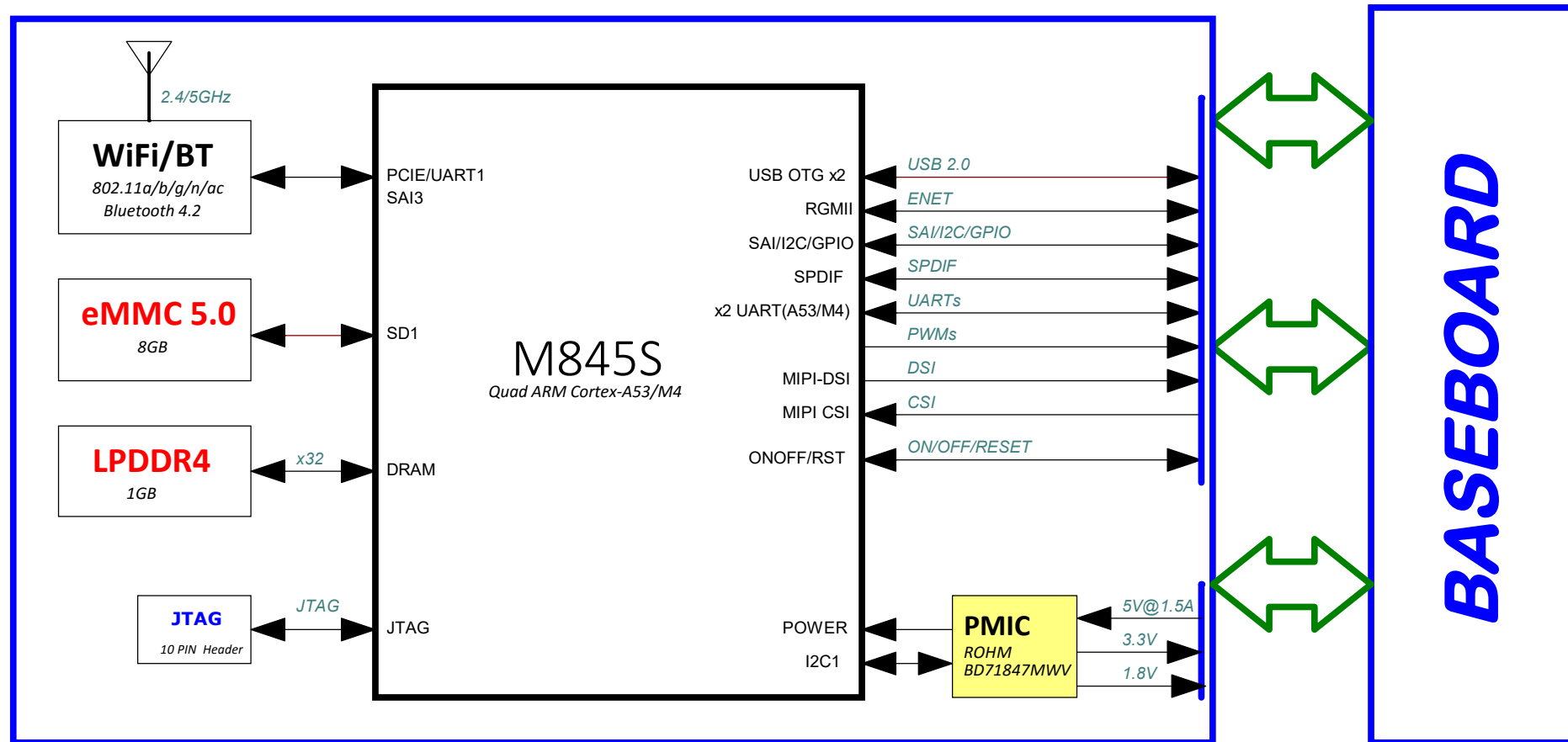


Table of Content

Page 1	Block Diagram	Page 7	CPU PWR
Page 2	Change history	Page 8	PMIC
Page 3	CPU MISC/DSI/CSI/USB	Page 9	SOM Interface
Page 4	CPU SAI/eNET/UART/I2C/GPIO	Page 10	Wi-Fi/Bluetooth
Page 5	CPU DRAM&LPDDR4	Page 11	Boot Configurations
Page 6	CPU NAND/SDHC&eMMC		

EVT1 version

2018/10/26

1. New schematic drawing

EVT2 version

2018/12/13

1. Change WIFI module for PCIe port
2. eMMC use SD1 port
3. All CPU GPIO power change to 3.3V except SD1
4. Add DDR/HW/BTB ID pin
5. Change M.2 and BTB con. pinout
6. C405 change to 1uF Cap.
7. Y201 change part symbol
8. All CPU clock signals add damping resistor
9. All I2C PU resistor change to NM except I2C1
10. Decrease PMIC DC/DC decoupling Cap.
10. R1956 change to NM

DVT version

2019/03/07

1. Change Boot_mode pin PD 100K ----Page3
2. Add JTAG nTRST & TDO PU 10K
Change TMS & TDI PU NM to 10K --- Page3
3. Change I2C1 PU 10K to 47K
Change I2C4 PU NM to 47K --- Page4
4. Change R2121 for GPIO1_IO00 PU 47K
Change R2122 for GPIO1_IO02 PU 47K
Change R2123 for GPIO1_IO03 PU 47K
Change R2124 for GPIO1_IO04 PD 47K
Add R2131 for GPIO1_IO05 PU 47K ---- Page4
5. Add R2134~7 for UART1 PU 47K ---- Page4
6. Add R2297 for UART2_RXD PU 47K
Add R2298 for UART2_TXD PU NM ---- Page4
7. DRAM ID function change to NAND_WE_B,
NAND_WP_B,QSPIA_DATA3 pins
and Add PD 47K / PU NM---- Page5
8. Del SD1_RESET_B series resistor R2119 ---- Page6
9. Add SD2 port PU 47K---- Page6
10. Add NAND port for WIFI GPIO function PU 47K---- Page6
11. Change PMIC BUCK VIN Cap to 22UF- Page8
12. Del PMIC_nINT,WDOG_B,I2C1_SDA,I2C1_SCL,SD2_VSEL
signal series 0R Resistor- Page8
13. Del WIFI module useless testpoint ---- Page10
14. Del WIFI module useless sleep clock circuit---- Page10
15. Del WIFI module GPIO series 0R resistor
and Add testpoint---- Page10
16. Change WIFI Power Bead to 0R Resistor
Change WIFI Power Cap to 22UF ---- Page10
17. Add BT ANT matching circuit--- Page10
18. Del Boot Device ID resistor -- Page11
19. HW ID function change to SAI5_RXFS,
SAI5_MCLK,GPIO1_IO13 pins
and Add PD 47K / PU NM---- Page11
20. Del BTB ID function resistor --- Page9

2019/03/08

1. Add Testpoint to WIFI pin 91&92 ----Page10
2. Change JTAG header J204 to NM ----Page3
3. Add 100R series resistor to ONOFF and SYS_nRST --- Page9
4. Add C609 & C610 Cap for WIFI Power --- Page10
5. Change HW ID setting to 001 --- Page11
6. Add 22R series resistor to SAI1_TXD7 and QSPIA_SCLK --- Page4,6

2019/03/11

1. Change SDIO port PU to 47K --- Page6
2. Add WIFI JTAG Port testpoint --- Page10

2019/03/19

1. Change REF_CLK_32K PU to NM --- Page4

2019/04/10

1. Change R2298 from NM to 47K --- Page4

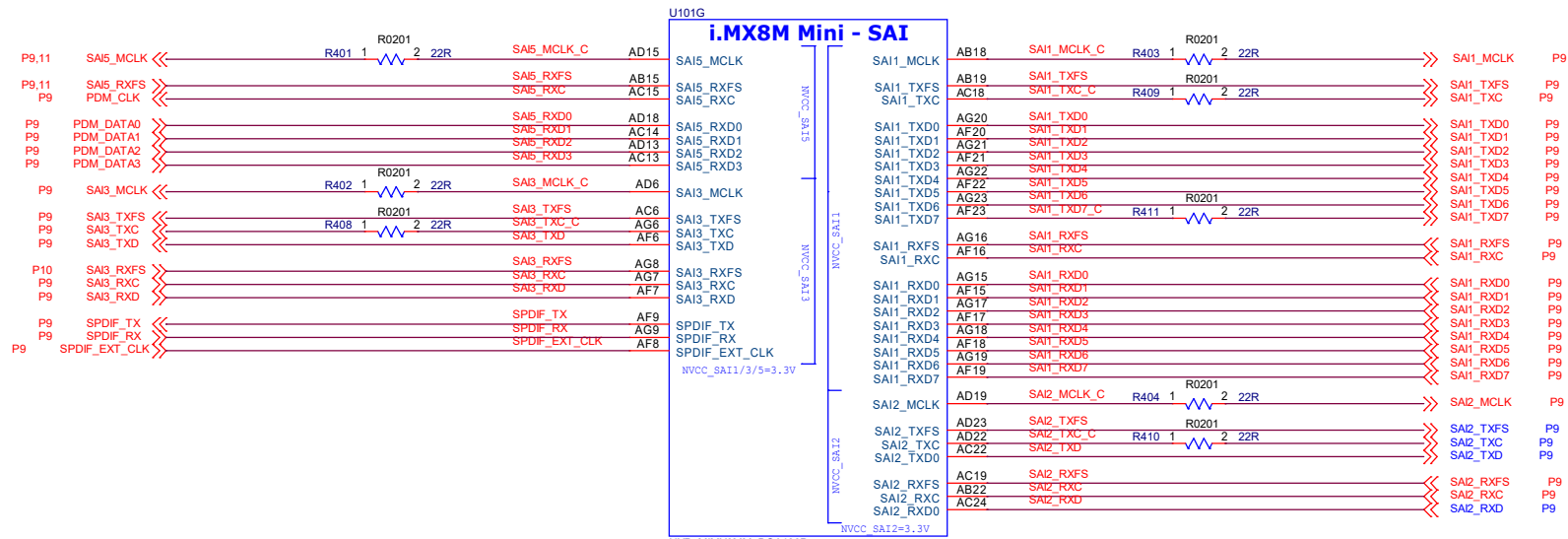
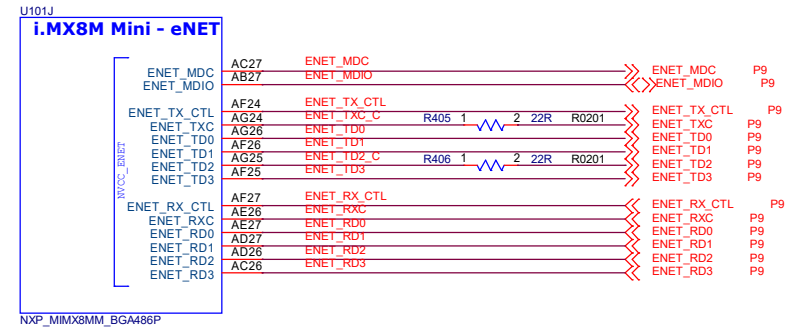
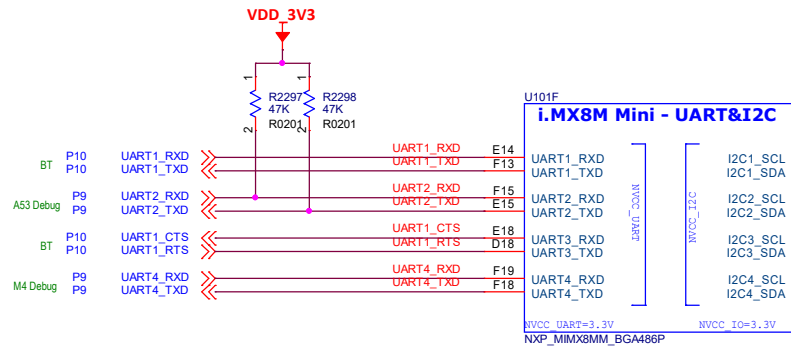
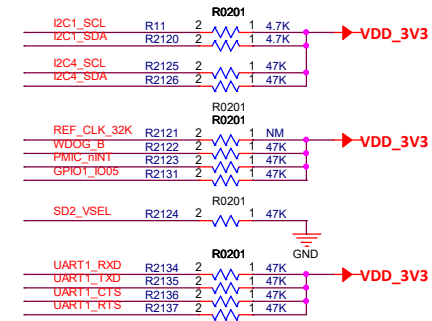
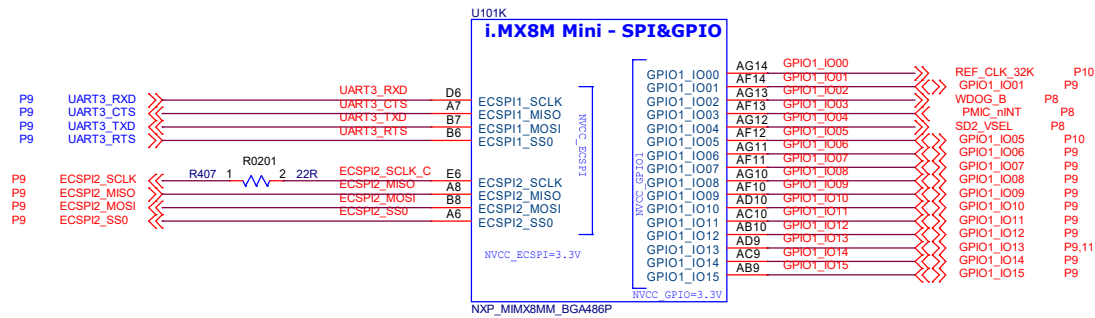
2019/04/24

1. Change HW ID to 010 --- Page11

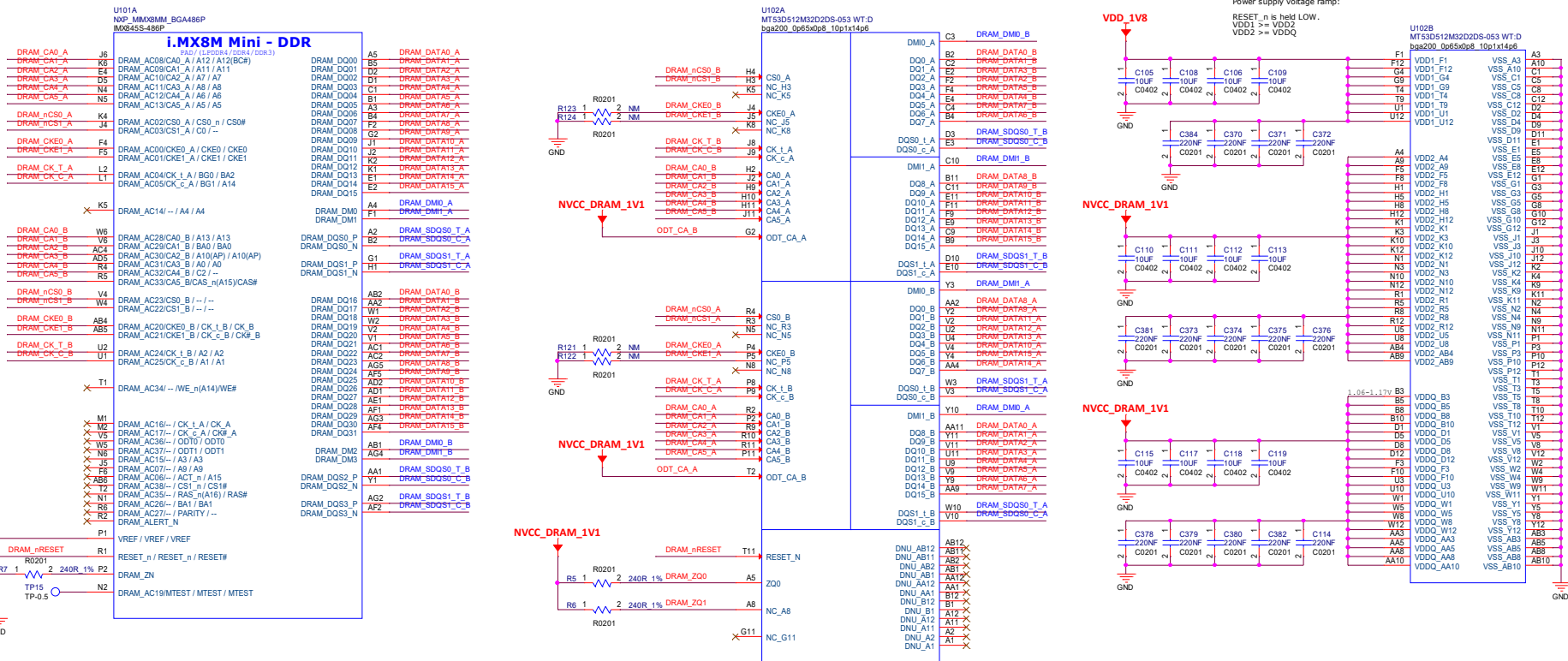
2019/07/11

1. Change HW ID to 011 --- Page11
2. Change C604,C605 to 1uF --- Page10

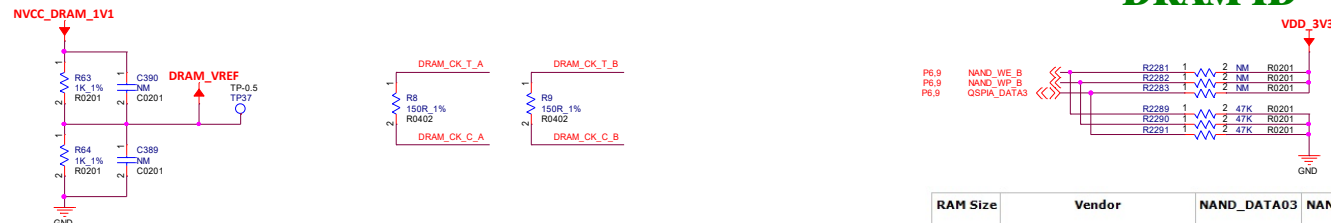
		InnoComm Mobile Technology Corp.	
Project Name : Mozart		Title : i.MX8M-MINI SoM	
Size : A3	Document Number : Change history	Rev : R003	
Date: Thursday, July 11, 2019		Sheet : 2	of 11



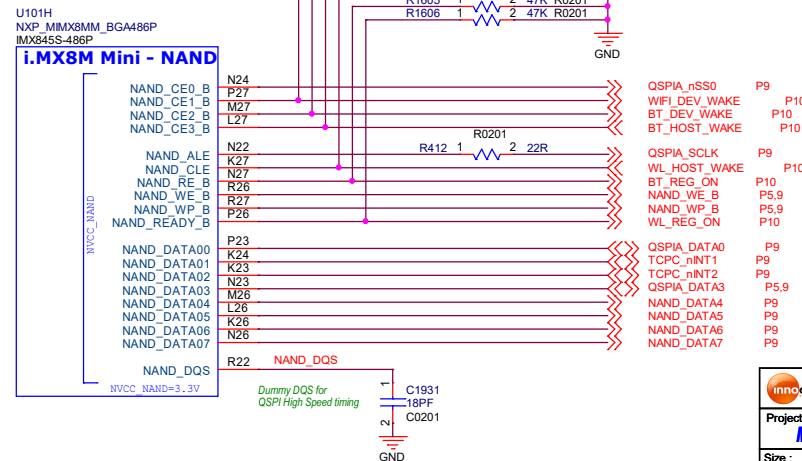
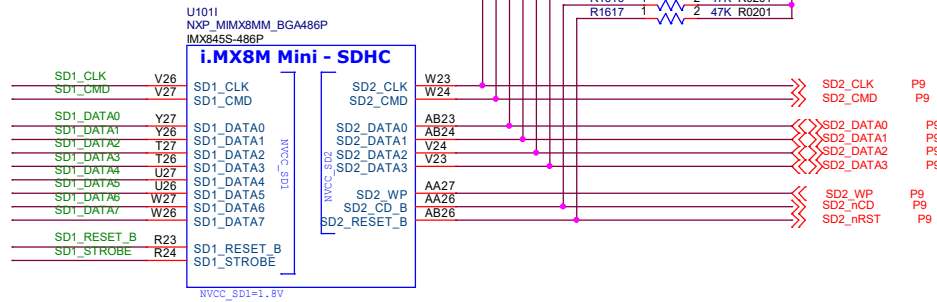
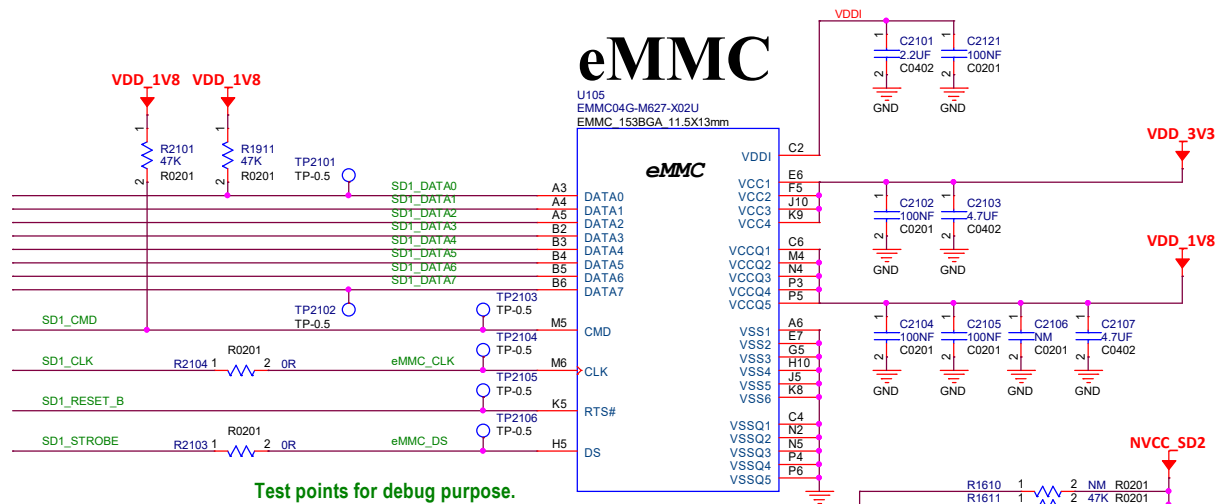
LPDDR4



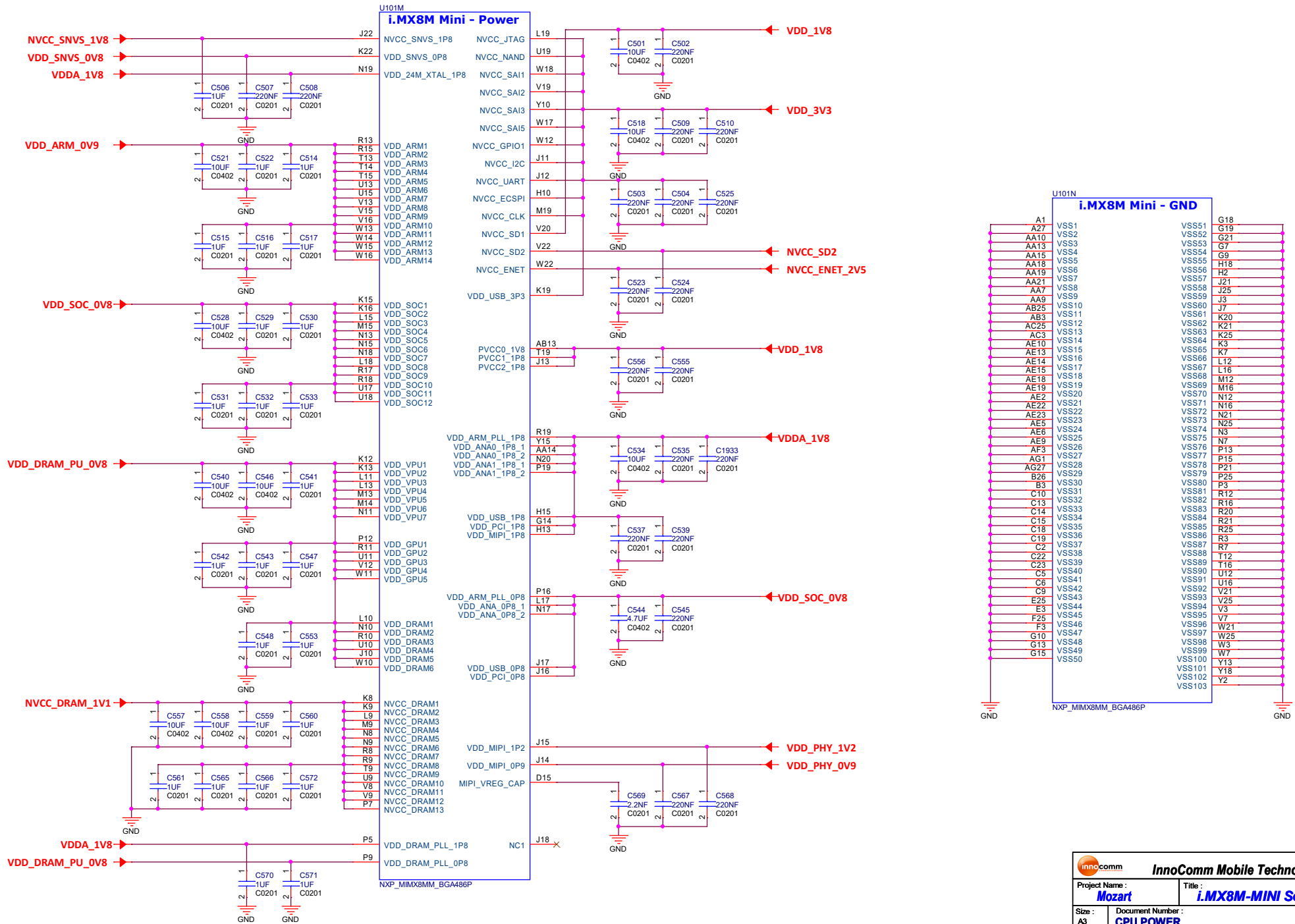
DRAM ID

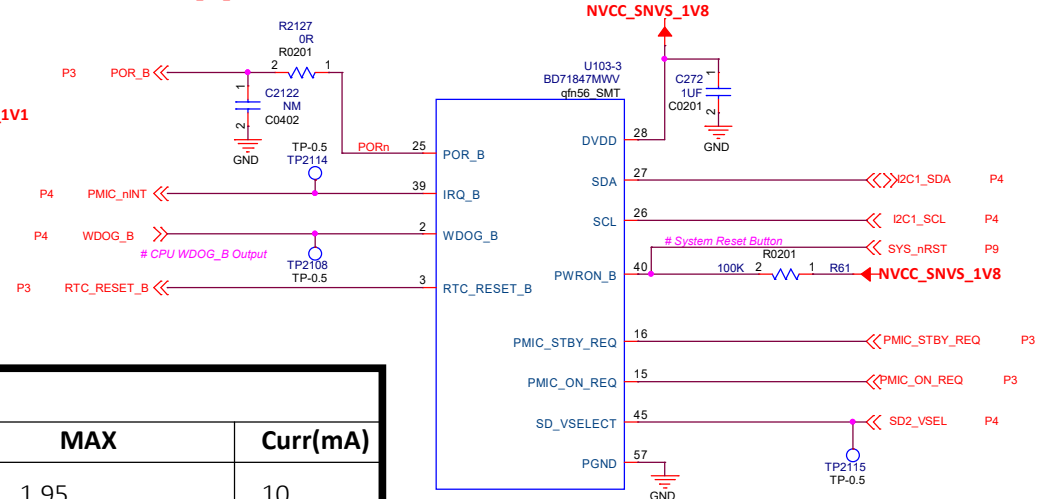
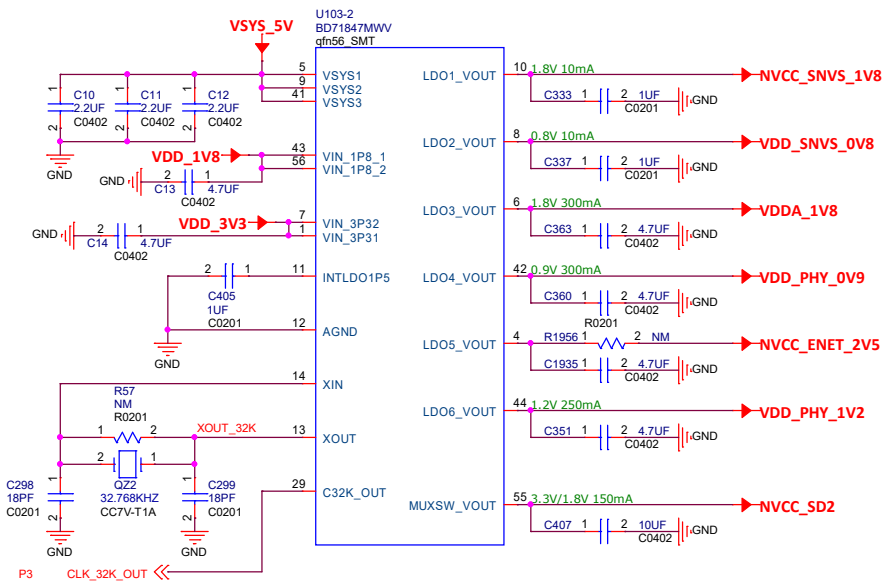
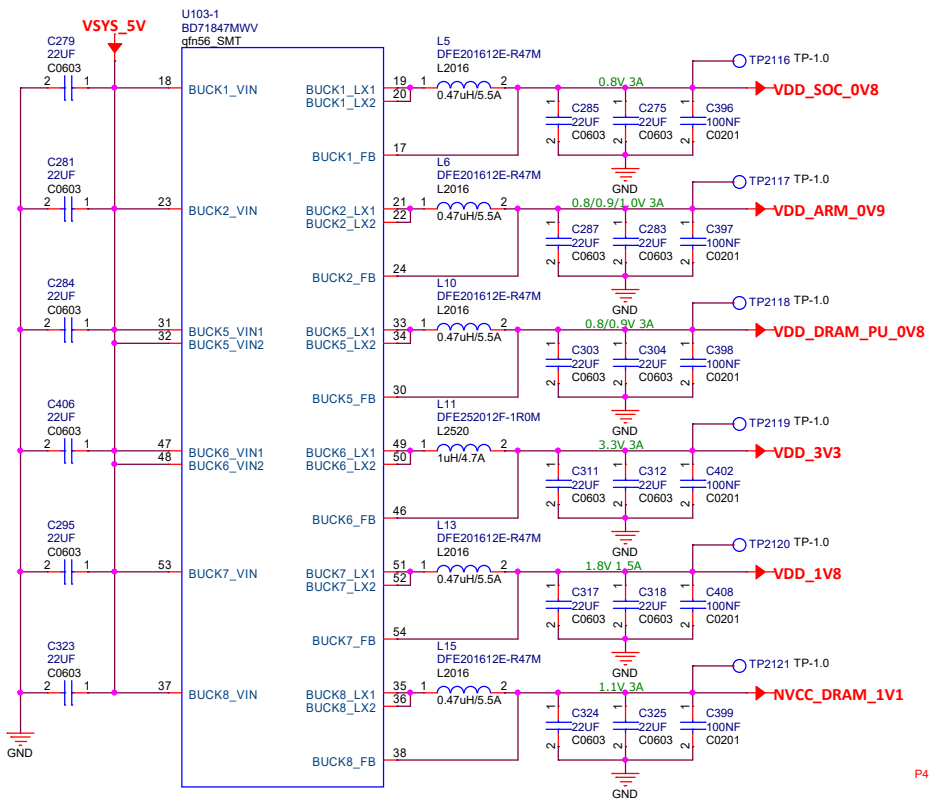


RAM Size	Vendor	NAND_DATA03	NAND_WP_B	NAND_WE
1GB	Leahkinn(LTHS0006FS4-ZNG1) Micron (MTS3B256M32D1) Kingston(D2516PC1CDGPLR)	0	0	0



M845S PWR

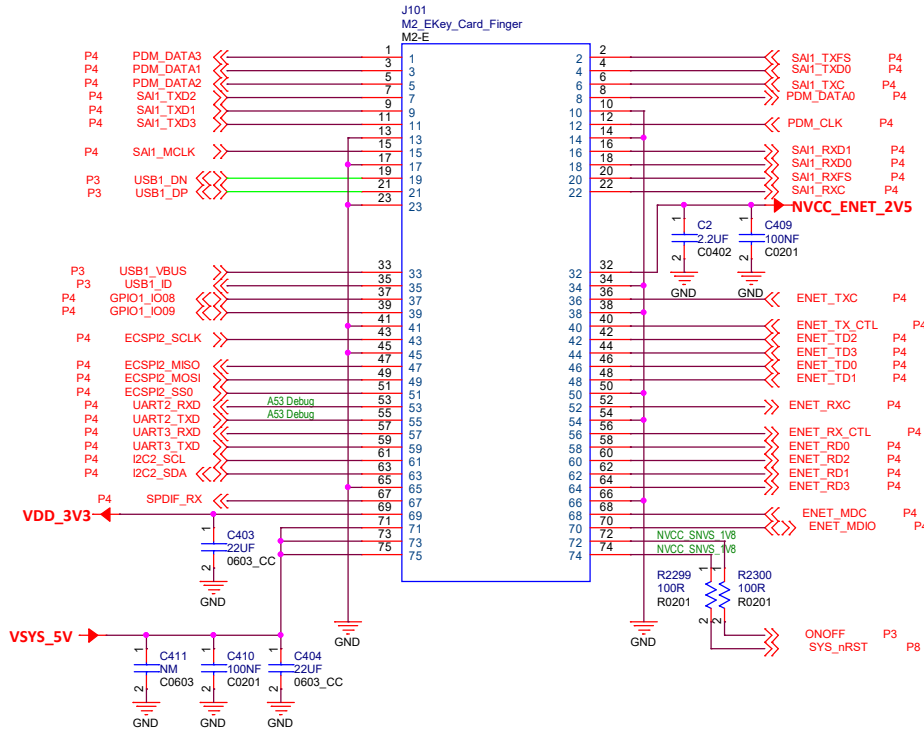




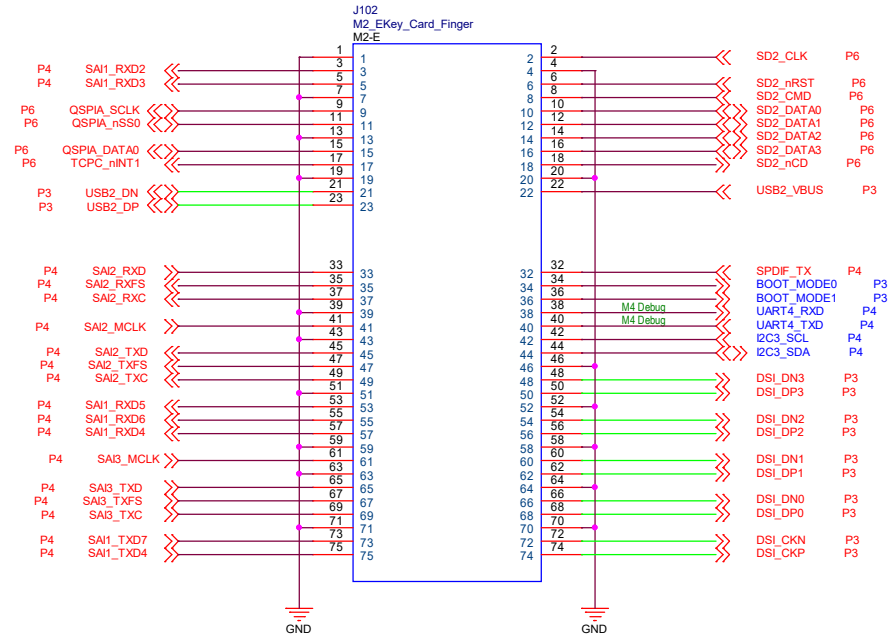
i.MX8M Mini LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Curr(mA)
1	NVCC_SNVS	LDO1	1.65	1.8	1.95	10
2	VDD_SNVS	LDO2	0.72/0.81	0.8	0.89/0.945	10
3	RTC_RESET_B	RTC_CLK	--	--	--	--
4	32K_OUT	RTC_RESET_B	--	--	--	--
5	VDD_SOC&VDDA_OP8&PHY_OP8	BUCK1	0.72	0.8	0.88	3600
6	VDD_GPU&VPU&DRAM	BUCK5	0.72/0.81	0.8/0.9	0.88/0.945	2500
6	PHY_OV9	LDO4	0.81	0.9	0.945	250
7	VDD_ARM	BUCK2	0.72/0.81/0.9	0.8/0.9/1.0	0.88/0.945/1.025	4000
7	VDDA_1P8&VDDA_DRAM	LDO3	1.71	1.8	1.89	300
8	NVCC_1V8	BUCK7	1.65	1.8	1.95	1500
9	NVCC_DRAM	BUCK8	1.045	1.1	3.6	3000
10	NVCC_3V3	BUCK6	3	3.3	3.6	3000
10	NVCC_SD2	MUXSW	3.0/1.65	3.3/1.8	1.155	150
11	PHY_1V2	LDO6	1.14	1.2	1.26	300
12	POR_B	POR_B	--	--	--	--

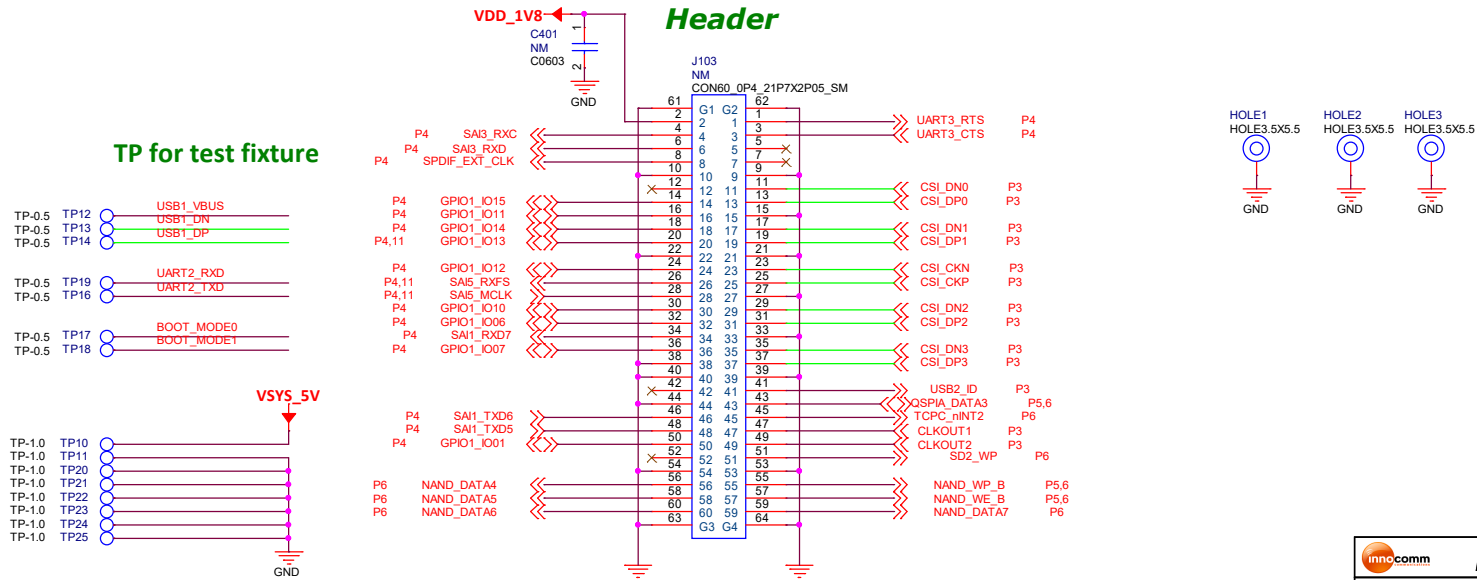
M.2 Con1



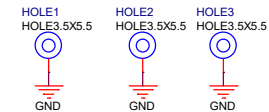
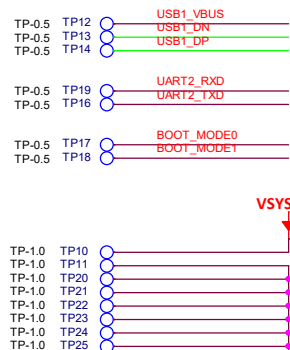
M.2 Con2

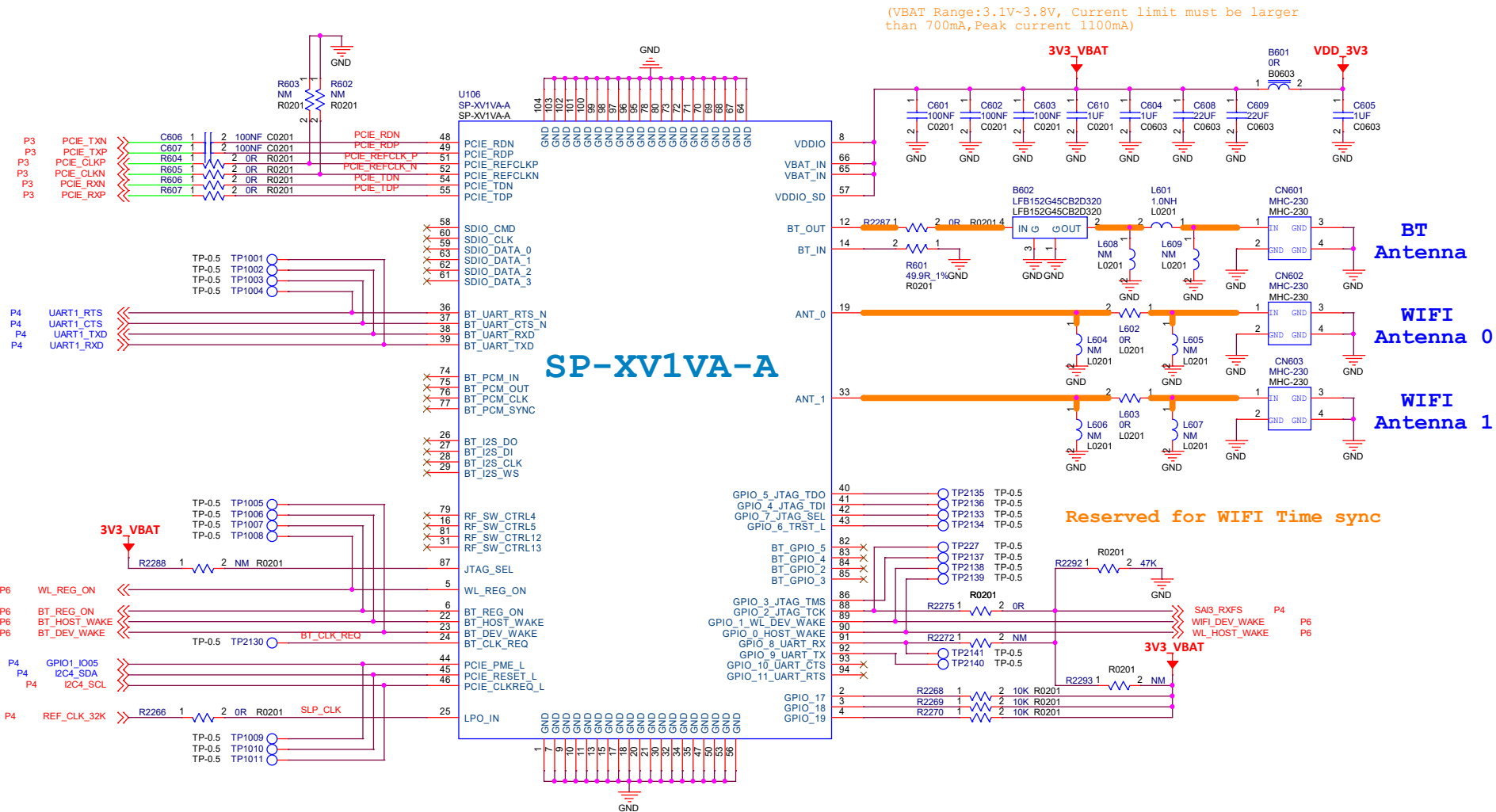


Header



TP for test fixture





i.MX8M Mini ROM Fuse

Address		7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
SD/eSD	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0x470[15:8]		010 - MMC/eMMC						
NAND	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
FlexSPI	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR		
SPINOR	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSP1 001 - eCSP2 010 - eCSP3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved	USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V	
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.				Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Boot Device: eMMC/SDHC1

BOOT_CFG[0-7]: 11100100

BOOT_CFG[8-15]: 01000100

Boot Device: MicroSD/SDHC2

BOOT_CFG[0-7]: 01000000

BOOT_CFG[8-15]: 01101000

BT_MODE

BOOT_MODE1	BOOT_MODE0
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BOOT TYPE:

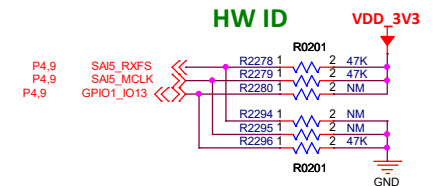
00 Boot From Fuses

01 Serial Downloader

10 Internal Boot (Development)

11 Reserved

Version	GPIO1_IO13	SAI5_MCLK	SAI5_RXFS
EVT2	0	0	0
DVT-A	0	0	1
DVT-B	0	1	0
DVT-C	0	1	1



inno comm		InnoComm Mobile Technology Corp.	
Project Name : Mozart		Title : i.MX8M-MINI SoM	
Size : A3	Document Number : Boot Configurations	Date: Thursday, July 11, 2019	Rev : R003
		Sheet : 11	of 11