



Mango system on module (SOM) is based on IPQ6010 SoC from Qualcomm, which incorporates a powerful quad-core ARM Cortex A53 processor with NEON SIMD DSP extension for each core, ideal for Routers, Gateways and Access Points. It comes with a high-power dual-band concurrent radio supporting WIFI 6 (802.11ax) technology 2x2 MIMO. Two Ethernet SerDes to connect to external multi-GbE PHYs. Advanced power management for low active standby power consumption. SOM supports one USB3.0, USB2.0, PCIe 3.0, miscellaneous interfaces, which can be configured as general-purpose I/O pins and other. SoC has hardware NAT engine and high-end security features like crypto engine and others. The module is in a surface mountable form. Commercial temperature range: 0-65°C, industrial temperature range: -40-85°C.

### Quick specs

- Wi-Fi 6 (802.11a/n/ac/ax) 5GHz with 2x2 MU-MiMo, 1201Mbps data-rate
- Wi-Fi 6 (802.11b/g/n/ac/ax) 2.4GHz with 2x2 MU-MiMo, 573,5Mbps data-rate
- MIPI DBI v2.0 type B display interface
- CPU - IPQ6010 (1.8GHz)
- OpenWRT Linux flash image
- 22 dBm per chain RF output power
- Size - 38,3 by 61,7 mm
- Available interfaces:  
50 GPIOs, 1 x PCIe 3.0, 1 x USB3.0, 1 x USB2.0, 6 x BLSP ports for UART, 2C and SPI interfaces, 4 x PWM, 1 x JTAG, 2 x multi-GbE ethernet SerDes, dual SDIO for eMMC and SD card, PTA QPIC for parallel NAND device and LCD support.

# Features

## Features

TABLE 1-1. MANGO FEATURES

| Feature list    |                                                               |                                                                                                 | MAN_100 Mango             |
|-----------------|---------------------------------------------------------------|-------------------------------------------------------------------------------------------------|---------------------------|
| Integrated core | Core type                                                     |                                                                                                 | IPQ-6010 ARM Cortex-A53   |
|                 | Core clock frequency                                          |                                                                                                 | 1.8GHz                    |
|                 | Cache                                                         |                                                                                                 | 512kB L2                  |
| Memory          | DRAM                                                          |                                                                                                 | DDR3L 512MB (up to 2GB)   |
|                 | NOR FLASH                                                     |                                                                                                 | 32MB                      |
| WIFI            | IEEE 802.11 b/g/n/ac/ax 2x2 MU-MIMO 2.4GHz 20/40 MHz 1024 QAM |                                                                                                 | 2412-2462MHz              |
|                 | IEEE 802.11 a/n/ac/ax 2x2 MU-MIMO 5GHz 20/40/80 MHz 1024 QAM  |                                                                                                 | 5150-5250MHz,5725-5850MHz |
| RF pin          | RF signal is fed to 2 external module pins                    |                                                                                                 | 2                         |
| Display         | LCD controller                                                |                                                                                                 | 1                         |
| Peripherals     | PCIe                                                          | PCIe 3.0                                                                                        | 1                         |
|                 | USB                                                           | USB 3.0                                                                                         | 1                         |
|                 |                                                               | USB 2.0                                                                                         | 1                         |
|                 | BLSP                                                          | SPI/UART/I <sup>2</sup> C configuration ports                                                   | 6                         |
|                 | GPIO                                                          | IN/OUT/INT                                                                                      | 64                        |
|                 | PWM                                                           | Audio Pulse Width Modulation interface                                                          | 4                         |
|                 | Parallel                                                      | For parallel NAND flash memory                                                                  | 1                         |
|                 | Ethernet                                                      | SerDes supports 6.25/5/3.125/1.25 Gbps Ethernet 5*1/4*1/2.5/1 GbE PHYs. PSGMII, QSGMII, SGMII/+ | 1                         |
|                 | Reset                                                         | Reset controlled via voltage monitor                                                            | 1                         |
|                 | SDIO3.0/eMMC                                                  | Secure Digital Input Output / Embedded Multi Media Card                                         | 1                         |

# Module pinout and Pin description

FIGURE 3-1. PIN ASSIGNMENTS



**TABLE 3-1. I/O DESCRIPTION (PAD TYPE) PARAMETERS**

| Symbol    | Description                  |
|-----------|------------------------------|
| AI        | Analog input                 |
| AO        | Analog output                |
| GND       | Ground                       |
| RF In/Out | RF input/output              |
| I         | Digital input signal         |
| O         | Digital output signal        |
| IO        | Digital bidirectional signal |
| Z         | High-impedance               |

**TABLE 3-2. POWER, GROUND AND RESET**

| Pin ID                                                                                                                                                                                                                                                                                                                        | Pin name    | Type | Description               |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|---------------------------|
| A83, A84, A85,B76,B77                                                                                                                                                                                                                                                                                                         | 3V3         | I    | 3.3V digital power        |
| A36,A39,A45,A49, B33, B36, B42, B45                                                                                                                                                                                                                                                                                           | 3V3_RF      | I    | 3.3V digital power for RF |
| A1, A2, A12, A24, A32, A34, A35, A37, A38, A40, A41, A42, A43, A44, A46, A47, A48, A50, A52, A76, A79, A82, A86, A87, A88, A97, A100, A102, B1, B18, B20, B30, B31, B32, B34, B35, B37, B38, B39, B40, B41, B43, B44, B46, B47, B55, B56, B58, B59, B60, B61, B62, B63, B64, B65, B66, B67, B68, B69, B72, B75, B78, B79, B90 | GND         | GND  | Ground                    |
| A81                                                                                                                                                                                                                                                                                                                           | PBIN_N      | I    | Power off/on the device   |
| B10                                                                                                                                                                                                                                                                                                                           | RESET_OUT_N | O    | Reset output              |
| A20                                                                                                                                                                                                                                                                                                                           | PMIC_RST_O  | O    | Hardware reset            |

**TABLE 3-3. RADIO**

| Pin ID | Pin name | Type      | Description             |
|--------|----------|-----------|-------------------------|
| A51    | TX0      | RF In/Out | Signal line for antenna |
| A33    | TX1      | RF In/Out | Signal line for antenna |

**TABLE 3-4. USB 3.0**

| Pin ID | Pin name      | Type   | Description                   |
|--------|---------------|--------|-------------------------------|
| B70    | USB_0_D_P     | AI, AO | USB HS data positive          |
| A75    | USB_0_D_N     | AI, AO | USB HS data negative          |
| B73    | USB_0_SS_RX_P | AI     | USB SS receive data positive  |
| A78    | USB_0_SS_RX_N | AI     | USB SS receive data negative  |
| A77    | USB_0_SS_TX_P | AO     | USB SS transmit data positive |
| B71    | USB_0_SS_TX_N | AO     | USB SS transmit data negative |

**TABLE 3-5. USB 2.0**

| Pin ID | Pin name  | Type   | Description          |
|--------|-----------|--------|----------------------|
| A80    | USB_1_D_P | AI, AO | USB HS data positive |
| B74    | USB_1_D_N | AI, AO | USB HS data negative |

**TABLE 3-6. PCIE GEN3**

| Pin ID | Pin name       | Type | Description                          |
|--------|----------------|------|--------------------------------------|
| A95    | PCIE_W_DISABLE | IO   |                                      |
| B87    | PCIE_CLK_REQn  | IO   | PCle clock request                   |
| A96    | PCIE_RSTn      | I    | PCle reset                           |
| B88    | PCIE_WAKE      | I    | PCle wake                            |
| B89    | PCIE_TX_N      | AO   | PCle transmitter differential signal |
| A98    | PCIE_TX_P      | AO   |                                      |
| A99    | PCIE_RX_P      | AI   | PCle receiver differential signal    |
| B91    | PCIE_RX_N      | AI   |                                      |
| B92    | PCIE_REFCLK_N  | AO   | Reference clock                      |
| A101   | PCIE_REFCLK_P  | AO   |                                      |

**TABLE 3-7. ETHERNET**

| Pin ID | Pin name        | Type | Description                      |
|--------|-----------------|------|----------------------------------|
| A74    | CLK_50M_NAPA_P  | AO   | 50 MHz differential output clock |
| A73    | CLK_50M_NAPA_N  | AO   |                                  |
| A72    | USXGMII0_TX_P   | O    | Transmitter differential signal  |
| A71    | USXGMII0_TX_N   | O    |                                  |
| A70    | USXGMII0_RX_P   | I    | Receiver differential signal     |
| A69    | USXGMII0_RX_N   | I    |                                  |
| A68    | CLK_50M_NAPA2_P | AO   | 50 MHz differential output clock |
| A67    | CLK_50M_NAPA2_N | AO   |                                  |
| A66    | MDC             | AO   | MDIO interface clock             |
| A65    | MDIO            | IO   | Management data input/output     |
| A64    | USXGMII1_RX_N   | I    | Receiver differential signal     |
| A63    | USXGMII1_RX_P   | I    |                                  |
| B57    | CLK_25M_OUT     | AO   | 25 MHz output clock              |
| A62    | USXGMII1_TX_N   | O    | Transmitter differential signal  |
| A61    | USXGMII1_TX_P   | O    |                                  |

TABLE 3-8. NAND

| Pin ID | Pin name        | Type | Description                                   |
|--------|-----------------|------|-----------------------------------------------|
| B23    | NAND_FLASH_ALE  | IO   | NAND controller ALE                           |
| A25    | NAND_DATA_0     | IO   | NAND/Display controller data                  |
| B24    | NAND_DATA_3     | IO   | NAND/Display controller data                  |
| A26    | NAND_DATA_2     | IO   | NAND/Display controller data                  |
| B25    | NAND_DATA_1     | IO   | NAND/Display controller data                  |
| A27    | NAND_FLASH_CS   | IO   | NAND controller select                        |
| B26    | NAND_FLASH_CLE  | IO   | NAND controller CLE. Boot up interface select |
| A28    | NAND_DATA_7     | IO   | NAND/Display controller data                  |
| B27    | NAND_DATA_6     | IO   | NAND/Display controller data                  |
| A29    | NAND_DATA_5     | IO   | NAND/Display controller data                  |
| B28    | NAND_DATA_4     | IO   | NAND/Display controller data                  |
| A30    | NAND_FLASH_OE   | IO   | NAND/Display controller read enable           |
| B29    | NAND_FLASH_WE   | IO   | NAND/Display controller write enable          |
| A31    | NAND_FLASH_BUSY | IO   | NAND controller busy input                    |

TABLE 3-9. EMMC/SD

| Pin ID | Pin name         | Type | Description              |
|--------|------------------|------|--------------------------|
| B80    | SD_MODE          | I    | eMMC/SD enable           |
| A89    | EMMC_DATA2       | IO   | Data2 for eMMC/SD        |
| B81    | EMMC_DATA3       | IO   | Data3 for eMMC/SD        |
| A90    | EMMC_CMD         | IO   | Command for eMMC/SD      |
| B82    | EMMC_CLK         | IO   | Clock for eMMC/SD        |
| A91    | EMMC_DATA0       | IO   | Data0 for eMMC/SD        |
| B83    | EMMC_DATA1       | IO   | Data1 for eMMC/SD        |
| A92    | SD_CARD_DETECT   | I    | SD card detect           |
| B84    | SD_WRITE_PROTECT | I    | SD card write protection |
| A93    | EMMC_DATA7       | IO   | Data7 only for eMMC      |
| B85    | EMMC_DATA6       | IO   | Data6 only for eMMC      |
| A94    | EMMC_DATA5       | IO   | Data5 only for eMMC      |
| B86    | EMMC_DATA4       | IO   | Data4 only for eMMC      |

TABLE 3-10. GPIO

| Pad # | Pad Name | Voltage | Type | GPIO CFG. FUNC_SEL | Function           | Functional Description                                                                                     |
|-------|----------|---------|------|--------------------|--------------------|------------------------------------------------------------------------------------------------------------|
| B22   | GPIO[0]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(0)     | Configurable I/O                                                                                           |
|       |          |         | I    | 1                  | QPIC_PAD_TE        | LCDC TE, VSYNC                                                                                             |
|       |          |         | I    | 2                  | WCI2_RXD(0)        | input                                                                                                      |
| A31   | GPIO[1]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(1)     | Configurable I/O                                                                                           |
|       |          |         | I    | 1                  | QPIC_PAD_BUSY_N    | NAND BUSY_NOT_READY input. Active low.                                                                     |
|       |          |         | O    | 2                  | MAC1_SA0(2)        | Wi-Fi MAC1 smart antenna                                                                                   |
| A23   | GPIO[2]  | 1.8V    | IO   | 0                  | GPIO_IN_OUT(2)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_LCD_RS_N  | LCDC RESX, reset signal. Active low.                                                                       |
|       |          |         | O    | 2                  | WCI2_TXD(0)        | Wi-Fi WCI 2.0 transmit data                                                                                |
| B29   | GPIO[3]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(3)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_WE_N      | NAND/LCDC write enable                                                                                     |
|       |          |         | O    | 2                  | MAC0_SA0(1)        | Wi-Fi MAC0 smart antenna                                                                                   |
| A30   | GPIO[4]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(4)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_OE_N      | NAND/LCDC read enable                                                                                      |
|       |          |         | O    | 2                  | MAC0_SA1(1)        | Wi-Fi MAC0 smart antenna                                                                                   |
| B28   | GPIO[5]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(5)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(4)    | NAND/LCDC data[4]                                                                                          |
|       |          |         | O    | 2                  | MAC2_SA0(1)        | Wi-Fi MAC2 smart antenna                                                                                   |
| A29   | GPIO[6]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(6)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(5)    | NAND/LCDC data[5]                                                                                          |
|       |          |         | O    | 2                  | MAC2_SA1(1)        | Wi-Fi MAC2 smart antenna                                                                                   |
| B27   | GPIO[7]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(7)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(6)    | NAND/LCDC data[6]                                                                                          |
| A28   | GPIO[8]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(8)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(7)    | NAND/LCDC data[7]                                                                                          |
| B21   | GPIO[9]  | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(9)     | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_LCD_CS_N  | LCD chip select                                                                                            |
|       |          |         | O    | 3                  | CXC_CLK(0)         | Wi-Fi WSI 1.0 clock                                                                                        |
|       |          |         | O    | 4                  | MAC1_SA0(3)        | Wi-Fi MAC1 smart antenna                                                                                   |
| B26   | GPIO[10] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(10)    | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_CLE_LB_N  | NAND CLE/LCDC DCX. CLE is command latch enable. Active high. DCX is data/command. 1 is data, 0 is command. |
| A27   | GPIO[11] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(11)    | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_NAND_CS_N | NAND chip select                                                                                           |
|       |          |         | I    | 2                  | WCI2_RXD(2)        | Wi-Fi WCI 2.0 receive data                                                                                 |
|       |          |         | O    | 3                  | MAC1_SA1(2)        | Wi-Fi MAC1 smart antenna                                                                                   |
| B25   | GPIO[12] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(12)    | Configurable I/O                                                                                           |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(1)    | NAND/LCDC data[1]                                                                                          |

| Pad # | Pad Name | Voltage | Type | GPIO CFG. FUNC_SEL | Function          | Functional Description                   |
|-------|----------|---------|------|--------------------|-------------------|------------------------------------------|
| A26   | GPIO[13] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(13)   | Configurable I/O                         |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(2)   | NAND/LCDC data[2]                        |
| B24   | GPIO[14] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(14)   | Configurable I/O                         |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(3)   | NAND/LCDC data[3]                        |
| A25   | GPIO[15] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(15)   | Configurable I/O                         |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(0)   | NAND/LCDC data[0]                        |
| A22   | GPIO[16] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(16)   | Configurable I/O                         |
|       |          |         | O    | 1                  | QPIC_PAD_DAT(8)   | NAND/LCDC data[8]                        |
|       |          |         | O    | 2                  | CXC_DATA(0)       | Wi-Fi WSI 1.0 data                       |
|       |          |         | O    | 3                  | MAC1_SA1(3)       | Wi-Fi MAC1 smart antenna                 |
| B23   | GPIO[17] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(17)   | Configurable I/O                         |
|       |          |         | O    | 1                  | QPIC_PAD_ALE_LB_N | NAND ALE. Active high.                   |
|       |          |         | O    | 3                  | WCI2_TXD(2)       | Wi-Fi WCI 2.0 transmit data              |
| A19   | GPIO[18] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(18)   | Configurable I/O                         |
|       |          |         | O    | 1                  | PWM0(0)           | Audio Pulse Width Modulation interface 0 |
|       |          |         | I    | 3                  | WCI2_RXD(3)       | Wi-Fi WCI 2.0 receive data               |
|       |          |         | O    | 4                  | MAC1_SA0(1)       | Wi-Fi MAC1 smart antenna                 |
| B17   | GPIO[19] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(19)   | Configurable I/O                         |
|       |          |         | O    | 1                  | PWM1(0)           | Audio Pulse Width Modulation interface 1 |
|       |          |         | O    | 3                  | WCI2_TXD(3)       | Wi-Fi WCI 2.0 transmit data              |
|       |          |         | O    | 4                  | MAC1_SA1(1)       | Wi-Fi MAC1 smart antenna                 |
| A18   | GPIO[20] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(20)   | Configurable I/O                         |
|       |          |         | O    | 1                  | PWM2(0)           | Audio Pulse Width Modulation interface 2 |
| B16   | GPIO[21] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(21)   | Configurable I/O                         |
|       |          |         | O    | 1                  | PWM3(0)           | Audio Pulse Width Modulation interface 3 |
| A17   | GPIO[22] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(22)   | Configurable I/O                         |
|       |          |         | O    | 3                  | PWM0(2)           | Audio Pulse Width Modulation interface 0 |
| B15   | GPIO[23] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(23)   | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM1(2)           | Audio Pulse Width Modulation interface 1 |
| A16   | GPIO[24] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(24)   | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM2(2)           | Audio Pulse Width Modulation interface 2 |
| B14   | GPIO[25] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(25)   | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM3(2)           | Audio Pulse Width Modulation interface 3 |
| A15   | GPIO[26] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(26)   | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM0(4)           | Audio Pulse Width Modulation interface 0 |

| Pad # | Pad Name | Voltage | Type | GPIO CFG. FUNC_SEL | Function         | Functional Description                   |
|-------|----------|---------|------|--------------------|------------------|------------------------------------------|
| B13   | GPIO[27] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(27)  | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM1(4)          | Audio Pulse Width Modulation interface 1 |
| A14   | GPIO[28] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(28)  | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM2(4)          | Audio Pulse Width Modulation interface 2 |
| B12   | GPIO[29] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(29)  | Configurable I/O                         |
|       |          |         | O    | 3                  | PWM0(3)          | Audio Pulse Width Modulation interface 0 |
| A13   | GPIO[30] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(30)  | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM1(3)          | Audio Pulse Width Modulation interface 1 |
| B11   | GPIO[31] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(31)  | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM2(3)          | Audio Pulse Width Modulation interface 2 |
| A11   | GPIO[32] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(32)  | Configurable I/O                         |
|       |          |         | O    | 2                  | PWM3(3)          | Audio Pulse Width Modulation interface 3 |
| B9    | GPIO[33] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(33)  | Configurable I/O                         |
| A10   | GPIO[34] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(34)  | Configurable I/O                         |
|       |          |         | O    | 2                  | MAC1_SA0(0)      | Wi-Fi MAC1 smart antenna                 |
|       |          |         | O    | 3                  | MAC0_SA0(0)      | Wi-Fi MAC0 smart antenna                 |
| B8    | GPIO[35] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(35)  | Configurable I/O                         |
|       |          |         | O    | 2                  | MAC1_SA1(0)      | Wi-Fi MAC1 smart antenna                 |
|       |          |         | O    | 3                  | MAC0_SA1(0)      | Wi-Fi MAC0 smart antenna                 |
| A9    | GPIO[36] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(36)  | Configurable I/O                         |
|       |          |         | O    | 2                  | MAC2_SA0(0)      | Wi-Fi MAC2 smart antenna                 |
| B7    | GPIO[37] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(37)  | Configurable I/O                         |
|       |          |         | O    | 2                  | MAC2_SA1(0)      | Wi-Fi MAC2 smart antenna                 |
| B4    | GPIO[42] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(42)  | Configurable I/O                         |
|       |          |         | O    | 1                  | BLSP2_UART_RFR_N | UART2 ready for receiving                |
|       |          |         | O    | 2                  | BLSP2_I2C_SCL    | I <sup>2</sup> C2 clock                  |
|       |          |         | O    | 3                  | BLSP2_SPI_CLK    | SPI2 clock                               |
| A6    | GPIO[43] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(43)  | Configurable I/O                         |
|       |          |         | I    | 1                  | BLSP2_UART_CTS_N | UART2 clear to send                      |
|       |          |         | O    | 2                  | BLSP2_I2C_SDA    | I <sup>2</sup> C2 data                   |
|       |          |         | O    | 3                  | BLSP2_SPI_CS_N   | SPI2 chip select                         |
| A21   | GPIO[44] | 1.8 V   | I    | 1                  | BLSP2_UART_RX    | UART2 receive serial data                |
|       |          |         | IO   | 2                  | BLSP2_SPI_MISO   | SPI2 master-in slave-out data            |
|       |          |         | IO   | 0                  | GPIO_IN_OUT(45)  | Configurable I/O                         |
| B19   | GPIO[45] | 1.8V    | O    | 1                  | BLSP2_UART_TX    | UART2 transmit serial data               |
|       |          |         | O    | 2                  | BLSP2_SPI_MOSI   | SPI2 master-out slave-in data            |

| Pad # | Pad Name | Voltage | Type | GPIO CFG. FUNC_SEL | Function         | Functional Description                   |
|-------|----------|---------|------|--------------------|------------------|------------------------------------------|
| A60   | GPIO[49] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(49)  | Configurable I/O                         |
|       |          |         | O    | 1                  | BLSP5_UART_TX    | UART5 transmit serial data               |
| A8    | GPIO[50] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(50)  | Configurable I/O                         |
|       |          |         | O    | 1                  | PWM0(1)          | Audio Pulse Width Modulation interface 0 |
|       |          |         | O    | 2                  | GP0_CLK(1)       | General Purpose clock                    |
| B6    | GPIO[51] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(51)  | Configurable I/O                         |
|       |          |         | I    | 1                  | PTA1_1           | Wi-Fi Co-exist PTA 1                     |
|       |          |         | O    | 2                  | PWM1(1)          | Audio Pulse Width Modulation interface 1 |
|       |          |         | O    | 3                  | GP1_CLK(1)       | General Purpose clock                    |
|       |          |         | I    | 4                  | RX_LOS(1)        | Ethernet Loss of Signal                  |
| A7    | GPIO[52] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(52)  | Configurable I/O                         |
|       |          |         | O    | 1                  | PTA1_2           | Wi-Fi Co-exist PTA 1                     |
|       |          |         | O    | 2                  | PWM2(1)          | Audio Pulse Width Modulation interface 2 |
|       |          |         | O    | 3                  | GP2_CLK(1)       | General Purpose clock                    |
| B5    | GPIO[53] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(53)  | Configurable I/O                         |
|       |          |         | I    | 1                  | PTA1_0           | Wi-Fi Co-exist PTA 1                     |
|       |          |         | O    | 2                  | PWM3(1)          | Audio Pulse Width Modulation interface 3 |
| A5    | GPIO[54] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(54)  | Configurable I/O                         |
| B3    | GPIO[55] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(55)  | Configurable I/O                         |
|       |          |         | O    | 1                  | BLSP4_UART_RFR_N | UART4 ready for receiving                |
|       |          |         | O    | 2                  | BLSP4_I2C_SCL    | I <sup>2</sup> C4 clock                  |
|       |          |         | O    | 3                  | BLSP4_SPI_CLK    | SPI4 clock                               |
| A4    | GPIO[56] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(56)  | Configurable I/O                         |
|       |          |         | I    | 1                  | BLSP4_UART_CTS_N | UART4 clear to send                      |
|       |          |         | O    | 2                  | BLSP4_I2C_SDA    | I <sup>2</sup> C4 data                   |
|       |          |         | O    | 3                  | BLSP4_SPI_CS_N   | SPI4 chip select                         |
| B2    | GPIO[57] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(57)  | Configurable I/O                         |
|       |          |         | I    | 1                  | BLSP4_UART_RX    | UART4 receive serial data                |
|       |          |         | IO   | 2                  | BLSP4_SPI_MISO   | SPI4 master-in slave- out data           |
| A3    | GPIO[58] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(58)  | Configurable I/O                         |
|       |          |         | O    | 1                  | BLSP4_UART_TX    | UART4 transmit serial data               |
|       |          |         | O    | 2                  | BLSP4_SPI_MOSI   | SPI4 master-out slave- in data           |
| B54   | GPIO[66] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(66)  | Configurable I/O                         |
|       |          |         | I    | 1                  | PTA2_0           | Wi-Fi Co-exist PTA 2                     |
|       |          |         | I    | 2                  | WCI2_RXD(1)      | Wi-Fi WCI 2.0 transmit data              |
|       |          |         | O    | 3                  | CXC_CLK(1)       | Wi-Fi WSI 1.0 clock                      |

| Pad # | Pad Name | Voltage | Type | GPIO CFG. FUNC_SEL | Function         | Functional Description         |
|-------|----------|---------|------|--------------------|------------------|--------------------------------|
| A59   | GPIO[67] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(67)  | Configurable I/O               |
|       |          |         | I    | 1                  | PTA2_1           | Wi-Fi Co-exist PTA 2           |
| B53   | GPIO[68] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(68)  | Configurable I/O               |
|       |          |         | O    | 1                  | PTA2_2           | Wi-Fi Co-exist PTA 2           |
|       |          |         | O    | 2                  | WCI2_TXD(1)      | Wi-Fi WCI 2.0 transmit data    |
|       |          |         | O    | 3                  | CXC_DATA(1)      | Wi-Fi WSI 1.0 data             |
| A58   | GPIO[69] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(69)  | Configurable I/O               |
|       |          |         | O    | 1                  | BLSP1_UART_RFR_N | UART1 ready for receiving      |
|       |          |         | O    | 2                  | BLSP1_I2C_SCL    | I <sup>2</sup> C1 clock        |
|       |          |         | O    | 3                  | BLSP1_SPI_CLK    | SPI1 clock                     |
| B52   | GPIO[70] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(70)  | Configurable I/O               |
|       |          |         | I    | 1                  | BLSP1_UART_CTS_N | UART1 clear to send            |
|       |          |         | O    | 2                  | BLSP1_I2C_SDA    | I <sup>2</sup> C1 data         |
|       |          |         | O    | 3                  | BLSP1_SPI_CS_N   | SPI1 chip select               |
| A57   | GPIO[71] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(71)  | Configurable I/O               |
|       |          |         | I    | 1                  | BLSP1_UART_RX    | UART1 receive serial data      |
|       |          |         | IO   | 2                  | BLSP1_SPI_MISO   | SPI1 master-in slave- out data |
| B51   | GPIO[72] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(72)  | Configurable I/O               |
|       |          |         | O    | 1                  | BLSP1_UART_TX    | UART1 transmit serial data     |
|       |          |         | O    | 2                  | BLSP1_SPI_MOSI   | SPI1 master-out slave- in data |
| A56   | GPIO[73] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(73)  | Configurable I/O               |
|       |          |         | O    | 1                  | BLSP3_UART_RFR_N | UART3 ready for receiving      |
|       |          |         | O    | 2                  | BLSP3_I2C_SCL    | I <sup>2</sup> C3 clock        |
|       |          |         | O    | 3                  | BLSP3_SPI_CLK    | SPI3 clock                     |
| B50   | GPIO[74] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(74)  | Configurable I/O               |
|       |          |         | I    | 1                  | BLSP3_UART_CTS_N | UART3 clear to send            |
|       |          |         | O    | 2                  | BLSP3_I2C_SDA    | I <sup>2</sup> C3 data         |
|       |          |         | O    | 3                  | BLSP3_SPI_CS_N   | SPI3 chip select               |
| A55   | GPIO[75] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(75)  | Configurable I/O               |
|       |          |         | I    | 1                  | BLSP3_UART_RX    | UART3 receive serial data      |
|       |          |         | IO   | 2                  | BLSP3_SPI_MISO   | SPI3 master-in slave- out data |
| B49   | GPIO[76] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(76)  | Configurable I/O               |
|       |          |         | O    | 1                  | BLSP3_UART_TX    | UART3 transmit serial data     |
|       |          |         | O    | 2                  | BLSP3_SPI_MOSI   | SPI3 master-out slave- in data |
| A54   | GPIO[77] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(77)  | Configurable I/O               |
|       |          |         | Z    | 1                  | BLSP3_SPI_CS1_N  | SPI3 additional CS[1]          |
| B48   | GPIO[78] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(78)  | Configurable I/O               |
|       |          |         | Z    | 1                  | BLSP3_SPI_CS2_N  | SPI3 additional CS[2]          |
| A53   | GPIO[79] | 1.8 V   | IO   | 0                  | GPIO_IN_OUT(79)  | Configurable I/O               |
|       |          |         | Z    | 1                  | BLSP3_SPI_CS3_N  | SPI3 additional CS[3]          |

TABLE 3-11. PIN STATUS ON BOOT

| Pin # | Pin name        | Pin name | Voltage | Internal Pull-down(PD)/ Pull-up(PU) | Type | Description                                                                                                           |
|-------|-----------------|----------|---------|-------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------|
| A23   | BOOT_CONFIG[0]  | GPIO_2   | 1.8 V   | PD                                  | I    | Auth enable:<br>0: No auth<br>1: Auth is required                                                                     |
| B29   | BOOT_CONFIG[1]  | GPIO_3   | 1.8 V   | PD                                  | I    | Fast boot (boot interface select):<br>000: SPI-NOR<br>001: eMMC<br>010: Para NAND<br>011: USB 2.0<br>100: SPI-NOR-GPT |
| B26   | BOOT_CONFIG[2]  | GPIO_10  | 1.8 V   | PD                                  | I    |                                                                                                                       |
| B23   | BOOT_CONFIG[3]  | GPIO_17  | 1.8 V   | PD                                  | I    |                                                                                                                       |
| B16   | BOOT_CONFIG[4]  | GPIO_21  | 1.8 V   | PD                                  | I    | Hash in fuse (SW use only)<br>0: PK hash is stored in boot ROM<br>1: PK hash is stored in OTP                         |
| B17   | BOOT_CONFIG[5]  | GPIO_19  | 1.8 V   | PU                                  | I    | Boot from ROM:<br>0: boot from code ram<br>1: boot from rom                                                           |
| A18   | BOOT_CONFIG[6]  | GPIO_20  | 1.8 V   | PD                                  | I    | Boot ROM boot speed:<br>00: Uniphy CMN clock - 24MHz<br>01: GPLLO- 200MHz<br>10: GPLLO- 400MHz<br>11: GPLLO- 800MHz   |
| A60   | BOOT_CONFIG[7]  | GPIO_49  | 1.8 V   | PD                                  | I    |                                                                                                                       |
| A8    | BOOT_CONFIG[8]  | GPIO_50  | 1.8 V   | PD                                  | I    | IMAGE_ENCRYPTION_ENABLE<br>0: UIE Disable<br>1: UIE Enable                                                            |
| A7    | BOOT_CONFIG[9]  | GPIO_52  | 1.8 V   | PD                                  | I    | watchdog_enable<br>0: watchdog enable.<br>1: watchdog disable                                                         |
| A5    | BOOT_CONFIG[10] | GPIO_54  | 1.8 V   | PD                                  | I    | Use Serial Num:<br>0: Use Serial Num<br>1: Use OEM ID                                                                 |
| A66   | BOOT_CONFIG[11] | GPIO_64  | 1.8 V   | PD                                  | I    | Board Type[2:0] detect the board and<br>autoload the Configuration data table<br>000: CP01<br>001: CP02<br>010: CP03  |
| B13   | BOOT_CONFIG[12] | GPIO_27  | 1.8 V   | PU                                  | I    |                                                                                                                       |
| A14   | BOOT_CONFIG[13] | GPIO_28  | 1.8 V   | PD                                  | I    |                                                                                                                       |
| A15   | forced_usb_boot | GPIO_26  | 1.8 V   | PD                                  | I    | 0: Not force boot from USB<br>1: Force boot from USB                                                                  |

**NOTE:** These pins are for boot configuration, use them cautiously.

## Electrical characteristics

TABLE 4-1. POWER SUPPLY DC CHARACTERISTICS

| Symbol | Parameter           | Minimum | Typical | Maximum | Units |
|--------|---------------------|---------|---------|---------|-------|
| DVDD33 | 3.3V Supply Voltage | 3.13    | 3.3     | 3.46    | V     |

TABLE 4-2. TEMPERATURE LIMIT RATINGS

| Parameter                        | Minimum | Maximum | Units |
|----------------------------------|---------|---------|-------|
| Storage Temperature (Commercial) | -40     | +70     | °C    |
| Storage Temperature (Industrial) | -40     | +90     | °C    |
| Commercial Operating Temperature | 0       | +65     | °C    |
| Industrial Operating Temperature | -40     | +85     | °C    |
| Humidity                         | 10      | 90      | %RH   |
| Storage humidity                 | 5       | 90      | %RH   |

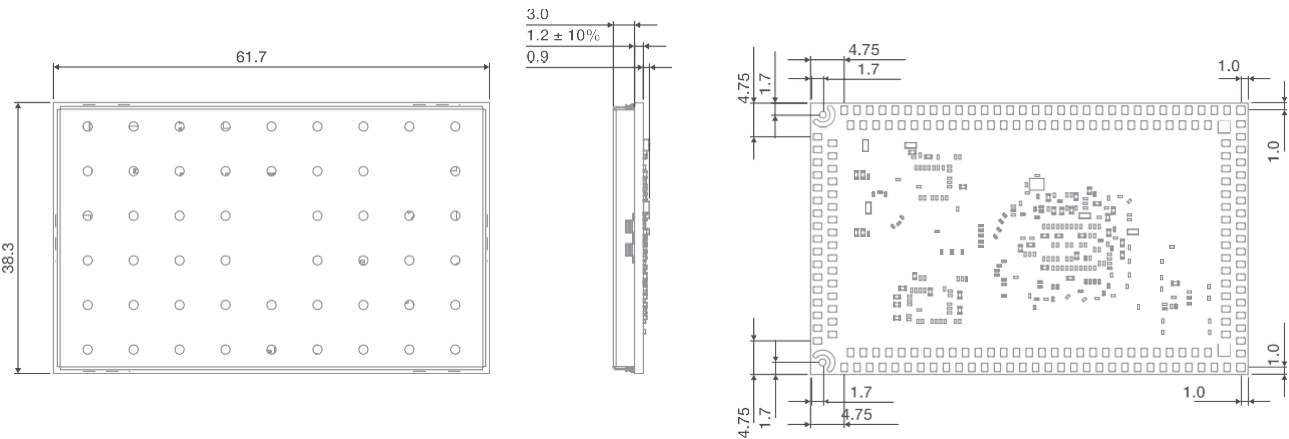
## Power management

Power consumption TABLE 5-1.

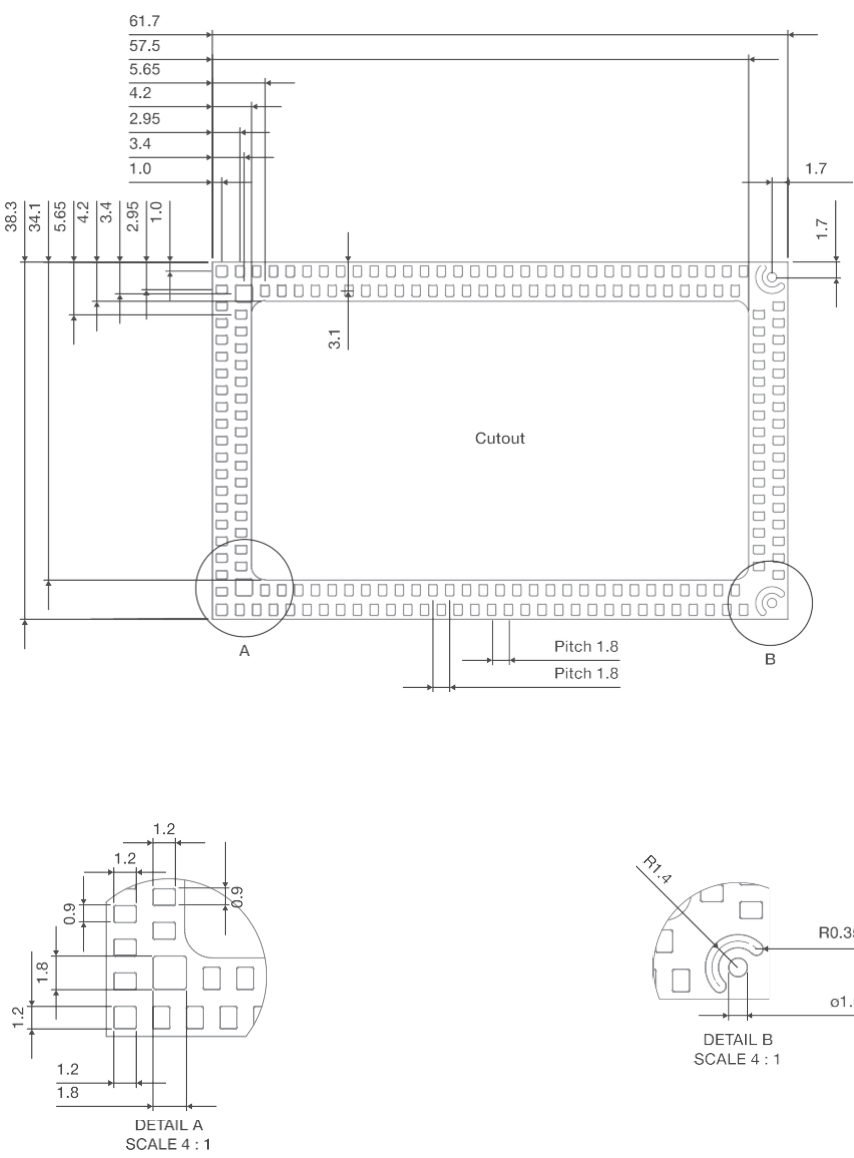
POWER CONSUMPTION

| Scenario                                    | Rate  | Voltage | Current | Total power |
|---------------------------------------------|-------|---------|---------|-------------|
| Throughput with iperf and 95% CPU load, 2x2 | MCS0  | 24 V    | 0.4 A   | 9.6 W       |
|                                             | MCS11 | 24 V    | 0.42 A  | 10.1 W      |

# 7. Mechanical characteristics



## PCB footprint



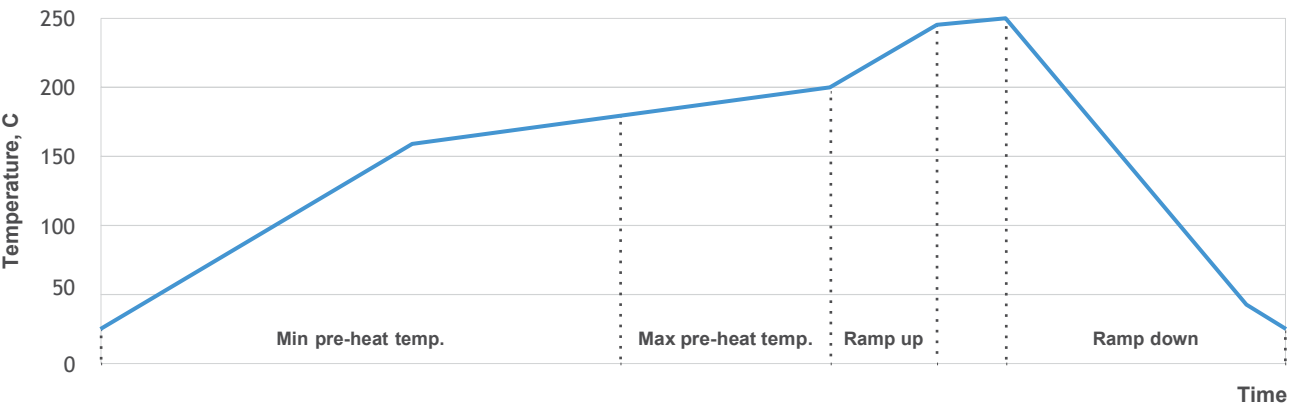
# 8. Reflow profile recommendations

## Reflow profile recommendation

| Process  |                                             | Unit | Value |
|----------|---------------------------------------------|------|-------|
| Pre-heat | Min pre-heat temperature                    | °C   | 150   |
|          | Max pre-heat temperature                    | °C   | 200   |
|          | Pre-heat time                               | s    | 150   |
|          | Ramp up rate                                | °C/s | 3     |
| Peak     | Maximum time maintained above 220           | s    | 120   |
|          | Peak temperature                            | °C   | 250   |
|          | Maximum time within 5°C of peak temperature | s    | 30    |
| Cooling  | Ramp down rate                              | °C/s | 4     |

To solder Mango module properly thicker layer of solder paste have to be used. Minimum thickness of stencil is 100µm.

## Reflow profile



# Design considerations

## Ethernet interface

### ETHERNET DESIGN GUIDELINES:

| Category                  | Guidelines/Remarks                                                                                                                                                  |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Groups                    | USXGMII[0..1]_TX_P, USXGMII[0..1]_RX_P, USXGMII[0..1]_TX_N, USXGMII[0..1]_RX_N                                                                                      |
| Route type                | Differential pair, 100 Ohm impedance                                                                                                                                |
| Length                    | < 1.5 in., try to route as short as possible                                                                                                                        |
| Length match within pair  | +/-5 mils                                                                                                                                                           |
| Length match across pairs | There is no requirement to length match the Tx and Rx pairs                                                                                                         |
| Spacing requirements      | 3 W spacing between pairs and to other signals                                                                                                                      |
| Vias/layer transitions    | Minimize layer transitions; where necessary limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of signal vias |
| Other                     | Each pair needs magnetic module (or combo module for all pairs) between PHY and Ethernet port                                                                       |

## USB

### USB 3.0 DESIGN GUIDELINES:

| Category                  | Guidelines/Remarks                                                                                                                                           |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Groups                    | USB_0_RX_P, USB_0_RX_N, USB_0_TX_P, USB_0_TX_N, USB_[0..1]_D_P, USB_[0..1]_D_N                                                                               |
| USB_RXP, USB_RXN          | Differential pair, 90 Ohm impedance for the super speed pairs according to USB3.0 specification                                                              |
| Route type                | Ensure continuous and unbroken return path without voids.<br>Differential pair, 90 Ohm impedance for the super speed pairs according to USB3.0 specification |
| Return path               | Ensure continuous and unbroken return path without voids                                                                                                     |
| Length                    | < 5 in.                                                                                                                                                      |
| Length match within pair  | +/- 5 mils                                                                                                                                                   |
| Length match across pairs | There is no requirement to length match the Tx and Rx pairs                                                                                                  |
| Spacing requirements      | 3 W spacing between pairs and to other signals                                                                                                               |
| Vias/layer transitions    | Avoid layer transitions and vias                                                                                                                             |
| AC coupling               | Use 0.1 uF capacitors on each signal line of the Tx pair from Mango module; place them symmetrically at the same point on the pair                           |
| Other                     | Clear the GND pour under the signal pads of the connector where SMD connectors are used                                                                      |

## Parallel NAND flash / LCD

### NAND FLASH DESIGN GUIDELINES:

| Category                    | Guidelines/Remarks                                                                                                                                                                                                           |
|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Signal/group                | NAND_CS_N<br>NAND_CLE_N<br>NAND_ALE_N<br>NAND_WE_N<br>NAND_OE_N<br>NAND_BUSY_N<br>NAND_DATA_[7:0]                                                                                                                            |
| Route type                  | Single-ended                                                                                                                                                                                                                 |
| Return path                 | Ensure continuous and unbroken return path without voids                                                                                                                                                                     |
| Length                      | < 5 in.                                                                                                                                                                                                                      |
| Length match                | 200 mils within group, 400 mils across groups                                                                                                                                                                                |
| Spacing requirements        | 2 W spacing to other signals                                                                                                                                                                                                 |
| GND shielding               | Not required                                                                                                                                                                                                                 |
| Vias/layer transitions      | Vias are acceptable                                                                                                                                                                                                          |
| Voltage                     | 3.3 V                                                                                                                                                                                                                        |
| Decoupling and power layout | Follow best design practices and provide decoupling close to the SDIO device.<br>Allocate one 0201 decap per pin and locate it close to the pin.<br>A bulk capacitor in the order of 1 MF or more is advised for the device. |
| Other                       | Some NAND controller output lines are used at power-up to sense boot configuration straps. Take care to minimize stubs in the path. A 10K pull-up is recommended on the NAND_CS signal at flash device                       |

## SD/eMMC

### SDIO DESIGN GUIDELINES:

| Category                    | Guidelines/Remarks                                                                                                                                                                                                         |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Signal/group                | CARD_DETECT<br>eMMC_CMD<br>eMMC_CLK<br>eMMC_DATA[7:0]                                                                                                                                                                      |
| Route type                  | Single-ended 50 Ohm impedance                                                                                                                                                                                              |
| Return path                 | Ensure continuous and unbroken return path without voids                                                                                                                                                                   |
| Length                      | < 4.5 in.                                                                                                                                                                                                                  |
| Length match                | 10 mils within group                                                                                                                                                                                                       |
| Spacing requirements        | 2 W spacing to other signals                                                                                                                                                                                               |
| GND shielding               | Not required                                                                                                                                                                                                               |
| Vias/layer transitions      | Vias are acceptable                                                                                                                                                                                                        |
| Voltage                     | 1.8 V / 3.3 V auto change according to SD card If configured as eMMC interface, it is fixed 1.8 V                                                                                                                          |
| Decoupling and power layout | Follow best design practices and provide decoupling close to the SDIO device.<br>Allocate one 0201 decap per pin and locate it close to the pin<br>A bulk capacitor in the order of 1 MF or more is advised for the device |
| Other                       | Pay attention to SDIO_CLK, add 22 Ohm damping resistor and 5 pF paralleled cap to GND                                                                                                                                      |

## PCIe

### PCIe DESIGN GUIDELINES FOR DATA SIGNALS:

| Category                  | Guidelines/Remarks                                                                                                                                                      |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Signal/group              | PCIe_TXP, PCIe_TXN<br>PCIe_RXP, PCIe_RXN                                                                                                                                |
| Route type                | Differential pair 100 Ohm impedance                                                                                                                                     |
| Return path               | Ensure continuous and unbroken return path without voids                                                                                                                |
| Length                    | < 5 in.                                                                                                                                                                 |
| Length match within pair  | +/- 5mils                                                                                                                                                               |
| Length match across pairs | There is no requirement to length match the Tx and Rx pairs                                                                                                             |
| Spacing requirements      | 3 W spacing between pairs and other signals after the breakout from module                                                                                              |
| GND shielding             | Provide GND shield at 3 W spacing away from the signal pairs. The GND shape must be stitched to the main GND in inner layers with vias at regular intervals of 100 mils |
| Vias/layer transitions    | Avoid layer transitions                                                                                                                                                 |
| AC coupling               | There are already 0.1 uF capacitors on each signal line of the Tx pair on the module; No additional coupling is needed                                                  |
| Voltage                   | The voltage rails for the PCIe interface are implemented with filters for the PLL (AVDDPLL_PCIE) and the I/O (AVDD) rails                                               |
| Other                     | Clear the GND pour under the paired signal pads of the connector where SMD connectors are used                                                                          |

### PCIe DESIGN GUIDELINES FOR REFCLK:

| Category                  | Guidelines/Remarks                                                                                                                                                                                                                                                                                         |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Signal/group              | PCIe_CLK_M, PCIe_CLK_P                                                                                                                                                                                                                                                                                     |
| Route type                | Differential pair 100 Ohm impedance                                                                                                                                                                                                                                                                        |
| Return path               | Ensure continuous and unbroken return path without voids                                                                                                                                                                                                                                                   |
| Length                    | < 5 in.                                                                                                                                                                                                                                                                                                    |
| Length match within pair  | +/- 5 mils                                                                                                                                                                                                                                                                                                 |
| Length match across pairs | There is no specific requirements to match lengths across different REFCLK pairs                                                                                                                                                                                                                           |
| Spacing requirements      | 3 W spacing between pairs and to other signals after the breakout from the module                                                                                                                                                                                                                          |
| GND shielding             | Minimize layer transitions.<br>Where necessary, limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of the signal vias. These vias should form a symmetric GSSG pattern and recommend clearing an oblong void at this transition point through layers |
| AC coupling               | Should not be used. The REFCLK must be DC connected to the loads                                                                                                                                                                                                                                           |

## Thermal considerations

Thermal flow equals GND current flow

- Greater copper cross section
- More heat flow, more current flow through Via and GND structure

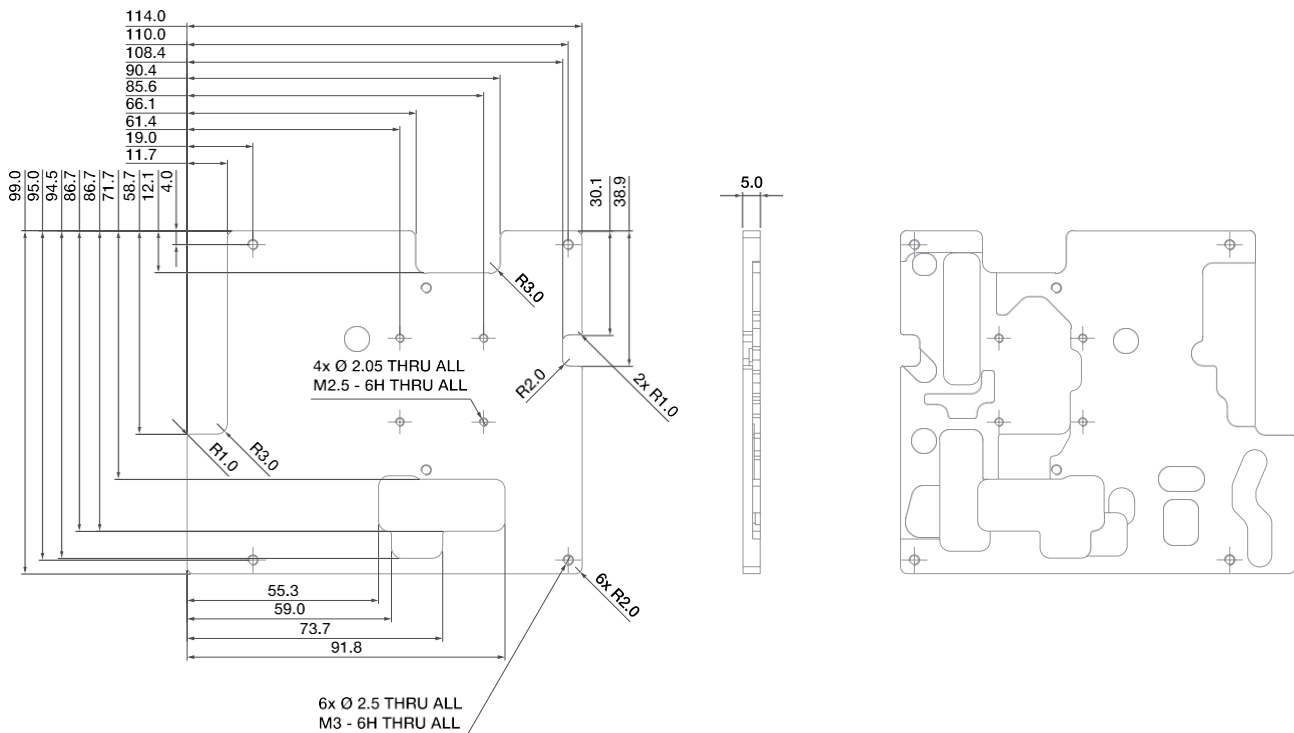
Vertical copper cross section

- Move the heat to other layers
- Internal layers conduct heat horizontally

Horizontal copper cross section

- Avoid fence of non-GND vias (reduce horizontal copper)
- Opening the solder mask in the top and bottom layers beneath the heat parts is the better way of radiating heat
- Also to have maximum GND copper possible with vertical copper (vias) to move heat from inner layers

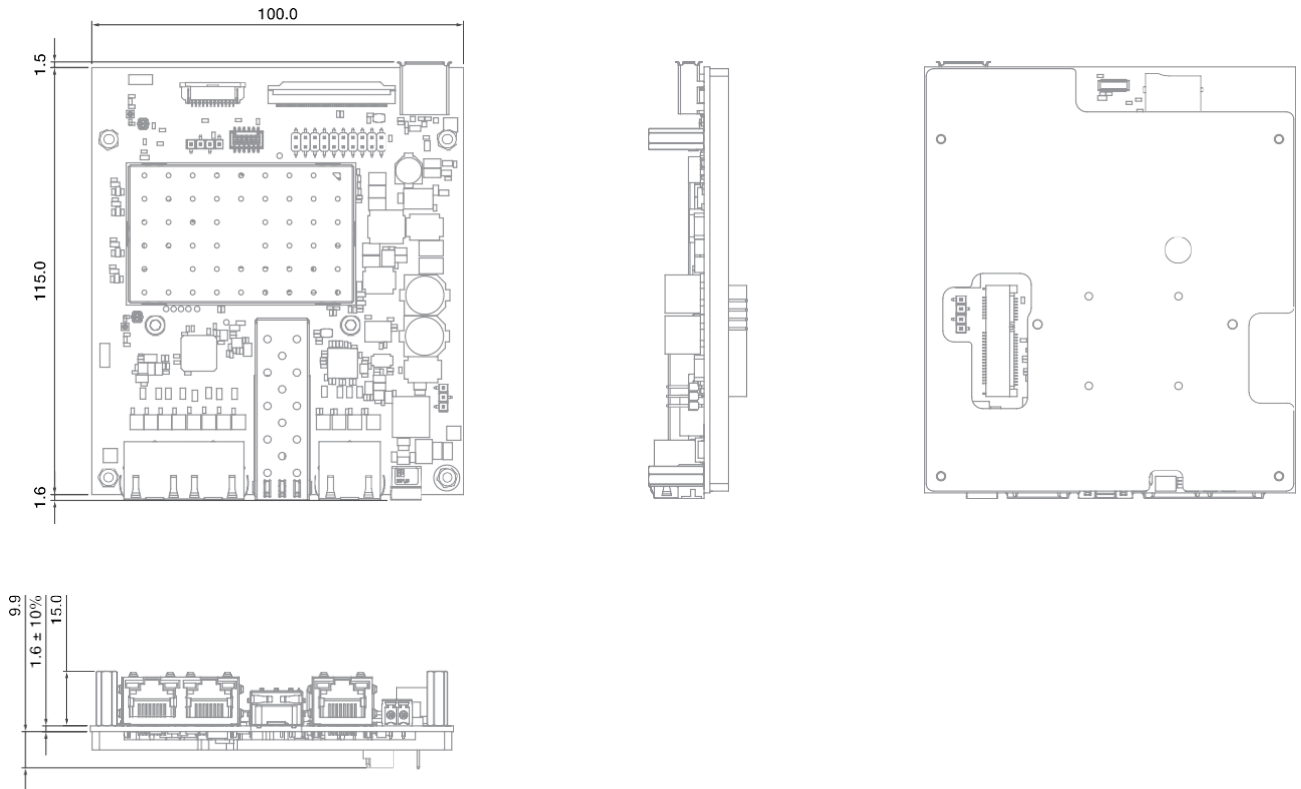
## Heatsink



Heatsink surface area has to be at least 120cm<sup>2</sup> and made from aluminium (or different metal with a better thermal conductivity).

# Development board

## DVK dimensions



## DVK interfaces

1. UART header
2. GPIO header
3. Boot configuration switch
4. USB 3.0 interface
5. DC power input 12-58 V
6. 2.5 Gbps Ethernet interface + POE passive 24-48V
7. SFP Port
8. 2 x 1Gbps Ethernet interface
9. WiFi antenna 1 and U.FL connector for external antenna
10. WiFi antenna 2 and U.FL connector for external antenna
11. SD card socket
12. EMMC module socket
13. mPCIE socket with PCIe3.0, USB2.0 interfaces
14. Programmable button (GPIO79)
15. Reset button
16. LEDs
17. Mounting holes

## BOOTSTRAP switch

| Config                         | 1 (B23) | 2(B26) | 3(B29) | 4(A15) | 5(A60) | 6(B80) |
|--------------------------------|---------|--------|--------|--------|--------|--------|
| Boot from SPI NOR Default      | OFF     | OFF    | OFF    | OFF    | NA     | NA     |
| Boot from eMMC                 | ON      | OFF    | OFF    | OFF    | NA     | NA     |
| Boot from NAND                 | OFF     | ON     | OFF    | OFF    | NA     | NA     |
| Boot from USB                  | ON      | ON     | OFF    | OFF    | NA     | NA     |
| Force boot from USB            | ON      | ON     | OFF    | ON     | NA     | NA     |
| Boot from SPI_NOR_GPT          | OFF     | OFF    | ON     | OFF    | NA     | NA     |
| Enable SFP interface           | NA      | NA     | NA     | NA     | ON     | NA     |
| Enable 2.5 Gbps ETH inter-face | NA      | NA     | NA     | NA     | OFF    | NA     |
| Enable eMMC interface          | NA      | NA     | NA     | NA     | NA     | ON     |

### 11.4. NAND memory

Mango DVK comes with 256 MB of NAND memory

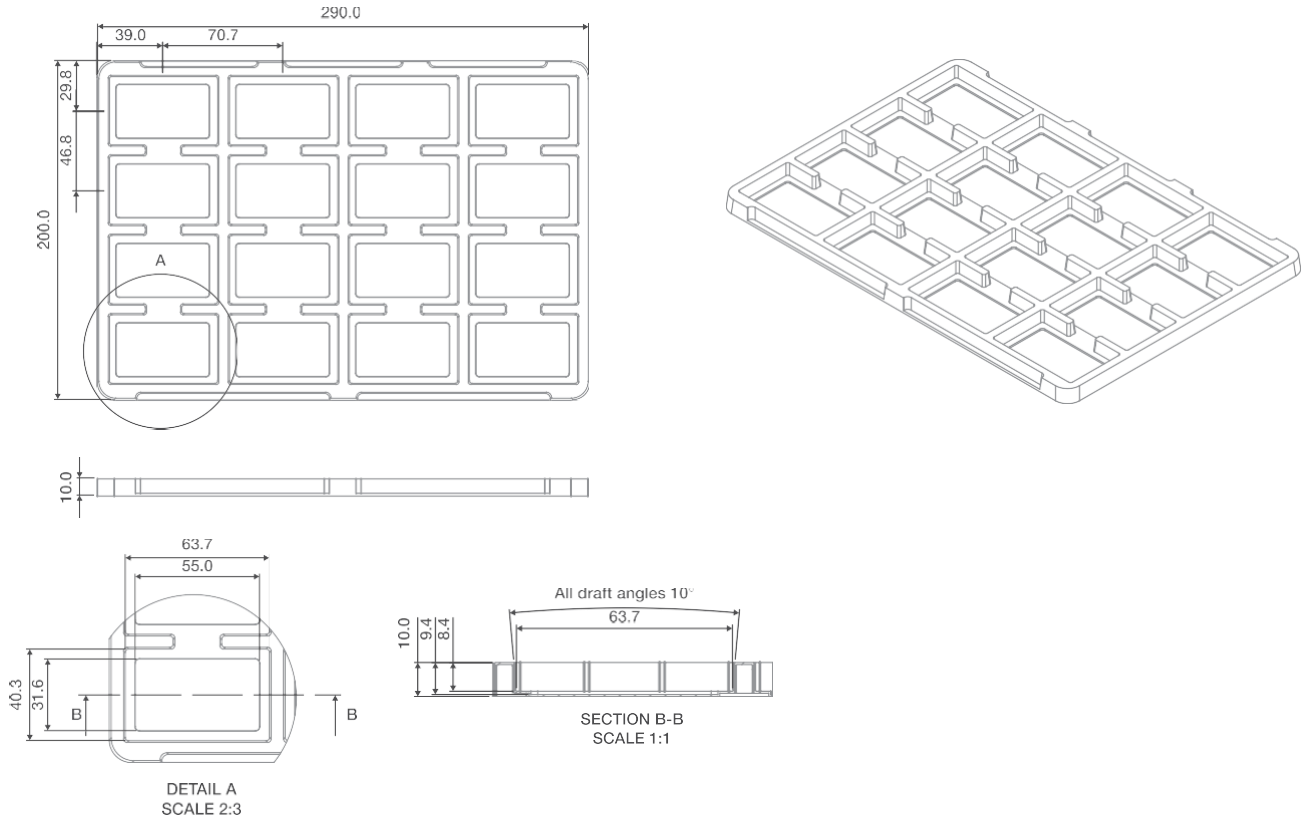
### 11.5. How to use U.FI

In order to use U.FI connector instead of antenna or MM8030-2610RJ3 you just need to re-solder a resistor 90 degree angle which is marked in a blue circle.

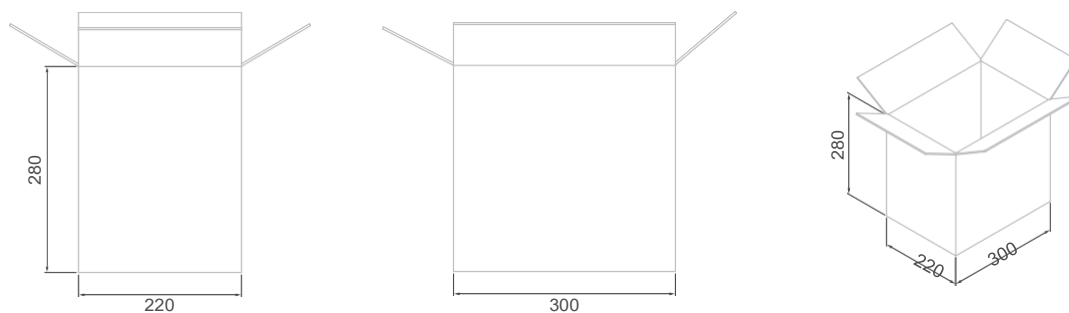
## Mango packaging and ordering info

Mango modules are packed into trays. Each tray fits 16 modules.  
Every 5 trays are vacuum sealed and one standard packaging box contains 400 modules.

**FIGURE 12-1. MANGO TRAY DIMENSIONS**



**FIGURE 12-2. STANDARD PACKAGING BOX DIMENSIONS**



**TABLE 12-3. ORDERING PART NUMBERS**

|                  |                                                                          |
|------------------|--------------------------------------------------------------------------|
| <b>Mango</b>     | Mango module, commercial temperature range 0°C to 65°C, IPQ 6010 SoC     |
| <b>Mango-I</b>   | Mango-I module, industrial temperature range -40°C to 85°C, IPQ 6010 SoC |
| <b>Mango-DVK</b> | Development kit, based on Mango-I module, IPQ 6010 SoC                   |

## Document Revision History

| Revision | Revision Date | Description                                                         |
|----------|---------------|---------------------------------------------------------------------|
| v1.0     | 09-11-2020    | Initial release                                                     |
| v1.1     | 19-10-2021    | Added RF characteristics and power consumption, other minor changes |
| V1.2     | 17-11-2021    | Added reflow recommendations                                        |
| V1.3     | 13-04-2022    | Renewed DVK dimensions and heatsink. Fixed BOOT_CONFIG[13] pin.     |

**FCC Caution:**

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

**IMPORTANT NOTE:**

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

**FCC Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

#### ISED Statement

This device complies with Industry Canada license -exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause interference, and (2) This device must accept any interference, including interference that may cause an undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Radiation Exposure Statement

This equipment complies with Canada radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

#### Déclaration d'exposition aux radiations

Cet équipement est conforme Canada limites d'exposition aux radiations dans un environnement non contrôlé. Cet équipement doit être installé et utilisé à distance minimum de 20cm entre le radiateur et votre corps.

This device is intended only for OEM integrators under the following condition: The transmitter module may not be co-located with any other transmitter or antenna. As long as the condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes:

Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne. Tant que les 1 condition ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

#### Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the ISED cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

Any company of the host device which install this modular with limit modular approval should perform the test of radiated emission and spurious emission according to RSS-247 and RSSGen requirement, only if the test result comply with RSS-247 and RSS-Gen

requirement, then the host can be sold legally.

5 GHz band (W52): Indoor use only

Note Importante:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ISED ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada. toute entreprise de l'hôte qui installent ce dispositif modulaire avec limite approbation devrait effectuer l'essai des modules et des rayonnements non essentiels des émissions rayonnées selon RSS-247 et le cnr - gen, seulement si le résultat d'essai conforme RSS-247 et le cnr - gen, puis l'hôte peut être vendu légalement.

End Product Labeling

The final end product must be labeled in a visible area with the following: Contains IC: 11468A-MAN.

Plaque signalétique du produit final

Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:

Contient des IC: 11468A-MAN.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

## Integration instructions for host product manufacturers according to KDB 996369

### D03 OEM

#### Manual v01

##### 13.1 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C&E has been investigated. It is applicable to the modular.

##### 13.2 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

##### 13.3 Limited module procedures

Not applicable

##### 13.4 Trace antenna designs

Not applicable

##### 13.5 RF exposure considerations

To maintain compliance with FCC's RF Exposure guidelines, This equipment should be installed and operated with minimum distance of 20cm from your body.

##### 13.6 Antennas

This radio transmitter FCC ID: **Z9WMAN** has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

| Antenna Chain | Antenna type | Input impedance (Ohm) | Maximum antenna gain                                              |
|---------------|--------------|-----------------------|-------------------------------------------------------------------|
| 0             | Chip         | 50                    | 2.09 dBi/2.4-2.5GHz<br>4.32 dBi/5.15-5.85GHz                      |
| 1             | Chip         | 50                    | 2.09 dBi/2.4-2.5GHz<br>4.32 dBi/5.15-5.85GHz                      |
| 0             | Whip         | 50                    | 4.0 dBi/2.4~2.5GHz<br>4.5dBi/5.15~5.25GHz<br>5.0dBi/5.725~5.85GHz |
| 1             | Whip         | 50                    | 4.0 dBi/2.4~2.5GHz<br>4.5dBi/5.15~5.25GHz<br>5.0dBi/5.725~5.85GHz |

##### 13.7 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains FCC ID: **Z9WMAN**"

##### 13.8 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

##### 13.9 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B