PERFECT WIRELESS EXPERIENCE

SC151

Hardware Guide

V1.0

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Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

Contents

Applicable Models

No.	Applicable Model	Description
1	SC151-CN-00	4GB+64GB memory, suitable for China
2	SC151-CN-20	6GB+128GB memory, suitable for China
3	SC151-GL-00	4GB+64GB memory, suitable for Global
4	SC151-GL-20	6GB+128GB memory, suitable for Global

Change History

V1.0 (2023-12-20)	Initial version.

1 Foreword

1.1 Description

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of the SC151 module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1 Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 38.300 V16.7.0: 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Range 1 Standalone
- 3GPP TS 38.521-3 V16.7.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios
- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11n, IEEE Std 802.11ac,

IEEE Std 802.11ax;

- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 +HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.2.0, December 7, 2014
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07, 2017
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.1.1, August 07, 2019
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.2
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment -Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS)and Cell Broadcast Service (CBS)
- PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB
- Universal Serial Bus Specification 2.0
- Universal Serial Bus Specification 3.0

2 Product Overview

2.1 Product Introduction

The module integrates core components such as Baseband, Memory, PMU, Transceiver, PA; it supports long distance multi-mode communication such as NR, FDD/TDD-LTE, and WCDMA short-distance radio transmission technology, as well as GNSS wireless positioning technology. The module is embedded with Androidoperating system and support various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 1. Introduction to bands of SC151-CN

Mode	Band
WCDMA	Band 1/8
FDD-LTE	Band 1/3/5/8
TDD-LTE	Band 34/38/39/40/41
NR Sub-6	n1/3/5/8/28A/41/78/79
WIFI802.11a/b/g/n/ac/ax	2402MHz~2482MHz 5170MHz~5835MHz
BT5.2	2402MHz~2480MHz
GNSS	GPS (L1+L5)/Beidou/GLONASS/Galileo/QZSS

Table 2. Introduction to bands of SC151-GL

Mode	Band
WCDMA	Band 1/2/4/5/6/8/9/19
FDD-LTE	Band 1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/32/66/71
TDD-LTE	Band 38/40*/41/42/43/48/

Mode	Band
NR Sub-6	n1/2/3/5/7/8/12/14/20/25/28/30/38*/40*/41/48/66/71/77/78
WIFI802.11a/b/g/n/ac/ax	2402MHz~2482MHz 5170MHz~5835MHz 5925MZ~7125MHz
BT5.2	2402MHz~2480MHz
GNSS	GPS（L1+L5)/Beidou/GLONASS/Galileo/QZSS

(* means unused band)

2.2 Key Features

Table 3. Key features

Feature	Description
Power Supply	DC: 3.5–4.4 V, typical: 3.8 V
Application processor	4-Series Arm Cortex applications processor (Kryo CPU) Kryo Gold: Two high-performance cores up to 2.2 GHz Kryo Silver: Six low-power cores up to 1.95 GHz
Memory	4GB + 64GB 6GB + 128GB
Power class	Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands Class 3 (23dBm±2dB) for NR FDD bands Class 3 (23dBm±2dB) for NR TDD bands Class 2 (26dBm±2dB) for NR N41/N77/N78/N79 bands
WCDMA features	Support 3GPP R8 DC-HSPA+

	Support 16-QAM, 64-QAM and QPSK modulation CAT6 HSUPA: Maximum uplink rate 5.76Mbps CAT24 HSDPA: Maximum downlink rate 42Mbps
LTE features	Support FDD/TDD R16 Support FDD/TDD cat18 256 QAM for UL, 256 QAM for DL Support DL 4×4 MIMO (MID&HIGH Bands only) The maximum uplink rate of FDD is 170Mbit/s, and the maximum downlink rate is 780 Mbit/s The maximum uplink rate of TDD is 200 Mbit/s, and the maximum downlink rate is 1200 Mbit/s
SA features	3GPP Release 16 256 QAM for UL, 256 QAM for DL 15KHz SCS for FDD ,30KHz SCS for TDD Maximum downlink 2CA Maximum uplink rate 950Mbps, maximum downlink rate 2Gbps
EN-DC features	LTE modulation: downlink-256QAM, uplink-256QAM NR modulation: downlink-256QAM, uplink-256QAM LTE downlink supports up to 4x4 MIMO NR downlink supports up to 4x4 MIMO Maximum uplink peak rate 550Mbps Maximum downlink peak rate 2.5Gbps
WLAN features	Support 2.4G and 5G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac and 802.11ax, 2x2 MIMO.
Bluetooth features	BT5.2 (BR/EDR+BLE)

Satellite positioning	GPS（L1+L5)/Beidou/GLONASS/Galileo/QZSS
MIMO	DL 4MIMO: LTE:B1/2/3/4/7/25/30/38/40/41/42/43/48/66 NR: n1/2/3/7/25/30/38/40/41/48/66/77/78/79 UL 2MIMO: SC151-CN(LTE: B3, NR: n3) SC151-GL(n41, n78, n79)
HPUE	HPUE: n41, n78, n79
SRS	SC151-CN: 2T4R：n41,n78,n79 SC151-GL: 1T2R: n41； 1T4R: n77, n78
LCD interface	One 4-Lane MIPI_DSI D-PHY 1.2 interface Maximum rate 2.5Gbps/lane
Camera interface	Three 4-Lane MIPI_CSI D-PHY 1.2 interfaces Maximum rate 2.5Gbps/lane, configurable as 4 + 4 + 4
Audio interface	Analog audio input: three analog microphone inputs, no internal bias. Analog audio output: A set of differential earphone output. A set of stereo handset output. A set of differential Lineout output, requiring external audio PA.
USB interface	USB conforms to the 3.1 Gen 1 specification and is downward compatible with USB2.0. It can be used for data transmission and software debugging.
UIM interface	Two UIM card interfaces supporting 1.8 or 2.95V UIM card adaptation Support dual UIM dual standby single pass, support hot plug
UART interface	A set of debugging UART serial ports A set of LPI UART serial ports

	A set of four-wire serial ports supporting RTS and CTS hardware flow control
SD interface	Support 4-bit SD3.0, 1.8V/2.95V SD cards, and hot plug
I2C interface	Multiple I2C interfaces can be used for peripherals such as TP, camera, sensor etc.
ADC interface	Two channel universal ADCs
RTC	Supported
Antenna interface	Seven
Physical characteristics	Dimensions: 56.5 mm x 42.5 mm x 2.85 mm Package: 636 LGA Weight: About 16.4 g
Temperature range	Operating temperature[1]: -30°C~75°C@ Storage temperature: -40°C~85°C
Software update	USB/OTA/SD
RoHS	Comply with RoHS standard

When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Hardware Block Diagram

The functional block diagram is as follows.

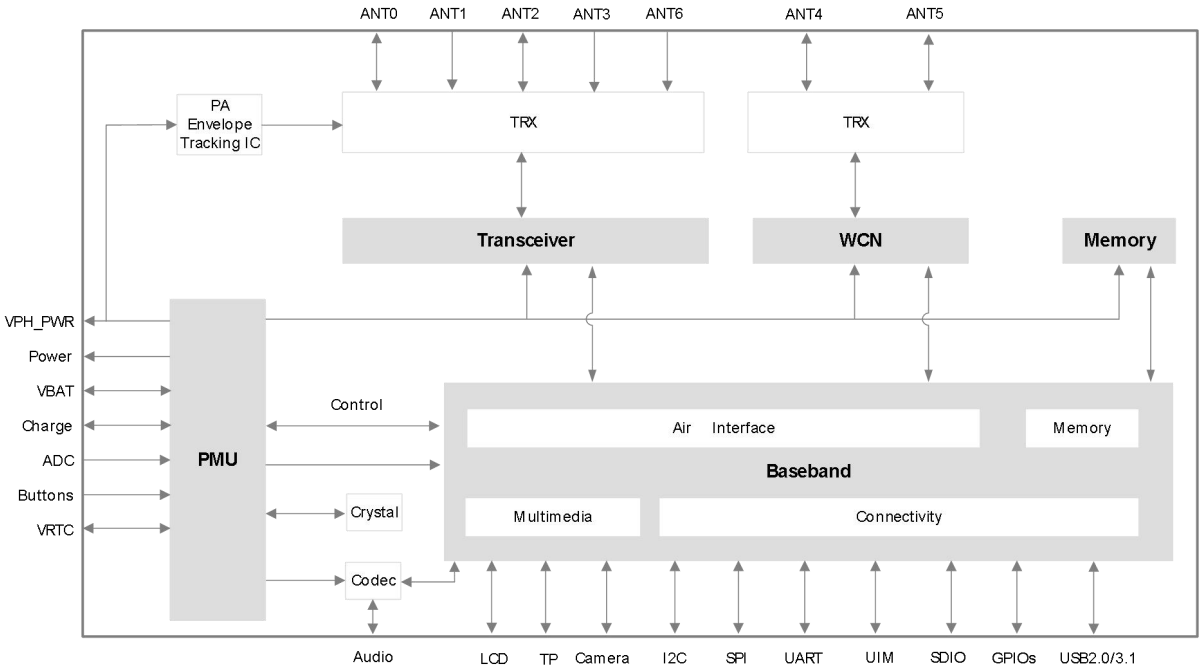


Figure 1. Hardware block diagram

2.4 Description of Development Kit

Fibocom configures a complete development board kit for the module, which makes it convenient for users to quickly understand the module performance. For the usage of development board, refer to *Fibocom_SC151_ADP User Guide* and *Fibocom_EVB-SOC_User Guide*.

3 Pin Definition

3.1 Pin Distribution

The SC151 module is packaged in a 636 LGA package. The pin assignment is as follows.

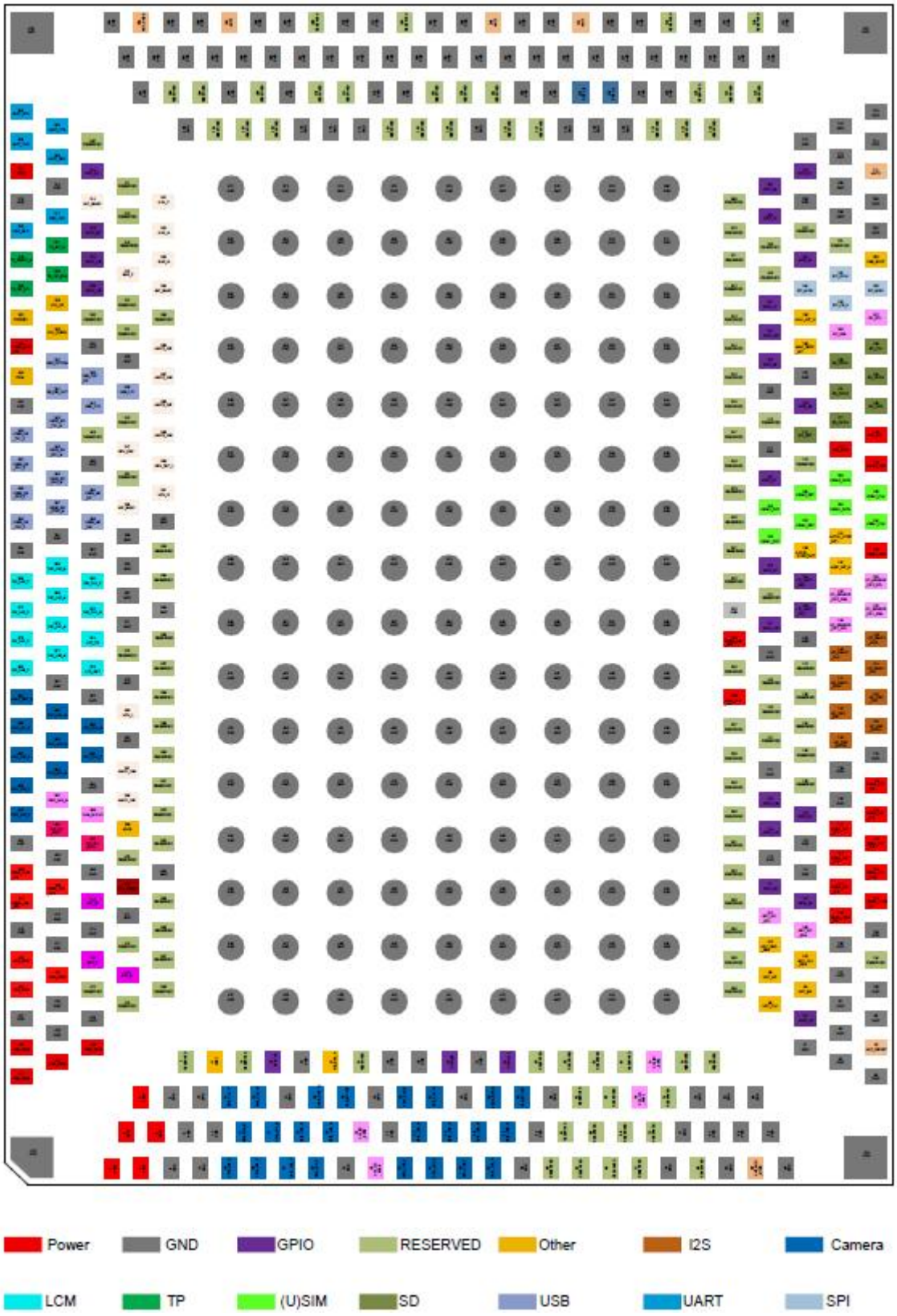


Figure 2. Pin distribution

3.2 Pin Description

Table 4. I/O type definition

Type	Description	Type	Description
PI	Power input	AIO	Analog input and output
PO	Power output	OD	Open drain
DI	Digital input	PU	Pull-up high level
DO	Digital output	PD	Pull-down low level
DIO	Digital input and output	T	Tristate, that is, high resistance state, which is determined by the peripheral circuit
AI	Analog input	G	Ground
AO	Analog output	- -	- -

Table 5. Power interfaces

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Feature
1, 2, 3, 4, 5	VBAT	PI/PO	- -	Module power supply	- -
420, 421, 424	VPH_PWR	PO	- -	The module supplies power to peripherals	- -
412	VREG_L6E_3P0	PO	- -	3.0V output power supply	- -
409	VREG_L4E_3P0	PO	- -	3.0V output power supply	- -
336	VREG_L21B_1P8	PO	- -	1.8V output power supply	- -
408	VREG_L21B_1P8	PO	- -	1.8V output power supply	- -
109	VREG_L21B_1P8	PO	- -	1.8V output power supply	- -
112	VREG_L21B_1P8	PO	- -	1.8V output power supply	- -
624	VREG_L4E_3P0	PO	- -	3.0V output power supply	- -

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Feature
626	VREG_L21B_1P8	PO	- -	1.8V output power supply	- -
312	VRTC	PI/PO	- -	Real-time clock power supply	- -
6, 8, 9, 10, 12, 13, 22, 23, 32, 34, 35, 37, 39, 46, 47, 56, 57, 58, 76, 77, 78, 81, 82, 83, 84, 85, 87, 88, 89, 90, 91, 93, 96, 97, 100, 101, 105, 108, 114, 115, 118, 125, 127, 129, 132, 143, 146, 171, 179, 182, 204, 205, 206, 208, 209, 212, 213, 214, 215, 216, 217, 218, 221, 224, 225, 228, 229, 230, 233, 234, 235, 236, 237 ,239, 240, 241, 243, 245, 246, 248, 249, 250, 252, 253, 255, 257, 260, 261, 264, 265, 266, 269, 270, 271, 272, 273, 275, 276, 277, 279, 281, 282, 284, 285, 288, 289, 290, 293, 295, 296, 297, 299, 300, 301, 303, 304, 313, 316, 334, 335, 344, 350, 359, 361, 362, 363, 364, 367, 371, 379, 381, 382, 387, 394, 404, 405, 406, 411, 413, 414, 416, 417, 425, 426, 427, 428, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 592, 595, 604, 623					298 GNDs

Table 6. Control interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
329	VOL_UP	DI	PU	Volume+	- -
333	VOL_DOWN	DI	PU	Volume-	- -
332	PWRKEY	DI	PU	Power on/off key interface	- -

Table 7. Charging Interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
418	BAT_P	AI	- -	Battery voltage detection input (+)	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
419	BAT_M	AI	- -	Battery voltage detection input (-)	- -
407	BAT_THERM	AI	- -	Battery temperature detection	- -
410	BAT_ID	AI	- -	Battery type detection	- -

Table 8. USIM interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
160	USIM1_VDD	PO	- -	(U)SIM1 card power supply	1.8V
165	USIM1_DATA	DI/DO	- -	(U)SIM1 card data	1.8V/2.95V
164	USIM1_CLK	DO	- -	(U)SIM1 card clock	1.8V/2.95V
162	USIM1_RST	DO	- -	(U)SIM1 card reset	1.8V/2.95V
159	USIM1_DET	DI	- -	(U)SIM1 card insertion and removal detection	1.8V
172	USIM2_VDD	PO	- -	(U)SIM2 card power supply	1.8V/2.95V
169	USIM2_DATA	DI/DO	- -	(U)SIM2 card data	1.8V/2.95V
168	USIM2_CLK	DO	- -	(U)SIM2 card clock	1.8V/2.95V
166	USIM2_RST	DO	- -	(U)SIM2 card reset	1.8V/2.95V
163	USIM2_DET	DI	- -	(U)SIM2 card insertion and removal detection	1.8V

Table 9. SDIO interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
176	VDD_SD	PO	- -	SD card power supply	2.95V
173	VDD_SDIO	PO	- -	SD card signal pull-up power supply	1.8V/2.95V
174	SD_DET	DI	- -	SD card insertion and removal detection	1.8V
181	SD_DATA3	DI/DO	- -	SDIO data bit 3	1.8V/2.95V

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
177	SD_DATA2	DI/DO	- -	SDIO data bit 2	1.8V/2.95V
185	SD_DATA1	DI/DO	- -	SDIO data bit 1	1.8V/2.95V
184	SD_DATA0	DI/DO	- -	SDIO data bit 0	1.8V/2.95V
180	SD_CMD	DI/DO	- -	SD card command	1.8V/2.95V
188	SD_CLK	DO	- -	SD card clock	1.8V/2.95V

Table 10. USB interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
429, 430, 431, 432	USB_VBUS	PI/ PO	- -	Charging power input Peripheral power supply in OTG mode Adapter insertion detection	- -
337	USB_OPTION	AI	- -	USB port configuration, power-on initialization test	- -
338	USB_PHY_PS	DI	- -	USB interface configuration detection	- -
341	SS_DIR_OUT	DO	- -	CC status output	- -
354	USB0_HS_DP	AI/ AO	- -	USB0 2.0 differential data (+)	- -
358	USB0_HS_DM	AI /AO	- -	USB0 2.0 differential data (-)	- -
356	USB0_SS_RX0_P	AI	- -	USB0 3.1 channel 1 receiving (+)	- -
353	USB0_SS_RX0_M	AI	- -	USB0 3.1 channel 1 receiving (-)	- -
360	USB0_SS_TX0_P	AO	- -	USB0 3.1 channel 1 transmitting (+)	- -
357	USB0_SS_TX0_M	AO	- -	USB0 3.1 channel 1 transmitting (-)	- -
352	USB0_SS_RX1_P	AI	- -	USB0 3.1 channel 2 receiving (+)	- -
349	USB0_SS_RX1_M	AI	- -	USB0 3.1 channel 2 receiving (-)	- -
348	USB0_SS_TX1_P	AO	- -	USB0 3.1 channel 2 transmitting (+)	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
345	USB0_SS_TX1_M	AO	- -	USB0 3.1 channel 2 transmitting (-)	- -
339	USB_CC1	AI	- -	USB Type-C control detection 1	- -
342	USB_CC2	AI	- -	USB Type-C control detection 2	- -

Table 11. SPI interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
197	SPI_SCLK	DO	- -	SPI clock	1.8V
193	SPI_CS_0	DO	- -	SPI chip selection	1.8V
196	SPI_MISO	DI	- -	SPI master input slave output	1.8V
194	SPI_MOSI	DO	- -	SPI master output slave input	1.8V

Table 12. UART interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
317	DBG_TXD	DO	_ _	Debug UART transmitting	1.8V
320	DBG_RXD	DI	_ _	Debug UART receiving	1.8V
154	LPI_UART_RXD	DI	_ _	LPI UART receiving	1.8V
150	LPI_UART_TXD	DO	_ _	LPI UART transmitting	1.8V
309	UART_RXD	DI	_ _	UART receiving	1.8V
308	UART_TXD	DO	_ _	UART transmitting	1.8V
305	UART_RTS	DO	_ _	UART requests to send	1.8V
306	UART_CTS	DI	_ _	UART clear to send	1.8V

LPI_ UART is only used for communication with sensors and audio IC, such as external codecs, WSA, Bluetooth, etc.

Table 13. I2C interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
189	I2C0_SDA	DI/DO	- -	I2C serial data	1.8V
192	I2C0_SCL	DO	- -	I2C serial clock	1.8V
152	LPI_SENSOR_I2C1_SDA	DI/DO	- -	Sensor I2C1 data	1.8V
149	LPI_SENSOR_I2C1_SCL	DO	- -	Sensor I2C1 clock	1.8V
153	LPI_SENSOR_I2C2_SDA	DI/DO	- -	Sensor I2C2 data	1.8V
156	LPI_SENSOR_I2C2_SCL	DO	- -	Sensor I2C2 clock	1.8V
71	CCI_I2C_SDA2	DI/DO	- -	CAM2 I2C data	1.8V
70	CCI_I2C_SCL2	DO	- -	CAM2 I2C data	1.8V
401	CCI_I2C_SDA1	DI/DO	- -	CAM1 I2C data	1.8V
402	CCI_I2C_SCL1	DO	- -	CAM1 I2C data	1.8V
33	CCI_I2C_SDA0	DI/DO	- -	CAM0 I2C data	1.8V
36	CCI_I2C_SCL0	DO	- -	CAM0 I2C data	1.8V

Table 14. NFC interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
95	NFC_CLK	DO	- -	NFC clock	1.8V
102	NFC_CLK_REQ	DI	- -	NFC clock request	1.8V
103	NFC_DWL_REQ	DO	- -	NFC download control request	1.8V
98	NFC_EN	DO	- -	NFC enabling	1.8V
99	NFC_INT	DI	- -	NFC interrupt	1.8V
106	NFC_I2C_SDA	DI/DO	- -	NFC I2C data	1.8V
107	NFC_I2C_SCL	DO	- -	NFC I2C clock	1.8V

Table 15. Display interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
366	DSI_CLK_P	AO	- -	MIPI DSI differential CLK +	- -
370	DSI_CLK_N	AO	- -	MIPI DSI differential CLK -	- -
380	DSI_LN0_P	AO	- -	MIPI DSI differential lane 0 +	- -
377	DSI_LN0_N	AO	- -	MIPI DSI differential lane 0 -	- -
376	DSI_LN1_P	AO	- -	MIPI DSI differential lane 1 +	- -
373	DSI_LN1_N	AO	- -	MIPI DSI differential lane 1 -	- -
372	DSI_LN2_P	AO	- -	MIPI DSI differential lane 2 +	- -
369	DSI_LN2_N	AO	- -	MIPI DSI differential lane 2 -	- -
368	DSI_LN3_P	AO	- -	MIPI DSI differential lane 3 +	- -
365	DSI_LN3_N	AO	- -	MIPI DSI differential lane 3 -	- -
374	LCD_TE	DI	- -	LCD tearing effect	1.8V
378	LCD_RST	DO	- -	LCD reset signal	1.8V
340	PWM1	DO	- -	Backlight control 1	- -

Table 16. TP interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
324	TS_RESET_N	DO	- -	TP reset	1.8V
321	TS_INT_N	DI	- -	TP interrupt	1.8V
325	TS_I2C_SDA	DI/DO	- -	TP I2C data	1.8V
328	TS_I2C_SCL	DO	- -	TP I2C data	1.8V

Table 17. Camera interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
14	CSI0_CLK_P	AI	- -	MIPI CSI0 differential CLK +	- -
18	CSI0_CLK_N	AI	- -	MIPI CSI0 differential CLK -	- -
16	CSI0_LN0_P	AI	- -	MIPI CSI0 differential lane 0 +	- -
17	CSI0_LN0_N	AI	- -	MIPI CSI0 differential lane 0 -	- -
20	CSI0_LN1_P	AI	- -	MIPI CSI0 differential lane 1 +	- -
21	CSI0_LN1_N	AI	- -	MIPI CSI0 differential lane 1 -	- -
24	CSI0_LN2_P	AI	- -	MIPI CSI0 differential lane 2 +	- -
25	CSI0_LN2_N	AI	- -	MIPI CSI0 differential lane 2 -	- -
28	CSI0_LN3_P	AI	- -	MIPI CSI0 differential lane 3 +	- -
29	CSI0_LN3_N	AI	- -	MIPI CSI0 differential lane 3 -	- -
30	CAM_MCLK0	DO	- -	Camera0 clock	1.8V
26	CAM_RST0	DO	- -	Camera0 reset	1.8V
147	GPIO_102	DI/DO	- -	Camera0 PWD signal	1.8V
38	CSI1_CLK_P	AI	- -	MIPI CSI1 differential CLK +	- -
42	CSI1_CLK_N	AI	- -	MIPI CSI1 differential CLK -	- -
40	CSI1_LN0_P	AI	- -	MIPI CSI1 differential lane 0 +	- -
41	CSI1_LN0_N	AI	- -	MIPI CSI1 differential lane 0 -	- -
44	CSI1_LN1_P	AI	- -	MIPI CSI1 differential lane 1 +	- -
45	CSI1_LN1_N	AI	- -	MIPI CSI1 differential lane 1 -	- -
48	CSI1_LN2_P	AI	- -	MIPI CSI1 differential lane 2 +	- -
49	CSI1_LN2_N	AI	- -	MIPI CSI1 differential lane 2 -	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
52	CSI1_LN3_P	AI	- -	MIPI CSI1 differential lane 3 +	- -
53	CSI1_LN3_N	AI	- -	MIPI CSI1 differential lane 3 -	- -
54	CAM1_MCLK	DO	- -	Camera1 clock	1.8V
50	CAM1_RST	DO	- -	Camera1 reset	1.8V
123	GPIO_108	DI/DO	- -	Camera1 PWD signal	1.8V
390	CSI2_CLK_P	AI	- -	MIPI CSI2 differential CLK +	- -
386	CSI2_CLK_N	AI	- -	MIPI CSI2 differential CLK -	- -
392	CSI2_LN0_P	AI	- -	MIPI CSI2 differential lane 0 +	- -
389	CSI2_LN0_N	AI	- -	MIPI CSI2 differential lane 0 -	- -
388	CSI2_LN1_P	AI	- -	MIPI CSI2 differential lane 1 +	- -
385	CSI2_LN1_N	AI	- -	MIPI CSI2 differential lane 1 -	- -
396	CSI2_LN2_P	AI	- -	MIPI CSI2 differential lane 2 +	- -
393	CSI2_LN2_N	AI	- -	MIPI CSI2 differential lane 2 -	- -
400	CSI2_LN3_P	AI	- -	MIPI CSI2 differential lane 3 +	- -
397	CSI2_LN3_N	AI	- -	MIPI CSI2 differential lane 3 -	- -
398	CAM2_MCLK	DO	- -	Camera2 clock	- -
384	CAM2_RST	DO	- -	Camera2 reset	1.8V
326	GPIO_105	DI/DO	- -	Camera2 PWD signal	1.8V
33	CCI_I2C_SDA0	DI/DO	- -	Camera0 I2C data	1.8V
36	CCI_I2C_SCL0	DO	- -	Camera0 I2C clock	1.8V
401	CCI_I2C_SDA1	DI/DO	- -	Camera1 I2C data	1.8V
402	CCI_I2C_SCL1	DO	- -	Camera1 I2C clock	1.8V

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
71	CCI_I2C_SDA2	DI/DO	- -	Camera2 I2C data	1.8V
70	CCI_I2C_SCL2	DO	- -	Camera2 I2C clock	1.8V
116	VREG_L1P_1P05	PO	- -	Camera 1.05V power output	- -
121	VREG_L2P_1P1	PO	- -	Camera 1.1V power output	- -
113	VREG_L3P_2P8	PO	- -	Camera 2.8V power output	- -
124	VREG_L4P_2P9	PO	- -	Camera 2.9V power output	- -
128	VREG_L5P_2P8	PO	- -	Camera 2.8V power output	- -
117	VREG_L6P_1P8	PO	- -	Camera 1.8V power output	
120	VREG_L7P_2P8	PO	- -	Camera 2.8V power output	- -

Table 18. Audio interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
581	AUX_P	AO	- -	Differential Lineout output+	External audio PA is required
582	AUX_M	AO	- -	Differential Lineout output -	
323	EAR_P	AO	- -	Handset differential output +	- -
583	EAR_M	AO	- -	Handset differential output -	- -
355	MIC_BIAS1	AO	- -	MIC1 bias output voltage	- -
584	MIC_BIAS2	AO	- -	MIC2 bias output voltage	- -
314	MIC_BIAS3	AO	- -	MIC3 bias output voltage	- -
395	AMIC1_INP	AI	- -	Analog MIC1 input +	- -
391	AMIC1_INM	AI	- -	Analog MIC1 input -	- -
586	AMIC2_INP	AI	- -	Analog MIC2 input +	- -
587	AMIC2_INM	AI	- -	Analog MIC2 input -	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
588	AMIC3_INP	AI	- -	Analog MIC3 input +	- -
589	AMIC3_INM	AI	- -	Analog MIC3 input -	- -
383	HPH_L	AO	- -	Headphone left channel output	- -
347	HPH_REF	AI	- -	Headphone reference ground	- -
591	HPH_R	AO	- -	Headphone right channel output	- -
590	HPH_DET_L	AI	- -	Headphone insertion and removal detection	- -

Table 19. LPI_DMIC interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
144	LPI_DMIC1_CLK	DO	- -	Digital MIC1 clock	1.8V
141	LPI_DMIC1_DATA	DI/DO	- -	Digital MIC1 data	1.8V
145	LPI_DMIC2_CLK	DO	- -	Digital MIC2 clock	1.8V
148	LPI_DMIC2_DATA	DI/DO	- -	Digital MIC2 data	1.8V

Table 20. MI2S interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
140	LPI_I2S2_CLK	DO	- -	LPI_I2S bit clock	1.8V
137	LPI_I2S2_WS	DO	- -	LPI_I2S field selection	1.8V
133	LPI_I2S2_DATA0	DI/DO	- -	LPI_I2S data channel 0	1.8V
136	LPI_I2S2_DATA1	DI/DO	- -	LPI_I2S data channel 1	1.8V
140	LPI_I2S2_CLK	DO	- -	LPI_I2S bit clock	1.8V

Table 21. Sensor interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
161	ACCEL_GYRO_INT1	DI	- -	Acceleration/gyro sensor interrupt 1	1.8V
158	ACCEL_GYRO_INT2	DI	- -	Acceleration/gyro sensor interrupt 2	1.8V
186	MAG_DRDY_INT	DI	- -	Geomagnetic sensor interrupt	1.8V
157	ALSP_INT_N	DI	- -	Light sensor interrupt	1.8V
190	HALL_INT_N	DI	- -	Hall sensor interrupt	1.8V
152	LPI_SENSOR_I2C1_SDA	DI/DO	- -	Sensor I2C1 data	1.8V
149	LPI_SENSOR_I2C1_SCL	DO	- -	Sensor I2C1 clock	1.8V
153	LPI_SENSOR_I2C2_SDA	DI/DO	- -	Sensor I2C2 data	1.8V
156	LPI_SENSOR_I2C2_SCL	DO	- -	Sensor I2C2 clock	1.8V

Table 22. ADC interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
399	ADC0	AI	- -	Universal ADC interface	Maximum sample voltage is 1.8V
11	ADC1	AI	- -	Universal ADC interface	

Table 23. Motor interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
27	VIB_DRV_P	PO	- -	Motor drive output	1.504V to 3.544V

Table 24. GPIO interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
110	GPIO_34	DI/DO	PD	General GPIO	--
111	GPIO_99	DI/DO	PD	General GPIO	--

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
43	GPIO_95	DI/DO	PD	General GPIO	--
198	GPIO_81	DI/DO	PD	General GPIO	--
123	GPIO_108	DI/DO	PD	General GPIO	--
51	GPIO_123	DI/DO	PD	General GPIO	--
178	GPIO_98	DI/DO	PD	General GPIO	--
210	GPIO_51	DI/DO	PD	General GPIO	--
203	GPIO_73	DI/DO	PD	General GPIO	--
94	GPIO_33	DI/DO	PD	General GPIO	--
119	GPIO_127	DI/DO	PD	General GPIO	--
19	GPIO_78	DI/DO	PD	General GPIO	--
155	GPIO_82	DI/DO	PD	General GPIO	--
191	GPIO_74	DI/DO	PD	General GPIO	--
122	GPIO_91	DI/DO	PD	General GPIO	--
167	GPIO_97	DI/DO	PD	General GPIO	--
183	GPIO_50	DI/DO	PD	General GPIO	--
187	GPIO_100	DI/DO	PD	General GPIO	--
207	GPIO_84	DI/DO	PD	General GPIO	--
310	GPIO_83	DI/DO	PD	General GPIO	--
318	GPIO_90	DI/DO	PD	General GPIO	--
322	GPIO_126	DI/DO	PD	General GPIO	BOOT_CONFIG
326	GPIO_105	DI/DO	PD	General GPIO	BOOT_CONFIG
147	GPIO_102	DI/DO	PD	General GPIO	--

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature

- The GPIO of BOOT_CONFIG can not be pulled up externally, otherwise it may cause no boot.
- All GPIOs do not allow level status changes during system startup.

Table 25. Antenna interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
211	ANT0	AI/AO	--	Antenna 0 interface	--
244	ANT1	AI/AO	--	Antenna 1 interface	--
256	ANT2	AI/AO	--	Antenna 2 interface	--
292	ANT3	AI/AO	--	Antenna 3 interface	--
302	ANT_GNSS	AI	--	GNSS antenna interface	--
92	ANT_WIFI/BT	AI/AO	--	WIFI/BT antenna interface	--
86	ANT_WIFI_MIMO	AI/AO	--	WIFI MIMO antenna interface	--

Table 26. Other interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
200	USB_BOOT	DI	PD	Force the module to enter emergency download mode	- -
242	GRFC_0	IO	--	Universal RF control 0	- -
238	GRFC_1	IO	--	Universal RF control 1	BOOT_CONFIG

Table 27. Reserved interfaces

Pin No.	DC Feature
327, 330, 331, 585, 346, 343, 258, 259, 262, 263, 267, 268, 274, 278, 280, 283, 286, 287, 291, 294, 298, 80, 195, 201, 219, 231, 227, 232, 415, 422, 423, 31, 75, 104, 199, 220, 222, 223, 226, 247, 251, 254, 608, 609, 610, 613,	RESERVED

Pin No.	DC Feature
614, 615, 616, 617, 618, 625, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 138, 139, 135, 134, 130, 131, 593, 594, 596, 597, 598, 599, 600, 601, 602, 603, 605, 606, 607,375, 619, 620, 621, 622, 79, 62, 66, 60, 61, 68, 69, 64, 65, 72, 73, 74, 67, 7, 126, 612, 611, 142, 15, 403, 311, 202, 175, 315, 319, 307, 151, 351, 170, 59, 55, 63	

4 Application Interfaces

4.1 Power Interfaces

4.1.1 Power Supply Circuit

The module provides five VBAT pins and three VPH_PWR pins. VBAT is used to connect external power supply to supply power to the module, and VPH_PWR pins are used to supply power to peripherals.

To ensure the instantaneous voltage of VBAT input power supply is no less than 3.5V, it is recommended to connect two 220μF tantalum capacitors with low ESR and filter capacitors of 1uF, 100nF, 39pF and 33pF in parallel to the VBAT input end of the module. Besides, the PCB cable of VBAT should be as short and wide as possible (no narrow than 3 mm) and the ground plane of the power section should be complete. That can reduce the equivalent impedance of the VBAT cable and ensure at maximum transmitting power, significant voltage drop will not occur at high currents.

To improve the anti-surge ability of the module, it is recommended to add a high-power surge tube near the VBAT end of the module. The reference design of the power supply circuit is shown in the following figure:

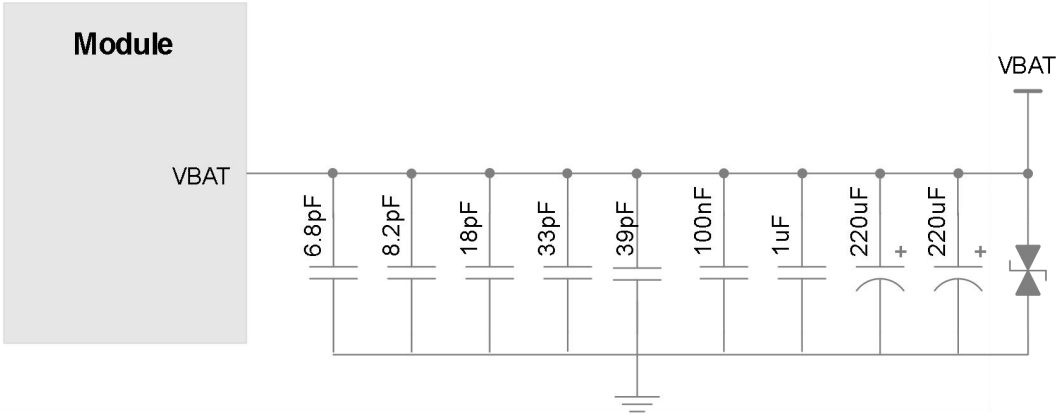


Figure 3. Power supply reference circuit

Filter capacitors should be placed close to the power supply pin, and the capacitance value should be smaller to be closer to the corresponding power supply pin. The filter capacitor is placed on the same side as the module, and must not cross the layer, otherwise there will be the risk of TIS interference, and

the trace is as short and wide as possible.

Table 28. Filter capacitor introduction

Recommended Capacitor	Description
ESD	ESD devices are required to protect ESD and EOS. It is recommended to use ESDH5V0FD1.
220uF x 2	For the stabilizing capacitor, select a low ESR (0.7Ω) capacitor with a capacitance value of not less than 220uF x 2. The recommended model is TAJC227K010RNJ. This capacitor must not be omitted, as it may lead to random system reboots.
1uF, 100nF	Filter out interference caused by clock and digital signals.
220pF, 150pF, 39pF, 33pF	Filter out low-frequency interference in 700MHz to 900MHz.
18pF, 10pF, 8.2pF	Filter out mid/high-frequency interference in the 1700MHz to 2700MHz.
6.8pF, 3.3pF	Filter out interference in the 3.5GHz to 5GHz frequency range.

Table 29. Power supply

Parameter	I/O	Minimum Value	Typical Value	Maximum Value	Unit
VBAT(DC)	PI/PO	3.5	3.8	4.4	V
VPH_PWR	PO	3.5	3.8	VBAT	V

The recommended filter capacitor can be adjusted by the customer based on specific circumstances. It is not a fixed value.

4.1.2 Voltage Drop

The input range of the VBAT power is 3.5 V to 4.4 V and the recommended value is 3.8 V. The performance of the power supply such as its load capacity and ripple will directly affect the operating performance and stability of the module. In extreme cases, the peak current of the module can reach 3A. If the power supply capacity is insufficient, the power supply transient voltage drops below 3.5 V, which may cause the module power off or restart. The power supply voltage drop is shown in the following figure:

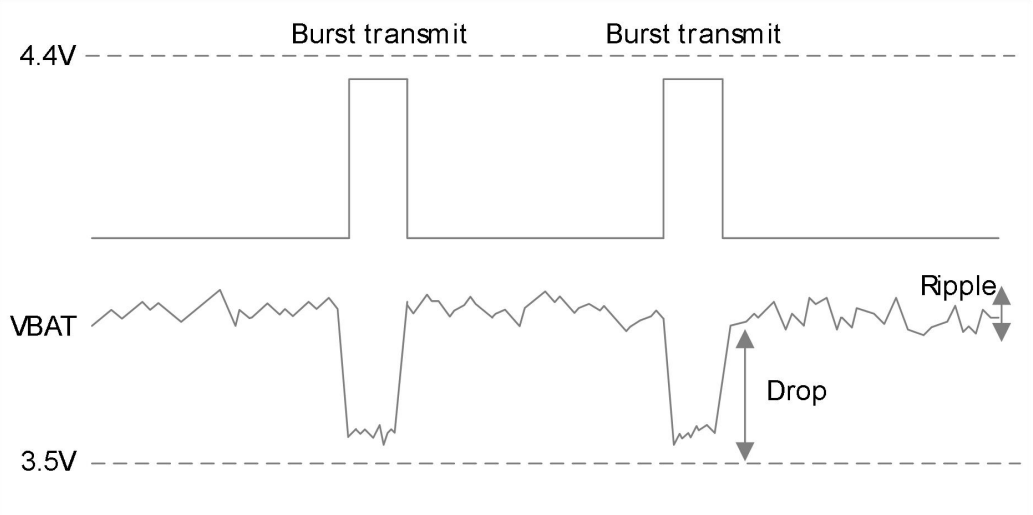


Figure 4. Power supply requirements

The voltage range of the VBAT power supply must be guaranteed between 3.5V and 4.4V, including the superposition value of voltage such as ripple, sag and transient overshoot.

4.1.3 VRTC Interfaces

The VRTC supplies power to the RTC clock in the module. After the module VBAT power supply is powered on, the VRTC outputs voltage. To maintain the real-time clock when the VBAT is off, use an external power supply (such as a button battery). The VRTC parameters are as follows:

Table 30. VRTC parameters

Parameter	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.0	3.0	3.25	V
VRTC input current (clock is normal)	-	12	30	uA

4.1.4 Power Output

The module has multiple power outputs, used for peripheral circuit power supply. In application, 33pF and 10pF capacitors can be connected in parallel to effectively filter high-frequency interference.

Table 31. Power output

Pin No.	Pin Name	Function	Default Voltage (V)	Drive Current (mA)	Sleep Status
420, 421, 424	VPH_PWR	Peripheral main power supply	VBAT	1A	ON
412	VREG_L6E_3P0	Sensor VDD power supply	3.0V	300mA	ON
409, 624	VREG_L4E_3P0	LCD/TP VDD power supply	3.0V	200mA	OFF
109, 112, 336, 408, 626	VREG_L21B_1P8	System IOVDD	1.8V	600mA	ON

4.2 Control Interfaces

4.2.1 Power-on/off

4.2.1.1 Power-on

The module has one power on control signal to control the module to power on/off, restart, sleep/wake up.

After VBAT is powered, pull down the PWRKEY pin for 2s to 6s can triggermodule power on. The button control and OC drive power on reference design is shownas follows:

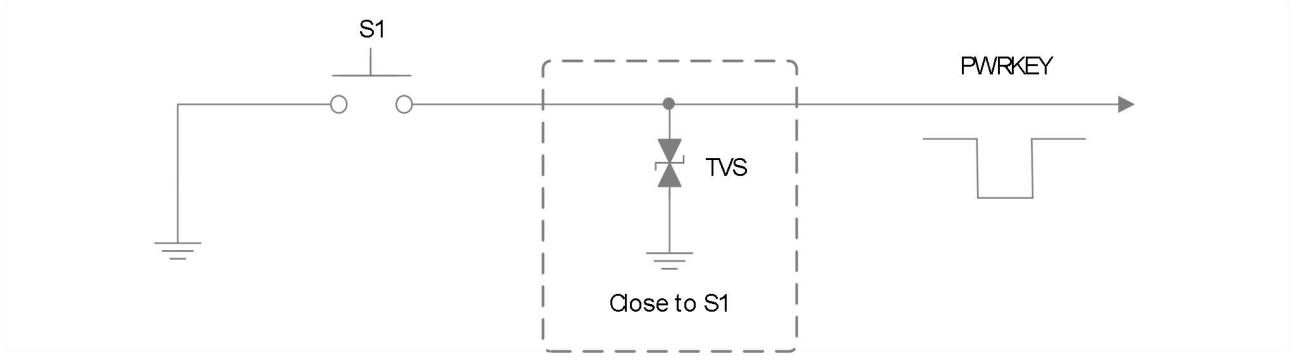


Figure 5. Reference design of key power-on circuit

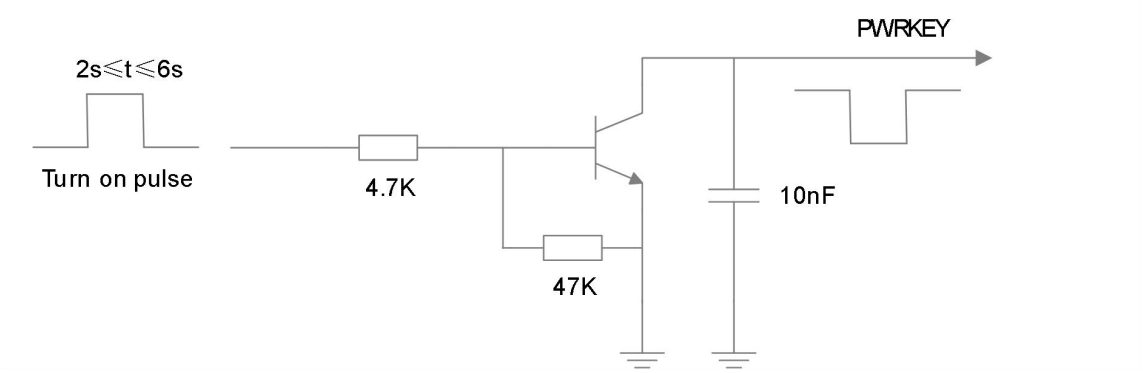


Figure 6. Reference design of OC drive power-on circuit

The power on sequence is shown in the following figure.

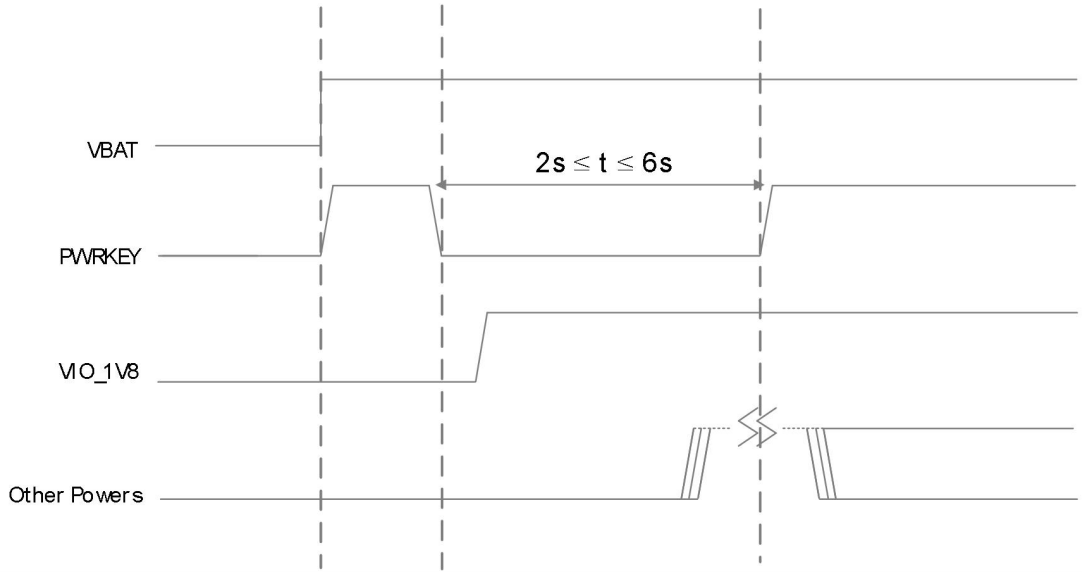


Figure 7. Startup timing sequence

4.2.1.2 Power-off

Normal power off: when the module is in operating mode, pull down the PWRKEY pin for 2s to 6s, user interface will display selection box (select power off or restart).

Forced reset: Pull down the PWRKEY pin for 8s to 15s to force the system to reset. The forced reset sequence is shown in the following figure:

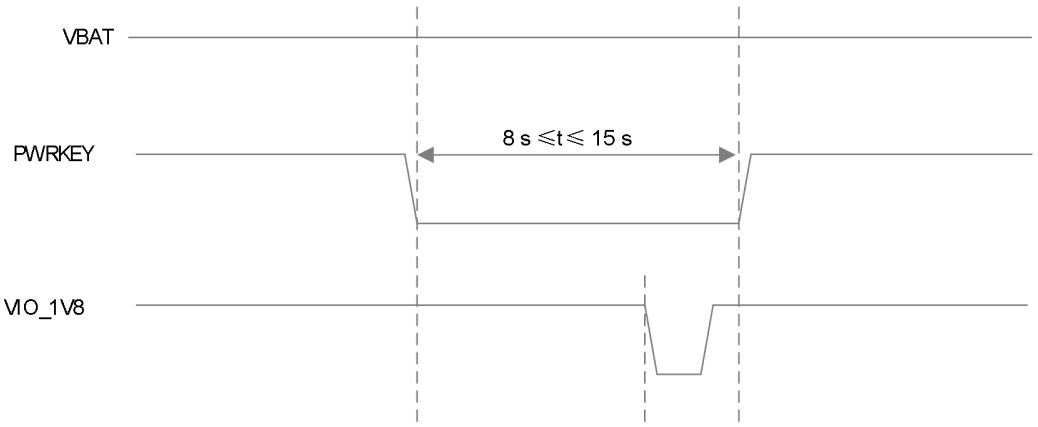


Figure 8. Forced reset timing sequence

When the system is abnormal or shutdown, you can use force power off method to reset the module, please use normal method generally, otherwise may cause data loss and other anomalies.

4.2.2 Sleep and Wakeup

Sleep: When the module is in standby mode, pull down the PWRKEY pin 0.5s, and the module will enter the sleep mode. The system supports automatic sleep. The time from standby to sleep can be configured through software.

Wakeup: When the module is in sleep mode, pull down the PWRKEY pin 0.5s, and the module can be woken up.

4.2.3 Volume Control

VOL_UP and VOL_DOWN are the volume up and volume down control button. For its circuit design, refer to the power on circuit design.

4.2.4 Forced Download

The module provides the USB_BOOT pin as the emergency download trigger interface. Pulling the USB_BOOT pin to VREG_L21B_1P8 during the booting phase triggers the module to enter the

emergency download mode. This is used for final processing when the product fails to start or run properly due to a fault. Reserve test sites for the convenience of subsequent software upgrades and commissioning. USB_BOOT reference circuit design is shown as follows:

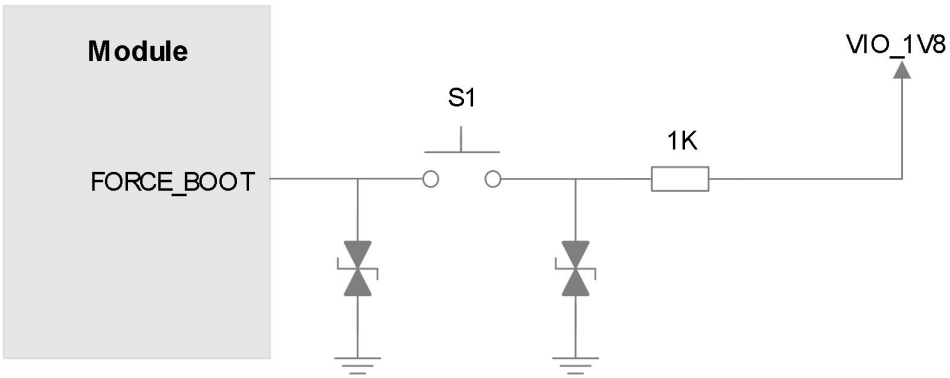


Figure 9. Reference circuit design of forced download

4.3 USB

4.3.1 USB Pin Definition

The module supports a set of USB 3.1 interface that is downward compatible with USB 2.0 (supports software download). USB 3.1 supports the SS (5Gbps) mode and cannot support software download. USB supports OTG and HUB expansion. The pin definition of USB interface is as follows:

Table 32 USB 3.1 pin definition

Pin No.	Pin Name	I/O	Description	Note
429, 430, 431, 432	USB_VBUS	PI/PO	USB insertion detection, charging, Host mode external power supply	- -
337	USB_OPTION	AI	USB interface type configuration, power-on initialization test	The pin is suspended when connected to the Type C port and is grounded when connected to the Micro B port
338	USB_PHY_PS	DI	USB interface configuration check	When connecting the Micro B port, connect 1K resistance to

			the ground. When connecting the Type C port, this pin connects to the SS_DIR_OUT	
341	SS_DIR_OUT	DO	CC status output	- -
356	USB0_SS_RX0_P	AI	USB0 3.1 channel 1 receiving (+)	- -
353	USB0_SS_RX0_M	AI	USB0 3.1 channel 1 receiving (-)	- -
360	USB0_SS_TX0_P	AO	USB0 3.1 channel 1 transmitting (+)	- -
357	USB0_SS_TX0_M	AO	USB0 3.1 channel 1 transmitting (-)	- -
352	USB0_SS_RX1_P	AI	USB0 3.1 channel 2 receiving (+)	- -
349	USB0_SS_RX1_M	AI	USB0 3.1 channel 2 receiving (-)	- -
348	USB0_SS_TX1_P	AO	USB0 3.1 channel 2 transmitting (+)	- -
345	USB0_SS_TX1_M	AO	USB0 3.1 channel 2 transmitting (-)	- -
339	USB_CC1	AI	USB0 Type-C control detection 1	- -
342	USB_CC2	AI	USB0 Type-C control detection 2	- -

Table 33. USB 2.0 pin definition

Pin No.	Pin Name	I/O	Description	Note
354	USB0_HS_DP	AI/AO	USB0 2.0 differential data (+)	Software download is supported
358	USB0_HS_DM	AI/AO	USB0 2.0 differential data (-)	

USB 3.1 (TYPE-C) circuit reference design is shown in the following figure.

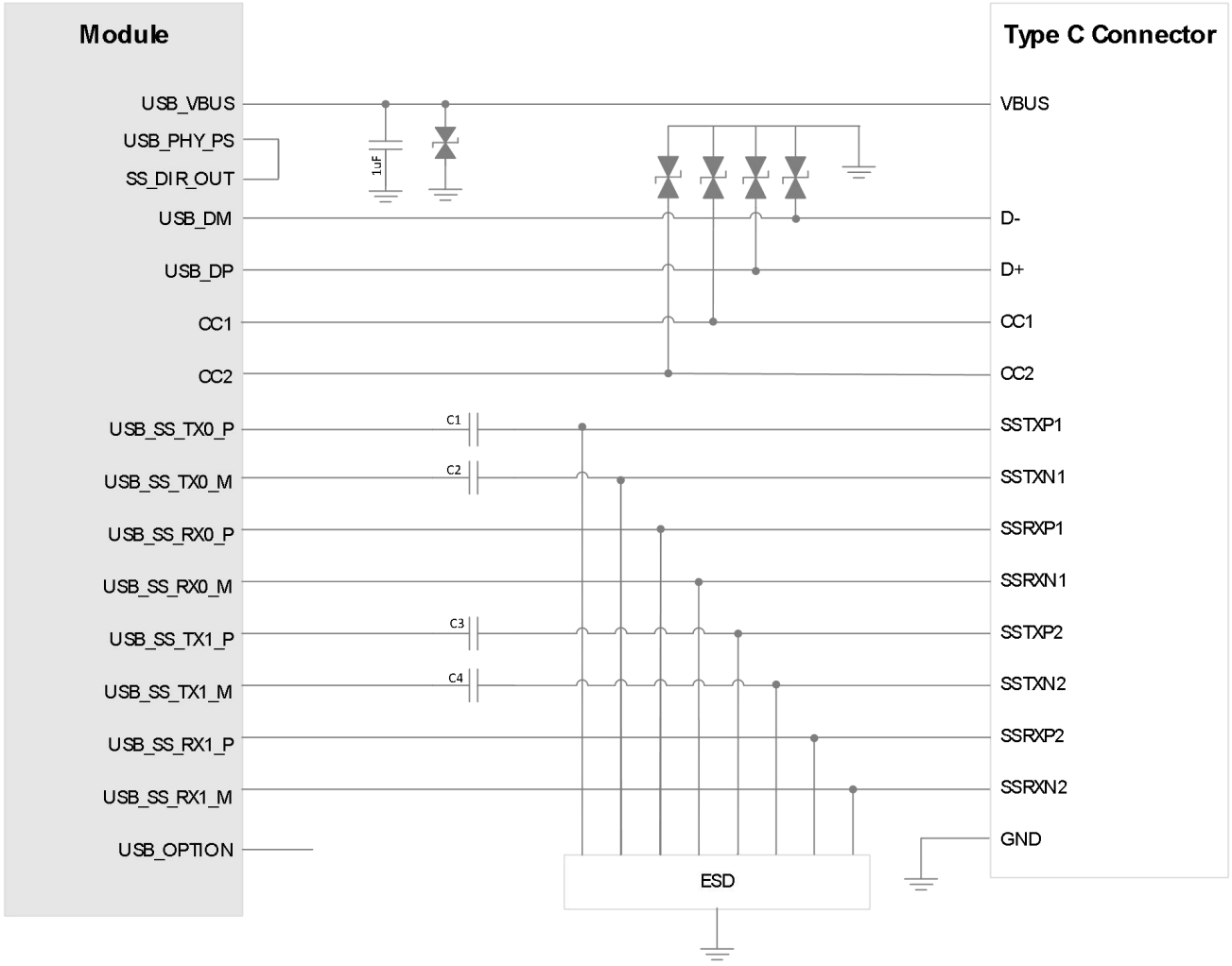


Figure 10. Reference circuit of USB 3.1

The reference circuit of USB 2.0 interface is designed as follows.

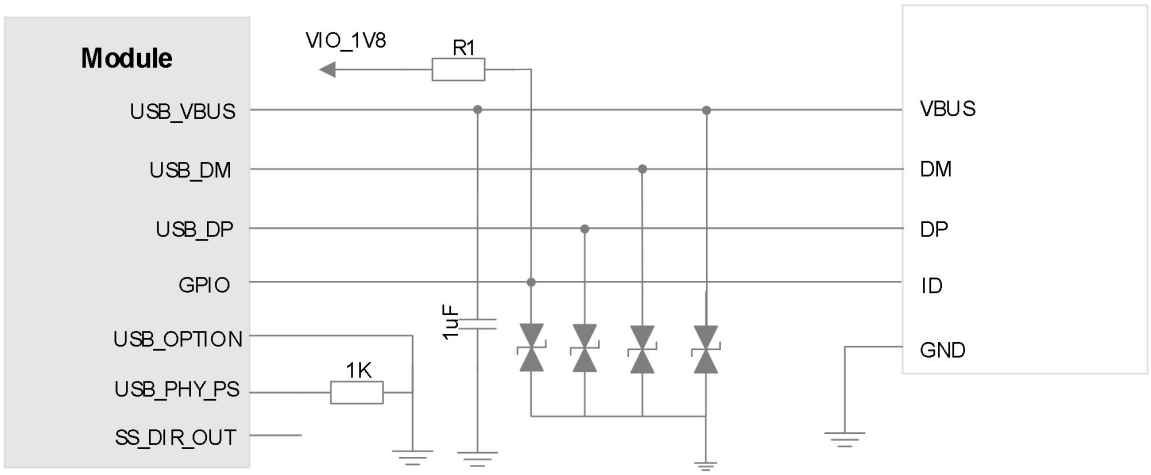


Figure 11. Reference circuit of USB 2.0

4.3.2 USB Design Considerations

USB is a high-speed signal line. It is important to pay special attention to follow guidelines in PCB layout:

- The USB signal line needs to be controlled with a 90Ω differential impedance with tolerance ±10%.
- The USB signal lines are treated with equal length, and the length difference of differential lines in the USB 2.0 signal group is controlled within 2 mm; The length difference of differential line in the USB 3.0 signal group is controlled within 0.7 mm, and the length difference between groups is controlled within 10 mm.
- It is recommended that the space of intra-lane differential line should be 4 times of the route width and the space between differential line and other routes should be controlled 4 times of the route width.
- ESD protection devices shall be added near the USB interface: The parasitic capacitance of ESD protection devices for USB 2.0 signals shall not exceed 2pF. The parasitic capacitance of the ESD protection device for USB 3.0 signals shall not exceed 0.2pF.

4.4 UART

The module defines three UART interfaces, all of which are in 1.8V voltage domain. Please refer to pin

description section for pin definition.

The voltage domain of each serial port is 1.8V. When communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip. The reference circuit design is as follows.

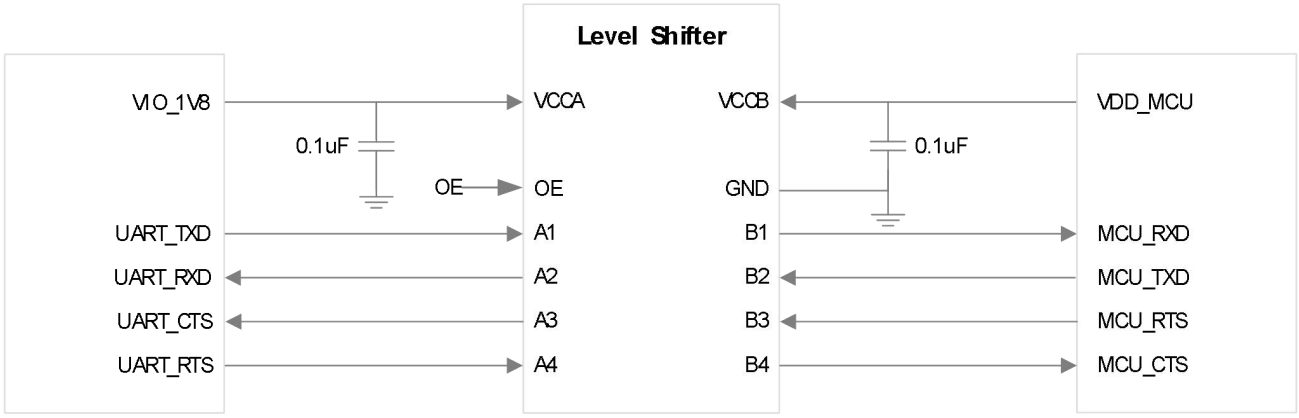


Figure 12. Reference design of level-shifting circuit

4.5 SPI

The module provides one set of SPI default interfaces that support master/slave mode. Please refer to pin description section for pin definition.

The reference schematic of SPI circuit is shown in the following figure.

Figure 13. SPI interface reference circuit

4.6 I2C

The module has multiple sets of general I2C interfaces, which can be used to connect peripherals respectively. Please refer to pin description section for pin definition.

Table 34. I2C interface pin definition

Pin No.	Pin Name	I/O	Description	Note
189	I2C0_SDA	DI/DO	I2C serial data	- -
192	I2C0_SCL	DO	I2C serial clock	- -
152	LPI_SENSOR_I2C1_SDA	DI/DO	External sensor I2C1 data	Dedicated to sensor
149	LPI_SENSOR_I2C1_SCL	DO	External sensor I2C1 clock	
153	LPI_SENSOR_I2C2_SDA	DI/DO	External sensor I2C2 data	
156	LPI_SENSOR_I2C2_SCL	DO	External sensor I2C2 clock	
325	TS_I2C_SDA	DI/DO	Touch screen I2C data signal	Dedicated to touch screen
328	TS_I2C_SCL	DO	Touch screen I2C clock signal	
71	CCI_I2C_SDA2	DI/DO	CAM2 I2C data	Dedicated to Camera
70	CCI_I2C_SCL2	DO	CAM2 I2C clock	
401	CCI_I2C_SDA1	DI/DO	CAM1 I2C data	
402	CCI_I2C_SCL1	DO	CAM1 I2C clock	
33	CCI_I2C_SDA0	DI/DO	CAM0 I2C data	
36	CCI_I2C_SCL0	DO	CAM0 I2C clock	

When I2C has more than one peripheral, ensure the uniqueness of every peripheral address. If one of the peripherals has high requirement for timeliness, do not set the peripherals to share one set of I2C interfaces.

4.7 SD

The module supports one set of SD card interface. Please refer to the pin description section for pin definition.

The SD card reference circuit is designed as follows:

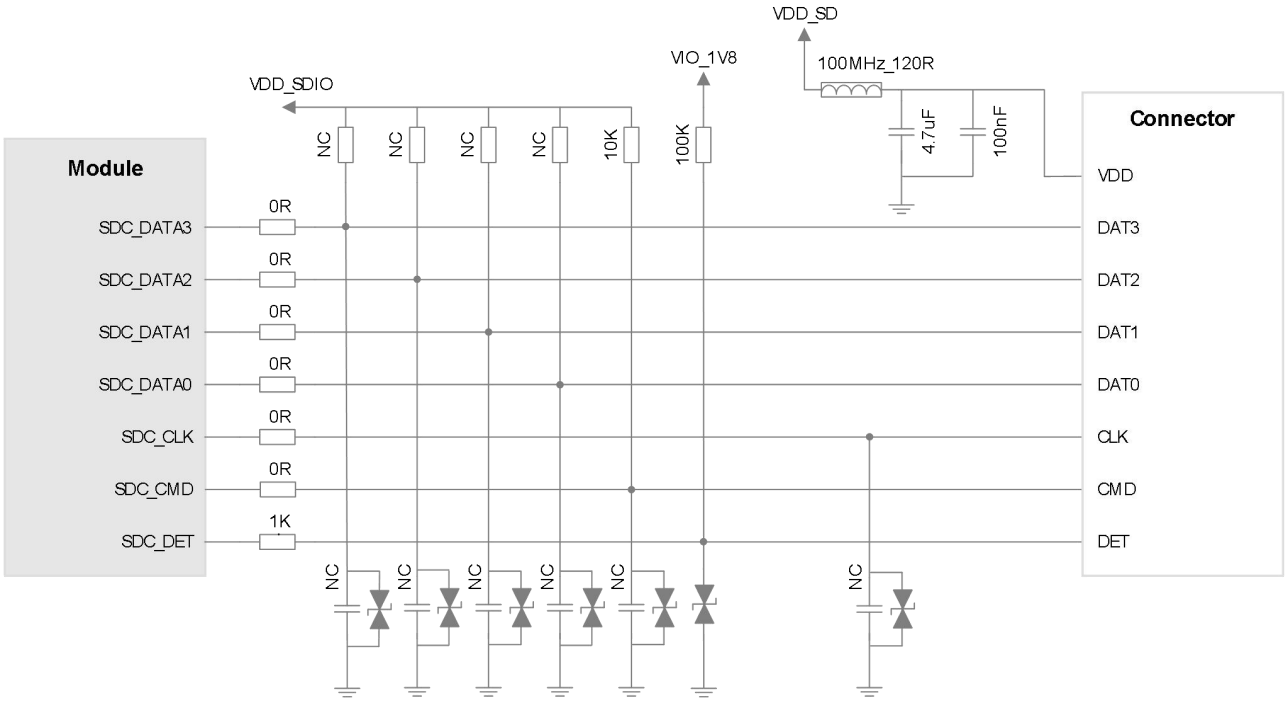


Figure 14. SD card reference circuit

EMC and ESD protection should be considered in the design of SDIO circuit, and the anti-interference ability should be improved to ensure the stable operation of SD card. The following rules should be strictly followed in the design:

- The length of the SDIO trace is ≤ 50 mm and the length difference between the clock signal and data signal traces is ≤ 2 mm.
- The SDIO signal line must be three-dimensionally grounded and kept away from RF antenna, DCDC power supply, clock signal line and other strong interference sources.
- The SDIO signals should have a complete reference ground and the impedance of the data lines should be controlled at 50Ω (±10%).
- The total capacitance of the load on the SDIO signal lines should be less than 1pF.

- VDD_SD is the peripheral driver power of the SD card and can provide about 600mA current. Pay attention to controlling the line width is greater than 0.6 mm.

- Use VREG_L21B_1P8 power supply for SD_DET pull-up.
- SD is a high-speed digital signal line, which needs to be shielded.
- The length of the clock and signal lines of SD card shall not exceed 50 mm. The TVS tube shall be selected with a parasitic capacitance less than 0.5pF.

4.8 (U)SIM

The module has two sets of (U)SIM interfaces, supports dual card dual standby, and supports hot plug. Please refer to pin description section for pin definition.

The (U)SIM reference circuit is designed as follows:

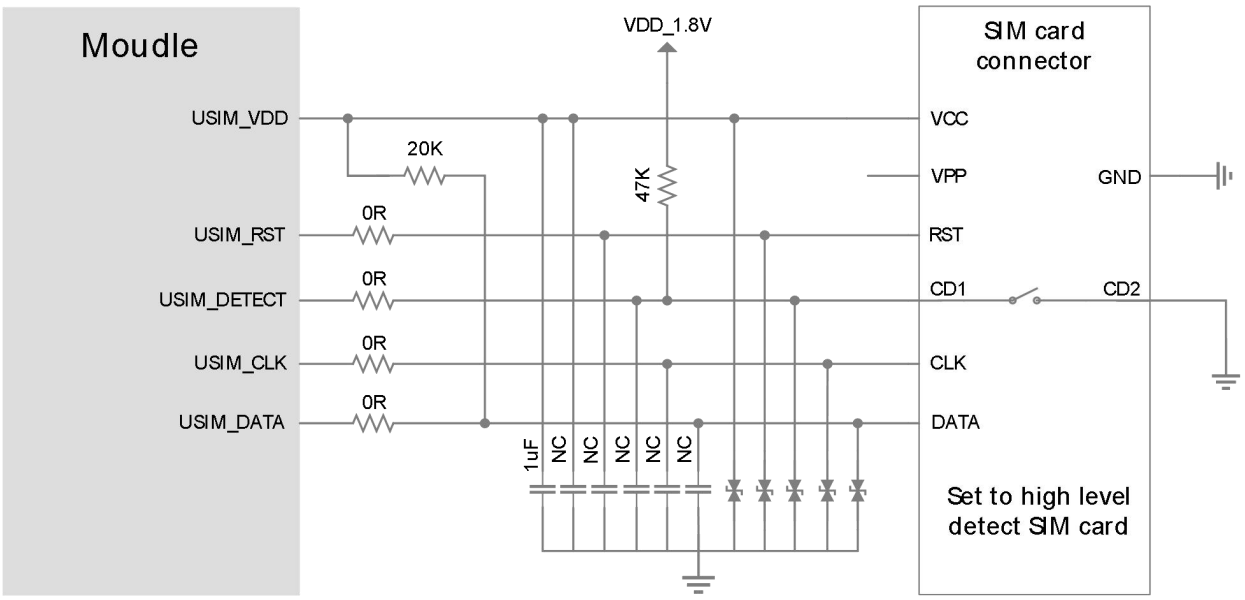


Figure 15. (U)SIM reference schematic

4.9 GPIO

The module has rich GPIO resources and the power domain is 1.8V. The pin definition is as follows:

Table 35. GPIO list

Pin No.	Pin Name	I/O	Function Description	Wake-up	Note

Pin No.	Pin Name	I/O	Function Description	Wake-up	Note
110	GPIO_34	PD:nppukp	Configurable I/O	YES	- -
111	GPIO_99	PD:nppukp	Configurable I/O	YES	BOOT_CONFIG
43	GPIO_95	PD:nppukp	Configurable I/O	YES	- -
198	GPIO_81	PD:nppukp	Configurable I/O	YES	BOOT_CONFIG
123	GPIO_108	PD:nppukp	Configurable I/O	YES	- -
51	GPIO_123	PD:nppukp	Configurable I/O	NO	- -
178	GPIO_98	PD:nppukp	Configurable I/O	YES	- -
210	GPIO_51	PD:nppukp	Configurable I/O	NO	- -
203	GPIO_73	PD:nppukp	Configurable I/O	YES	- -
94	GPIO_33	PD:nppukp	Configurable I/O	YES	BOOT_CONFIG
119	GPIO_127	PD:nppukp	Configurable I/O	NO	- -
19	GPIO_78	PD:nppukp	Configurable I/O	NO	BOOT_CONFIG
155	GPIO_82	PD:nppukp	Configurable I/O	NO	- -
191	GPIO_74	PD:nppukp	Configurable I/O	NO	BOOT_CONFIG
122	GPIO_91	PD:nppukp	Configurable I/O	YES	- -
167	GPIO_97	PD:nppukp	Configurable I/O	YES	- -
183	GPIO_50	PD:nppukp	Configurable I/O	YES	- -
187	GPIO_100	PD:nppukp	Configurable I/O	NO	BOOT_CONFIG
207	GPIO_84	PD:nppukp	Configurable I/O	YES	- -
310	GPIO_83	PD:nppukp	Configurable I/O	YES	- -
318	GPIO_90	PD:nppukp	Configurable I/O	NO	- -
322	GPIO_126	PD:nppukp	Configurable I/O	NO	- -
326	GPIO_105	PD:nppukp	Configurable I/O	YES	- -

Pin No.	Pin Name	I/O	Function Description	Wake-up	Note
147	GPIO_102	PD:nppukp	Configurable I/O	YES	- -

- The GPIO of BOOT_CONFIG can not be pulled up externally, otherwise it may cause no boot.
- All GPIOs do not allow level status changes during system startup.

Table 36. Parameter description

Parameter	Description
B	Bidirectional digital with CMOS input
NP	pdpukp = default no-pull with programmable options following the colon (:)
PD	nppukp = default pull-down with programmable options following the colon (:)
PU	nppdkp = default pull-up with programmable options following the colon (:)
KP:	nppdpu = default keeper with programmable options following the colon (:)

4.10 ADC

The module has two universal ADC interfaces, and the maximum voltage input is 1.8V. Please refer to the pin description section for pin definition.

4.11 Battery

The module supports switch-mode lithium battery charging and is compatible with QC2.0 and QC3.0 protocols. The maximum charging current can reach 2A. When charging, heat dissipation design can be carried out according to the heating situation of the whole machine.

Table 37. Battery interface definition

Pin No.	Pin Name	I/O	Description	Note
418	BAT_P	AI	Battery voltage detection	Connect to the positive end of the battery and cannot be left

Pin No.	Pin Name	I/O	Description	Note
			input (+)	unconnected
419	BAT_M	AI	Battery voltage detection input (-)	Connect to the negative end of the battery and cannot be left unconnected
407	BAT_THERM	AI	Battery temperature detection	Connect 10K to GND when not used
410	BAT_ID	AI	Battery type detection	Unconnected when not in use

The default configuration of module temperature detection resistor is 10K. Software adaptation is required for other types of batteries. The battery reference circuit is designed as follows:

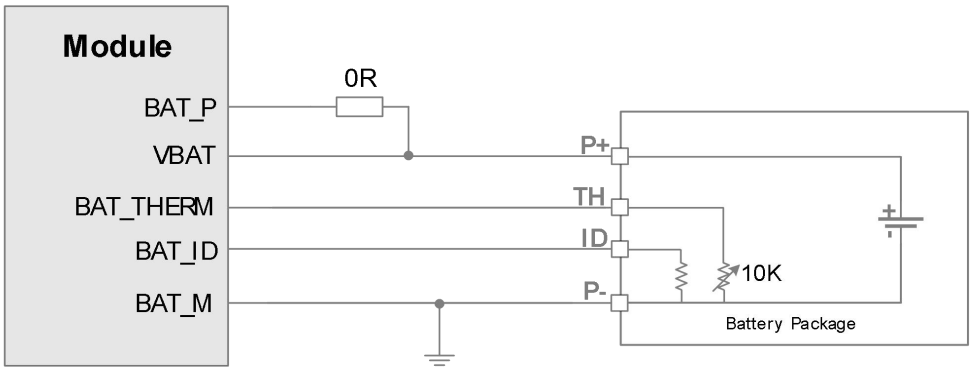


Figure 16. Reference schematic of battery circuit

4.12 LCD

The screen interface is based on the MIPI_DSI standard and supports one group of 4-Lane high-speed differential data transmission with a maximum FHD+ resolution. Please refer to the pin description section for pin definition.

The LCD reference design is shown in the following figure.

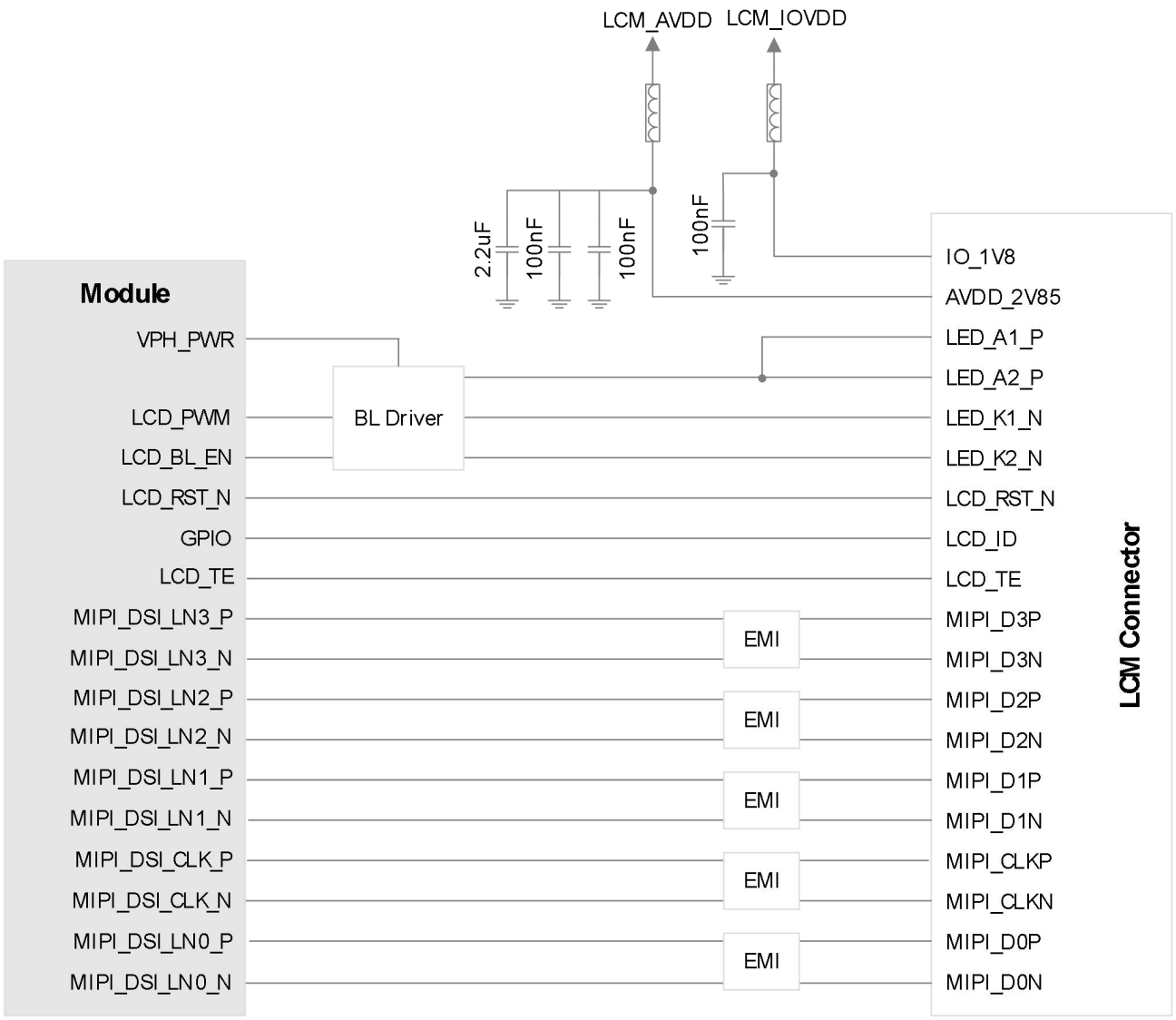


Figure 17. Reference schematic of LCD interface circuit

Precautions for LCD design are as follows:

- It is recommended to connect the common mode inductor in series near the LCD connector to reduce EMI.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance ±10%.
- The length difference of the differential line within the group is controlled within 0.7 mm, and the length difference between the groups is controlled within 2.1 mm.
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 1.5 times of the route

width.

4.13 Touch Panel

The TP circuit reference design is shown as follows:

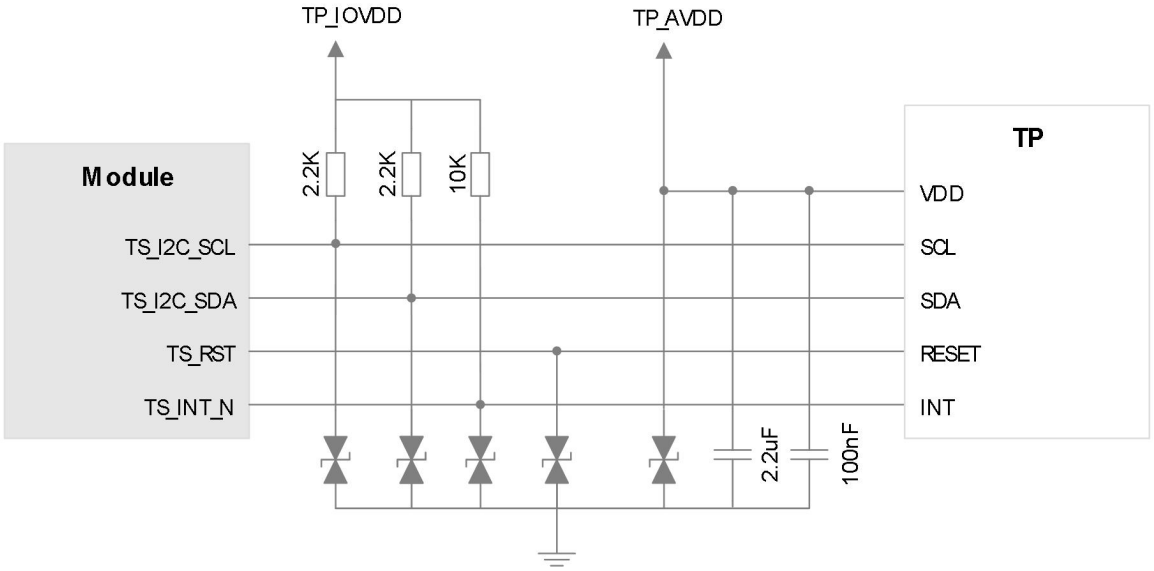


Figure 18. Reference schematic of TP circuit

4.14 Camera

The camera interface of the module is based on the MIPI_CSI standard and can support three (4 lane +4 lane +4 lane) camera combinations. Please refer to the pin description section for pin definition.

The camera circuit reference design is shown in the following figure.

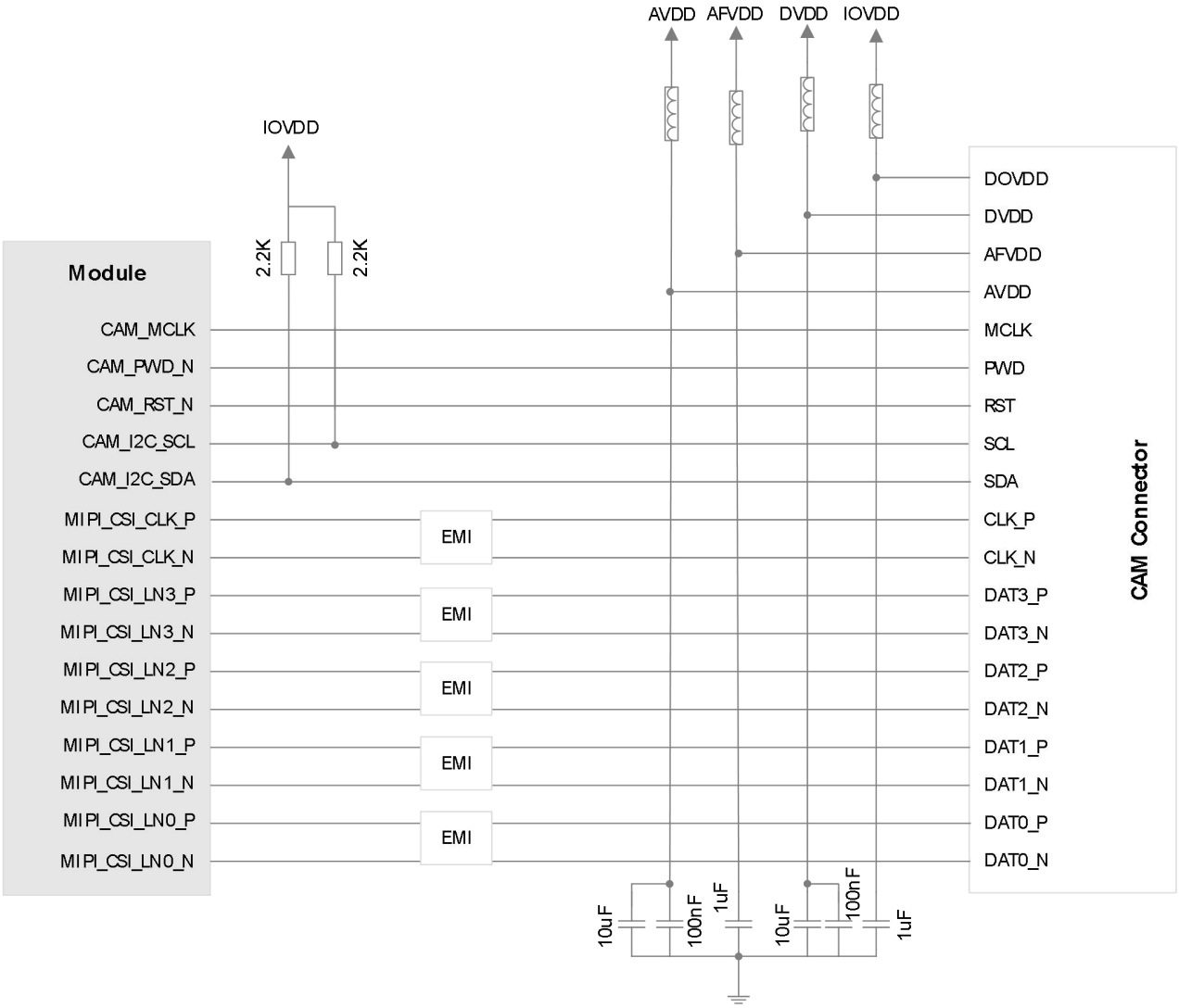


Figure 19. Reference schematic of camera circuit

Design Guidelines of Camera

MIPI_CSI is a high-speed signal. Pay attention to the following points during PCB layout:

- It is recommended to connect a common-mode inductor in series on the MIPI high-speed signal line near the camera connector end to reduce EMI.
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance ±10%.
- The length difference of differential lines in MIPI signal line groups shall be controlled within 0.7 mm,

and the length difference between groups shall be controlled within 2.1 mm.

- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 1.5 times of the route width.

Precautions for design of other signal lines:

- CAM_MCLK is a high-speed clock signal and requires three-dimensional grounding.
- AVDD and DVDD of camera power supply shall be routed away from interference sources to avoid introducing power supply noise. It is recommended to add LDO with high power supply noise rejection ratio.
- If the cameras are to share I2C, select two cameras that do not work at the same time, and make sure that the two cameras have different addresses.

4.15 Audio

4.15.1 Analog Audio Interface

The module supports three analog input interfaces and three analog output interfaces. Please refer to the pin description section for pin definition.

The reference design of MEMS type microphone differential input is as follows:

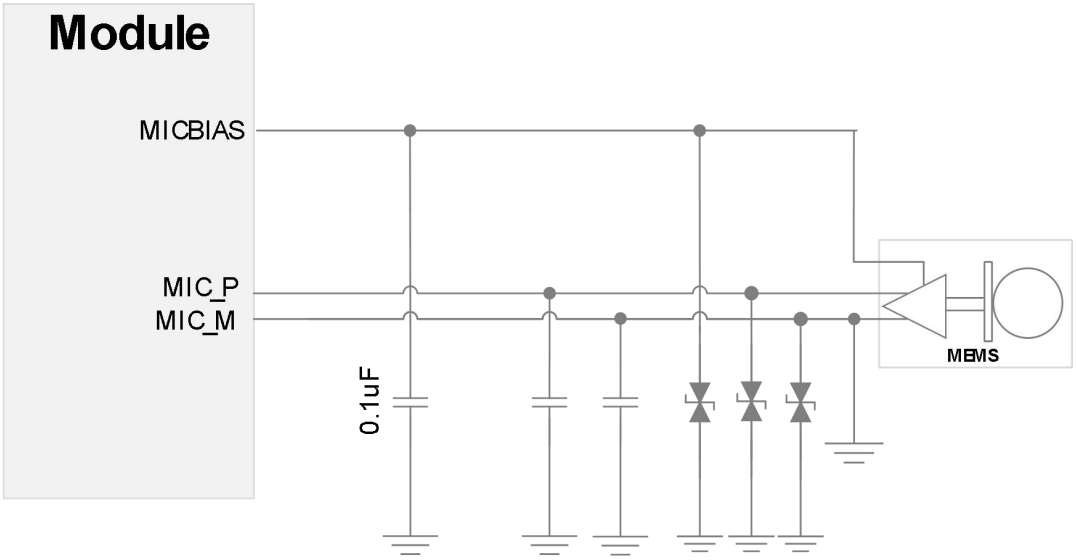


Figure 20. Reference schematic of MIC circuit

The reference design of the earphone is as follows:

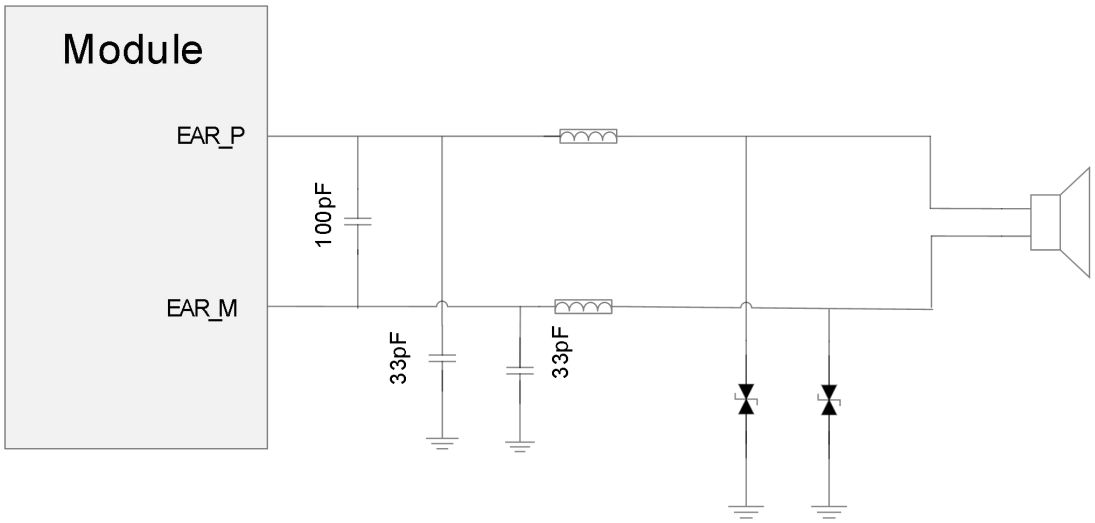


Figure 21. Reference schematic of receiver circuit

The reference circuit of speaker is as follows:

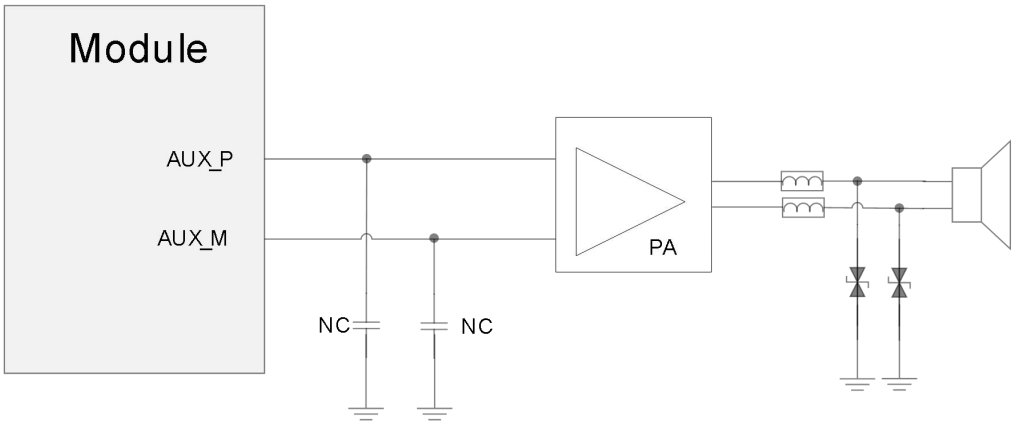


Figure 22. Reference schematic of speaker circuit

The reference design of the headphone is as follows:

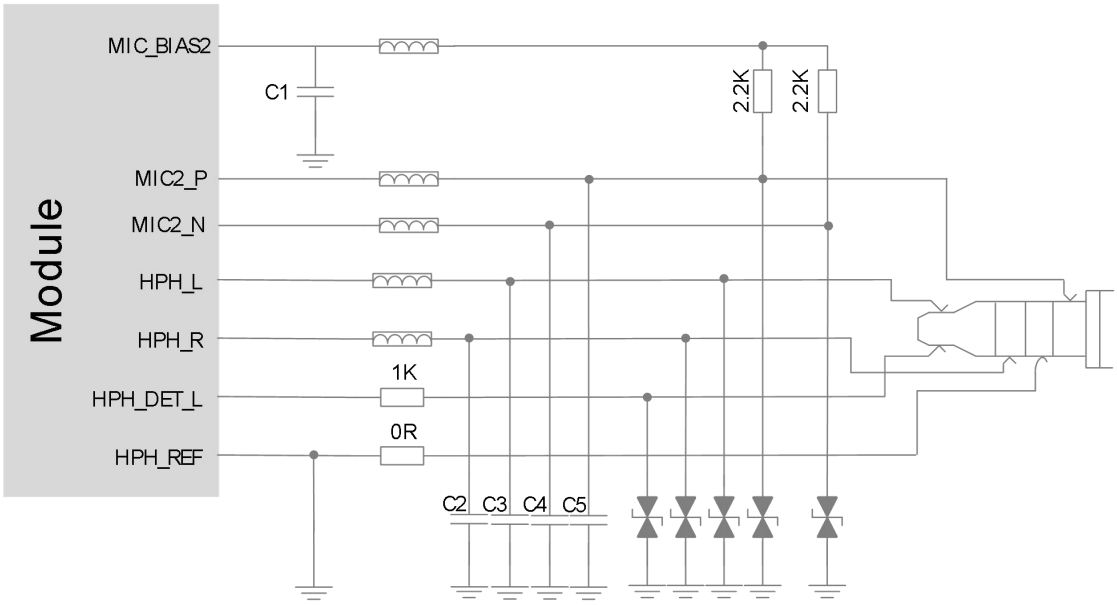


Figure 23. Reference schematic of headphone circuit

Design guidelines of audio interface:

- Add pull-up resistance to corresponding MIC BIAS of the three groups of MICs;
- A set of Class-AB differential AUX PA output cannot directly drive the speaker, and audio power amplifier is required when in use;
- Both the receiver and AUX PA output are of differential type and must follow the differential routing

principles;

- Keep audio routes away from radiation and interference sources, such as antennas or power supplies.

4.15.2 LPI_I2S

The module has one set of LPI_I2S interfaces, which is used to connect external audio Codec. Please refer to the pin description section for pin definition.

4.16 Motor Interfaces

The module has a motor drive interface and only supports ERM motors. Please refer to the pin description section for pin definition.

The following figure shows the reference circuit of motor interface.

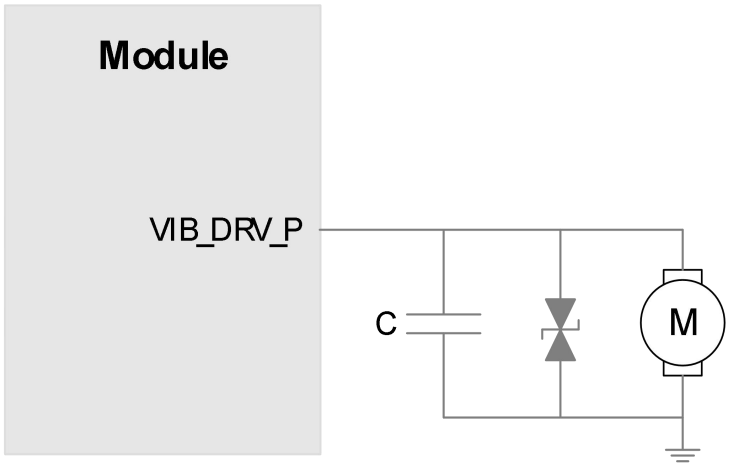


Figure 24. Reference schematic of motor circuit

5 Antenna Interfaces

5.1 Definition of Antenna Interfaces

Table 38. Definition of antenna interfaces for SC151-CN

Pin No.	Pin Name	Function Description	TX	RX	Frequency Range
211	ANT0	Antenna 0 interface 5GNR （N1/N3/N5/N8/ N28A TRX, N41/ N78/ N79 TRX1）& LTE LMHB TRX	WCDMA: B1/B8 LTE: B1/B3/B5/B8/B34/B38/B39/B40/B41 NR: N1/N3/N5/N8/N28A/ N78/N79/N41	WCDMA: B1/B8 LTE: B1/B3/B5/B8/B34/B38/B39/B40/B41 NR: N1/N3/N5/N8/N28A/ N78/N79/N41	700MHz-5GHz
244	ANT1	Antenna 1 interface 5GNR (N1/ N41/ N78/ N79 DRX MIMO) & LTE(B1/B41 DRX MIMO)	- -	LTE: B1/B41 NR: N1/N41/N78/N79	1900MHz-5GHz
256	ANT2	Antenna 2 interface 5GNR (N1 PRX MIMO, N41/ N78/ N79 TRx0) &LTE(B1/B41 PRX MIMO)	NR: N41/N78/N79	LTE: B1/B41 NR: N1/N41/N78/N79	1900MHz-5GHz
292	ANT3	Antenna 3 interface 5GNR (N1/ N3/N5/N8/N28A/ N41/ N78/ N79 DRX) LTE(LB/MB/HB DRX)	- -	WCDMA: B1/B8 LTE: B1/ B3/ B5/ B8/ B34/ B38/ B39/ B40/ B41 NR: N1/ N28A/ N78/ N79/ N41	700MHz-5GHz
302	ANT_GNSS	GNSS antenna interface	- -	L1/L5	- -
92	ANT_WIFI/BT	WI-FI/BT antenna interface	2.4G/5G/BT	2.4G/5G/BT	- -

86	ANT_WIFI_MIMO	WI-FI MIMO antenna interface	2.4G/5G	2.4G/5G	- -

Table 38. Definition of antenna interfaces for SC151-GL

Pin No.	Pin Name	Function Description	TX	RX	Frequency Range
211	ANT0	Antenna 0 interface, LTE/NR LB TRX MHB B1/B3/B41/32 TX/PRX MHB B7/40/30/7 PRXMIMO UHB PRXMIMO UHB SRS	WCDMA: B1/5/6/8/19 LTE: B1/3(TX1)/5/8/12/13/14/17/18/19/20/26/28/38/41/71 NR: N1/3(TX1)/5/8/12/14/20/28/38/41/71/ SRS: N77/78	WCDMA: B1/5/6/8/19（Primary Rx) LTE: PRX:B1/5/8/12/13/14/17/18/19/20/26/28/ 38/41/71 PRX MIMO: B2/3/4/7/25/30/40/66 NR: PRX: N1/5/8/12/14/20/28/38/41/71 PRX MIMO: N2/3/4/7/25/30/40/66/77/78	617MHz-4.2GHz
244	ANT1	Antenna 1 interface, MHB DRX MIMO UHB DRX MIMO UHB SRS	SRS: N77/78	LTE: DRX MIMO: B1/2/3/4/7/25/30/38/40/41/66 NR: DRX MIMO: N1/2/3/4/7/25/30/38/40/41/66/77/78	1710MHz-4.2GHz
256	ANT2	Antenna 2 interface, MHB B1/B3/B41/32 PRX MIMO MHB B7/40/30/7 TX/PRX UHB TX/PRX	LTE：2/3(TX0)/4/7/25/30/40/42/43/48/66 NR: 2/3(TX0)/7/25/30/40/48/66/77/78 WCDMA: 2/4/9	LTE: PRX: 2/3/4/7/25/30/40/42/43/48/66 PRX MIMO: 1/38/41 NR: PRX:2/3/7/25/30/40/48/66/77/78 PRX MIMO: 1/38/41 WCDMA: 2/4/9 (Primary Rx）	1710MHz-4.2GHz
292	ANT3	Antenna 3 interface, LTE/NR LB DRX MHB DRX UHB DRX UHB SRS	SRS: N77/78	LTE: DRX: 1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/32/38/40/41/42/43/48/66/71 NR: DRX: 1/2/3/5/7/8/12/14/20/25/28/30/38/40/41/48	617MHz-4.2GHz

				/66/71/77/78 WCDMA: 1/2/4/5/6/8/9/19 （Diversity Rx）	
302	ANT_GNSS	Antenna GNSS interface	- -	L1/L5	- -
92	ANT_WIFI/BT	Antenna WIFI/BT interface	2.4G/5G/6G/BT	2.4G/5G/6G/BT	- -
86	ANT_WIFI_MIMO	Antenna WIFI MIMO interface	2.4G/5G/6G	2.4G/5G/6G	- -

5.2 Operating Frequency

5.2.1 Cellular

Tables 39. Reference table of cellular frequency for SC151-CN

Mode	Band	TX（MHz）	RX（MHz）
WCDMA	Band 1	1920-1980	2110-2170
	Band 8	880-915	925-960
LTE FDD	Band 1	1920-1980	2110-2170
	Band 3	1710-1785	1805-1880
	Band 5	824-849	869-894
	Band 8	880-915	925-960
LTE TDD	Band 34	2010-2025	2010-2025
	Band 38	2570-2620	2570-2620
	Band 39	1880-1920	1880-1920
	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690
NR FDD	n1	1920-1980	2110-2170
	n3	1710-1785	1805-1880

Mode	Band	TX（MHz）	RX（MHz）
	n5	824-849	869-894
	n8	880-915	925-960
	n28A	703-733	758-788
NR TDD	n41	2496-2690	2496-2690
	n78	3300-3800	3300-3800
	n79	4400-5000	4400-5000

Tables 40. Reference table of cellular frequency for SC151-GL

Mode	Band	TX（MHz）	RX（MHz）
WCDMA	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 6	830-840	875-885
	Band 8	880-915	925-960
	Band 9	1749.9-1784.9	1844.9-1879.9
	Band 19	830-845	875-890
LTE FDD	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690

Mode	Band	TX（MHz）	RX（MHz）
	Band 8	880-915	925-960
	Band 12	699-715.9	729-745.9
	Band 13	777-786.9	746-755.9
	Band 14	788-798	758-768
	Band 17	704-715.9	734-745.9
	Band 18	815-830	860-875
	Band 19	830-845	875-890
	Band 20	832-862	791-821
	Band 25	1850-1915	1930-1995
	Band 26	814-849	859-894
	Band 28	703-748	758-803
	Band 30	2305-2315	2350-2360
	Band 66	1710-1780	2110-2200
	Band 71	663-698	617-652
LTE TDD	Band 38	2570-2620	2570-2620
	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690
	Band 42	3400-3600	3400-3600
	Band 43	3600-3800	3600-3800
	Band 48	3550-3700	3550-3700
NR FDD	n1	1920-1980	2110-2170
	n2	1850-1910	1930-1990
	n3	1710-1785	1805-1880

Mode	Band	TX（MHz）	RX（MHz）
	n5	824-849	869-894
	n7	2500-2570	2620-2690
	n8	880-915	925-960
	n12	699-715.9	729-745.9
	n14	788-798	758-768
	n20	832-862	791-821
	n25	1850-1915	1930-1995
	n28	703-748	758-803
	n30	2305-2315	2350-2360
	n66	1710-1780	2110-2200
	n71	663-698	617-652
NR TDD	n38	2570-2620	2570-2620
	n40	2300-2400	2300-2400
	n41	2496-2690	2496-2690
	n48	3550-3700	3550-3700
	n77	3300-4200	3300-4200
	n78	3300-3800	3300-3800

5.2.2 WIFI

The module supports 2.4G/5G/6G(SC151-GL) WLAN wireless communication, and supports 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac and 802.11ax. The maximum throughput is 3600Mbps (2 x 2 + 2 x 2 11ax DBS) with the following characteristics:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode

- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- 2.4G band supports CCK, OFDM, HT20,HT40,HT40-,HT40+,VHT20 and VHT40, HE20 and HE40
- 5G band supports OFDM, HT20,HT40,HT40-,HT40+,VHT20, VHT40, VHT80, VHT160, HE20, HE40, HE80 and HE160
- 6G (SC151-GL) band supports OFDM, HE20, HE40, HE80 and HE160
- Test condition: 3.8V power supply, environment temperature of 25°C

Table 41. WIFI transmitting power for sc151-cn

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	18±3
		11Mbps	20	18±3
	802.11g	6Mbps	20	17±3
		54Mbps	20	15±3
	802.11n	MCS0	20	17±3
		MCS7	20	15±3
		MCS0	40	17±3
		MCS7	40	15±3
	802.11ax	MCS0	20	17±3
		MCS11	20	10±3
		MCS0	40	17±3
		MCS11	40	10±3
5G	802.11a	6Mbps	20	17±3

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
		54Mbps	20	15±3
	802.11n	MCS0	20	17±3
		MCS7	20	15±3
		MCS0	40	17±3
		MCS7	40	15±3
	802.11ac	MCS0	20	17±3
		MCS8	20	15±3
		MCS0	40	17±3
		MCS9	40	14±3
		MCS0	80	17±3
		MCS9	80	13±3
		MCS0	160	17±3
		MCS9	160	10±3
	802.11ax	MCS0	20	15±3
		MCS11	20	12±3
		MCS0	40	17±3
		MCS11	40	12±3
		MCS0	80	17±3
		MCS11	80	12±3
		MCS0	160	17±3
		MCS11	160	10±3

Table 41. WIFI transmitting power for sc151-gl

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	18±3
		11Mbps	20	18±3
	802.11g	6Mbps	20	17±3
		54Mbps	20	15±3
	802.11n	MCS0	20	17±3
		MCS7	20	15±3
		MCS0	40	17±3
		MCS7	40	15±3
	802.11ax	MCS0	20	17±3
		MCS11	20	10±3
		MCS0	40	17±3
		MCS11	40	10±3
5G	802.11a	6Mbps	20	17±3
		54Mbps	20	15±3
	802.11n	MCS0	20	17±3
		MCS7	20	15±3
		MCS0	40	17±3
		MCS7	40	15±3
	802.11ac	MCS0	20	17±3
		MCS8	20	15±3
		MCS0	40	17±3
		MCS9	40	14±3
		MCS0	80	17±3
		MCS9	80	13±3
		MCS0	160	17±3
		MCS9	160	10±3

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
	802.11ax	MCS0	20	15±3
		MCS11	20	12±3
		MCS0	40	17±3
		MCS11	40	12±3
		MCS0	80	17±3
		MCS11	80	12±3
		MCS0	160	17±3
		MCS11	160	10±3
6G	802.11a	6Mbps	20	TBD
		54Mbps	20	TBD
	802.11ax	MCS0	20	TBD
		MCS11	20	TBD
		MCS0	40	TBD
		MCS11	40	TBD
		MCS0	80	TBD
		MCS11	80	TBD
		MCS0	160	TBD
		MCS11	160	TBD

Table 42. WIFI receiving sensitivity for sc151-cn

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-89
		11Mbps	20	-89
	802.11g	6Mbps	20	-89
		54Mbps	20	-71
	802.11n	MCS0	20	-89

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
		MCS7	20	-71
		MCS0	40	-85
		MCS7	40	-69
	802.11ax	MCS0	20	-89
		MCS11	20	-62
		MCS0	40	-86
		MCS11	40	-59
5G	802.11a	6Mbps	20	-90
		54Mbps	20	-72
	802.11n	MCS0	20	-90
		MCS7	20	-71
		MCS0	40	-87
		MCS7	40	-68
	802.11ac	MCS0	20	-90
		MCS8	20	-69
		MCS0	40	-88
		MCS9	40	-64
		MCS0	80	-87
		MCS9	80	-61
	802.11ax	MCS0	20	-90
		MCS11	20	-62
		MCS0	40	-88
		MCS11	40	-60

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
		MCS0	80	-85
		MCS11	80	-54
		MCS0	160	-82
		MCS11	160	-52

Table 42. WIFI receiving sensitivity for sc151-gl

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-89
		11Mbps	20	-89
	802.11g	6Mbps	20	-89
		54Mbps	20	-71
	802.11n	MCS0	20	-89
		MCS7	20	-71
		MCS0	40	-85
		MCS7	40	-69
	802.11ax	MCS0	20	-89
		MCS11	20	-62
		MCS0	40	-86
		MCS11	40	-59
5G	802.11a	6Mbps	20	-90
		54Mbps	20	-72
	802.11n	MCS0	20	-90
		MCS7	20	-71
		MCS0	40	-87
		MCS7	40	-68
	802.11ac	MCS0	20	-90

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
		MCS8	20	-69
		MCS0	40	-88
		MCS9	40	-64
		MCS0	80	-87
		MCS9	80	-61
	802.11ax	MCS0	20	-90
		MCS11	20	-62
		MCS0	40	-88
		MCS11	40	-60
		MCS0	80	-85
		MCS11	80	-54
		MCS0	160	-82
		MCS11	160	-52
6G	802.11a	6Mbps	20	TBD
		54Mbps	20	TBD
	802.11ax	MCS0	20	TBD
		MCS11	20	TBD
		MCS0	40	TBD
		MCS11	40	TBD
		MCS0	80	TBD
		MCS11	80	TBD
		MCS0	160	TBD
		MCS11	160	TBD

Microstrip line is recommended for RF routing of WIFI antenna. The insertion loss of 2.4G band is controlled within 0.2dB, the insertion loss of 5G band is controlled within 0.8dB, and the impedance is controlled within 50Ω.

Table 43. WIFI operating frequency

Mode	Frequency	Unit
2.4G	2402 to 2482	MHz
5G	5170 to 5835	MHz
6G	5925 to 7125	MHz

5.2.3 Bluetooth

The module supports BT5.2 (BR/EDR+BLE) standard. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK. The BR/EDR channel bandwidth is 1MHz and can accommodate 79 channels. The BLE can accommodate 40 channels. Its main features are as follows:

- BT 4.2+BR/EDR+BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 44. BT rate and version information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	- -
BT2.0+EDR	3Mbit/s	> 80Kbit/s	- -
BT3.0+HS	24Mbit/s	Refer to 3.0+HS	- -
BT4.2 LE	24Mbit/s	Refer to 4.2 LE	- -
BT5.2	48Mbit/s	Refer to 5.2 LE	- -

Test condition: 3.8V power supply, environment temperature of 25°C

Table 45. BT performance indicator

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitter	16±2.5	14±2.5	14±2.5	8±2.5	dBm
Sensitivity	-80	-80	-75	-89	dBm

The sensitivity here is a typical value. Microstrip line is recommended for the RF routing of Bluetooth antenna, with insertion loss within 0.2dB and impedance at 50Ω.

Table 46. BT operating frequency

Mode	Frequency	Unit
Bluetooth	2402 to 2480	MHz

5.2.4 GNSS

The module supports multiple positioning systems including GPS /Beidou/GLONASS/Galileo/QZSS. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS. LNA is embedded in the module, which can effectively improve the sensitivity of GNSS. Test condition: 3.8V power supply, environment temperature of 25°C

Table 47. GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-157	dBm
C/N	-130dBm	38.5	dB-Hz
TTFF	Cold Start	45	s
	Warm Start	42	s
	Hot Start	3	s
CEP	Static accuracy (95% @-	5	m

Parameter	Description	Typical Result	Unit
	130dBm)		

Table 48. GNSS operating frequency

Mode	Frequency	Unit
GPS	L1: 1575.42±1.023 L5: 1176.45±5.11	MHz
GLONASS	1597.5-1605.9	MHz
BeiDou	1561.098±2.046	MHz
Galileo	E1: 1575.42±2.02	MHz
QZSS	L1: 1575.42±1.023	MHz

5.3 Antenna Design Circuit

The following figure shows an antenna circuit for a cellular network:

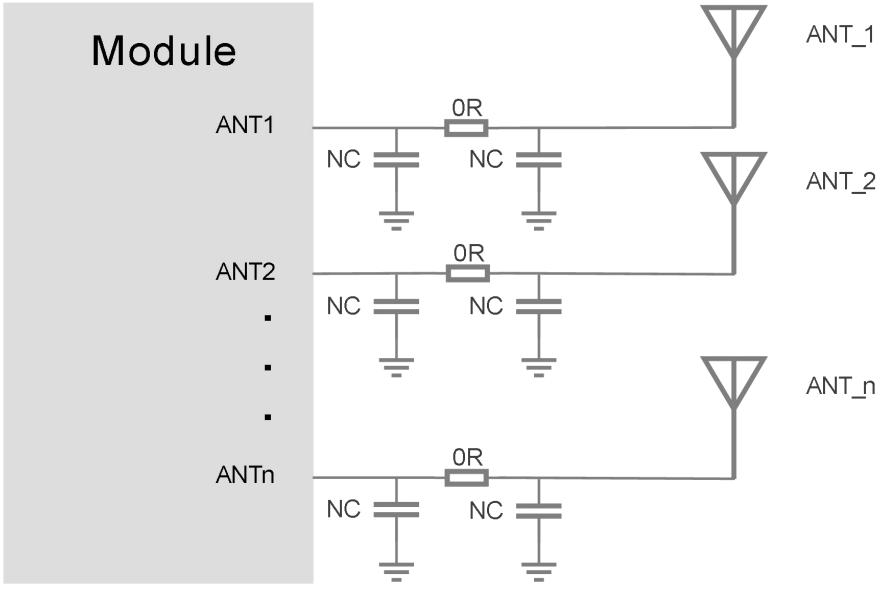


Figure 25. Reference circuit of cellular network antenna

The module has a built-in LNA. The passive antenna is used in the design of the device. Microstrip line is recommended for the GNSS RF routing, with insertion loss within 0.2dB and impedance at 50Ω.

The power supply of the active antenna is fed from the signal line of the antenna through the 56nH inductor. The common active antenna is powered by 3.3V to 5.0V. The power consumption of the active antenna is very small, but the power supply is required to be stable and clean. It is recommended to use LDO with high performance to supply power to the antenna. The active antenna gain is required to be less than 17dB. If the gain is greater than 17dB, the reserved π-type matching needs to be used to increase the attenuation network.

The following figures show the reference circuits of GNSS antenna.

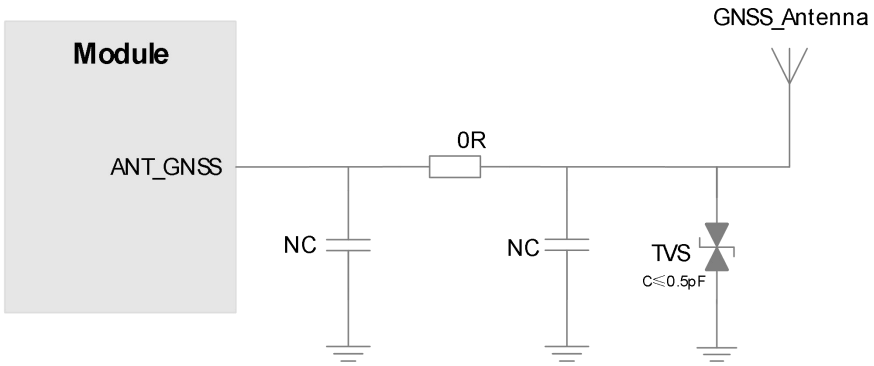


Figure 26. Reference circuit of GNSS passive antenna

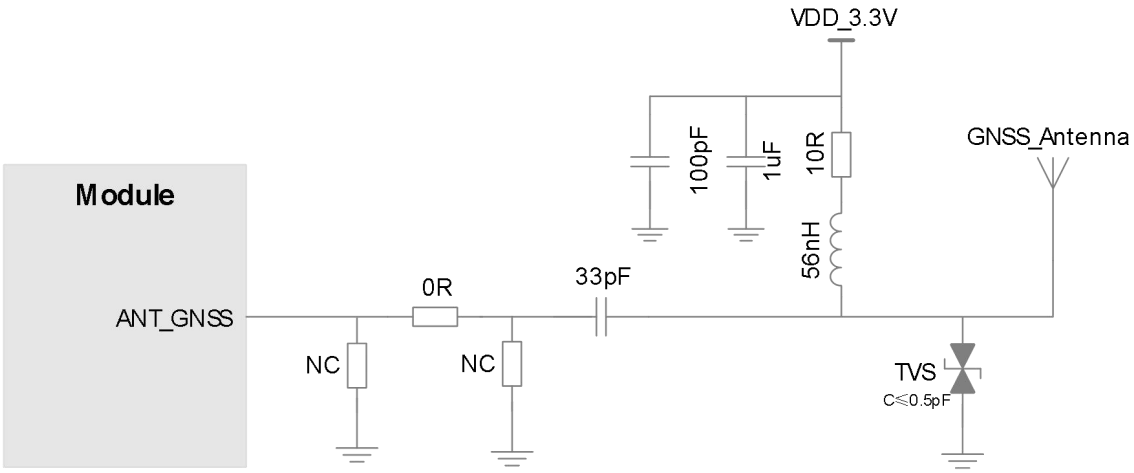


Figure 27. Reference circuit of GNSS active antenna

5.4 Antenna Performance Requirements

Table 49. Antenna performance requirements

Standard	Antenna Performance Requirement
WCDMA/LTE/NR	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB (0.617GHz to 1GHz) Insertion loss: < 1.5dB (1.4GHz to 2.2GHz) Insertion loss: < 2dB (2.3GHz to 5GHz)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 2dB
GNSS	Frequency range: 1559MHz to 1607MHz 1166.22MHz to 1186.68MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical value) Passive antenna gain: > 0dBi Active antenna NF: < 1.5dB (typical value) Active antenna gain: > -2dBi
Isolation between GPS and MAIN antennas:	> 20dB
Isolation between WIFI and MAIN antennas:	> 20dB

5.5 PCB Layout Reference Design

In practical applications, the shorter the RF microstrip trace, the better. Impedance is usually closely related to the width (W) and thickness of the trace, the height (H) of the reference layer, the spacing (S) between the trace and the left and right sides of the ground, and the dielectric constant of the material. The impedance control model of RF microstrip line is divided into planar reference model and coplanar impedance model. Generally, if the planar reference model can meet the requirements, the coplanar impedance model should not be used.

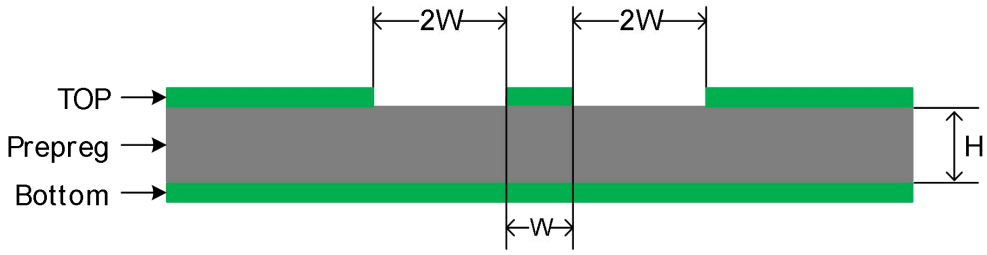


Figure 28. Planar reference model for a two-layer board

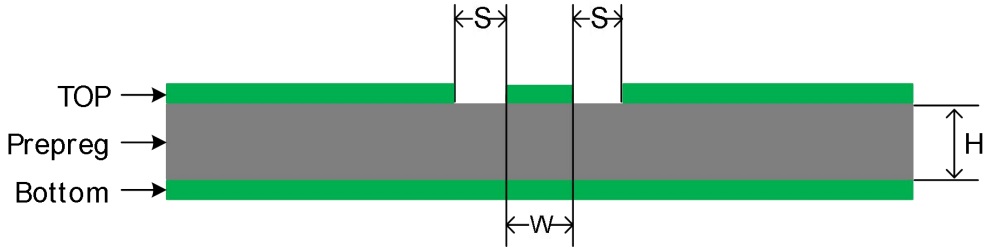


Figure 29. Coplanar impedance model for a two-layer board

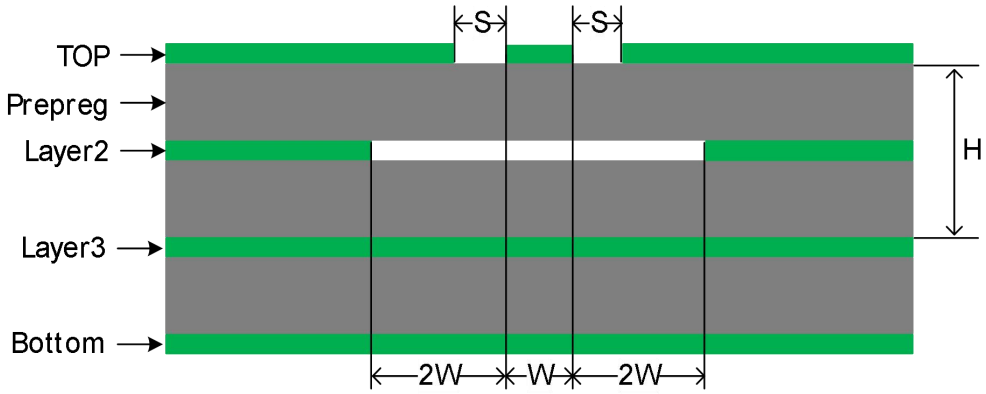


Figure 30. Coplanar impedance model for a four-layer board

The design rules are as follows:

- The RF trace impedance is controlled to 50Ω, and the reference ground must be kept intact.
- The RF routing should be curved as far as possible, and both sides of the routing should be protected by vias. The distance between vias and traces should be greater than 2 times the line width.
- There should be clearance below the RF connector, and the RF routing should be far away from the interference source to avoid crossing and paralleling with the interference source.

6 Electrical Features

6.1 Normal Operating Voltage

The following table shows the normal operating voltage range of the module, and all the performance indicators of the module are guaranteed within this operating voltage range.

Table 50. Operating voltage

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.4	V
USB_VBUS	3.7	5.0	12.6	V
VRTC	2.0	3.0	3.25	V

6.2 Absolute Maximum Voltage

The following table shows the absolute maximum rated parameters of the module, which can cause permanent damage to the device if it exceeds the absolute maximum parameter range.

Table 51. Absolute maximum parameters

Parameter	Min	Max	Unit
VBAT	-0.3	6	V
USB_IN	-0.3	15	V

6.3 Operating Temperature and Storage Temperature

Table 52. Operating temperature and storage temperature

Parameter	Min	Max	Unit
Operating ambient temperature	-30	75	°C
Storage temperature	-40	85	°C

6.4 Power Consumption

The power consumption measurement is closely related to the operating state of the module, and the test conditions are as follows:

The ambient temperature is 25°C and the power supply voltage is 3.8V.

Table 53. Operating current for SC151-CN

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Power on but not boot	320	uA
	Soft power-off leakage current	The module is powered on, and then powered off by AT commands or selecting an option from the pop-up box.	400	
I_{sleep}	Radio Off	Airplane mode standby status	4.5	mA
	WCDMA	DRX=8	10	
	LTE FDD	DPC (Default Paging Cycle)=#256	11	
	LTE TDD	DPC (Default Paging Cycle)=#256	11	
	NR FDD	Long DRX (ms10)	11	
	NR TDD	Long DRX (ms10)	11	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band 1 @ max power	800	mA
		Band 8 @ max power	750	
$I_{LTE-RMS}$	LTE FDD RMS Current	Band 1 @max power (10MHz,1RB)	850	mA
		Band 3 @max power (10MHz,1RB)	1100	
		Band 5 @max power (10MHz,1RB)	700	
		Band 8 @max power (10MHz,1RB)	720	
	LTE TDD	Band 34 @max power (10MHz,1RB)	380	

Parameter	Description	Condition	Typical Result	Unit
	RMS Current	Band 38 @max power (10MHz,1RB)	400	
		Band 39 @max power (10MHz,1RB)	350	
		Band 40 @max power (10MHz,1RB)	380	
		Band 41 @max power (10MHz,1RB)	450	
I_{NR-RMS}	NR FDD RMS Current	n1 @ max power (10M, SCS=15KHz)	950	mA
		n3 @ max power (10M, SCS=15KHz)	1050	
		n5 @ max power (10M, SCS=15KHz)	850	
		n8 @ max power (10M, SCS=15KHz)	860	
		n28A @ max power (10M, SCS=15KHz)	850	
	NR TDD RMS Current	n41 @ max power (100MHz,SCS=30KHz)	480	mA
		n78 @ max power (100MHz,SCS=30KHz)	480	
		n79 @ max power (100MHz,SCS=30KHz)	480	

Table 54. Operating current for SC151-GL

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Power on but not boot	320	uA
	Soft power-off leakage current	The module is powered on, and then powered off by AT commands or selecting an option from the pop-up box.	400	
I_{sleep}	Radio Off	Airplane mode standby status	4.5	mA
	WCDMA	DRX=8	TBD	
	LTE FDD	DPC (Default Paging Cycle)=#256	TBD	
	LTE TDD	DPC (Default Paging Cycle)=#256	TBD	

Parameter	Description	Condition	Typical Result	Unit
	NR FDD	Long DRX (ms10)	TBD	
	NR TDD	Long DRX (ms10)	TBD	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band 1 @ max power	800	mA
		Band 2 @ max power	750	
		Band 4 @ max power	TBD	
		Band 5 @ max power	760	
		Band 6 @ max power	700	
		Band 8 @ max power	750	
		Band 9 @ max power	700	
		Band 19 @ max power	720	
$I_{LTE-RMS}$	LTE FDD RMS Current	Band 1 @max power (10MHz,1RB)	770	mA
		Band 2 @max power (10MHz,1RB)	720	
		Band 3 @max power (10MHz,1RB)	730	
		Band 4 @max power (10MHz,1RB)	720	
		Band 5 @max power (10MHz,1RB)	670	
		Band 7 @max power (10MHz,1RB)	850	
		Band 8 @max power (10MHz,1RB)	810	
		Band 12 @max power (10MHz,1RB)	640	
		Band 13 @max power (10MHz,1RB)	530	
		Band 14 @max power (10MHz,1RB)	570	
		Band 17 @max power (10MHz,1RB)	550	
		Band 18 @max power (10MHz,1RB)	550	

Parameter	Description	Condition	Typical Result	Unit
		Band 19 @max power (10MHz,1RB)	550	
		Band 20 @max power (10MHz,1RB)	620	
		Band 25 @max power (10MHz,1RB)	630	
		Band 26 @max power(10MHz,1RB)	540	
		Band 28 @max power (10MHz,1RB)	640	
		Band 30 @max power (10MHz,1RB)	780	
		Band 66 @max power (10MHz,1RB)	740	
		Band 71 @max power (10MHz,1RB)	550	
	LTE TDD RMS Current	Band 38 @max power (10MHz,1RB)	400	
		Band 40 @max power (10MHz,1RB)	380	
		Band 41 @max power (10MHz,1RB)	400	
		Band 42 @max power (10MHz,1RB)	400	
		Band 43 @max power (10MHz,1RB)	400	
		Band 48 @max power (10MHz,1RB)	400	
$I_{NR-RMSn}$	NR FDD RMS Current	n1 @ max power (10M, SCS=15KHz)	TBD	mA
		n2 @ max power (10M, SCS=15KHz)	TBD	
		n3 @ max power (10M, SCS=15KHz)	TBD	
		n5 @ max power (10M, SCS=15KHz)	TBD	
		n7 @ max power (10M, SCS=15KHz)	TBD	
		n8 @ max power (10M, SCS=15KHz)	TBD	
		n12 @ max power (10M, SCS=15KHz)	TBD	
		n14 @ max power (10M, SCS=15KHz)	TBD	

Parameter	Description	Condition	Typical Result	Unit
		n20 @ max power (10M, SCS=15KHz)	TBD	
		n25 @ max power (10M, SCS=15KHz)	TBD	
		n28 @ max power (10M, SCS=15KHz)	TBD	
		n30 @ max power (10M, SCS=15KHz)	TBD	
		n66 @ max power (10M, SCS=15KHz)	TBD	
		n71 @ max power (10M, SCS=15KHz)	TBD	
	NR TDD RMS Current	n38 @ max power (100MHz,SCS=30KHz)	TBD	mA
		n40 @ max power (100MHz,SCS=30KHz)	TBD	
		n41 @ max power (100MHz,SCS=30KHz)	TBD	
		n48 @ max power (100MHz,SCS=30KHz)	TBD	
		n77 @ max power (100MHz,SCS=30KHz)	TBD	
		n78 @ max power (100MHz,SCS=30KHz)	TBD	

The above power consumption data is the test result of SC151-CN-00. On this basis, the power consumption of memory increases by 1mA for each additional specification.

6.5 Maximum Transmitting Power

The maximum transmitting power is the transmitting power measured at the antenna pin at an ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when designing, so as to avoid excessive insertion loss affecting TRP indicators. The maximum transmitting power of the module is as follows:

Test conditions: power supply voltage of 3.8V, ambient temperature of 25℃, LTE maximum power test 10M bandwidth 12RB, SA FDD maximum power test 10M bandwidth 12RB, and SA TDD maximum power test 20M bandwidth 12RB (N79 maximum power test 40M bandwidth 12RB)

Table 55. RF transmitting power for SC151-CN

Mode	Band	Max Power(dBm)	Min Power(dBm)
WCDMA	Band 1	24+1.7/-3.7	< -49
	Band 8	24+1.7/-3.7	< -49
LTE FDD	Band 1	23±2.7	< -39
	Band 3	23±2.7	< -39
	Band 5	23±2.7	< -39
	Band 8	23±2.7	< -39
LTE TDD	Band 34	23±2.7	< -39
	Band 38	23±2.7	< -39
	Band 39	23±2.7	< -39
	Band 40	23±2.7	< -39
	Band 41	23±2.7	< -39
NR FDD	n1	23±2	< -39
	n3	23±2	< -39
	n5	23±2	< -39
	n8	23±2	< -39
	n28A	23+2/-2.5	< -39
NR TDD	n41	26+2/-3	< -39
	n78	26+2/-3	< -39
	n79	26+2/-3	< -39

Table 56. RF transmitting power for SC151-GL

Mode	Band	Max Power(dBm)	Min Power(dBm)
WCDMA	Band 1	24+1.7/-3.7	< -49
	Band 2	24+1.7/-3.7	< -49
	Band 4	24+1.7/-3.7	< -49

Mode	Band	Max Power(dBm)	Min Power(dBm)
	Band 5	24+1.7/-3.7	< -49
	Band 6	24+1.7/-3.7	< -49
	Band 8	24+1.7/-3.7	< -49
	Band 19	24+1.7/-3.7	< -49
	Band 9	24+1.7/-3.7	< -49
LTE FDD	Band 1	23±2.7	< -39
	Band 2	23±2.7	< -39
	Band 3	23±2.7	< -39
	Band 4	23±2.7	< -39
	Band 5	23±2.7	< -39
	Band 7	23±2.7	< -39
	Band 8	23±2.7	< -39
	Band 12	23±2.7	< -39
	Band 13	23±2.7	< -39
	Band 14	23±2.7	< -39
	Band 17	23±2.7	< -39
	Band 18	23±2.7	< -39
	Band 19	23±2.7	< -39
	Band 20	23±2.7	< -39
	Band 25	23±2.7	< -39
	Band 26	23±2.7	< -39
	Band 28	23±2.7	< -39
	Band 30	23±2.7	< -39

Mode	Band	Max Power(dBm)	Min Power(dBm)
	Band 66	23±2.7	< -39
	Band 71	23±2.7	< -39
LTE TDD	Band 38	23±2.7	< -39
	Band 40	23±2.7	< -39
	Band 41	23±2.7	< -39
	Band 42	23±2.7	< -39
	Band 43	23±2.7	< -39
	Band 48	23±2.7	< -39
NR FDD	n1	23±2.7	< -39
	n2	23±2.7	< -39
	n3	23±2.7	< -39
	n5	23±2.7	< -39
	n7	23±2.7	< -39
	n8	23±2.7	< -39
	n12	23±2.7	< -39
	n14	23±2.7	< -39
	n20	23±2.7	< -39
	n25	23±2.7	< -39
	n28	23+2.7/-3.2	< -39
	n30	23±2.7	< -39
	n66	23±2.7	< -39
	n71	23±2.7	< -39
NR TDD	n38	23+2.7/-2.7	< -39

Mode	Band	Max Power(dBm)	Min Power(dBm)
	n40	23+2.7/-2.7	< -39
	n41	26+2.7/-3.7	< -39
	n48	23+2.7/-3.7	< -39
	n77	26+3/-4	< -39
	n78	26+3/-4	< -39

6.6 Receiving Sensitivity

Receiving sensitivity is the receiving sensitivity of the module measured at the antenna pin at an ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when designing, so as to avoid excessive insertion loss affecting TIS indicators. The receiving sensitivity of the module is as follows:

Test conditions: power supply of 3.8V and environment temperature of 25°C

Table 57. Four-antenna RF receiving sensitivity for SC151-CN

Mode	Band	Typical Value	3GPP Requirement	Unit
LTE FDD	Band 1	-102.5	-99	dBm
LTE TDD	Band 41	-100	-97	dBm
NR FDD	n1	-100	-99.5+TT	dBm
NR TDD	n41	-88	-87.4+TT	dBm
	n78	-93.5	-87.8+TT	dBm
	n79	-93	-87.8+TT	dBm

Table 58. Four-antenna RF receiving sensitivity for SC151-GL

Mode	Band	Typical Value	3GPP Requirement	Unit
LTE FDD	Band 1	TBD	-99	dBm

Mode	Band	Typical Value	3GPP Requirement	Unit
	Band 2	TBD	-97	dBm
	Band 3	TBD	-96	dBm
	Band 4	TBD	-99	dBm
	Band 7	TBD	-97	dBm
	Band 25	TBD	-95.5	dBm
	Band 30	TBD	-98	dBm
	Band 66	TBD	-98.5	dBm
LTE TDD	Band 38	TBD	-99	dBm
	Band 40	TBD	-99	dBm
	Band 41	TBD	-97	dBm
	Band 42	TBD	-97.2	dBm
	Band 43	TBD	-97.2	dBm
	Band 48	TBD	-97.2	dBm
NR FDD	n1	-100	-99.5+TT	dBm
	n2	TBD	-97.5+TT	dBm
	n3	TBD	-96.5+TT	dBm
	n7	TBD	-97.5+TT	dBm
	n25	TBD	-96+TT	dBm
	n30	TBD	-98.5+TT	dBm
	n66	TBD	-99+TT	dBm
NR TDD	n38	TBD	-99.5+TT	dBm
	n40	TBD	-99.5+TT	dBm

Mode	Band	Typical Value	3GPP Requirement	Unit
	n41	TBD	-87.4+TT	dBm
	n48	TBD	-96.7+TT	dBm
	n77	TBD	-87.8+TT	dBm
	n78	TBD	-87.8+TT	dBm

Table 59. Dual-antenna RF receiving sensitivity for SC151-CN

Mode	Band	Typical Value	3GPP Requirement	Unit
WCDMA	Band 1	-108	-106	dBm
	Band 8	-110	-103	dBm
LTE FDD	Band 1	-98	-96.3	dBm
	Band 3	-97	-93.3	dBm
	Band 5	-99	-94.3	dBm
	Band 8	-99	-93.3	dBm
LTE TDD	Band 34	-97	-96.3	dBm
	Band 38	-97	-96.3	dBm
	Band 39	-97	-96.3	dBm
	Band 40	-98	-96.3	dBm
	Band 41	-97	-94.3	dBm
NR FDD	n1	-97.5	-96.8 +TT	dBm
	n3	-96	-93.8 +TT	dBm
	n5	-97.5	-94.8+TT	dBm
	n8	-99	-93.8+TT	dBm
	n28A	-97	-95.5 +TT	dBm
NR TDD	n41	-85.5	-84.7 +TT	dBm
	n78	-88	-85.6+TT	dBm
	n79	-88	-85.6+TT	dBm

Table 60. Dual-antenna RF receiving sensitivity for SC151-GL

Mode	Band	Typical Value	3GPP Requirement	Unit
WCDMA	Band 1	-108	-106.7	dBm
	Band 2	TBD	-104.7	dBm
	Band 4	TBD	-106.7	dBm
	Band 5	-109	-104.7	dBm
	Band 6	-109	-106.7	dBm
	Band 8	-110	-103.7	dBm
	Band 9	-110	-105.7	dBm
	Band 19	-109	-106.7	dBm
LTE FDD	Band 1	-98	-96.3	dBm
	Band 2	-101	-94.3	dBm
	Band 3	TBD	-93.3	dBm
	Band 4	-100	-96.3	dBm
	Band 5	-99	-94.3	dBm
	Band 7	-99	-94.3	dBm
	Band 8	-101	-93.3	dBm
	Band 12	-101	-93.3	dBm
	Band 13	-101	-93.3	dBm
	Band 14	-101	-93.3	dBm
	Band 17	-100	-93.3	dBm
	Band 18	-100	-96.3	dBm
	Band 19	-100	-96.3	dBm
	Band 20	-101	-93.3	dBm
	Band 25	-101	-92.8	dBm
	Band 26	-100	-93.8	dBm

Mode	Band	Typical Value	3GPP Requirement	Unit
	Band 28	-101	-94.8	dBm
	Band 30	-99	-95.3	dBm
	Band 66	-100	-95.8	dBm
	Band 71	-102	-93.5	dBm
LTE TDD	Band 38	-99	-96.3	dBm
	Band 40	-99	-96.3	dBm
	Band 41	-99	-94.3	dBm
	Band 42	-102	-95	dBm
	Band 43	-102	-95	dBm
	Band 48	-102	-95	dBm
NR FDD	n1	TBD	-96.8 +TT	dBm
	n2	TBD	-94.8+TT	dBm
	n3	TBD	-93.8 +TT	dBm
	n5	TBD	-94.8+TT	dBm
	n7	TBD	-94.8+TT	dBm
	n8	TBD	-93.8+TT	dBm
	n12	TBD	-93.8 +TT	dBm
	n14	TBD	-93.8 +TT	dBm
	n20	TBD	-93.8 +TT	dBm
	n25	TBD	-93.3+TT	dBm
	n28	TBD	-95.5+TT	dBm
	n30	TBD	-95.8+TT	dBm
	n66	TBD	-96.3+TT	dBm
	n71	TBD	-94+TT	dBm
NR TDD	n38	TBD	-96.8+TT	dBm
	n40	TBD	-96.8+TT	dBm

Mode	Band	Typical Value	3GPP Requirement	Unit
	n41	TBD	-84.7 +TT	dBm
	n48	TBD	-94+TT	dBm
	n77	TBD	-85.6+TT	dBm
	n78	TBD	-85.6+TT	dBm

- The LTE sensitivity test bandwidth is 10M. Refer to 3GPP for the RB configuration.
- The bandwidth of 5GNR FDD sensitivity test is 10M. Refer to 3GPP for the RB configuration.
- The bandwidth of 5GNR TDD sensitivity test is 100M. Refer to 3GPP for the RB configuration.
- TT (Test Tolerance): For tolerance values of the test receiving sensitivity, refer to 3GPP protocol 38.521-1. The details are shown in the following table:

Test Tolerance (TT) for RX sensitivity level	
f ≤ 3.0GHz	3.0GHz < f ≤ 6.0GHz
0.7dB	1.0dB

Table 61. LTE CA band combinations for SC151-CN

CA configuration	ULCA	DL 4×4 MIMO
CA_1A-5A	- -	1A
CA_3A-5A	- -	- -
CA_1A-8A	- -	1A
CA_3A-8A	- -	- -
CA_5A-41A	- -	41A
CA_8A-41A	- -	41A
CA_39A-41A	- -	41A

CA configuration	ULCA	DL 4×4 MIMO
CA_1C	1C	1C
CA_3C	- -	- -
CA_38C	- -	- -
CA_40C	- -	- -
CA_41C	41C	41C
CA_40D	- -	- -
CA_41D	41C	41D
CA_40A-40A	- -	- -
CA_40A-40C	- -	- -
CA_41A-41A	41C	41A
CA_41A-41C	41C	41A-41C
CA_41A-41A-41A	41C	41A-41A

Table 62. NR CA band combinations for SC151-CN

CA configuration	ULCA	DLCA
CA_n28A-n41A	- -	n41A (4×4 MIMO)
CA_N41A-N28A		N28A(2×2 MIMO)

Table 63. EN-DC band combinations for SC151-CN

5G-NR	Sub-Category	EN-DC Combination	4G DL 4×4 MIMO	5G-NR DL 4×4 MIMO	4G UL	5G-NR UL
TDD	1DL+FR1	DC_1A_n78A	1A	n78A	1A	n78A
TDD	1DL+FR1	DC_3A_n78A	- -	n78A	3A	n78A
TDD	1DL+FR1	DC_5A_n78A	- -	n78A	5A	n78A
TDD	1DL+FR1	DC_8A_n78A	- -	n78A	8A	n78A
TDD	1DL+FR1	DC_3A_n41A	- -	n41A	3A	n41A
TDD	1DL+FR1	DC_39A_n41A	- -	n41A	39A	n41A

5G-NR	Sub-Category	EN-DC Combination	4G DL 4×4 MIMO	5G-NR DL 4×4 MIMO	4G UL	5G-NR UL
TDD	1DL+FR1	DC_3A_n79A	- -	n79A	3A	n79A
TDD	1DL+FR1	DC_39A_n79A	- -	n79A	39A	n79A
TDD	1DL+FR1	DC_40A_n79A	- -	n79A	40A	n79A

SC151-GL_ENDC&CA refer to Fibocom_SC151-GL_CA_ENDC_List_V1.0.xlsx

6.7 Electrostatic Features

In the application of the module, static electricity generated by human body and static electricity generated by friction between micro-electronics are discharged to the module through various channels and may cause damage to the module. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, ESD protection should added at the designed circuit interfaces and at the points susceptible to damage or impact from electrostatic discharge. Anti-static gloves should be worn during production. The ESD protection level at 25℃ ambient temperature and 45% humidity is described in the following table.

Table 64. ESD protection level

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±4	±8	kV
Other interface	±0.5	±1	kV

- The data is tested based on the development board of Fibocom.
- ESD performance is strongly related to PCB design, and key control signals should be protected.
- When designing the whole machine, pay attention to maintain the integrity and connectivity of GND.

6.8 Reliability

The reliability test of Fibocom is conducted according to the industrial level. For the reliability test results, refer to *Fibocom_SC151_Industry Standard Reliability Test Report_V1.0*.

6.9 Thermal Design

For more thermal design guidance, refer to Fibocom_General Thermal Design Guide for Modules.

7 Structure Specifications

7.1 Product Appearance

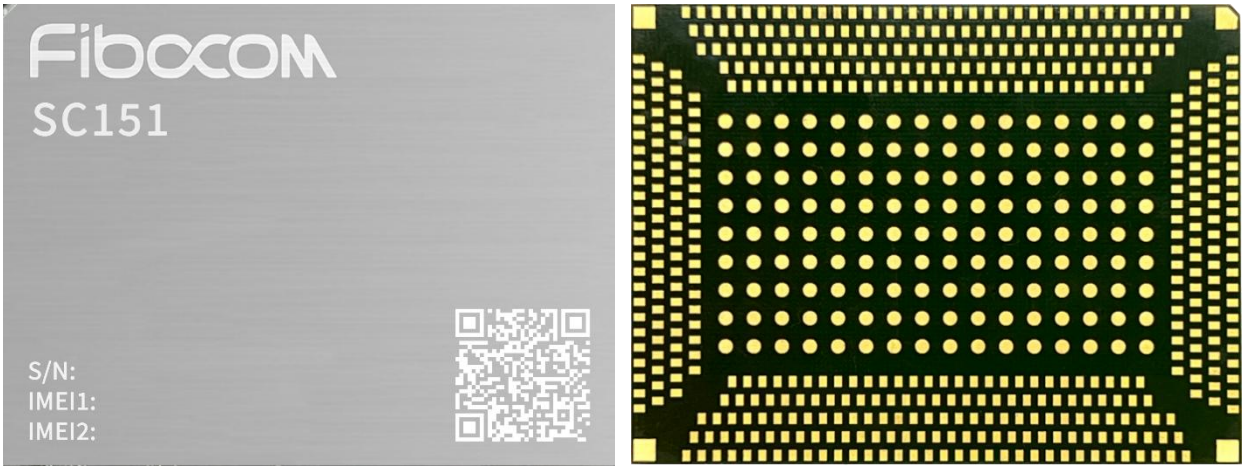
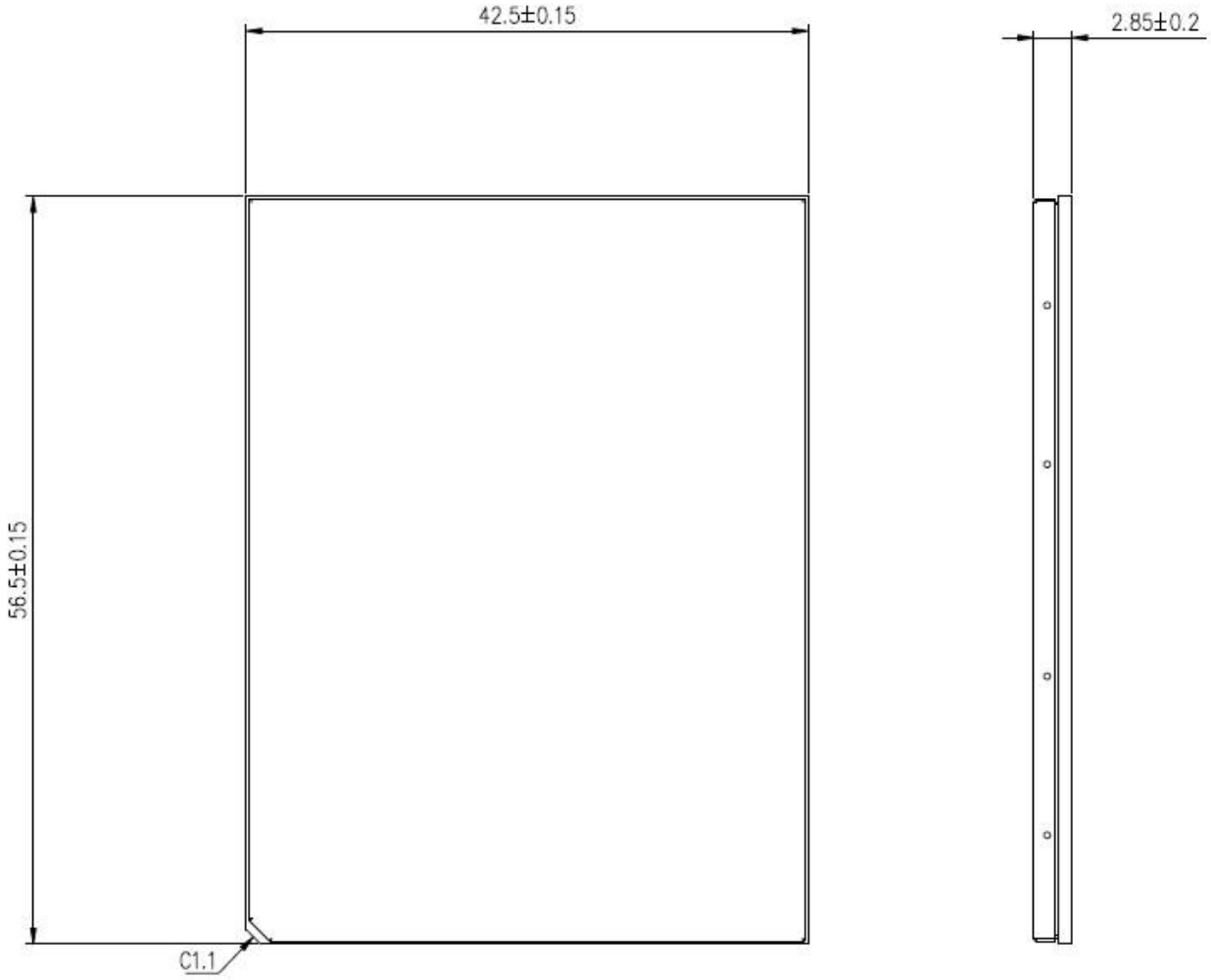


Figure 31. Product appearance

7.2 Structure Dimensions



Top View

Side View

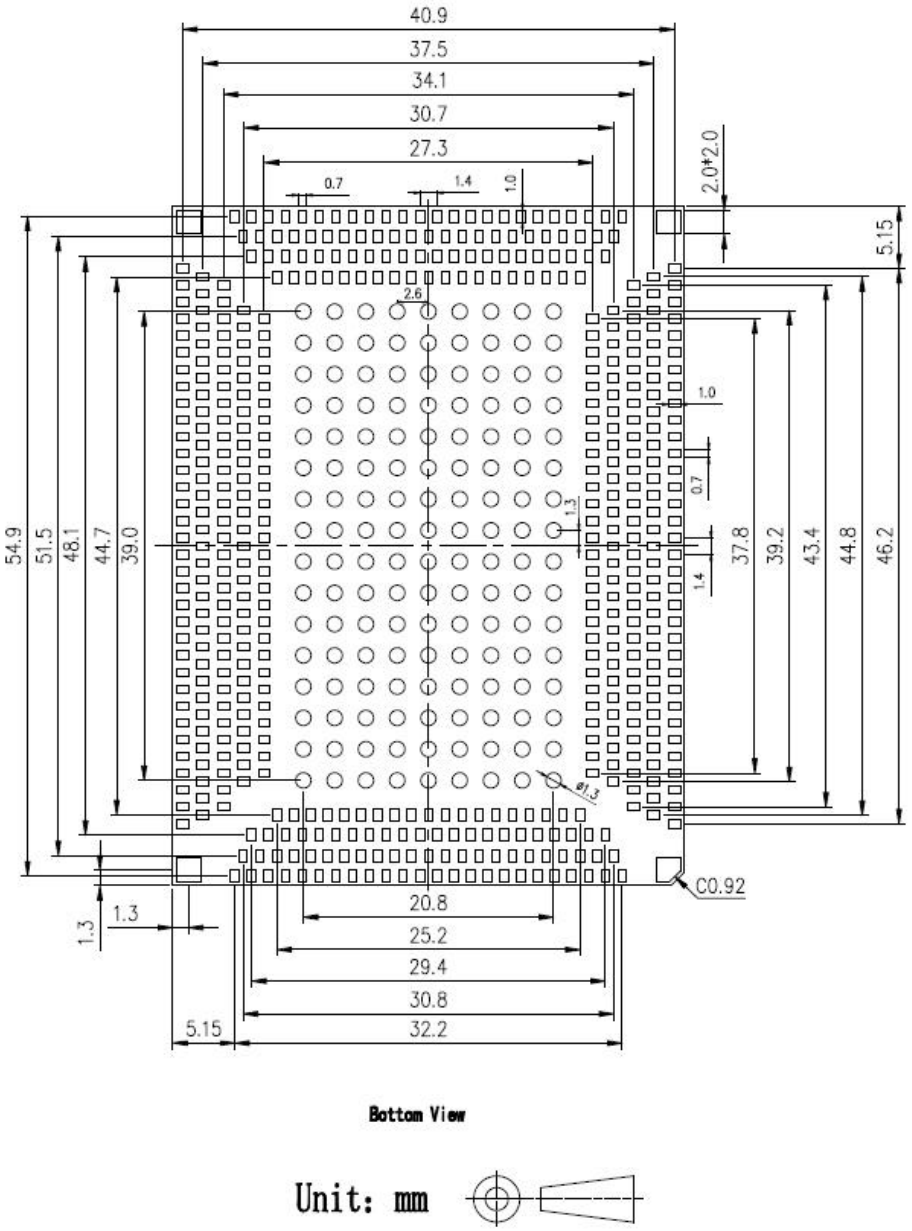


Figure 32. Structure dimensions (unit: mm)

7.3 PCB Package

The following figure shows the PCB package size of the module, and users can design the PCB package by themselves. Fibocom also provides users with a designed document "Fibocom_SC151_SCH & PCB Package", which can be found in the package.

8 Storage, Production and Packaging

8.1 Storage, Production and Packaging

Refer to the *Fibocom_SC151_SMT Design Guide* for storage, production, and packaging.

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling.

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily removed. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOSC151GL” “Contains IC: 21374-SC151GL”. The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

3) Note: When B48 using these max tune up power, the host manufacturer should reduce the antenna gain to meet the FCC maximum EIRP limit.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 21374-SC151GL”

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 21374-SC151GL "

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Appendix A. Reference Documents

Category	Document Name
Hardware	Fibocom_SC151_CA_ENDC_List
Reference design	Fibocom_SC151_Package
	Fibocom_SC151_Reference Design
Development kit	Fibocom_SC151_ADP User Guide
	Fibocom_EVB-SOC_User Guide
User Guide	Fibocom_Design Guide_RF Antenna
	Fibocom_SC151_SMT Design Guide
	Fibocom_General Thermal Design Guide for Modules

Appendix B. Acronyms and Abbreviations

Acronym and Abbreviation	Description
AR	Augmented Reality
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Down Link
DLCA	Down Link Carrier Aggregation
ECC	Envelope Correlation Coefficient
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	Multiple-input and multiple-output

MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter

UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VSWR	Voltage Standing Wave Ratio
VR	Virtual Reality
WCDMA	Wideband Code Division Multiple Access