



SC162

Hardware Guide

V1.0

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Applicable Model

No.	Applicable Model	Description
1	SC162-EAU-46	4GB+64GB discrete eMMC, 5G, suitable for use in Europe and Asia
2	SC162-EAU-20	4GB+64GB eMCP, 5G, suitable for use in Europe and Asia
3	SC162-EAU-21	4GB+64GB eMCP, 4G, suitable for use in Europe and Asia
4	SC162-EAU-60	8GB+128GB uMCP, 5G, suitable for use in Europe and Asia
5	SC162-EAU-61	8GB+128GB uMCP, 4G, suitable for use in Europe and Asia
6	SC162-EAU-70	8GB+256GB uMCP, 5G, suitable for use in Europe and Asia
7	SC162-NA-20	4GB+64GB eMCP, 5G, suitable for use in North America
8	SC162-NA-21	4GB+64GB eMCP, 4G, suitable for use in North America
9	SC162-NA-60	8GB+128GB uMCP, 5G, suitable for use in North America
10	SC162-NA-61	8GB+128GB uMCP, 4G, suitable for use in North America

Change History

V1.0 (2025-08-22)	Initial version. Added applicable models and specification parameters for NA regions.
V0.1 (2025-07-02)	Draft version.

1 Foreword

1.1 Product Introduction

The SC162 series smart module integrates core components such as baseband, MCP, PMU, transceiver, and PA. It supports long-distance communication in different modes, including NR, FDD-LTE, TDD-LTE, and WCDMA. In addition, it supports Wi-Fi/BT short-distance wireless transmission and GNSS wireless positioning. The SC162 series module is embedded with the Android operating system and supports various interfaces such as MIPI, USB, UART, SPI, and I2C. It is the optimal solution for the core system of wireless smart products.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station(MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD);Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V15.0.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 38.300 V15.5.0: 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V15.2.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Range 1 Standalone;
- 3GPP TS 38.521-3 V15.2.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios;
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment -Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB
- Universal Serial Bus Specification 2.0
- Universal Serial Bus Specification 3.0

Warning

FCC Regulatory Compliance

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom wires Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

The antenna is external detachable antenna ; It needs to be connected to the device via RF cable.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “ Contains FCC ID: ZMOSC162NA ” .

The FCC ID can be used only when all FCC compliance requirements are met.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user ' s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help. Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part 27, part 90 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator

is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Industry Canada Statement

This device complies with Industry Canada 's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

(For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the ant

This device is intended only for OEM integrators under the following conditions:

enna and users, and 2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être ins-

tallée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with

another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considérée comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur

OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:"

Contient des IC: 21374-SC162NA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as shown in this manual.

Notes: the device for operation in the band 5150-5350 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module. Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Notes: l'appareil destiné à fonctionner dans la bande 5150 - 5350 MHz est uniquement destiné à une utilisation en intérieur pour réduire le risque d'interférences nuisibles aux systèmes de satellites mobiles à canal commun.

2 Overview

2.1 Product Introduction

The following table describes the network modes and frequency bands supported by the SC162 series module.

Table 1. Supported frequency bands for EAU

Network Mode	Frequency Band
WCDMA	Band 1/5/8
FDD-LTE	Band 1/3/5/7/8/20/28
TDD-LTE	Band 38/40/41
NR Sub-6	n1/n3/n5/n7/n8/n20/n28/n38/n40/n41
Wi-Fi	2402MHz to 2482MHz 5170MHz to 5835MHz
BT	2402MHz to 2480MHz
GNSS	GPS (L1+L5)/GLONASS/BeiDou/Galileo

Table 2. Supported frequency bands for NA

Network Mode	Frequency Band
FDD-LTE	Band 2/4/5/7/12/13/14/17/25/26/66/71
TDD-LTE	Band 41
Wi-Fi	2402MHz to 2482MHz 5170MHz to 5835MHz
BT	2402MHz to 2480MHz
GNSS	GPS (L1+L5)/GLONASS/BeiDou/Galileo

2.2 Key Features

The SC162 series module can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, and security monitoring and multimedia terminals. The following table describes the detailed performance parameters of the SC162 series module.

Table 3. Performance parameters

Item	Description
Power supply	DC: 3.5V to 4.4V, typical voltage value: 3.8V
Application processor	Customized 64-bit Arm v8-compliant application processor Kryo Gold: dual high-performance cores with 2.073 GHz Kryo Silver: hexa low-power cores with 1.708 GHz
Storage	4GB+64GB
	8GB+128GB
	8GB+256GB
Power class	Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands Class 3 (23dBm±2dB) for NR FDD bands Class 3 (23dBm±2dB) for NR TDD bands Class 2 (26dBm±2dB) for B41/n41/n78/n79 bands
WCDMA features	3GPP Release 8 DC-HSPA+ is supported. 16-QAM, 64-QAM, and QPSK modulation are supported. CAT7 HSPA+: maximum uplink rate of 5.76 Mbps CAT24 DC-HSPA+: maximum downlink rate of 42 Mbps
LTE features	FDD/TDD R15 CAT18 is supported. The RF bandwidth of 1.4 MHz to 20 MHz is supported. Downlink supports multi-user MIMO. 256 QAM for UL, 256 QAM for DL. DL 2×2 MIMO is supported. The FDD maximum uplink rate is 170 Mbps, and the maximum downlink rate is 780 Mbps. The TDD maximum uplink rate is 150 Mbps, and the maximum downlink rate is 900 Mbps.
SA features	3GPP Release 15 256 QAM for UL, 256 QAM for DL 15kHz SCS for FDD, 30kHz SCS for TDD Maximum uplink rate: 900 Mbps, maximum downlink rate: 2 Gbps
WLAN features	2.4G and 5G WLAN wireless communication is supported. 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, 802.11ax, and SISO are supported.
Bluetooth feature	BT5.1 (BR/EDR+BLE)
Satellite positioning	GPS (L1+L5)/GLONASS/BeiDou/Galileo

Item	Description
MIMO	DL 2MIMO
SMS	Text and PDU modes Point-to-point MO and MT SMS cell broadcast SMS message storage: stored in the module by default
LCD interface	1 set of 4-Lane MIPI DSI interface Up to FHD+ (2520×1080) @ 60 fps
Camera interface	3 sets of 4-Lane (4+4+4 configuration) MIPI CSI interfaces, defaulting to D-PHY 1.2 interfaces @2.5 Gbps per lane. The single-camera configuration supports up to 16MP (megapixels), while the dual-camera configuration supports up to 32MP+16MP @30 fps.
Audio interface	Audio input: 1 set of digital microphone input Audio output: 3 sets of I2S interfaces, which can be connected to an external Codec chip.
USB interface	Support for USB 3.1 Gen1 with DisplayPort1.4 Support for USB 2.0 and USB OTG (external 5V power supply required)
(U)SIM interface	2 sets of (U)SIM card interfaces, supporting 1.8V/2.95V (U)SIM card self-adaptation Dual-(U)SIM dual-standby single-active and hot plug are supported.
UART interface	One 4-lane serial interface that supports RTS and CTS hardware flow control One 2-lane debugging serial interface One 2-lane serial interface
SDIO interface	Support for SD 3.0 and 4-bit SDIO, as well as hot plugging
I2C interface	Multiple sets of I2C interfaces, which can be used for peripherals such as TP, camera, and sensor.
ADC interface	2 channels
RTC clock	Supported
Antenna interface	4
Physical characteristics	Dimensions: (41.0±0.15) mm x (41.0±0.15) mm x (2.6±0.2) mm Packaging: 148 LCC pins + 128 LGA pins Weight: About 11 g
Temperature range	Operating temperature ¹⁾ : -30°C to 75°C Storage temperature: -40°C to 85°C
Software update	USB/OTA/SD
RoHS	Compliant with RoHS standards



¹⁾Operating temperature: Within this temperature range, the module can work normally and module performance meets 3GPP specifications.

2.3 Function Block Diagram

The main hardware features of the SC162 series module include:

- Baseband
- Wireless transceiver
- PMU
- Storage
 - Communication expansion interface (USB/UART/I2C/SDIO/SPI, etc.)
 - (U)SIM interface
 - MIPI DSI interface
 - MIPI CSI interface

The following figure shows the function block diagram of the SC162 series module.

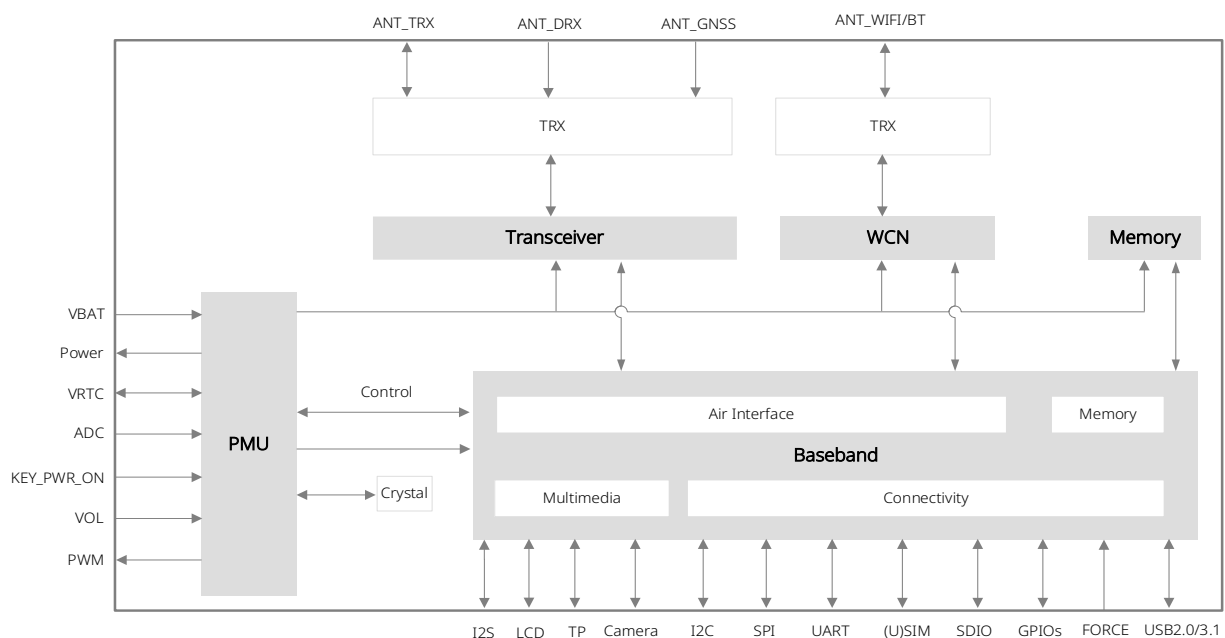


Figure 1. Function block diagram

3.1 Pin Distribution

The diagram illustrates the pin-to-pin mapping for the Raspberry Pi 4 Model B, showing connections between the 40-pin header and the 28-pin micro-USB header. The connections are organized into two main sections: the top section for the 40-pin header and the bottom section for the 28-pin header. Each section contains a grid of colored squares representing individual pins, with their corresponding functions and pin numbers. The top section is labeled 'FORCE_USB_BOOT' and the bottom section is labeled 'SD_CARD_DET_N'. The diagram shows various connections, including power (VCC, GND), data (GPIO, I2C, SPI, UART), and peripheral (USB, Ethernet, Camera) pins. The colors of the squares correspond to the colors of the pins on the physical board.

Top Section (40-pin header):

- Pin 1:** FORCE_USB_BOOT
- Pin 2:** NC
- Pin 3:** GND
- Pin 4:** VBAT
- Pin 5:** VBAT
- Pin 6:** VBAT
- Pin 7:** GND
- Pin 8:** NC
- Pin 9:** NC
- Pin 10:** GND
- Pin 11:** USB_DM
- Pin 12:** USB_DP
- Pin 13:** GND
- Pin 14:** NC
- Pin 15:** GND
- Pin 16:** USB_ID
- Pin 17:** UIM2_DETECT
- Pin 18:** UIM2_RESET
- Pin 19:** UIM2_CLK
- Pin 20:** UIM2_DATA
- Pin 21:** VREG_L5E_UIM2
- Pin 22:** UIM1_DETECT
- Pin 23:** UIM1_RESET
- Pin 24:** UIM1_CLK
- Pin 25:** UIM1_DATA
- Pin 26:** VREG_L4E_UIM1
- Pin 27:** GND
- Pin 28:** VREG_L9E_P2P96
- Pin 29:** SDC2_CLK
- Pin 30:** SDC2_CMD
- Pin 31:** SDC2_DATA0
- Pin 32:** SDC2_DATA1
- Pin 33:** SDC2_DATA2
- Pin 34:** SDC2_DATA3
- Pin 35:** SD_CARD_DET_N
- Pin 36:** GND
- Pin 37:** NC

Bottom Section (28-pin header):

- Pin 38:** GPIO_17
- Pin 39:** GPIO_18
- Pin 40:** GPIO_12
- Pin 41:** TS_I2C_SCL
- Pin 42:** TS_INT_N
- Pin 43:** TS_RST_N
- Pin 44:** PWM_PM6150L
- Pin 45:** UART_TX/GPIO_2
- Pin 46:** UART_RX/GPIO_3
- Pin 47:** UART_CTS/GPIO_0
- Pin 48:** UART_RTS/GPIO_1
- Pin 49:** LCD_RST_PM6150L
- Pin 50:** LCD_TE
- Pin 51:** GND
- Pin 52:** MIPI_DSIO_CLK_M
- Pin 53:** MIPI_DSIO_CLK_P
- Pin 54:** MIPI_DSIO_LANED_M
- Pin 55:** MIPI_DSIO_LANED_P
- Pin 56:** MIPI_DSIO_LANE1_M
- Pin 57:** MIPI_DSIO_LANE1_P
- Pin 58:** MIPI_DSIO_LANE2_M
- Pin 59:** MIPI_DSIO_LANE2_P
- Pin 60:** MIPI_DSIO_LANE3_M
- Pin 61:** MIPI_DSIO_LANE3_P
- Pin 62:** GND
- Pin 63:** MIPI_CSIO_CLK_M
- Pin 64:** MIPI_CSIO_CLK_P
- Pin 65:** MIPI_CSIO_LANED_M
- Pin 66:** MIPI_CSIO_LANED_P
- Pin 67:** MIPI_CSIO_LANE1_M
- Pin 68:** MIPI_CSIO_LANE1_P
- Pin 69:** GND
- Pin 70:** MIPI_CSIO_CLK_M
- Pin 71:** MIPI_CSIO_CLK_P
- Pin 72:** MIPI_CSIO_LANE0_M
- Pin 73:** MIPI_CSIO_LANE0_P
- Pin 74:** GND

Connections:

- GPIO_8:** 111
- GPIO_9:** 110
- ACCEL_GYRO_INT1:** 109
- ACCEL_GYRO_INT2:** 108
- MAG_INT_N:** 107
- ALSP_INT_N:** 106
- FT_ID_GPIO_11:** 105
- GPIO_13:** 104
- GRFC_122:** 103
- GRFC_121:** 102
- CAM_MCLK1:** 101
- GPIO_7:** 100
- GPIO_142:** 99
- GPIO_135:** 98
- GPIO_16:** 97
- GPIO_15:** 96
- GND:** 95
- ANT_TRX:** 94
- GND:** 93
- KEY_VOL_DOWN:** 92
- KEY_VOL_UP:** 91
- DBG_UART_TX:** 90
- DBG_UART_RX:** 89
- SNS_I2C4_SDA:** 88
- SNS_I2C4_SCL:** 87
- GPIO_14:** 86
- CCI_I2C_SDA2:** 85
- CCI_I2C_SCL2:** 84
- CAM0_PWD_N:** 83
- CAM0_RST_N:** 82
- CAM2_PWD_N:** 81
- CAM2_RST_N:** 80
- GND:** 79
- ANT_WIFI/BT:** 78
- GND:** 77
- CAM_MCLK0:** 76
- CAM_MCLK2:** 75
- GPIO_6:** 112
- GPIO_84:** 118
- GPIO_83:** 117
- SPI_MOSI:** 116
- SPI_MISO:** 115
- SPI_CS:** 114
- SPI_CLK:** 113
- GPIO_6:** 112
- GPIO_13:** 104
- GRFC_122:** 103
- GRFC_121:** 102
- CAM_MCLK1:** 101
- GPIO_7:** 100
- GPIO_142:** 99
- GPIO_135:** 98
- GPIO_16:** 97
- GPIO_15:** 96
- GND:** 95
- ANT_TRX:** 94
- GND:** 93
- KEY_VOL_DOWN:** 92
- KEY_VOL_UP:** 91
- DBG_UART_TX:** 90
- DBG_UART_RX:** 89
- SNS_I2C4_SDA:** 88
- SNS_I2C4_SCL:** 87
- GPIO_14:** 86
- CCI_I2C_SDA2:** 85
- CCI_I2C_SCL2:** 84
- CAM0_PWD_N:** 83
- CAM0_RST_N:** 82
- CAM2_PWD_N:** 81
- CAM2_RST_N:** 80
- GND:** 79
- ANT_WIFI/BT:** 78
- GND:** 77
- CAM_MCLK0:** 76
- CAM_MCLK2:** 75
- GPIO_6:** 112
- GPIO_84:** 118
- GPIO_83:** 117
- SPI_MOSI:** 116
- SPI_MISO:** 115
- SPI_CS:** 114
- SPI_CLK:** 113
- GPIO_6:** 112

Figure 2. Pin distribution (top view)

3.2 Pin Description

Table 4. I/O parameters

Parameter	Description
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 5. Power supply

Pin Name	Pin No.	I/O	Description	Remarks
VBAT	4,5,6	PI	Main power input	--
VCOIN	126	PIO	RTC clock power supply pin	--
VREG_L11A_1P8	129	PO	1.8V voltage output	--
VREG_L14A_1P8	122	PO	1.8V voltage output	--
VREG_L9E_2P96	28	PO	SD card power supply	--
VREG_L4E_UIM1	26	PO	(U)SIM card 1 power supply	1.8V/3V adaptive
VREG_L5E_UIM2	21	PO	(U)SIM card 2 power supply	1.8V/3V adaptive
VREG_L8A_1P8	130	PO	1.8V voltage output	--
VREG_L6A_3P0	265	PO	3.0V voltage output	Available for sensor power supply

Table 6. Button interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
KEY_PWR_N	123	DI	--	Power-on/off button	1.1V
CBL_PWR_N	165	DI	--	Button for power-on and automatic startup	--
KEY_VOL_UP	91	DI	--	Volume +	--
KEY_VOL_DOWN	92	DI	--	Volume -	--
FORCE_USB_BOOT	1	DI	--	USB forced download	--

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
				button	

Table 7. (U)SIM interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
UIM1_DATA	25	DI,DO	--	(U)SIM1 data signal	--
UIM1_CLK	24	DO	--	(U)SIM1 clock signal	--
UIM1_RESET	23	DO	--	(U)SIM1 reset signal	--
UIM1_DETECT	22	DI	--	(U)SIM1 hot-plug detection signal	--
UIM2_DATA	20	DI,DO	--	(U)SIM2 data signal	--
UIM2_CLK	19	DO	--	(U)SIM2 clock signal	--
UIM2_RESET	18	DO	--	(U)SIM2 reset signal	--
UIM2_DETECT	17	DI	--	(U)SIM2 hot-plug detection signal	--

Table 8. SD card interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
SD_CARD_DET_N	35	DI	--	SD card detection	--
SDC2_CLK	29	DO	--	SD card clock	--
SDC2_CMD	30	DI,DO	--	SD card command interface	--
SDC2_DATA0	31	DI,DO	--	SD card data bit 0	--
SDC2_DATA1	32	DI,DO	--	SD card data bit 1	--
SDC2_DATA2	33	DI,DO	--	SD card data bit 2	--
SDC2_DATA3	34	DI,DO	--	SD card data bit 3	--

Table 9. USB interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
USB_IN_DET	168	DI	--	USB insertion detection	--
USB0_HS_DP	12	AI,AO	--	USB 2.0 differential data signal +	--
USB0_HS_DM	11	AI,AO	--	USB 2.0 differential data signal -	--

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
DP_AUX_P	274	AI,AO	--	DisplayPort auxiliary transmission channel +	--
DP_AUX_M	263	AI,AO	--	DisplayPort auxiliary transmission channel -	--
USB0_SS_RX0_P	173	AI	--	USB 3.1 differential data reception +	--
USB0_SS_RX0_M	175	AI	--	USB 3.1 differential data reception -	--
USB0_SS_TX0_P	172	AO	--	USB 3.1 differential data transmission +	--
USB0_SS_TX0_M	174	AO	--	USB 3.1 differential data transmission -	--
USB0_SS_RX1_P	269	AI	--	USB 3.1 differential data reception +	--
USB0_SS_RX1_M	254	AI	--	USB 3.1 differential data reception -	--
USB0_SS_TX1_P	270	AO	--	USB 3.1 differential data transmission +	--
USB0_SS_TX1_M	255	AO	--	USB 3.1 differential data transmission -	--
GPIO_12	40	DI	--	DisplayPort hot-plug detection	--
USB_PHY_PS	276	DI	--	USB PHY port selection	--
USB0_ID	16	DI	--	USB ID detection	--

Table 10. UART interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
DBG_UART_RX	89	DI	PD	Debug serial interface RX	--
DBG_UART_TX	90	DO	PD	Debug serial interface TX	--
UART_CTS/GPIO_0	47	DI	PD	4-wire UART CTS	--
UART_RTS/GPIO_1	48	DO	PD	4-wire UART RTS	--
UART_TX/GPIO_2	45	DO	PD	4-wire UART data transmission	--
UART_RX/GPIO_3	46	DI	PD	4-wire UART data reception	--

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
UART_RX/GPIO_27	207	DI	PD	2-wire UART data reception	--
UART_TX/GPIO_28	209	DO	PD	2-wire UART data transmission	--

Table 11. I2C interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
APPS_I2C_SDA	267	DI,DO	PD	APPS I2C data line	1.8V
APPS_I2C_SCL	268	DO	PD	APPS I2C clock	1.8V
SNS_I2C4_SDA	88	DI,DO	PD	Sensor I2C data signal	1.8V
SNS_I2C4_SCL	87	DO	PD	Sensor I2C clock signal	1.8V
TS_I2C_SDA	150,158	DI,DO	PD	TP I2C data signal	1.8V
TS_I2C_SCL	41	DO	PD	TP I2C clock signal	1.8V
CCI_I2C_SDA0	208	DI,DO	PD	Camera 0 I2C data signal	1.8V
CCI_I2C_SCL0	206	DO	PD	Camera 0 I2C clock signal	1.8V
CCI_I2C_SDA2	85	DI,DO	PD	Camera 1 I2C data signal	1.8V
CCI_I2C_SCL2	84	DO	PD	Camera 1 I2C clock signal	1.8V

Table 12. Audio interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
DMIC1_CLK	145	DO	PD	Digital MIC clock signal	--
DMIC1_DATA	144	DI	PD	Digital MIC data signal	--
LPI_I2S2_CLK	137	DI,DO	PD	LPI_I2S2 serial clock	--
LPI_I2S2_WS	138	DI,DO	PD	LPI_I2S2 field selection	--
LPI_I2S2_DATA0	139	DI,DO	PD	LPI_I2S2 data channel 0	--
LPI_I2S2_DATA1	140	DI,DO	PD	LPI_I2S2 data channel 1	--
MI2S_0_SCK	247	DO	PD	MI2S_0 serial clock	--
MI2S_0_WS	238	DI,DO	PD	MI2S_0 frame clock	--
MI2S_0_DATA0	239	DI,DO	PD	MI2S_0 data channel 0	--
MI2S_0_DATA1	240	DI,DO	PD	MI2S_0 data channel 1	--
LPASS_EXT_MCLK0	251	DO	PD	MI2S_0 system master clock	--

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
MI2S_2_SCK	212	DO	PD	MI2S_2 serial clock	--
MI2S_2_WS	215	DI,DO	PD	MI2S_2 field selection	--
MI2S_2_DATA0	216	DI,DO	PD	MI2S_2 data channel 0	--
MI2S_2_DATA1	217	DI,DO	PD	MI2S_2 data channel 1	--
MI2S_2_MCLK	219	DO	PD	MI2S_2 system master clock	--

Table 13. SPI interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
SPI_CLK	113	DO	PD	SPI clock	1.8V
SPI_CS	114	DO	PD	SPI chip select	1.8V
SPI_MOSI	116	DO	PD	SPI master-out, slave-in	1.8V
SPI_MISO	115	DI	PD	SPI master-in, slave-out	1.8V

Table 14. LCD interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
MIPI_DSI0_CLK_P	53	AO	--	LCD DSI differential clock +	--
MIPI_DSI0_CLK_M	52	AO	--	LCD DSI differential clock -	--
MIPI_DSI0_LANE0_P	55	AO	--	LCD DSI differential lane 0 +	--
MIPI_DSI0_LANE0_M	54	AO	--	LCD DSI differential lane 0 -	--
MIPI_DSI0_LANE1_P	57	AO	--	LCD DSI differential lane 1 +	--
MIPI_DSI0_LANE1_M	56	AO	--	LCD DSI differential lane 1 -	--
MIPI_DSI0_LANE2_P	59	AO	--	LCD DSI differential lane 2 +	--
MIPI_DSI0_LANE2_M	58	AO	--	LCD DSI differential lane 2 -	--
MIPI_DSI0_LANE3_P	61	AO	--	LCD DSI differential lane 3 +	--

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
MIPI_DSI0_LANE3_M	60	AO	--	LCD DSI differential lane 3 -	--
LCD_TE	50	DI	--	LCD tearing effect signal	--
LCD_RST	49	DO	--	LCD reset signal	--
PWM_PM6150L	44	DO	--	LCD backlight control	--

Table 15. TP interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
TS_RESET_N	43	DO	--	TP reset signal	--
TS_INT_N	42	DI	--	TP interrupt signal	--

Table 16. Sensor interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
ACCEL_GYRO_INT1	109	DI	PD	Accelerometer and gyroscope sensor interrupt 1	--
ACCEL_GYRO_INT2	108	DI	PD	Accelerometer and gyroscope sensor interrupt 2	--
MAG_INT_N	107	DI	PD	Magnetometer interrupt	--
ALSP_INT_N	106	DI	PD	Proximity and ambient light sensor interrupt	--

Table 17. Camera interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
MIPI_CSI0_CLK_P	71	AI	--	Camera 0 MIPI clock +	--
MIPI_CSI0_CLK_M	70	AI	--	Camera 0 MIPI clock -	--
MIPI_CSI0_LANE0_P	73	AI	--	Camera 0 CSI lane 0 +	--
MIPI_CSI0_LANE0_M	72	AI	--	Camera 0 CSI lane 0 -	--
MIPI_CSI0_LANE1_P	184	AI	--	Camera 0 CSI lane 1 +	--
MIPI_CSI0_LANE1_M	185	AI	--	Camera 0 CSI lane 1 -	--
MIPI_CSI0_LANE2_P	186	AI	--	Camera 0 CSI lane 2 +	--
MIPI_CSI0_LANE2_M	187	AI	--	Camera 0 CSI lane 2 -	--
MIPI_CSI0_LANE3_P	188	AI	--	Camera 0 CSI lane 3 +	--
MIPI_CSI0_LANE3_M	189	AI	--	Camera 0 CSI lane 3 -	--

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
MIPI_CSI1_CLK_P	257	AI	--	Camera 1 CSI clock +	--
MIPI_CSI1_CLK_M	256	AI	--	Camera 1 CSI clock -	--
MIPI_CSI1_LANE0_P	271	AI	--	Camera 1 CSI lane 0 +	--
MIPI_CSI1_LANE0_M	258	AI	--	Camera 1 CSI lane 0 -	--
MIPI_CSI1_LANE1_P	272	AI	--	Camera 1 CSI lane 1 +	--
MIPI_CSI1_LANE1_M	259	AI	--	Camera 1 CSI lane 1 -	--
MIPI_CSI1_LANE2_P	273	AI	--	Camera 1 CSI lane 2 +	--
MIPI_CSI1_LANE2_M	260	AI	--	Camera 1 CSI lane 2 -	--
MIPI_CSI1_LANE3_P	262	AI	--	Camera 1 CSI lane 3 +	--
MIPI_CSI1_LANE3_M	261	AI	--	Camera 1 CSI lane 3 -	--
MIPI_CSI2_CLK_P	64	AI	--	Camera 2 CSI clock +	--
MIPI_CSI2_CLK_M	63	AI	--	Camera 2 CSI clock -	--
MIPI_CSI2_LANE0_P	66	AI	--	Camera 2 CSI lane 0 +	--
MIPI_CSI2_LANE0_M	65	AI	--	Camera 2 CSI lane 0 -	--
MIPI_CSI2_LANE1_P	68	AI	--	Camera 2 CSI lane 1 +	--
MIPI_CSI2_LANE1_M	67	AI	--	Camera 2 CSI lane 1 -	--
MIPI_CSI2_LANE2_P	181	AI	--	Camera 2 CSI lane 2 +	--
MIPI_CSI2_LANE2_M	183	AI	--	Camera 2 CSI lane 2 -	--
MIPI_CSI2_LANE3_P	180	AI	--	Camera 2 CSI lane 3 +	--
MIPI_CSI2_LANE3_M	179	AI	--	Camera 2 CSI lane 3 -	--
CAM_MCLK0	76	DO	PD	Camera 0 clock signal	--
CAM0_RST_N	82	DO	PD	Camera 0 reset signal	--
CAM0_PWD_N	83	DO	PD	Camera 0 power-down signal	--
CAM_MCLK1	101	DO	PD	Camera 1 clock signal	--
CAM1_RST_N	218	DO	PD	Camera 1 reset signal	--
CAM1_PWD_N	220	DO	PD	Camera 1 power-down signal	--
CAM_MCLK2	75	DO	PD	Camera 2 clock signal	--
CAM2_RST_N	80	DO	PD	Camera 2 reset signal	--
CAM2_PWD_N	81	DO	PD	Camera 2 power-down signal	--

Table 18. Antenna interface

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
ANT_TRX	94	AI,AO	--	Main antenna	--
ANT_DRX	132	AI	--	Diversity receive antenna	--
ANT_WIFI/BT	78	AI,AO	--	Wi-Fi/BT antenna	--
ANT_GNSS	120	AI	--	GNSS antenna	--

Table 19. Other interfaces

Pin Name	Pin No.	I/O	Reset Value	Description	DC Feature
FT_ID/GPIO_11 ¹⁾	105	DI	PD	Mode identification GPIO	--
ADC1_PM6150L	243	AI	PD	General-purpose ADC1 interface	--
ADC2_PM6150L	128	AI	PD	General-purpose ADC2 interface	--
2, 8, 9, 14, 37, 124, 125, 127, 134, 135, 141, 142, 147, 148, 151, 159, 166, 167, 169, 192, 193, 194, 195, 198, 199, 200, 201, 202, 203, 223, 224, 225, 227, 233, 234, 241, 242, 244, 248, 252, 264, 266				NC	--
3, 7, 10, 13, 15, 27, 36, 51, 62, 69, 74, 77, 79, 93, 95, 119, 121, 131, 133, 136, 143, 146, 149, 152, 153, 154, 155, 156, 157, 160, 161, 162, 163, 164, 170, 171, 176, 177, 178, 182, 190, 191, 196, 197, 204, 205, 228, 229, 230, 231, 232, 235, 236, 237, 246, 250, 253, 275				GND	--



1). FT_ID/GPIO_11 is a boot_config GPIO. External pull-up is prohibited. Otherwise, a power-on failure may occur.

Table 20. GPIO interface

Pin Name	Pin No.	I/O	Reset Value	Wakeup Function	DC Feature
GPIO_9	110	DI,DO	PD	Y	PD:nppukp
GPIO_13	104	DI,DO	PD	Y	PD:nppukp
GPIO_14	86	DI,DO	PD	N	PD:nppukp
GPIO_15	96	DI,DO	PD	N	PD:nppukp

Pin Name	Pin No.	I/O	Reset Value	Wakeup Function	DC Feature
GPIO_16	97	DI,DO	PD	Y	PD:nppukp
GPIO_17	38	DI,DO	PD	Y	PD:nppukp
GPIO_18	39	DI,DO	PD	Y	PD:nppukp
GPIO_135	98	DI,DO	PD	N	PD:nppukp
GPIO_142	99	DI,DO	PD	Y	PD:nppukp
GPIO_7	100	DI,DO	PD	Y	PD:nppukp
GPIO_121	102	DI,DO	PD	N	PD:nppukp
GPIO_122	103	DI,DO	PD	Y	PD:nppukp
GPIO_6	112	DI,DO	PD	N	PD:nppukp
GPIO_8	111	DI,DO	PD	Y	PD:nppukp
GPIO_83	117	DI,DO	PD	Y	PD:nppukp
GPIO_84	118	DI,DO	PD	Y	PD:nppukp
GPIO_33	222	DI,DO	PD	N	PD:nppukp
GPIO_55	210	DI,DO	PD	Y	PD:nppukp
GPIO_49	226	DI,DO	PD	N	PD:nppukp
GPIO_86	245	DI,DO	PD	N	PD:nppukp
GPIO_147	221	DI,DO	PD	Y	PD:nppukp
GPIO_87	211	DI,DO	PD	Y	PD:nppukp
GPIO_32	213	DI,DO	PD	N	PD:nppukp
GPIO_37	214	DI,DO	PD	Y	PD:nppukp
GPIO_52	249	DI,DO	PD	Y	PD:nppukp

NP: pdpukp = default no-pull with programmable options following the colon (:)

PD: nppukp = default pull-down with programmable options following the colon (:)

PU: nppdkp = default pull-up with programmable options following the colon (:)

KP: nppdpu = default keeper with programmable options following the colon (:)



1. GPIOs marked with "PU" cannot be used for functions such as LCD backlight driver enable control, flash driver enable control, and audio amplifier enable control.
2. All GPIOs must maintain stable levels during system startup.

4 Application Interfaces

4.1 Power Interface

4.1.1 Power Input

The SC162 series module provides three VBAT pins for connection to an external power supply. The input voltage range of the power supply is 3.5 V to 4.4 V and the typical value is 3.8 V. The performance of the power supply such as its load capacity and ripple will directly affect the operating performance and stability of the module. In extreme cases, the instantaneous peak current of the module can reach 4A. If the power supply capacity is insufficient and the power supply voltage instantaneously drops below 3.5 V, the module may be powered off or restarted.

The following figure shows the voltage drop.

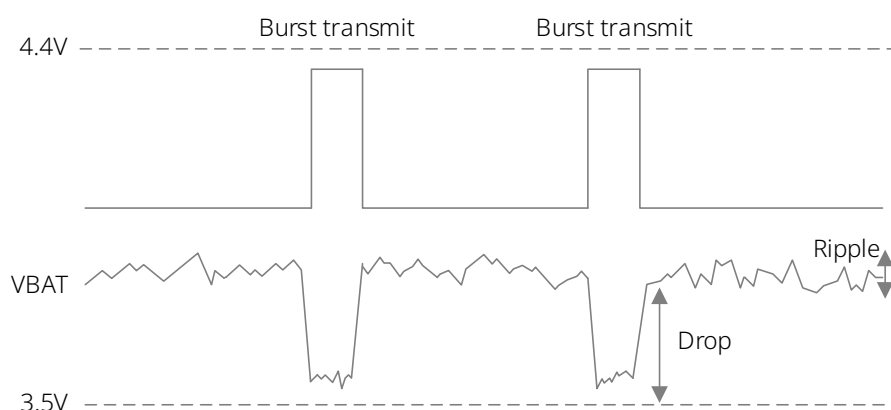


Figure 3. Voltage drop

The external power supply supplies the module by VBAT pins. To ensure that the instantaneous voltage is no less than 3.5 V, it is recommended to connect two 22uF capacitors with filter capacitors of 1uF, 100nF, 39pF, and 33pF in parallel to the VBAT input of the module. Besides, the PCB trace of VBAT should be as short and wide as possible (no narrow than 4 mm) and the ground plane of the power supply part should be as complete as possible. That can reduce the equivalent impedance of the VBAT routing and ensure at maximum transmit power, significant voltage drop will not occur at high currents.

Table 21. Power supply

Parameter	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.4	V



The voltage range of the VBAT power supply must be within the range of 3.5 V to 4.4 V, including superimposed values from ripple, voltage drop, and transient overshoot.

The following figure shows the reference design of the power supply circuit.

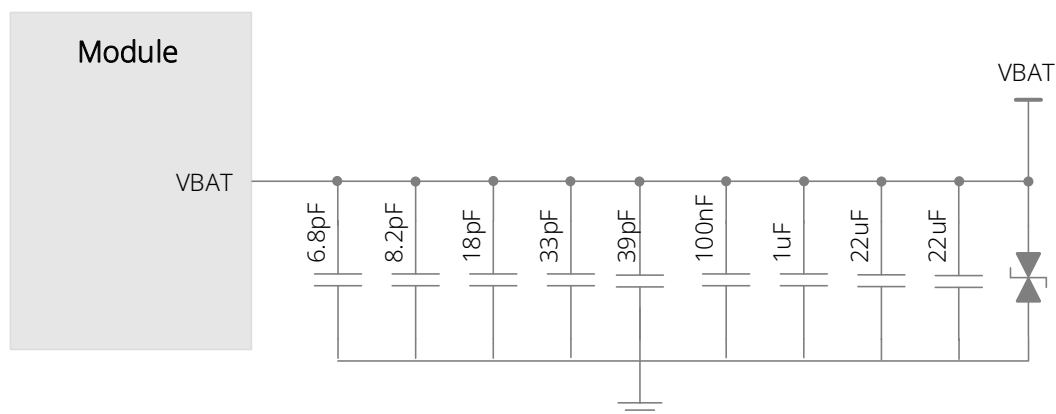


Figure 4. Reference design of power supply circuit

The following table describes the filter capacitor design of the power supply.

Table 22. Filter capacitor design

Recommended Capacitor	Application	Description
22uF x 2	Voltage-stabilizing capacitor	Reduce power fluctuations during module operation.
1uF, 100nF	Filter capacitor	Filter out interference caused by clock and digital signals.
39pF, 33pF, 18pF, 8.2pF, 6.8pF	Decoupling capacitor	Filter out high-frequency interference.

4.1.2 VCOIN

VCOIN is the internal RTC power supply of the module. When the module is not powered by VBAT, the RTC may lose accuracy. It is recommended to update and synchronize the time via the network after the module is powered on. The following table describes the VCOIN parameters.

Table 23. VCOIN parameters

Parameter	Minimum Value	Typical Value	Maximum Value	Unit
VCOIN output voltage	2.0	3.0	3.25	V
VCOIN input voltage	2.0	3.0	3.25	V
VCOIN input current	--	20	--	uA

The VCOIN power supply uses the reference circuit shown in the following figure when powered by an external power source.

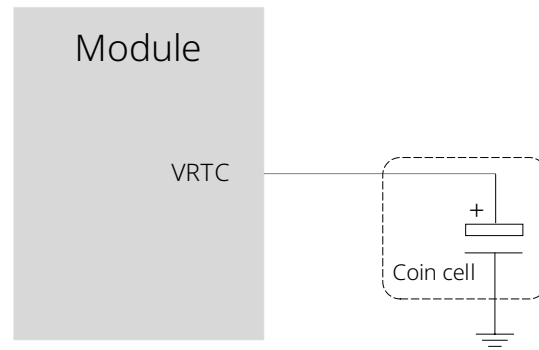


Figure 5. Reference design of VCOIN circuit

4.1.3 Power Output

The module's output power supply can be applied to powering peripheral circuits or other scenarios requiring a power supply.

Table 24. Power output parameters

Pin Name	Default Voltage (V)	Programmable Voltage Range (V)	Drive Current (mA)	Maximum Load Capacitance
VREG_L11A_1P8	1.8	1.504 to 2.000	600	4.7uf
VREG_L14A_1P8	1.8	1.504 to 2.000	600	15uF
VREG_L9E_2P96	3.0	2.7 to 3.544	600	10uF
VREG_L4E_UIM1	1.8/3.0	1.620 to 3.300	150	2.2uf
VREG_L5E_UIM2	1.8/3.0	1.648 to 3.304	150	2.2uf
VREG_L8A_1P8	1.8	1.504 to 3.544	150	2.2uf
VREG_L6A_3P0	3.0	1.504 to 3.544	600	15uF

4.2 Control Interface

4.2.1 Power-on/off

The module supports dual-path power control signals for module power-on/off, reboot, and sleep/wakeup mode switching.

Table 25. Power-on/off pin definition

Pin Name	Pin No.	I/O	Description	DC Feature
KEY_PWR_N	123	DI	This pin can be used for module power-on/off, reboot, and sleep/wakeup mode switching.	Active-low
CBL_PWR_N	165	DI	This pin can be used only for startup.	Active-low

Pin Name	Pin No.	I/O	Description	DC Feature
			Pulling this pin low before power-on can trigger automatic startup.	

4.2.1.1 Power-on

After the module's VBAT pin is powered on, pull low the KEY_PWR_N pin for 2s to 6s to trigger the module to start. The reference designs of key-triggered power-on circuit and OC driver power-on circuit are shown in the following figures.

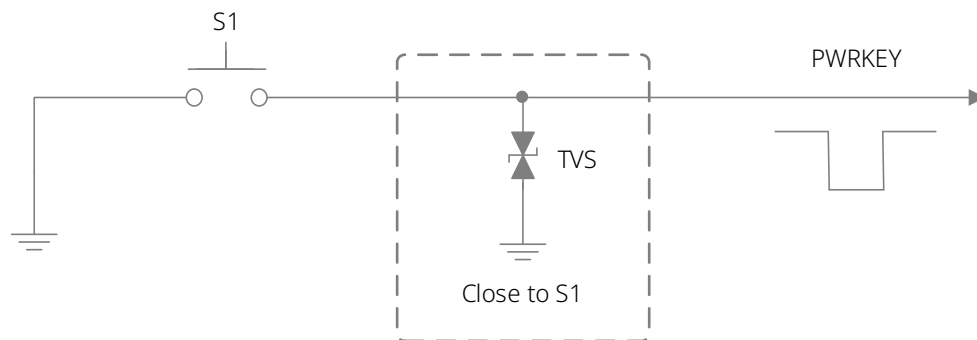


Figure 6. Key-triggered power-on circuit

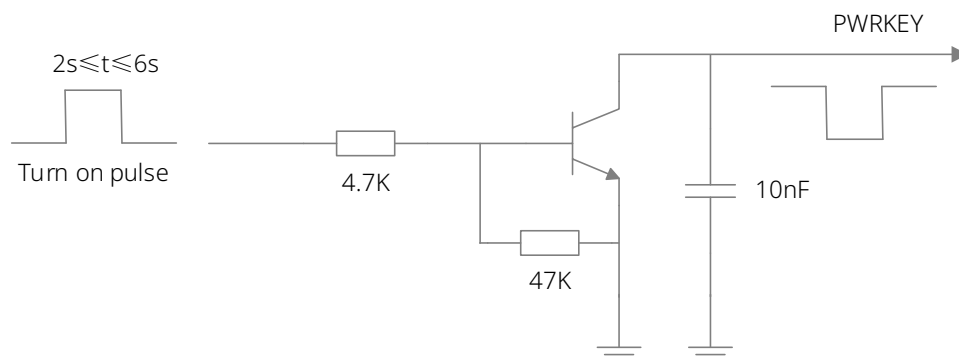


Figure 7. OC driver power-on circuit

The CBL_PWR_N pin is connected to ground through a 1KΩ resistor, enabling automatic module startup upon power application. The following figure shows the reference circuit of automatic startup upon power application.

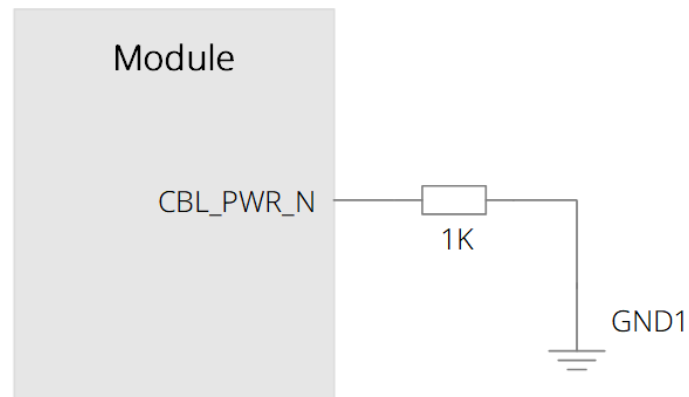


Figure 8. Reference circuit of automatic startup upon power application

Based on startup timing requirements, it is necessary to ensure VBAT power is stable for at least 100ms before KEY_PWR_ON is pulled low to trigger module startup. The following figure shows the startup timing sequence.

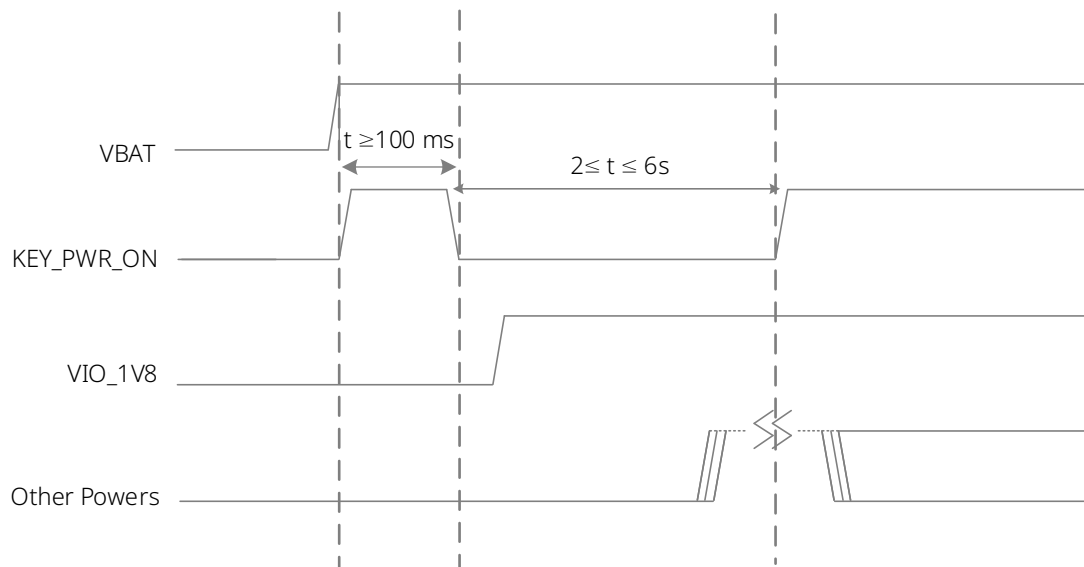


Figure 9. Startup timing sequence



In addition to triggering module startup by pulling low the KEY_PWR_ON pin, pulling low Pin 165 (CBL_PWR_N) can also trigger module startup. This pin is suitable for application scenarios where automatic startup upon power-on is required.

4.2.1.2 Power-off

Normal power-off: When the module is in operating mode, pull low the KEY_PWR_N pin for 0.6s to 6s. A dialog box is displayed, reminding you to power off or restart the module.

4.2.2 Sleep/Wakeup

Sleep: When the module is in standby mode, pull low the KEY_PWR_N pin for 0.1s to 0.5s and then release it. The module will enter sleep mode. The system supports automatic sleep. The time from standby to sleep can be configured through software.

Wakeup: When the module is in sleep mode, pull low the KEY_PWR_N pin for 0.1s to 0.5s and then release it. The module will be woken up.

4.2.3 Volume Control

Pins KEY_VOL_DOWN and KEY_VOL_UP are the volume- key and volume+ key. For the volume key circuit design, you can refer to the power-on circuit design.

4.2.4 Forced Download

The module provides the FORCE_USB_BOOT pin as an emergency download trigger interface. In the booting phase, pulling up FORCE_USB_BOOT to VREG_L18B_1P8 can trigger the module to enter the emergency download mode. This is the final processing mode when the product fails to start or run normally. To facilitate subsequent software upgrade and product debugging, please reserve test points. The following figure shows the FORCE_USB_BOOT reference circuit design.

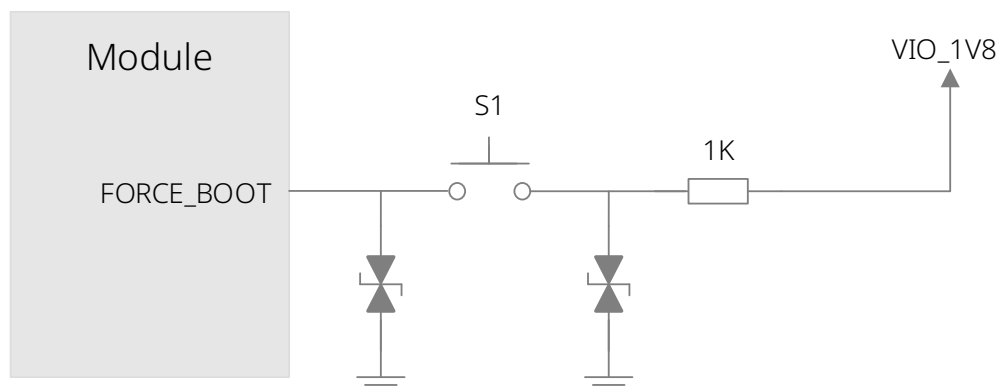


Figure 10. Reference circuit design for forced download

4.3 USB

The module supports one USB 3.1 Gen1 interface and is backward compatible with USB 2.0 interface. Software download is not supported in USB 3.1 Gen1 SS (5 Gbps) mode. The USB 2.0 interface supports the HS (480 Mbps) mode, and is backward compatible with USB 1.1 FS (12 Mbps). It also supports software download, USB OTG function, and HUB expansion. Please refer to the pin description section for pin definition.

The following figures show the reference circuit design of USB interfaces.

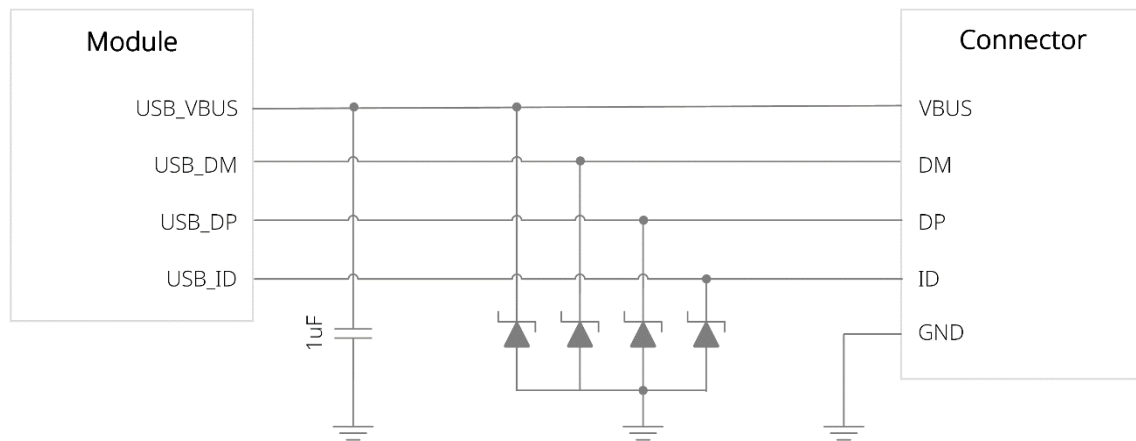


Figure 11. USB 2.0 reference design circuit (without DCDC)

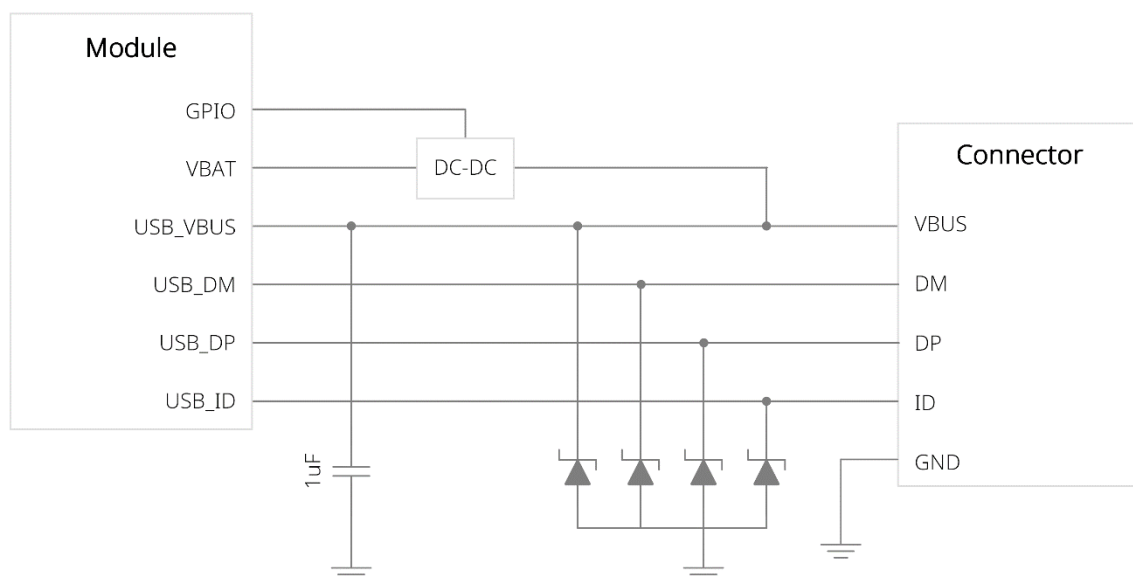


Figure 12. USB 2.0 reference design circuit (with DCDC)

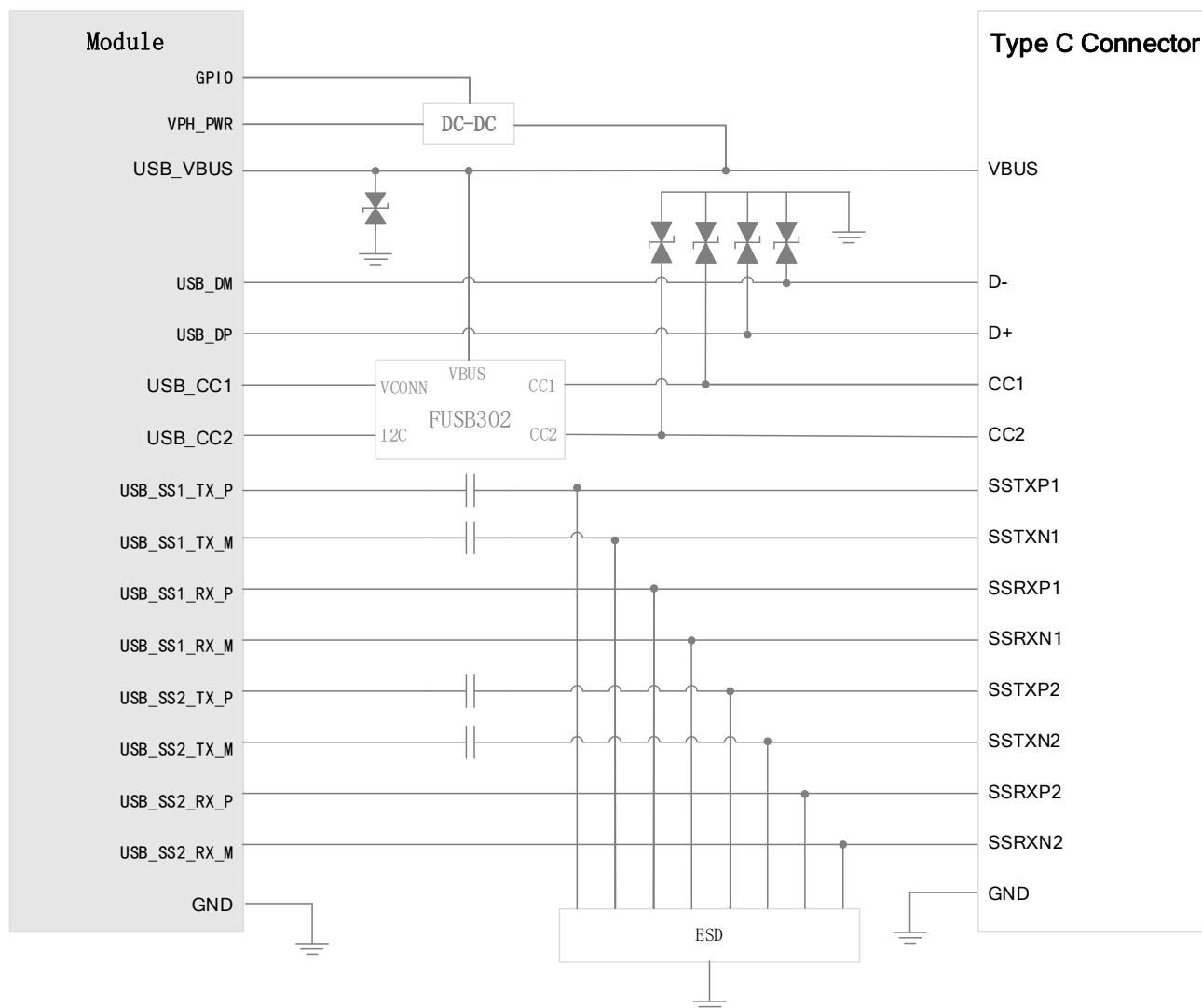


Figure 13. USB 3.1 Type-C reference circuit design (with DCDC)

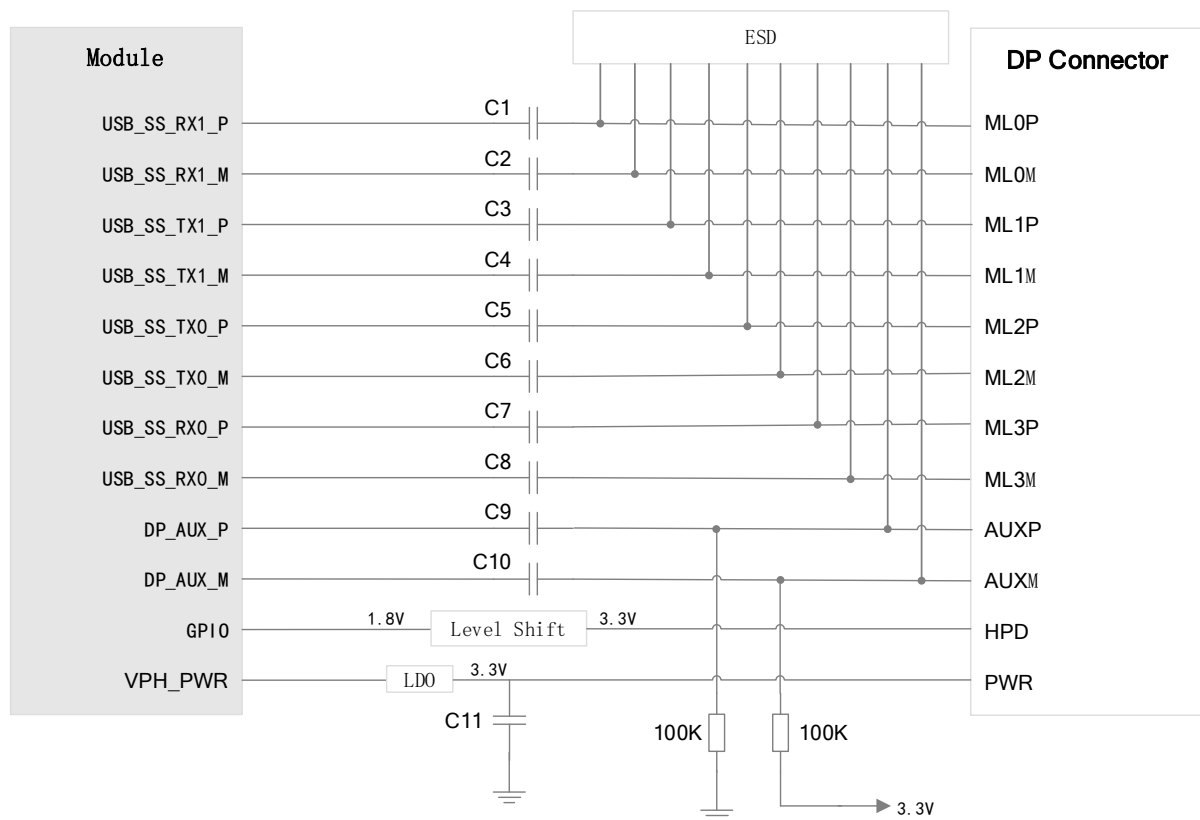


Figure 14. DisplayPort reference circuit design

PCB Design

USB 2.0 design precautions:

- The ESD protector for USB_DP/DM requires a junction capacitance of less than 2pF.
- USB_DP and USB_DM are high-speed differential signal lines. The highest transmission rate is 480 Mbps. Please pay attention to the following requirements during PCB layout:
 - USB_DP and USB_DM signal lines should be equal in length and parallel to avoid right-angle routing. The difference of cabling length must be within 2 mm, and proper 90Ω differential impedance control should be implemented.
 - USB 2.0 differential signal line should be laid on the signal layer nearest to the ground, with proper ground shielding.
- For the reference circuit design DC-DC that supports the OTG function, please use the 5V output.

USB 3.1 design precautions:

- USB 3.1 is a high-speed signal line and requires proper shielding implementation (3D-enclosed differential pair routing) and strict adherence to high-speed differential signaling guidelines.
- USB 3.1 and DP share multiplexed pins. The USB 3.1 lanes can be configured for DisplayPort operation when USB 3.1 functionality is not required.
- The differential impedance must be at $90\Omega \pm 10\%$. The difference of cabling length must be within 0.7 mm.

- The parasitic capacitance of the ESD protector must be less than 0.5 pF.

4.4 SDIO

The module supports one SDIO interface. Please refer to the pin description section for pin definition.

The following figure shows the reference circuit design of SDIO interface.

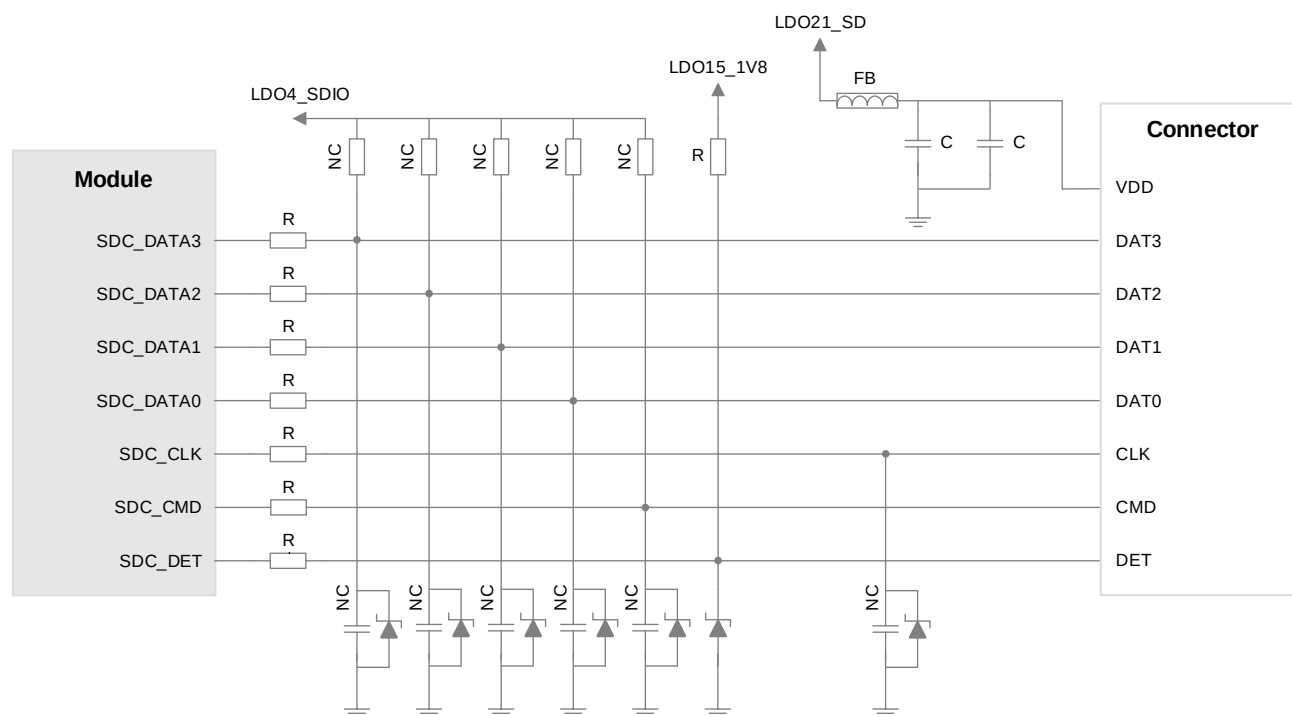


Figure 15. SD card reference circuit

The reference circuit design of SDIO interface must strictly comply with the following requirements:

1. VREG_L9E_2P96 is the SD card driver power supply, can provide about 600mA current, and requires a trace width greater than 0.6 mm.
2. Pull up SD_DET with VREG_L11A_1P8.
3. SDIO is a high-speed digital signal line that requires shielding. All high-speed signal lines must be equal in length, and attention should be paid to their line width.
4. The routing length of the SDIO bus must not exceed 50 mm, and the parallel-connected TVS equivalent capacitance must not exceed 0.5pF.

4.5 (U)SIM

The module supports two sets of (U)SIM card interfaces, featuring dual-card dual-standby with single-call capability, with both interfaces supporting the hot plug function. Please refer to the pin description section for pin definition.

The following figure shows the (U)SIM card reference circuit design.

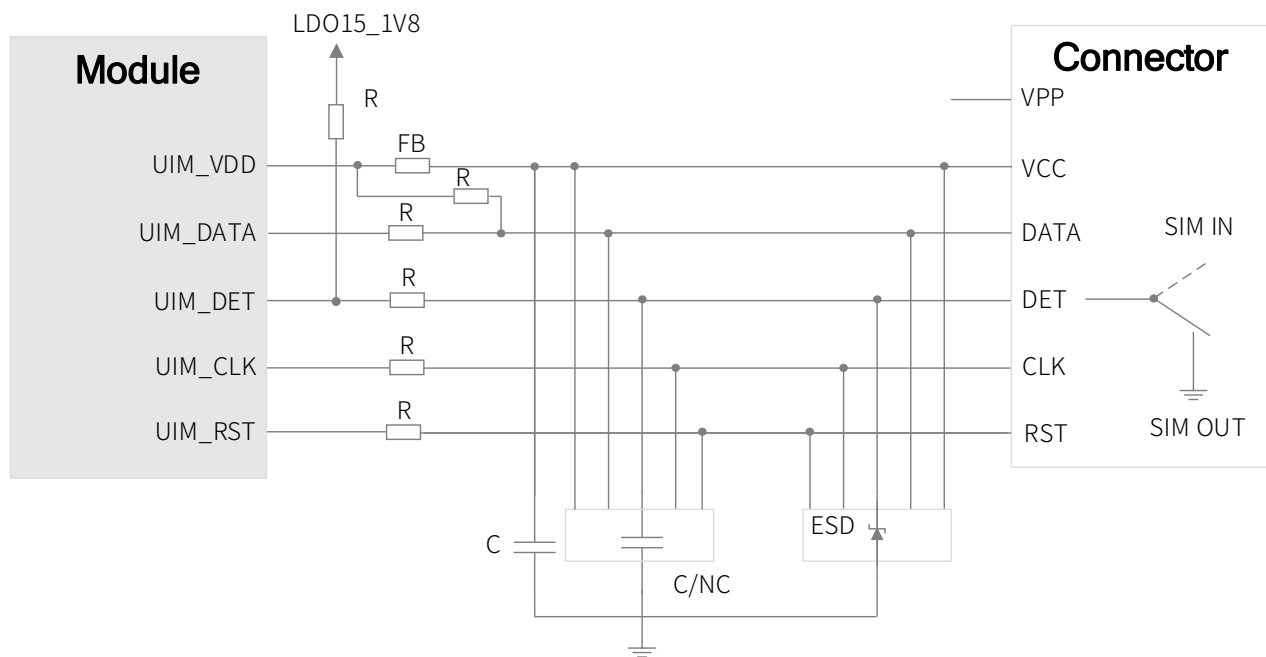


Figure 16. (U)SIM card reference circuit

4.6 LCD

The module supports one 4-lane MIPI_DSI interface. Please refer to the pin description section for pin definition.

The following figure shows the reference circuit.

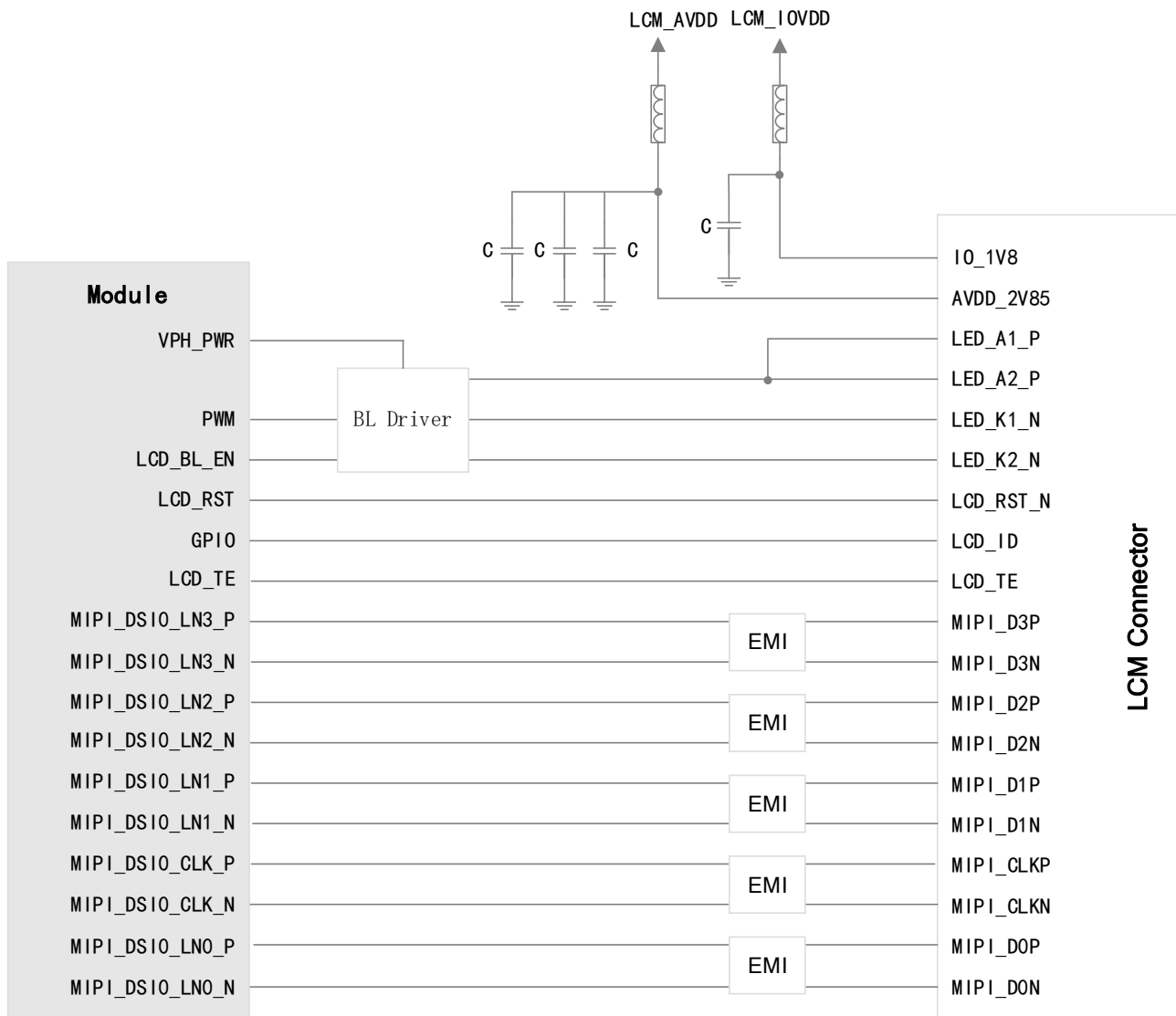


Figure 17. LCD reference circuit

PCB design:

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the electromagnetic interference.
- MIPI routing is recommended to be designed in the inner layer, with 3D shielding.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance $\pm 10\%$.
- The maximum total length of routing shall not exceed 75 mm. The number of via holes cannot exceed 4.
- The intra lane match of differential line must be controlled within 0.5 mm.
- The inter lane match of differential line must be controlled within 2 mm.
- It is recommended that the space of intra-lane differential line should be 1.5 times of the trace width and the space between differential line and other traces should be controlled 3 times of the trace width.
- The total parasitic capacitance of the device on the MIPI differential signal line cannot exceed 1.0pF.

4.7 UART

The module supports three UART interfaces, which are all in the 1.8V power domain. Please refer to the pin description section for pin definition.

The power domain of each serial port is 1.8V. When communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip. The reference circuit design is shown in the following figure.

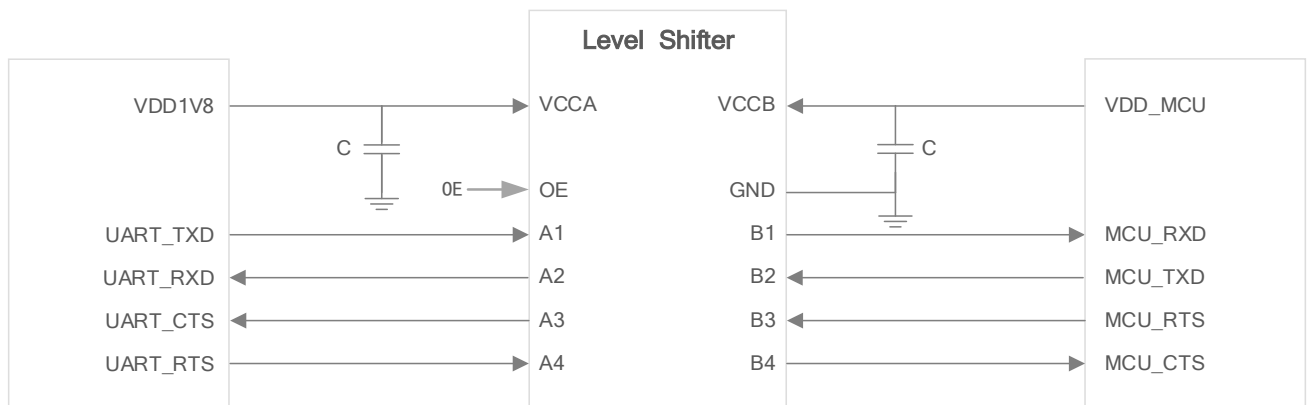


Figure 18. UART reference circuit design

4.8 SPI

The module provides one SPI default interface that only supports master mode. Please refer to the pin description section for pin definition.

The reference schematic of SPI circuit is shown in the following figure.



Figure 19. SPI interface reference circuit

4.9 I2C

The module supports multiple I2C interfaces that only support master mode. The interfaces are respectively used for peripherals such as TP, camera, and sensor. Please refer to the pin description

section for pin definition.



When I2C has more than one peripheral, ensure each peripheral address is unique. When mounting peripherals with high real-time requirements, do not share I2C with other peripherals.

4.10 TP

The module provides one I2C interface that can be used to connect to the TP and it provides power, interrupt, and reset pins required for the TP. Please refer to the pin description section for pin definition.

The following figure shows the TP reference circuit design.

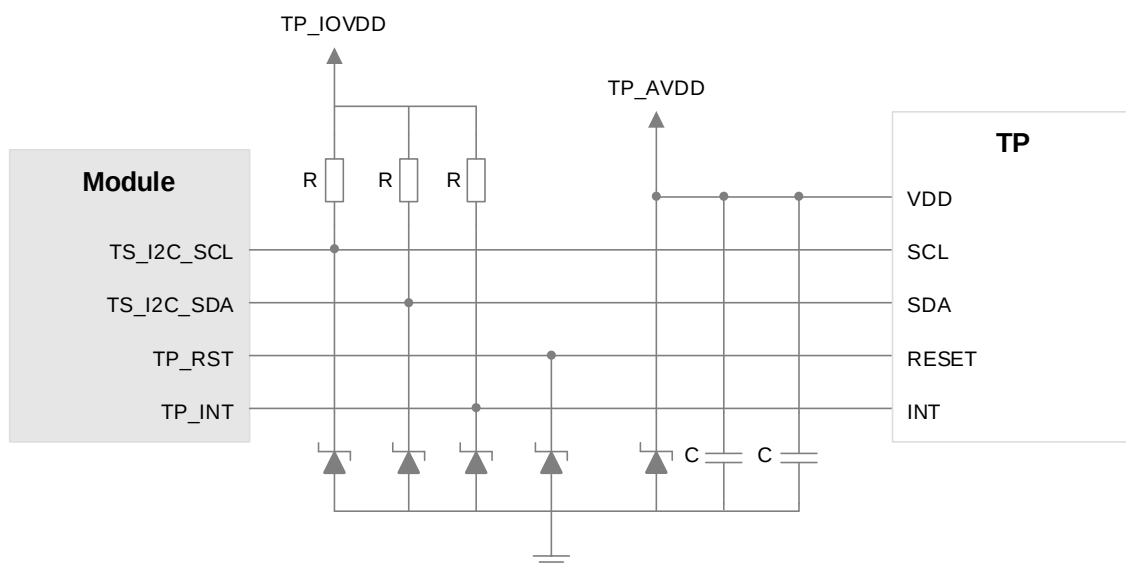


Figure 20. TP reference circuit

4.11 Audio

The module provides two MI2S interfaces and one LPI_I2S interface to connect to external audio codec. Please refer to the pin description section for pin definition.

4.12 Camera

The module supports three sets of 4-lane CSI(4/4/4) D-PHY 1.2 interfaces, with a maximum rate of 2.5 Gbps per lane, and can support a maximum of 32MP. Please refer to the pin description section for camera pin definition.

The following figure shows the 4-lane camera reference circuit design.

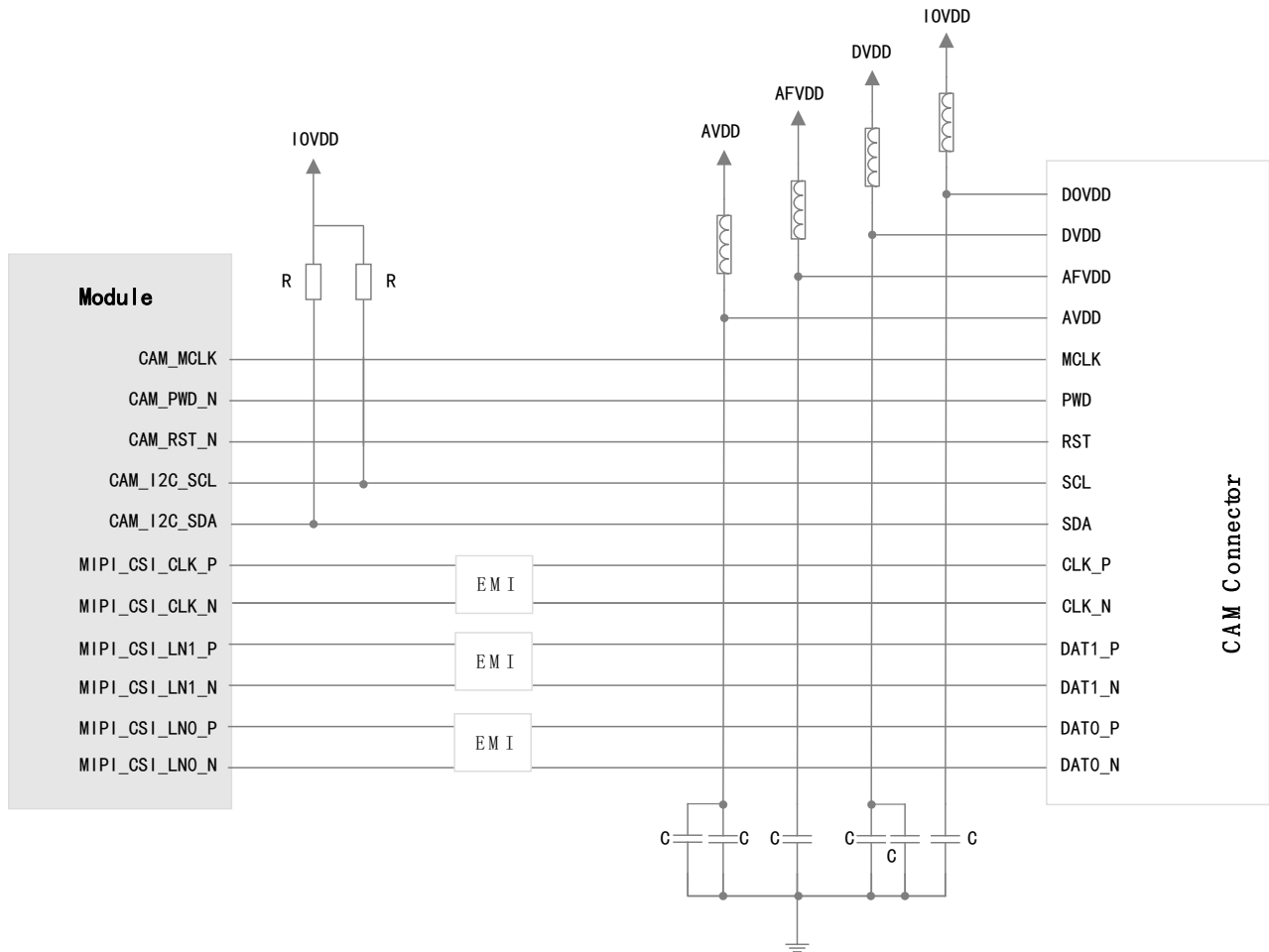


Figure 21. 4-lane camera reference circuit

MIPI is a high-speed signal line. Please pay attention to the following requirements during PCB layout:

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the circuit electromagnetic interference.
- MIPI routing is recommended to be designed in the inner layer, with 3D shielding.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance $\pm 10\%$.
- The maximum total length of routing shall not exceed 75 mm. The number of via holes cannot exceed 4.
- The intra lane match of differential line must be controlled within 0.5 mm.
- The inter lane match of differential line must be controlled within 2 mm.
- It is recommended that the space of intra-lane differential line should be 1.5 times of the trace width and the space between differential line and other traces should be controlled 3 times of the trace width.
- The total parasitic capacitance of the device on the MIPI differential signal line cannot exceed 1.0pF.

Precautions for design of other signal lines:

- CAM_CLK is a high-speed clock signal and requires 3D shielding.
- If two cameras share the I2C, you need to confirm that the I2C addresses of the two cameras do not conflict with each other.
- The analog power supply VDDCAMA routing should be away from interference sources. Otherwise, it is easy to introduce interference of power noise.
- It is recommended to add LDO with high PSRR ability to the camera analog power supply near the camera.

4.13 Sensor

The module supports I2C and interrupt interfaces for communication with various sensors, including accelerometers, ambient light and proximity sensors, and geomagnetic sensors. Please refer to the pin description section for pin definition.



- 1) Use VREG_L11A_1P8 as the pull-high power supply of I2C and interrupt signals.
- 2) The sensor I2C is dedicated to the sensor and cannot be used by other peripherals.

4.14 GPIO

The module provides abundant GPIO ports (1.8V power domain) for general-purpose use. Please refer to the pin description section for pin definition.

4.15 ADC

The module supports two ADC interfaces. Please refer to the pin description section for pin definition.

Pin Name	Pin No.	I/O	Description	Remarks
ADC1_PM6150L	243	AI	General-purpose ADC1 interface	ADC detection, with the voltage input range of 0V to 1.8V.
ADC2_PM6150L	128	AI	General-purpose ADC2 interface	ADC detection, with the voltage input range of 0V to 5V.

5 RF Characteristics

5.1 Antenna Interface

Table 26. Antenna interface

Pin No.	Pin Name	TX	RX	DRX
94	ANT_TRX	WCDMA: 1,5,8 LTE: 1,3,4,5,8,7,8,20,28,38,40,41 NR: 1,3,5,8,7,8,20,28,38,40,41	WCDMA: 1,5,8 LTE: 1,3,5,8,7,8,20,28,38,40,41 NR: 1,3,5,8,7,8,20,28,38,40,41	--
132	ANT_DRX	--	--	LTE: 1,3,5,8,7,8,20,28,38,40,41 NR: 1,3,5,8,7,8,20,28,38,40,41
78	ANT_WIFI/BT	Wi-Fi/BT antenna interface	2.4G/5G/BT	--
120	ANT_GNSS	GNSS antenna interface	GNSS	--

5.2 Operating Frequency

5.2.1 Cellular

Table 27. Operating band for EAU

Mode	Band	Tx (MHz)	Rx (MHz)
WCDMA	Band 1	1920-1980	2110-2170
	Band 5	826-846	871-892
	Band 8	880-915	925-960
LTE FDD	Band 1	1920-1980	2110-2170
	Band 3	1710-1785	1805-1880
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 8	880-915	925-960

Mode	Band	Tx (MHz)	Rx (MHz)
LTE TDD	Band 20	832-862	791-821
	Band 28	703-748	758-803
	Band 38	2570-2620	2570-2620
	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690
NR	N1	1920-1980	2110-2170
	n3	1710-1785	1805-1880
	n5	824-849	869-894
	n7	2500-2570	2620-2690
	n8	880-915	925-960
	n20	832-862	791-821
	n28	703-748	758-803
	n38	2570-2620	2570-2620
	n40	2300-2400	2300-2400
	n41	2496-2690	2496-2690

Table 28. Operating band for NA

Mode	Band	Tx (MHz)	Rx (MHz)
LTE FDD	Band 2	1850-1910	1930-1990
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 12	699-716	729-746
	Band 13	777-787	746-756
	Band 14	788-798	758-768
	Band 17	704-716	734-746
	Band 25	1850-1915	1930-1995
	Band 26	814-849	859-894
	Band 66	1710-1780	2110-2180
	Band 71	663-698	617-652
	Band 41	2496-2690	2496-2690
NR	N2	1850-1910	1930-1990

Mode	Band	Tx (MHz)	Rx (MHz)
	n5	824-849	869-894
	n7	2500-2570	2620-2690
	N12	699-716	729-746
	n25	1850-1915	1930-1995
	N66	1710-1780	2110-2180
	N71	663-698	617-652
	n41	2496-2690	2496-2690

5.2.2 Wi-Fi

The module supports 2.4G and 5G WLAN wireless communication, and supports 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac, and 802.11ax, with a maximum throughput of 866 Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN).
- Support ad hoc mode.
- Support WAPI.
- Support AP mode.
- Support Wi-Fi Direct.
- Support MCS 0-7 for HT20 and HT40.
- Support MCS 0-8 for VHT20.
- Support MCS 0-9 for VHT40 and VHT80.

Test conditions: power supply of 3.8V and environment temperature of 25°C.

Table 29. Wi-Fi transmit power

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1 Mbps	20	17±3
		11 Mbps	20	17±3
	802.11g	6 Mbps	20	16±3
		54 Mbps	20	13±3
	802.11n	MCS0	20	15±3
		MCS7	20	13±3
		MCS0	40	14±3
		MCS7	40	12±3
5G	802.11a	6 Mbps	20	16±3

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
	802.11n	54 Mbps	20	14±3
		MCS0	20	15±3
		MCS7	20	12±3
		MCS0	40	14±3
		MCS7	40	12±3
	802.11ac	MCS0	20	15±3
		MCS8	20	12±3
		MCS0	40	14±3
		MCS9	40	11±3
		MCS0	80	13±3
		MCS9	80	9±3

Table 30. Wi-Fi receiver sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1 Mbps	20	-88
		11 Mbps	20	-83
	802.11g	6 Mbps	20	-88
		54 Mbps	20	-71
	802.11n	MCS0	20	-88
		MCS7	20	-70
		MCS0	40	-85
		MCS7	40	-68
	802.11a	6 Mbps	20	-89
		54 Mbps	20	-74
5G	802.11n	MCS0	20	-89
		MCS7	20	-69
		MCS0	40	-85
		MCS7	40	-65
	802.11ac	MCS0	20	-89
		MCS8	20	-66
		MCS0	40	-86

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
		MCS9	40	-62
		MCS0	80	-82
		MCS9	80	-57

Microstrip line is recommended for RF routing of Wi-Fi antenna. The insertion loss is controlled within 0.2dB, and the impedance is controlled at 50Ω.

Table 31. Wi-Fi operating frequency

Mode	Frequency	Unit
2.4G	2402-2482	MHz
5G	5170-5835	MHz

5.2.3 Bluetooth

The module supports BT5.1 (BR/EDR+BLE) standards. The modulation methods include GFSK, 8-DPSK and $\pi/4$ -DQPSK. The BR/EDR channel bandwidth is 1 MHz and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2 + BR/EDR + BLE.
- Support for ANT protocol.
- Support for BT-WLAN coexistence operation, including optional concurrent reception.
- Up to 3.5 piconets (master, slave, and page scanning).

Table 32. BT rate and version information

Version	Date Rate	Throughput	Remarks
BT1.2	1 Mbit/s	> 80 Kbit/s	--
BT2.0+EDR	3 Mbit/s	> 80 Kbit/s	--
BT3.0+HS	24 Mbit/s	Refer to 3.0+HS.	--
BT4.2 LE	24 Mbit/s	Refer to 4.2 LE.	--
BT5.1	24 Mbit/s	Refer to 5.1 LE.	--

Test conditions: power supply of 3.8V and environment temperature of 25°C.

Table 33. BT performance indicators

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitter	11±2.5	10±2.5	10±2.5	6±3	dBm
Sensitivity	-80	-80	-75	-89	dBm



The sensitivity here is a typical value. Microstrip line is recommended for RF routing of Bluetooth antenna. The insertion loss is controlled within 0.2 dB, and the impedance is controlled at 50Ω.

Table 34. BT operating frequency

Mode	Frequency	Unit
Bluetooth	2402-2480	MHz

5.2.4 GNSS

The module supports multiple positioning systems including GPS, GLONASS and BeiDou. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS.

Test conditions: power supply of 3.8V and environment temperature of 25°C.

Table 35. GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-157	dBm
C/No	-130 dBm	38	dB-Hz
TTFF	Cold start	45	s
	Warm start	40	s
	Hot start	3	s
CEP	Static accuracy (95% @-130 dBm)	3	m

Table 36. GNSS operating band

Mode	Band	Unit
GPS	1575.42±1.023	MHz
	1176.45±10.23	MHz
GLONASS	1597.42-1605.8	MHz
BeiDou	1561.098±2.046	MHz
Galileo	1575.42±2.02	CBOC

5.3 Antenna Performance Requirements

The module provides four antenna interfaces: main, diversity, Wi-Fi/BT, and GNSS. The following table describes antenna requirements.

Table 37. Antenna parameters

Mode	Antenna Requirement
WCDMA/LTE/NR	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization: vertical direction Insertion loss: < 1 dB (0.7GHz to 1GHz) Insertion loss: < 1.5 dB (1.4GHz to 2.2GHz) Insertion loss: < 2 dB (2.3GHz to 2.7GHz)
Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization: vertical direction Insertion loss: < 1 dB
GNSS	Frequency range: 1559MHz-1607MHz; 1166.22MHz-1186.68MHz Polarization: right-hand circular polarization or linear polarization VSWR: < 2 (typical value) Passive antenna gain: > 0 dBi Active antenna NF: < 1.5 dB (typical value) Active antenna gain: > -2 dBi
Isolation between GNSS and main antennas	> 20 dB
Isolation between Wi-Fi and LTE antennas	> 20 dB

5.4 Antenna Circuit Design

5.4.1 Cellular Antenna Design

The following figure shows an antenna circuit for a cellular network.

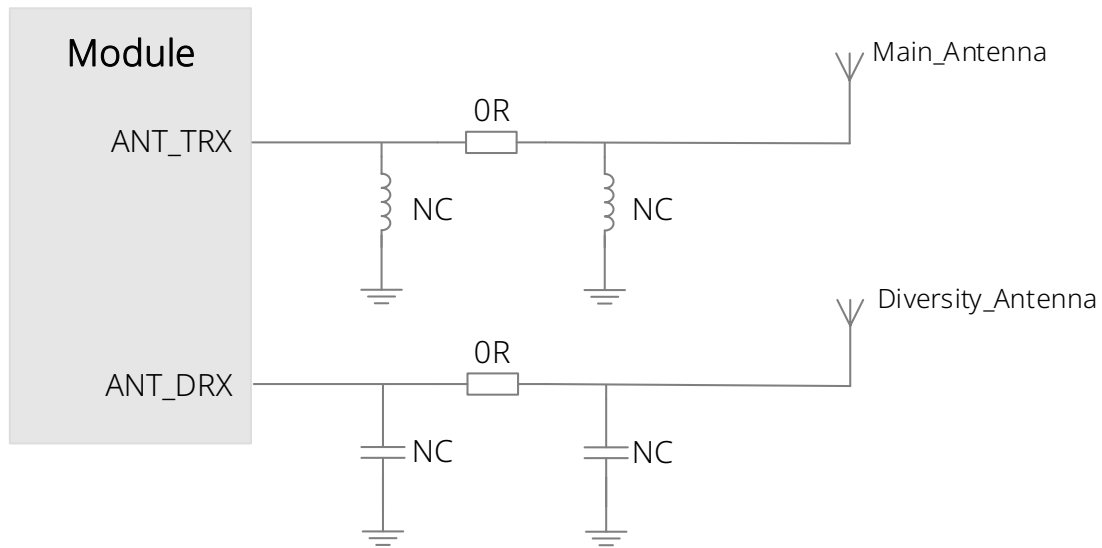


Figure 22. Antenna reference circuit of cellular network

5.4.2 Wi-Fi Antenna Design

The following figure shows a Wi-Fi/BT antenna reference circuit.

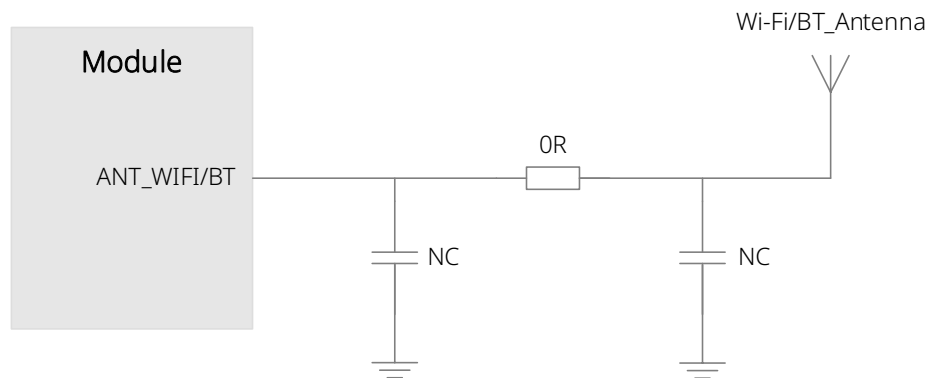


Figure 23. Wi-Fi/BT antenna reference circuit

5.4.3 GNSS Antenna Design

Passive antenna reference design

The module has a built-in LNA. Passive antenna is used in the design of the device. Microstrip line is recommended for RF routing of GNSS. The insertion loss is controlled within 0.2 dB, and the impedance is controlled at 50Ω. The following figure shows the reference circuit.

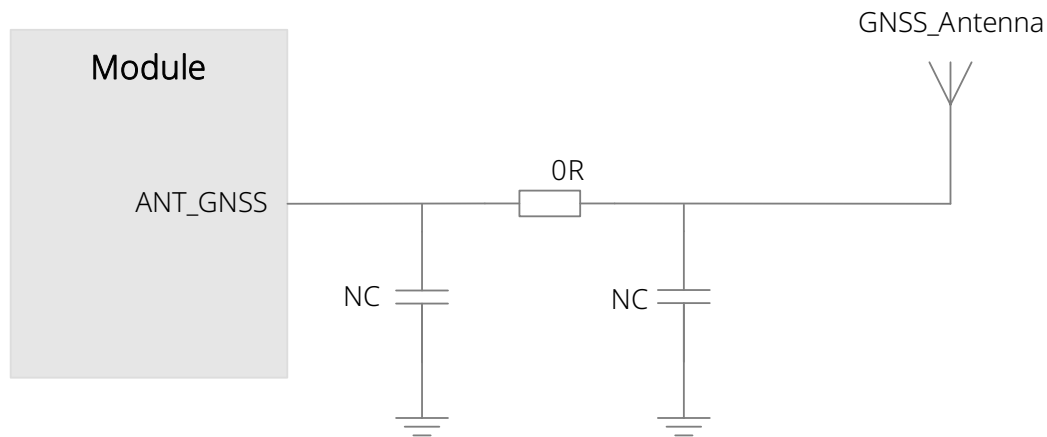


Figure 24. Reference circuit design of GNSS passive antenna

Active antenna reference design

The power supply for active antenna is fed from the antenna's signal line through a 56nH inductor. Common active antennas operate with a 3.3V to 5.0V power supply. The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-performance LDO be used to power the antenna. The active antenna gain should be lower than 17 dB. If the gain is higher than 17 dB, the reserved π -type matcher needs to be used to increase the attenuation network.

The following figure shows the active antenna reference circuit.

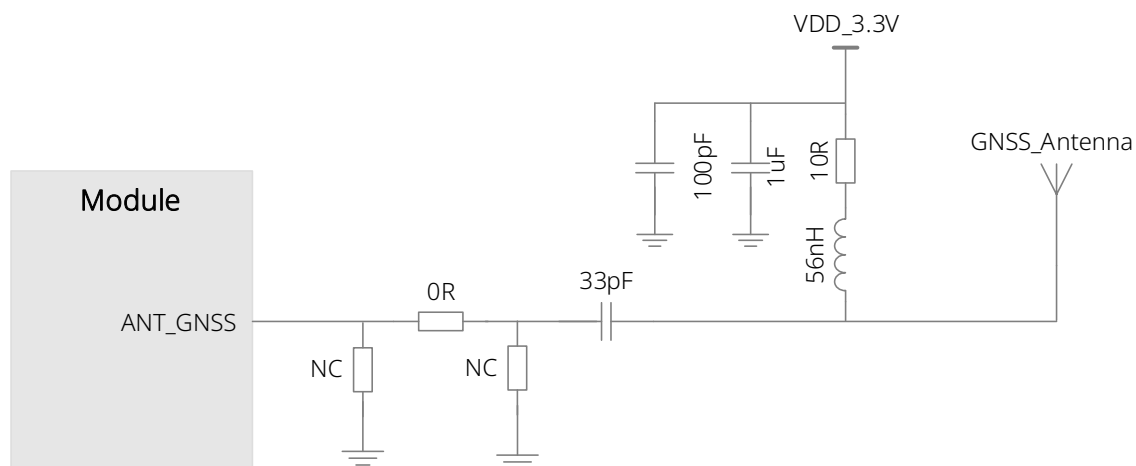


Figure 25. Reference circuit design of GNSS active antenna

5.5 RF Layout Design Guide

For modules that do not have an RF connector, you need to route an RF cable to connect to the antenna feeding point or connector. It is recommended to use a microstrip line for RF routing. The shorter the better. The insertion loss should be controlled within 0.2 dB, and impedance should be controlled at 50Ω.

In general, the impedance of an RF signal line is determined by the dielectric constant of the material,

the trace width (W), the ground clearance (S), and the height of the reference ground plane (H). The control of the characteristic impedance of PCB is usually implemented in two ways: microstrip line and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip line and coplanar waveguide when the impedance line is at 50Ω .

- Complete microstrip line structure

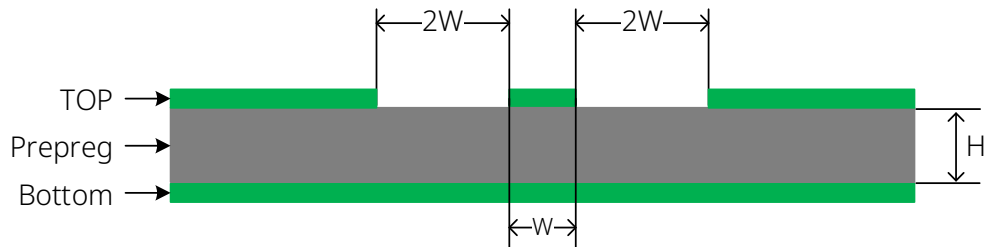


Figure 26. Planar reference model for a two-layer board

- Complete coplanar waveguide structure

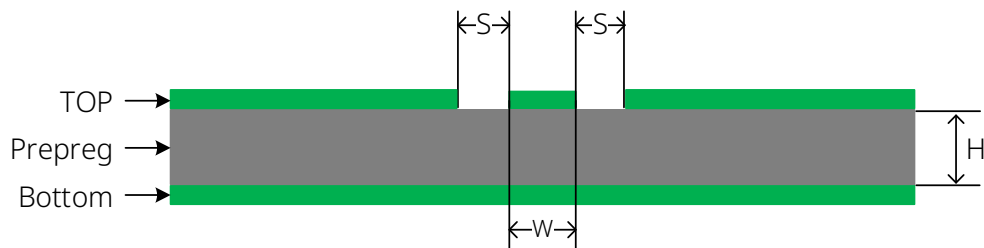


Figure 27. Coplanar impedance model for a two-layer board

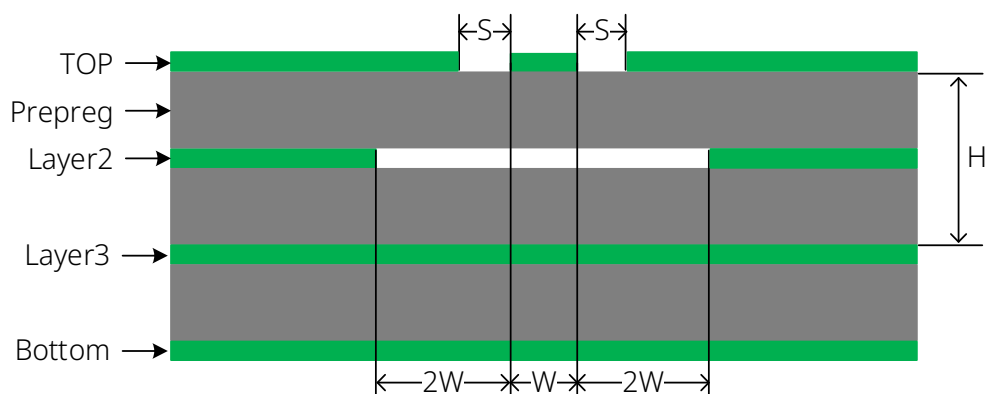


Figure 28. Coplanar impedance model for a four-layer board

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of RF signal, it is recommended to observe the following principles:

- The impedance simulation tool should be used to accurately control the RF signal line at 50Ω

impedance.

- The GND pin adjacent to the RF pin should not have a thermal pad and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, right-angle routing should be avoided. The recommended route angle is 135°.
- When implementing connector packaging, keep the signal pin away from the ground.
- The reference ground plane of the RF signal line should be kept intact. Adding a certain amount of ground holes around the signal line and the reference ground can improve the RF performance. The distance between the ground holes and the signal line should be at least 2 times of the trace width ($2 \times W$).

6 Electrical Characteristics

6.1 Normal Operating Voltage

The following table shows the normal operating voltage range of the module, and all the performance indicators of the module are guaranteed within this operating voltage range.

Table 38. Operating voltage

Power Supply	Minimum Value	Typical Value	Maximum Value	Unit
VBAT	3.5	3.8	4.4	V
VCOIN	2.0	3.0	3.25	V
USB_VBUS	3	5	20	V

6.2 Absolute Maximum Voltage

The basic functions of the module are limited by the absolute maximum/minimum voltage. Do not exceed the absolute voltage ratings related to the module, as this may cause permanent damage. Furthermore, normal operation of the module is not guaranteed even within the absolute maximum/minimum voltage range.

Table 39. Absolute maximum voltage

Power Supply	Minimum Value	Maximum Value	Unit
VBAT	3.0	5.2	V
USB_VBUS	2.3	32	V

6.3 Operating Temperature and Storage Temperature

Table 40. Operating temperature and storage temperature

Item	Minimum Value	Maximum Value	Unit
Operating ambient temperature	-30	75	°C
Storage temperature	-40	85	°C

6.4 Power Consumption

The power consumption measurement is closely related to the operating state of the module. The test conditions are as follows:

The environment temperature is 25°C and the power supply voltage is 3.8V.

Table 41. Operating current for EAU

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage	Power supply, not power on	125	uA
	Software power-off current	By AT command or selecting the power-off menu in LCD	125	uA
$I_{sleep}^{2)}$	Radio off	AT+CFUN=4 Airplane mode (4GB + 64GB)	5	mA
	WCDMA	DRX=8	9.5	mA
	TDD LTE	DPC (Default Paging Cycle) =#256	10.5	mA
	FDD LTE	DPC (Default Paging Cycle) =#256	10.5	mA
	FDD NR	--	TBD	mA
	TDD NR	--	TBD	mA
$I_{WCDMA-RMS}$	WCDMA RMS current	Band1@ max power	660	mA
		Band5@ max power	680	mA
		Band8@ max power	600	mA
$I_{LTE-RMS}$	FDD data RMS current	Band1@max power (10MHz, 1RB)	646	mA
		Band3@max power (10MHz, 1RB)	621	mA
		Band5@max power (10MHz, 1RB)	600	mA
		Band7@max power (10MHz, 1RB)	644	mA
		Band8@max power (10MHz, 1RB)	572	mA
		Band20@max power (10MHz, 1RB)	578	mA
	TDD data RMS current	Band28@max power (10MHz, 1RB)	635	mA
		Band38@max power (10MHz, 1RB)	344	mA
		Band40@max power (10MHz, 1RB)	348	mA
		Band41@max power (10MHz, 1RB)	351	mA
I_{NR-RMS}	FDD data RMS current	N1@max power (10MHz, 15kHz)	750	mA
		N3@max power (10MHz, 15kHz)	730	mA
		N5@max power (10MHz, 15kHz)	670	mA
		N7@max power (10MHz, 15kHz)	750	mA

Parameter	Description	Condition	Typical Result	Unit
		N8@max power (10MHz, 15kHz)	680	mA
		N20@max power (10MHz, 15kHz)	688	mA
		N28@max power (10MHz, 15kHz)	760	mA
		N38@max power (10MHz, 15kHz)	460	mA
	TDD data	N40@max power (10MHz, 15kHz)	450	mA
	RMS current	N41@max power (100MHz, 30kHz)	500	mA

Table 42. Operating current for NA

Parameter	Description	Condition	Typical Result	Unit
I _{off}	Static leakage	Power supply, not power on	125	uA
	Software power off current	By AT command or select the power off menu in LCD	125	uA
I _{sleep} ²⁾	Radio Off	AT+CFUN=4 Airplane mode (4GB+64GB)	5	mA
	WCDMA	DRX=8	9.5	mA
	TDD LTE	DPC (Default Paging Cycle) =#256	10.5	mA
	FDD LTE	DPC (Default Paging Cycle) =#256	10.5	mA
I _{LTE-RMS}	FDD data RMS current	Band2@max power(10MHz, 1RB)	620	mA
		Band4@max power(10MHz, 1RB)	650	mA
		Band5@max power(10MHz, 1RB)	600	mA
		Band7@max power(10MHz, 1RB)	740	mA
		Band12@max power(10MHz, 1RB)	660	mA
		Band13@max power(10MHz, 1RB)	600	mA
		Band14@max power(10MHz, 1RB)	600	mA
		Band17@max power(10MHz, 1RB)	620	mA
		Band25@max power(10MHz, 1RB)	620	mA
		Band26@max power(10MHz, 1RB)	620	mA
		Band66@max power(10MHz, 1RB)	660	mA
		Band71@max power(10MHz, 1RB)	635	mA
	TDD data	Band41@max power(10MHz, 1RB)	351	mA

Parameter	Description	Condition	Typical Result	Unit
I _{NR-RMS}	RMS current			
	FDD data RMS current	N2@max power(10MHz, 15 kHz)	700	mA
		N5@max power(10MHz, 15 kHz)	670	mA
		N7@max power(10MHz, 15 kHz)	750	mA
		N12@max power(10MHz, 15 kHz)	680	mA
		N25@max power(10MHz, 15 kHz)	688	mA
		N66@max power(10MHz, 15 kHz)	700	mA
		N71@max power(10MHz, 15 kHz)	700	mA
	TDD data RMS current	N41@max power(100MHz, 30 kHz)	500	mA



²⁾The data of Isleep is the test result under 4GB LPDDR4X. For every 1GB increase in LPDDR4X capacity on this result, the corresponding data shall be synchronously increased by 1 mA on their respective basis.

6.5 Transmit Power

The following table describes the transmit power of the module on each band.

Test conditions: 3.8V power supply, environment temperature 25°C, LTE maximum power test performed on 10MHz 1RB, and NR maximum power test performed on 10MHz 1RB

Table 43. RF transmit power

Mode	Band	Max Power (dBm)	Min Power (dBm)
WCDMA	Band 1	24	< -57
	Band 5	24	< -57
	Band 8	24	< -57
LTE FDD	Band 1	23	< -42
	Band 2	23	< -42
	Band 3	23	< -42
	Band 4	23	< -42
	Band 5	23	< -42
	Band 7	23	< -42
	Band 8	23	< -42

Mode	Band	Max Power (dBm)	Min Power (dBm)
LTE TDD	Band 12	23	< -42
	Band 13	23	< -42
	Band 14	23	< -42
	Band 17	23	< -42
	Band 20	23	< -42
	Band 25	23	< -42
	Band 26	23	< -42
	Band 28	23	< -42
	Band 66	23	< -42
	Band 71	23	< -42
	Band 38	23	< -42
	Band 40	23	< -42
	Band 41	23	< -42

6.6 Receiver Sensitivity

The following table describes the sensitivity of the module on each band.

Table 44. SC162-EAU RF receiver sensitivity

Mode	Band	PRX	DRX	PRX+DRX	3GPP Requirement	Unit
WCDMA	Band 1	-108	--	--	-106	dBm
	Band 5	-109	--	--	-104.7	dBm
	Band 8	-109	--	--	-103	dBm
LTE FDD	Band 1	-97.5	-96.5	-100	-96.3	dBm
	Band 3	-97.5	-96.5	-100	-93.3	dBm
	Band 5	-99.5	-98.5	-102	-94.3	dBm
	Band 7	-96	-95	-98.5	-93.3	dBm
	Band 8	-99	-98.5	-101.5	-93.3	dBm
	Band 20	-98	-97.5	-100.5	-93.3	dBm
	Band 28	-97	-96	-99.5	-93.3	dBm
LTE TDD	Band 38	-97	-96	-99.5	-96.3	dBm
	Band 40	-97.5	-96.5	-100	-96.3	dBm
	Band 41	-96.5	-95.5	-99	-94.3	dBm
NR FDD	N1	-95	-94	-97.5	-93.1	dBm
	N3	-95	-95	-97.5	-88.2	dBm
	N5	-95.5	-95.5	-98	-90.1	dBm
	N7	-95.5	-97	-98	-91.1	dBm
	N8	-95	-95	-98	-89.3	dBm
	N20	-95	-95.5	-98	-89.1	dBm
	N28	-94	-95	-96.5	-90.1	dBm
NR TDD	N38	-87.5	-87.5	-90	-84.7 +TT	dBm
	N40	-88.5	-88	-91	-84.7 +TT	dBm
	N41	-87	-87.5	-89.5	-84.7 +TT	dBm

Table 45. SC162-NA RF receiver sensitivity

Mode	Band	PRX	DRX	PRX+DRX	3GPP Requirement	Unit
LTE FDD	Band 2	-98	-98	-100	-94.3	dBm
	Band 4	-97.5	-98	-100	-96.3	dBm
	Band 5	-99	-99	-102	-94.3	dBm
	Band 7	-97	-97	-99	-93.3	dBm
	Band 12	-98	-99	-101	-93.3	dBm

Mode	Band	PRX	DRX	PRX+DRX	3GPP Requirement	Unit
	Band 13	-98	-99	-102	-93.3	dBm
	Band 14	-98	-99	-101	-93.3	dBm
	Band 17	-98	-99	-101	-93.3	dBm
	Band 25	-98	-97.5	-100	-94.3	dBm
	Band 26	-98	-97.5	-101	-93.8	dBm
	Band 66	-97.5	-97.5	-100	-95.8	dBm
	Band 71	-97.5	-96	-101	-93.5	dBm
LTE TDD	Band 41	-96.3	-96.5	-99	-94.3	dBm



1. LTE receiver sensitivity is measured in DL 10MHz Full RB.

receiver sensitivity is measured in DL 100MHz SCS=30kHz Full RB.

6.7 Electrostatic Protection

In the application of the module, static electricity generated by human bodies and static electricity generated by friction between micro-electronics may be discharged to the module through various channels and cause damage to the module. Therefore, ESD protection should be emphasized. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken.

For example, ESD protection should be performed at the designed circuit interfaces and at the points susceptible to damage or impact from electrostatic discharge. Anti-static gloves should be worn during production.

Test conditions: temperature of 25°C and humidity of 45% to 60%

Table 46. ESD protection level

Location	Air Discharge	Contact Discharge
VBAT, GND	±10KV	±5KV
Antenna interface	±10KV	±5KV



1. The data is tested based on Fibocom development board.
2. ESD performance is strongly related to PCB design. Pay special attention to the protection of key control signals.
3. When designing the whole device, the GND should maintain integrity and connectivity.

6.8 Reliability

Fibocom's reliability tests are conducted on an industrial scale. For details about reliability test results, see the corresponding reliability test report.

6.9 Thermal Design

For more thermal design guidance, see *Fibocom_Module General Thermal Design Guide*.

7 Structure Specifications

7.1 Product Appearance



Figure 29. Product appearance

7.2 Structural Dimensions

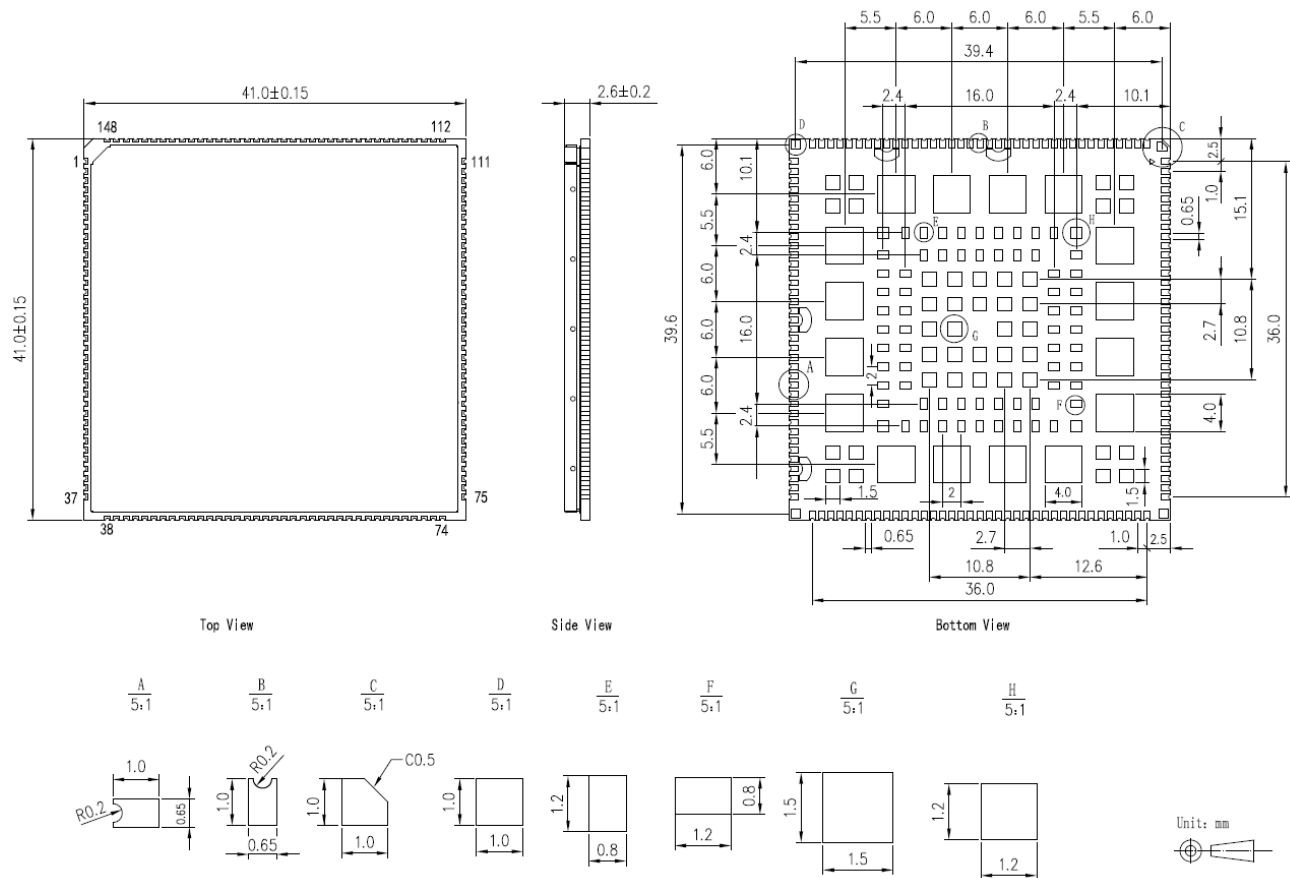


Figure 30. Structure dimensions (unit: mm)

7.3 PCB Package

Users can design the PCB package by themselves. Fibocom also provides a design document *Fibocom_SC162_PACKAGE* for users, which can be found in the product package.

8 Storage, Production and Packaging

8.1 Storage, Production and Packaging

For details about storage, production, and packaging, see *Fibocom_SC162_SMT Design Guide*.

Appendix A Reference Documents

Category	Document Name
Reference design	Fibocom_SC162_PACKAGE
	Fibocom_SC162_Reference Design
Development kit	Fibocom_SC162_ADP User Guide
	Fibocom_EVKB-SOC_User Guide
User guide	Fibocom_Design Guide_RF Antenna
	Fibocom_SC162_SMT Design Guide
	Fibocom_Module General Thermal Design Guide

Appendix B Acronyms and Abbreviations

Acronym and Abbreviation	Full Name
AR	Augmented Reality
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Downlink
DLCA	Downlink Carrier Aggregation
ECC	Envelope Correlation Coefficient
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	multiple-input and multiple-output
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying

Acronym and Abbreviation	Full Name
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VSWR	Voltage Standing Wave Ratio
VR	Virtual Reality
WCDMA	Wideband Code Division Multiple Access