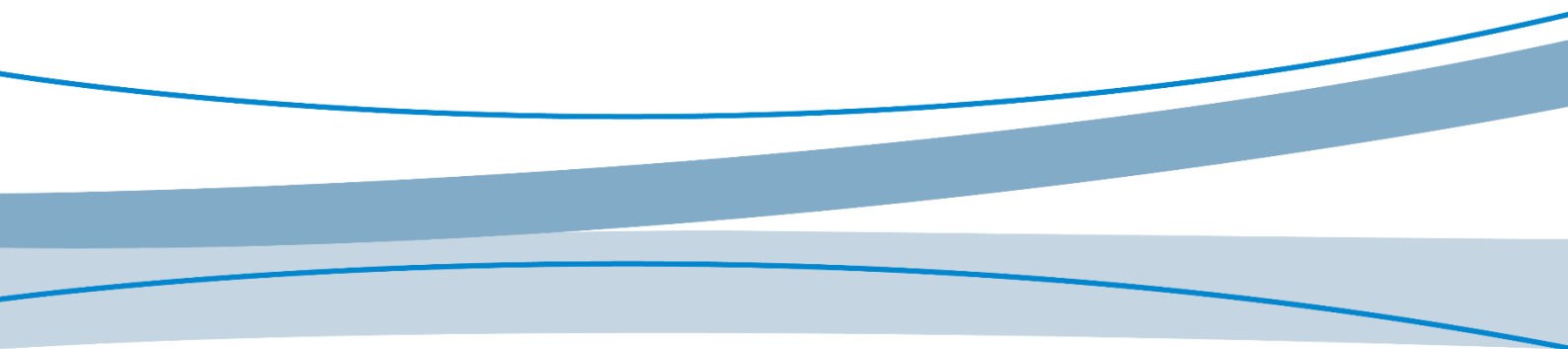




SC206

Hardware Guide

V1.0



FCC Regulatory Compliance

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are compliant with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom wires Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

The antenna is external detachable antenna ; It needs to be connected to the device via RF cable.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: ZMO SC206NA".

The FCC ID can be used only when all FCC compliance requirements are met.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part 27, part 90 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISSED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions:

(For module device use) 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and 2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module) 1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considérée comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC:21374-SC206NA".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 21374-SC206NA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module. Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

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signal strength.

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Applicable Model

No.	Applicable Model	Description
1	SC206-NA-46	4GB + 64GB memory, suitable for the North American region.

Change History

V1.0 (2025-04-21)	Updated weight data. Updated power consumption data. Update the working voltage of VBUS_USB_DET.
V0.1 (2025-03-21)	Draft

1 Foreword

1.1 Description

This document describes information on electrical characteristics, RF performance, structural dimensions, and application environment of the SC206 module. With the help of this document and other related documents, the application developer can quickly understand the hardware functions of the SC206 module and develop the hardware of the product.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1 Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V15.0.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11n, IEEE Std 802.11ac, IEEE Std 802.11ax;
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 +HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.2.0, December 7, 2014
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07, 2017
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.1.1, August 07, 2019
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.2
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment -Data Circuit terminating Equipment (DTE -

DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

- PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB
- Universal Serial Bus Specification 2.0
- Universal Serial Bus Specification 3.0

2 Product Overview

2.1 Product Introduction

SC206 is packaged in LCC+LGA, which is a highly integrated 4G wireless communication module and supports GSM/WCDMA/LTE-FDD/LTE-TDD network modes. The module can provide stable and high-speed data transmission services, suitable for most mobile operator networks around the world, and can be used in CPE, VR/AR, gateways, TV boxes, intelligent monitoring, intelligent POS, and other applications.

Table 1. Band introduction

System	Band Configuration
FDD-LTE	Band2/4/5/7/12/13/17/25/26/66/71
TDD-LTE	Band41 (2496-2690MHz)
WIFI 802.11a/b/g/n/ac	2402-2482MHz; 5170-5835MHz
BT5.0	2402-2480 MHz
GNSS	GPS/BeiDou/GLONASS/Galileo/QZSS

2.2 Key Features

Table 2. Key features

Category	Function Description	Item
Power supply	DC: 3.5V–4.4V, typical voltage: 3.8V	SC206 series
Storage configuration	4GB LPDDR4X+64GB UFS	SC206-NA-46
Function interface	Audio interface: Analog input x 3; Analog output x 3	SC206 series
	USB ports: 1 set of USB ports. The USB ports comply with the USB 3.1 Gen 1 standard and are backward compatible with USB 2.0. They can be used for data transfer, software debugging, etc.	SC206 series
	Display interface: 1 set of 4-Lane MIPI DSI D-PHY 1.2 interface	SC206 series
	Camera interface: 2 sets of 4-Lane MIPI CSI D-PHY 1.2 interfaces, with a maximum data rate of 2.5Gbps per lane, can be configured as 4+4 or 4+2+1.	SC206 series
	SIM interface: Two groups of SIM card interfaces, dual card dual standby, 1.8V and 3V adaptation, supports hot plug detection	SC206 series
	UART interface: 1 set of dedicated debugging UART 1 set of 2-wire UART	SC206 series
	SD interface: Supports 4-bit SD3.0, supports 1.8V/3V SD card, supports hot plug detection	SC206 series
	ADC interface: 2 universal ADC	SC206 series
	I2C interface: 5 sets of I2C interfaces, suitable for peripherals such as touch screens, cameras, sensors	SC206 series
	Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands	SC206 series
LTE features	Support 3GPP R10 UL supports QPSK and 16QAM modulations DL supports QPSK, 16QAM, and 64QAM modulations	SC206 series

Category	Function Description	Item
	DL supports up to 2 x 2 MIMO. FDD-LTE: Maximum uplink rate 50Mbps, maximum downlink rate 150 Mbps TDD-LTE: Maximum uplink rate 30Mbps, maximum downlink rate 130 Mbps	
GSM features	GPS/BeiDou/GLONASS/Galileo/QZSS	SC206 series
WLAN	Supports 2.4G, 5G WLAN wireless communication, supports 802.11a/b/g/n/ac	SC206 series
BT	BT5.0	SC206 series
Physical features	Dimensions: (40.5±0.15) mm x (40.5±0.15) mm x (2.75±0.2) mm Package: LCC+LGA Weight: about 9.7 g	SC206 series
Temperature features	Operating temperature: -30°C to +75°C, which meets the requirements of 3GPP standard Storage temperature: -40°C to +85°C	SC206 series
Software upgrade	Through USB/SD/FOTA	SC206 series
Environmental compliance	RoHS compliant, halogen free	SC206 series

2.3 Hardware Block Diagram

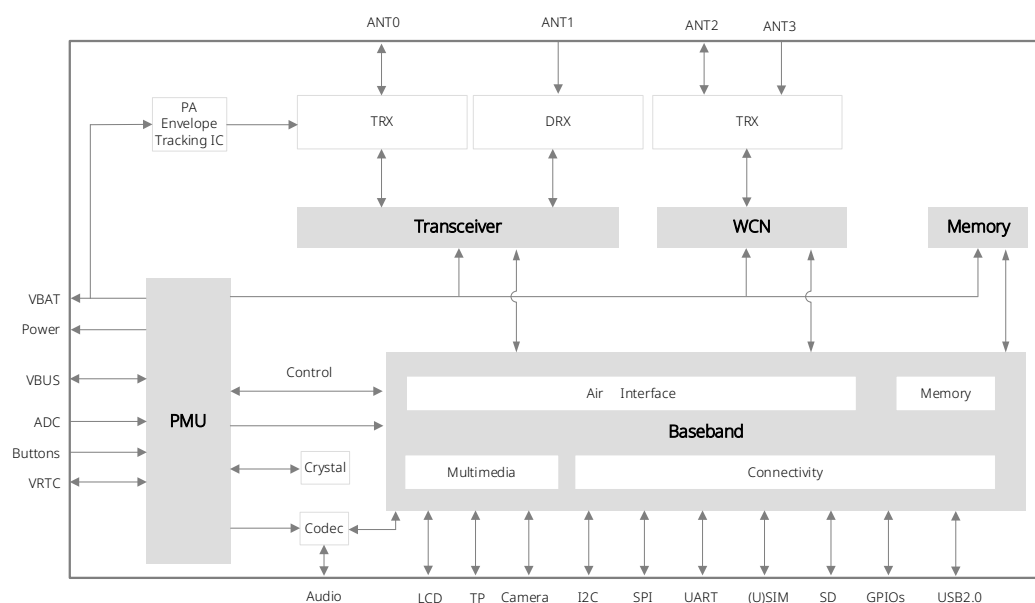


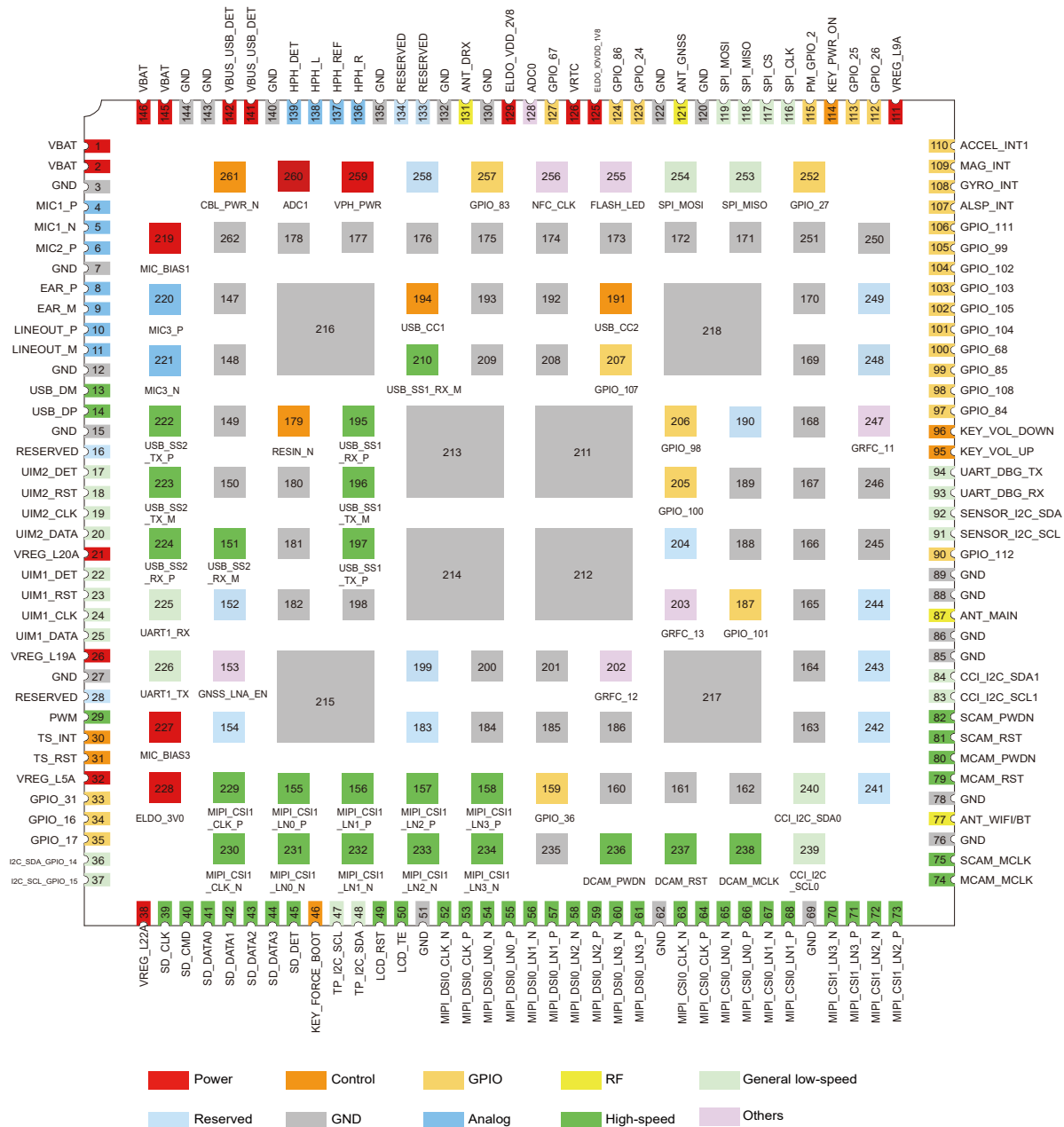
Figure 1. Hardware block diagram

Fibocom configures a complete development board kit for the module, which makes it convenient for users to quickly understand the module performance. Refer to *Fibocom_SC206_ADP User Guide* and *Fibocom_EVKB-SOC_User Guide* for the usage of development board.

3 Pin Definition

3.1 Pin Distribution

SC206 series modules are in LCC+LGA package, with a total of 262 pins. The following figure is a TOP perspective view.



3.2 Pin Description

Table 3. I/O type definition

Type	Description	Type	Description
PI	Power input	AIO	Analog input and output
PO	Power output	OD	Open drain
DI	Digital input	PU	Pull-up high level
DO	Digital output	PD	Pull-down low level
DIO	Digital input and output	T	Tristate, that is, high resistance state, which is determined by the peripheral circuit
AI	Analog input	G	Ground
AO	Analog output	--	--

Table 4. Power interfaces

Pin	Pin Name	I/O	Reset Value ¹	Pin Description	DC Feature
1,2, 145, 146	VBAT	PI	--	Module baseband power	3.5-4.4V
126	VRTC	PI/PO	--	Real-time clock power	3V
129	ELDO_VDD_2V8	PO	--	Camera analog power	2.8V, enabled by PMGPIO_5
111	VREG_L9A	PO	--	1.8V output power	1.8V
259	VPH_PWR	PO	--	General peripheral power output (internally connected to VBAT)	3.5-4.4V
21	VREG_L20A	PO	--	(U)SIM2 card power supply	1.8V/3V
26	VREG_L19A	PO	--	(U)SIM1 card power supply	1.8V/3V
125	ELDO_IOVDD_1V8	PO	--	Camera IO power	1.8V, enabled by GPIO_58
228	ELDO_3V0	PO	--	3.0V output power	3.0V, enabled by GPIO_54
32	VREG_L5A	PO	--	SD card signal pull-up power	1.8V/2.96V
38	VREG_L22A	PO	--	SD card power output	2.96V

Table 5. Ground interfaces

Pin	Pin Name	I/O	Reset Value ¹	Pin Description	DC Feature
3,7,12,15,27,51,62,69,76,78,85,86,88,89,120,122,130,132,135,140,143,144,147,148,149,150,160,161,162,163,164,165,166,167,168,169,170,171,172,173,174,175,176,177,178,180,181,182,184,185,186,188,189,192,193,198,200,201,208,209,211,212,213,214,215,216,217,218,235,245,246,250,251,262					GND

Table 6. Control interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
46	KEY_FORCE_BOOT	DI	PD	USB forced download	1.8V
95	KEY_VOL_UP	DI	PU	Volume+	1.8V
96	KEY_VOL_DOWN	DI	PU	Volume-	1.8V
114	KEY_PWR_ON	DI	PU	Power-on/off	1.1V
179	RESET_N	DI	PU	Soft reset	1.8V
261	CBL_PWR_N	DI	PU	Grounding triggers automatic startup	1.1V

Table 7. USIM interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
25	USIM1_DATA	DI/DO	--	USIM1 data	1.8V/3V
24	USIM1_CLK	DO	--	USIM1 clock	1.8V/3V
23	USIM1_RST	DO	--	USIM1 reset	1.8V/3V
22	USIM1_DET	DI	--	USIM1 hot-plug detection	1.8V
20	USIM2_DATA	DI/DO	--	USIM2 data	1.8V/3V
19	USIM2_CLK	DO	--	USIM2 clock	1.8V/3V
18	USIM2_RST	DO	--	USIM2 reset	1.8V/3V
17	USIM2_DET	DI	--	USIM2 hot-plug detection	1.8V

Table 8. SDIO interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
45	SD_DET	DI	--	SD card plug and unplug detection	1.8V
44	SD_DATA3	DI/DO	--	SDIO DATA3	1.8V/2.96V
43	SD_DATA2	DI/DO	--	SDIO DATA2	1.8V/2.96V

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
42	SD_DATA1	DI/DO	--	SDIO DATA1	1.8V/2.96V
41	SD_DATA0	DI/DO	--	SDIO DATA0	1.8V/2.96V
40	SD_CMD	DI/DO	--	SD card command	1.8V/2.96V
39	SD_CLK	DO	--	SD card clock	1.8V/2.96V

Table 9. I2C interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
91	SENSOR_I2C_SCL	DO	PD	Sensor I2C clock	1.8V
92	SENSOR_I2C_SDA	DI/DO	PD	Sensor I2C data	1.8V
36	I2C_SDA_GPIO_14	DI/DO	PU	CC logic I2C data	1.8V
37	I2C_SCL_GPIO_15	DO	PU	CC logic I2C clock	1.8V
83	CCI_I2C_SCL1	DO	PU	Camera I2C1 clock	1.8V
84	CCI_I2C_SDA1	DI/DO	PU	Camera I2C1 data	1.8V
239	CCI_I2C_SCL0	DO	PD	Camera I2C0clock	1.8V
240	CCI_I2C_SDA0	DI/DO	PD	Camera I2C0data	1.8V
47	TP_I2C_SCL	DO	PD	CTP I2C clock	1.8V
48,183	TP_I2C_SDA	DI/DO	PD	CTP I2C data	1.8V

Table 10. USB interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
141,142	VBUS_USB_DET	DI	--	VBUS input detection	--
13	USB_DM	AI/AO	--	USB 2.0 differential data signal (-)	--
14	USB_DP	AI/AO	--	USB 2.0 differential data signal (+)	--
210	USB_SS1_RX_M	AI	--	USB 3.1 differential data receive (-)	--
195	USB_SS1_RX_P	AI	--	USB 3.1 differential data receive (+)	--
196	USB_SS1_TX_M	AO	--	USB 3.1 differential data send (-)	--
197	USB_SS1_TX_P	AO	--	USB 3.1 differential data send (+)	--
151	USB_SS2_RX_M	AI	--	USB 3.1 differential data receive (-)	--
224	USB_SS2_RX_P	AI	--	USB 3.1 differential data receive (+)	--
223	USB_SS2_TX_M	AO	--	USB 3.1 differential data send (-)	--
222	USB_SS2_TX_P	AO	--	USB 3.1 differential data send (+)	--

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
194	USB_CC1	AI/AO	--	USB_CC1	--
191	USB_CC2	AI/AO	--	USB_CC2	--

Table 11. UART interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
93	DBG_UART_RX	DI	PD	Debug UART receive	1.8V
94	DBG_UART_TX	DO	PD	Debug UART send	1.8V
225	UART1RX	DI	PD	UART1 receive	1.8V
226	UART1TX	DO	PU	UART1 send	1.8V

Table 12. SPI interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
116	SPI_CLK	DI	PD	SPI clock	1.8V
117	SPI_CS	DO	PD	SPI chip select	1.8V
118,253	SPI_MISO	DI	PD	SPI master in slave out	1.8V
119,254	SPI_MOSI	DO	PD	SPI master out slave in	1.8V

Table 13. ADC interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
128	ADC0	AI	--	Analog-to-digital input port	1.8V
260	ADC1	AI	--	Analog-to-digital input port	1.8V

Table 14. LCD interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
29	PWM	DO	PD	PWM output	1.8V/VPH
49	LCD_RST	DO	PD	LCD rest	1.8V
50	LCD_TE	DI	PD	LCD tearing effect	1.8V
52	MIPI_DSI0_CLK_N	AO	--	LCD MIPI clock (-)	--
53	MIPI_DSI0_CLK_P	AO	--	LCD MIPI clock (+)	--
54	MIPI_DSI0_LN0_N	AO	--	LCD MIPI data0 (-)	--
55	MIPI_DSI0_LN0_P	AO	--	LCD MIPI data0 (+)	--
56	MIPI_DSI0_LN1_N	AO	--	LCD MIPI data1 (-)	--

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
57	MIPI_DSI0_LN1_P	AO	--	LCD MIPI data1 (+)	--
58	MIPI_DSI0_LN2_N	AO	--	LCD MIPI data2 (-)	--
59	MIPI_DSI0_LN2_P	AO	--	LCD MIPI data2 (+)	--
60	MIPI_DSI0_LN3_N	AO	--	LCD MIPI data3 (-)	--
61	MIPI_DSI0_LN3_P	AO	--	LCD MIPI data3 (+)	--

Table 15. CTP interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
30	TP_INT	DI	PD	CTP interrupt	1.8V
31	TP_RST	DO	PD	CTP rest	1.8V

Table 16. Camera interface

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
80	MCAM_PWDN	DO	PD	MCAM PWDN	1.8V
79	MCAM_RST	DO	PD	MCAM reset	1.8V
74	MCAM_MCLK	DO	PD	MCAM clock	1.8V
230	MIPI_CSI1_CLK_N	AI	--	MIPI CSI1 clock 0 (-)	--
229	MIPI_CSI1_CLK_P	AI	--	MIPI CSI1 clock 0 (+)	--
231	MIPI_CSI1_LN0_N	AI	--	MIPI CSI1 data 0 (-)	--
155	MIPI_CSI1_LN0_P	AI	--	MIPI CSI1 data 0 (+)	--
232	MIPI_CSI1_LN1_N	AI	--	MIPI CSI1 data 1 (-)	--
156	MIPI_CSI1_LN1_P	AI	--	MIPI CSI1 data 1 (+)	--
233	MIPI_CSI1_LN2_N	AI	--	MIPI CSI1 data 2 (-)	--
157	MIPI_CSI1_LN2_P	AI	--	MIPI CSI1 data 2 (+)	--
234	MIPI_CSI1_LN3_N	AI	--	MIPI CSI1 data 3 (-)	--
158	MIPI_CSI1_LN3_P	AI	--	MIPI CSI1 data 3 (+)	--
82	SCAM_PWDN	DO	PD	SCAM PWDN	1.8V
81	SCAM_RST	DO	PD	SCAM reset	1.8V
75	SCAM_MCLK	DO	PD	SCAM clock	1.8V
63	MIPI_CSI0_CLK_N	AI	--	MIPI CSI0 clock 0 (-)	--
64	MIPI_CSI0_CLK_P	AI	--	MIPI CSI0 clock 0 (+)	--

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
65	MIPI_CSI0_LN0_N	AI	--	MIPI CSI0 data 0 (-)	--
66	MIPI_CSI0_LN0_P	AI	--	MIPI CSI0 data 0 (+)	--
67	MIPI_CSI0_LN1_N	AI	--	MIPI CSI0 data 1 (-)	--
68	MIPI_CSI0_LN1_P	AI	--	MIPI CSI0 data 1 (+)	--
72	MIPI_CSI0_LN2_N	AI	--	MIPI CSI0 data 2 (-)	--
73	MIPI_CSI0_LN2_P	AI	--	MIPI CSI0 data 2 (+)	--
70	MIPI_CSI0_LN3_N	AI	--	MIPI CSI0 data 3 (-)	--
71	MIPI_CSI0_LN3_P	AI	--	MIPI CSI0 data 3 (+)	--
236	DCAM_PWDN	DO	PD	DCAM PWDN	1.8V
237	DCAM_RST	DO	PD	DCAM reset	1.8V
238	DCAM_MCLK	DO	PD	DCAM clock	--

Table 17. Audio interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
4	MIC1_P	AI	--	Main MIC input (+)	--
5	MIC1_M	AI	--	Main MIC input (-)	--
6	MIC2_P	AI	--	Headphone MIC input (+)	--
220	MIC3_P	AI	--	Auxiliary microphone input (+)	--
221	MIC3_M	AI	--	Auxiliary microphone input (-)	--
8	EAR_P	AO	--	Receiver output (+)	--
9	EAR_M	AO	--	Receiver output (-)	--
10	LINEOUT_P	AO	--	Differential Lineout output (+)	--
11	LINEOUT_M	AO	--	Differential Lineout output (-)	--
136	HPH_R	AO	--	Headphone right channel	--
137	HPH_GND	AO	--	Headphone reference ground	--
138	HPH_L	AO	--	Headphone left channel	--
139	HS_DET	AI	--	Headphone plug and unplug detection	--
219	MIC_BIAS1	PO	--	MIC bias voltage 1	--
227	MIC_BIAS3	PO	--	MIC bias voltage 3	--

Table 18. ANT interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
77	ANT_WIFI/BT	AI/AO	--	Wi-Fi/BT antenna	50Ω
87	ANT_MAIN	AI/AO	--	Main antenna	50Ω
121	ANT_GNSS	AI	--	GNSS antenna	50Ω
131	ANT_DRX	AI	--	Diversity antenna	50Ω

Table 19. Antenna tuner interface

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
247	GRFC11_GPIO_48*	DO	PD	General RF control 11 or common GPIO	1.8V
202	GRFC12_GPIO_49	DO	PD	General RF control 12 or common GPIO	1.8V
203	GRFC13_GPIO_50*	DO	PD	General RF control 13 or common GPIO	1.8V

Table 20. GPIO interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
33	GPIO_31	DI/DO	PD	General purpose input/output	1.8V
34	GPIO_16	DI/DO	PD	General purpose input/output	1.8V
35	GPIO_17	DI/DO	PD	General purpose input/output	1.8V
90	GPIO_112	DI/DO	PD	General purpose input/output	1.8V
97	GPIO_84	DI/DO	PD	General purpose input/output	1.8V
98	GPIO_108	DI/DO	PD	General purpose input/output	1.8V
99	GPIO_85	DI/DO	PD	General purpose input/output	1.8V
100	GPIO_68	DI/DO	PD	General purpose input/output	1.8V
101	GPIO_104	DI/DO	PD	General purpose input/output	1.8V
102	GPIO_105	DI/DO	PD	General purpose input/output	1.8V
103	GPIO_103	DI/DO	PD	General purpose input/output	1.8V
104	GPIO_102	DI/DO	PD	General purpose input/output	1.8V
105	GPIO_99	DI/DO	PD	General purpose input/output	1.8V
106	GPIO_111	DI/DO	PD	General purpose input/output	1.8V
112	GPIO_26	DI/DO	PD	General purpose input/output	1.8V
113	GPIO_25	DI/DO	PD	General purpose input/output	1.8V
115	PM_GPIO_2	DI/DO	PD	General purpose input/output	1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
123	GPIO_24	DI/DO	PD	General purpose input/output	1.8V
124	GPIO_86	DI/DO	PD	General purpose input/output	1.8V
127	GPIO_67	DI/DO	PD	General purpose input/output	1.8V
159	GPIO_36	DI/DO	PD	General purpose input/output	1.8V
187	GPIO_101	DI/DO	PD	General purpose input/output	1.8V
205	GPIO_100	DI/DO	PD	General purpose input/output	1.8V
206	GPIO_98	DI/DO	PD	General purpose input/output	1.8V
207	GPIO_107*	DI/DO	PD	General purpose input/output	1.8V
252	GPIO_27	DI/DO	PD	General purpose input/output	1.8V
257	GPIO_83	DI/DO	PD	General purpose input/output	1.8V

Table 21. Interrupt interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
107	ALSP_INT	DI	PD	Ambient light sensor interrupt signal	1.8V
108	GYRO_INT	DI	PD	G-sensor interrupt signal	1.8V
109	MAG_INT	DI	PD	Magnetometer interrupt signal	1.8V
110	ACCEL_INT1	DI	PD	G-sensor interrupt signal 1	1.8V

Table 22. FLASH_LED interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
255	FLASH_LED	PO	--	Flashlight/torch drive output	Flashlight: I _{max} = 1.5 A. Torch: I _{max} = 388 mA.

Table 23. Other interfaces

Pin	Pin Name	I/O	Reset Value	Pin Description	DC Feature
256	NFC_CLK*	DO	--	NFC clock	--
153	GNSS_ELNA_EN	DO	--	GNSS_LNA Enable	Cannot be used as a general-purpose GPIO.

Table 24. Reserved pins

Pin	DC Feature
16,241,242, 204,199,190,152,249,248,28,243,244,154,133,134,258	Unconnected



- 1. Reset Value: The state during pin initialization.
- 2. Pins marked with "*" are reserved or under development.
- 3. ELDO_3V0 on Pin 228 is a power supply pin, and it will not lose power even when the system is in sleep mode.

4 Application Interfaces

4.1 Power Interfaces

4.1.1 Power Pin Definition

Table 25. Power pin definition

Pin Name	Pin No.	I/O	Reset Value	Pin Description	DC Feature
VBAT	1, 2, 145, 146	PI	--	Module power	3.5-4.4V

4.1.2 Power Supply Circuit

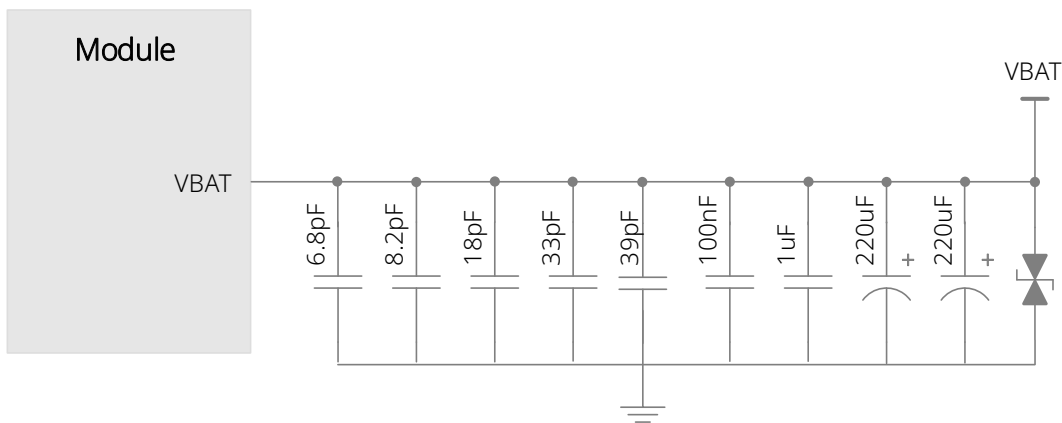


Figure 3. Power supply reference circuit

Filter capacitors should be placed close to the power supply pin, and the capacitance value should be smaller to be closer to the corresponding power supply pin. The filter capacitor should be placed on the same side as the module, and must not cross the layer, otherwise there will be the risk of TIS interference, and the trace should be as short and wide as possible.

Table 26. Filter capacitor introduction

Recommended Capacitor	Application	Description
220μF x 2	Regulating capacitor	To reduce power fluctuations during module operation, low ESR capacitors are required. LDO or DCDC power supply requires capacitor with a capacitance of no less than 440μF. Battery power supply requires capacitors with a capacitance of 100-220μF.
1μF, 100nF	Low frequency	Filter out interference caused by clock and digital signals.

Recommended Capacitor	Application	Description
	filter capacitors	
39pF, 33pF, 18pF, 8.2pF, 6.8pF	Decoupling capacitor	Filter out high frequency interference.



The recommended filter capacitor can be adjusted by the customer based on specific circumstances. It is not a fixed value.

4.1.3 Voltage Drop

The input voltage range of VBAT power supply is 3.5V-4.4V and the recommended input voltage is 3.8V. Module's power supply performance, such as the load capacity and ripple can directly affect module performance and stability during module operation. In extreme conditions, the peak current may reach 3A. If the power supply capacity is insufficient, the voltage may drastically drop to below 3.5V and the module may experience shutdown or restart. The following figure shows the power supply requirements.

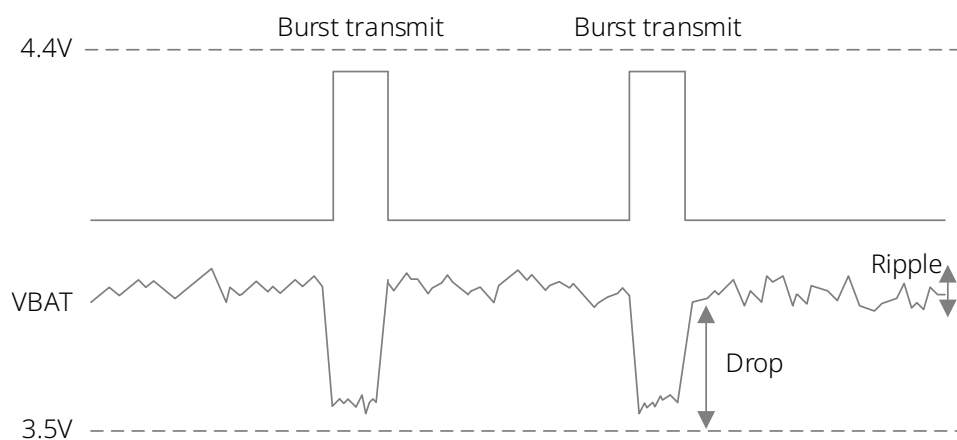


Figure 4. Power supply requirements



Due to the high peak current (about 3A) during the operation of the 4G module, the VBAT voltage fluctuation will gradually decrease with the increase of regulating capacitor, but the fluctuation cannot be completely eliminated. Therefore, customers must note that the power supply system of the module must be separated from the power supply of other control chips to avoid voltage fluctuations from affecting the power stability of the control chip, leading to system shutdown. If necessary, please consult with Fibocom technical support.

4.1.4 VRTC

VRTC is the power supply for the internal RTC clock of the module. When the module's VBAT power is applied, VRTC will output voltage; when VBAT is disconnected, if real-time clock maintenance is required, an external power source (such as a coin cell battery) must be supplied. The VRTC parameters are as follows.

Table 27. VBATBK parameters

Parameter	Minimum Value	Typical Value	Maximum Value	Unit
VRTC output voltage	2.0	3.0	3.25	V
VRTC input voltage (clock works well)	2.0	3.0	3.25	V
VRTC input current (clock works well)	--	12	--	μA

When the VRTC is powered by an external battery, the reference circuit is as follows.

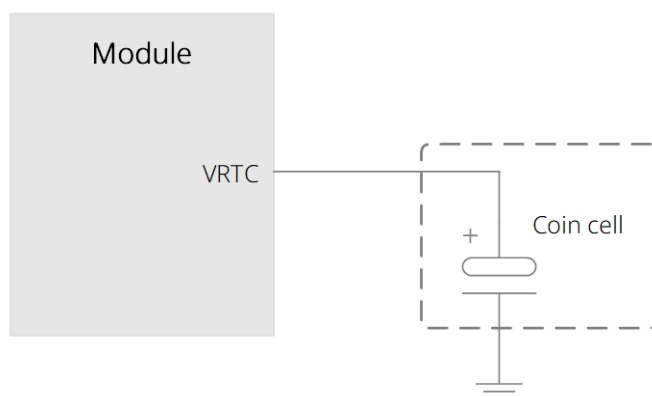


Figure 5. Reference circuit of VRTC power supply

4.1.5 Power Output

The module has multiple power output channels for supplying power to peripheral circuits. If you need to use power output, you can connect a 33 pF with a 10 pF capacitor in parallel to effectively eliminate high-frequency interference.

Table 28. Power output

Pin Name	Default Voltage (V)	Drive Current (mA)	Maximum Load Capacity	Remarks
ELDO_VDD_2V8	2.8	500	3.7μF	Enabled by PMGPIO_5
VREG_L9A	1.8	400	1μF	--
VPH_PWR	(=VBAT)	1000	--	--

Pin Name	Default Voltage (V)	Drive Current (mA)	Maximum Load Capacity	Remarks
VREG_L20A	1.8/3.0	100	5 μ F	--
VREG_L19A	1.8/3.0	100	5 μ F	--
ELDO_IOVDD_1V8	1.8	300	9 μ F	Enabled by GPIO_58
ELDO_3V0	3.0	300	9 μ F	Enabled by GPIO_54
VREG_L5A	1.8/2.96	20	5 μ F	--
VREG_L22A	2.96	800	23.5 μ F	--



The load capacitance on the power output pins must not exceed the maximum load capacity value.

4.2 Power-on/off Interfaces

4.2.1 Power on/off Pin Definition

Table 29. Power on/off pin definition

Pin Name	Pin NO.	I/O	Reset Value	Pin Description	DC Feature
KEY_P WR_ON	114	DI	PU	Module power-on/off control signal, active low In the power-off state, pull down the PWRKEY for 2s to 8s, then release it to power on the module. In the power-on state, pull down the PWRKEY for 2s to 6s, then release it to pop up the shutdown and restart menu.	1.1V
CBL_P WR_N	261	DI	PU	Module power on automatic startup control signal, active low. In the shutdown state, keep pulling down the pin, and the module will automatically turn on when powered on.	1.1V

The module provides two power control methods. You can select one as required.

4.2.2 Power-On/Power-Off/Reset

4.2.2.1 Power-On

The module has one power-on control signal that governs the module's power on/off, restart, and sleep/wake functions.

After VBAT is powered, you can turn on the module by pulling the KEY_PWR_ON pin low for 2 to 8 seconds. The power-on circuit with a keystroke and the open-collector (OC) driver power-on reference circuit are as follows:

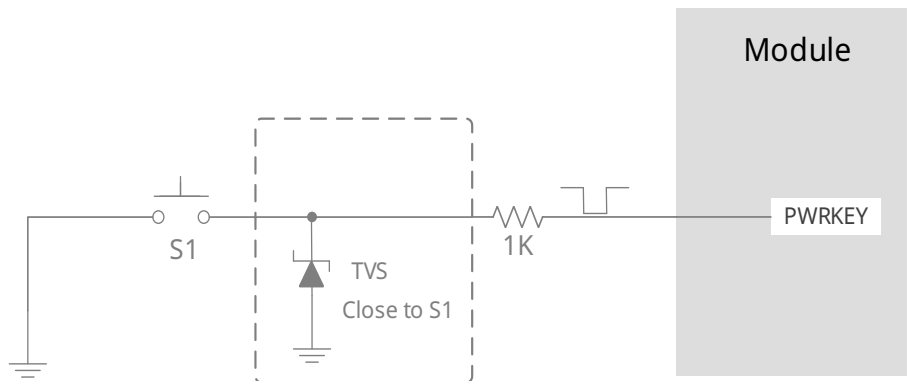


Figure 6. PWRKEY power on/off circuit

Use GPIO to control KEY_PWR_ON for module power on/off. It is recommended to use an OC drive circuit to control KEY_PWR_ON. The power on/off circuit is shown in the following figure.

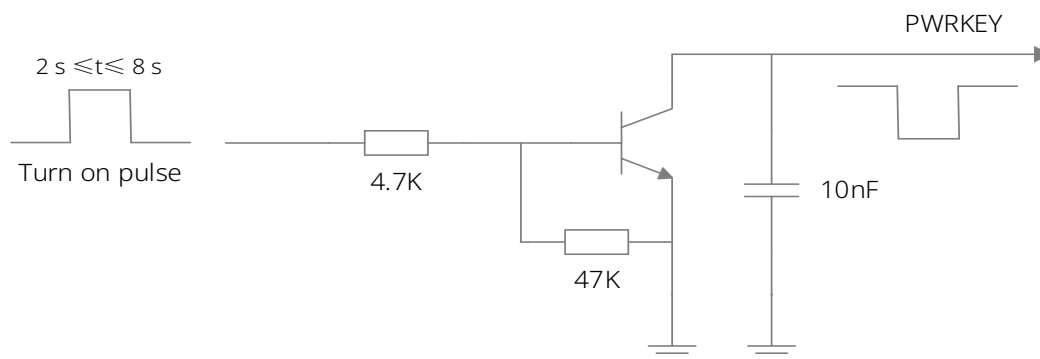


Figure 7. Drive power-on reference circuit

The module supports automatic turn-on upon power supply:

By connecting the CBL_PWR_N pin in series with a 0Ω resistor to GND, the module can be automatically turned on upon power on.

For modules using the automatic turn-on feature, the only way to shut down the module is by cutting

off power to VBAT. The circuit is shown in the following diagram:

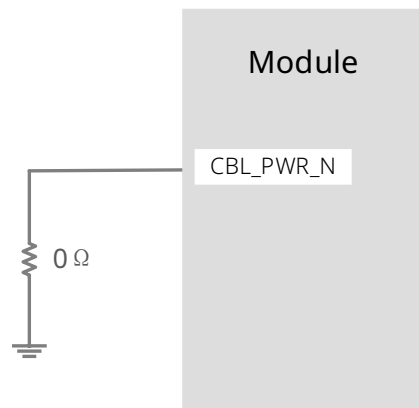


Figure 8. Automatic power-on circuit

When the module is in the power-off state, according to the power-up sequence requirements, after VBAT is powered and runs stable for 100 ms, pull the KEY_PWR_ON pin low for 2 to 8 seconds to trigger the module to turn on.

The turn-on sequence is shown in the figure below:

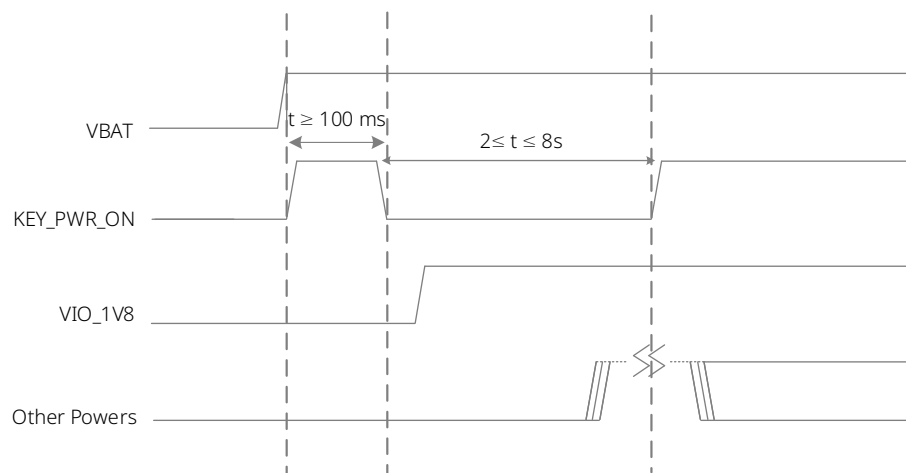


Figure 9. PWRKEY turn-on sequence



In addition to triggering the module to turn on by pulling the KEY_PWR_ON pin low, pulling the pin 261 CBL_PWR_N low will also trigger the module to turn on. This pin is suitable for scenarios that require automatic turn-on upon power on.

4.2.2.2 Power-Off and Reset

Normal shutdown: While the module is on, pulling the KEY_PWR_ON pin low for more than 2 seconds will bring up a selection dialog on the display (to choose between shutdown or restart).

Forced shutdown: Pulling the KEY_PWR_ON pin low for 9 to 15 seconds will force the system to shut down. The forced shutdown sequence is shown in the figure below.

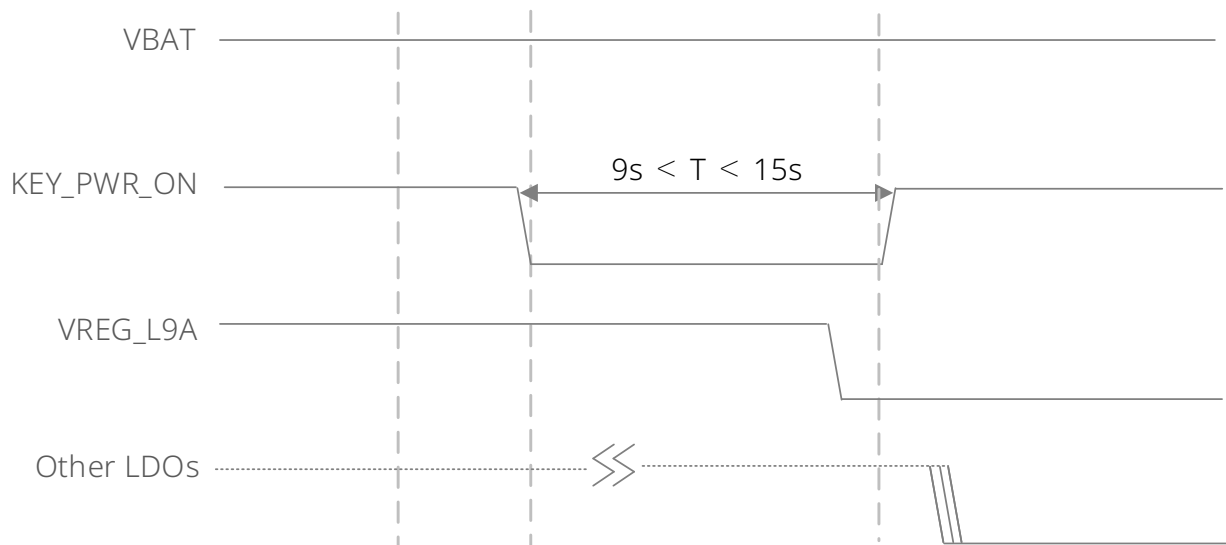


Figure 10. PWRKEY power-off Sequence



When the system experiences abnormalities or a freeze, you can perform a forced shutdown on the module. Under normal circumstances, please use the normal shutdown method to turn off the device, as failure to do so may result in data loss or other irregularities.

Reset: Pull the RESET_N pin low for 4 seconds to reset the system.

4.2.3 Sleep and Wake-up

Sleep: When the module is in standby mode, pulling the PWRKEY pin low for 0.5 s will put the module into sleep mode. The system supports automatic sleep, and the duration of transitioning from standby to sleep can be configured via software.

Wake-up: When the module is in sleep mode, pulling the PWRKEY pin low for 0.5 s will wake up the module.

4.2.4 Forced Download

The module provides the KEY_FORCE_BOOT pin as an emergency download interface. Short-circuiting KEY_FORCE_BOOT and VREG_L9A during power-on will force the module into emergency download mode, serving as a last-resort solution when the device fails to boot or operate normally. To facilitate future software upgrades and debugging, please reserve this pin.

The reference circuit is as follows:

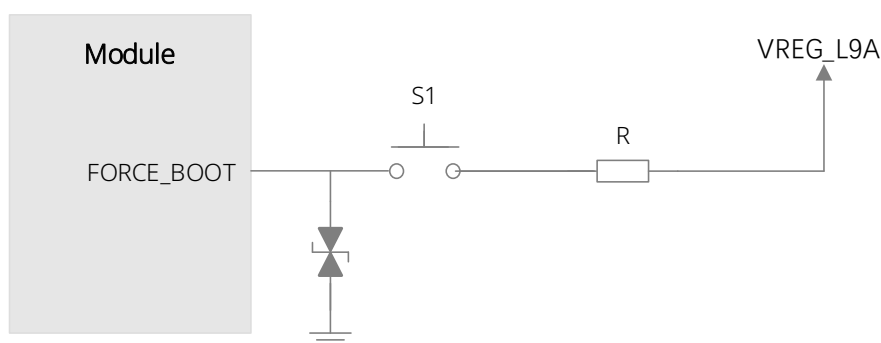


Figure 11. Design of forced download interface

4.3 USB Interface

The module provides one USB 3.1 interface, which is backward compatible with the USB 2.0 interface. USB 3.1 supports the SuperSpeed (SS) mode (5Gbps), but does not support software downloading.

USB 2.0 supports the High-Speed (HS) mode (480Mbps), is backward compatible with Full-Speed (FS) and Low-Speed (LS), and supports software downloading.

USB also supports OTG functionality and HUB expansion interfaces. It has an integrated CC control pin, supporting Type-C connectors. The module does not support charging functionality internally and requires an external charging IC. The VBUS_USB_DET only has the function of detecting input charging power.

Table 30. USB pin definition

Pin Name	Pin No.	I/O	Reset Value	Function	DC Feature
VBUS_USB_DET	141, 142	DI	--	VBUS input detection	--
USB_DM	13	AI/AO	--	USB 2.0 differential data signal (-)	--
USB_DP	14	AI/AO	--	USB 2.0 differential data signal (+)	--
USB_SS1_RX_M	210	AI	--	USB 3.1 differential data receive (-)	--
USB_SS1_RX_P	195	AI	--	USB 3.1 differential data receive (+)	--
USB_SS1_TX_M	196	AO	--	USB 3.1 differential data send (-)	--
USB_SS1_TX_P	197	AO	--	USB 3.1 differential data send (+)	--
USB_SS2_RX_M	151	AI	--	USB 3.1 differential data receive (-)	--
USB_SS2_RX_P	224	AI	--	USB 3.1 differential data receive (+)	--
USB_SS2_TX_M	223	AO	--	USB 3.1 differential data send (-)	--
USB_SS2_TX_P	222	AO	--	USB 3.1 differential data send (+)	--

Pin Name	Pin No.	I/O	Reset Value	Function	DC Feature
USB_CC1	194	AI/AO	--	USB_CC1	--
USB_CC2	191	AI/AO	--	USB_CC2	--

4.3.1 USB 3.1 (Type-C) Reference Circuit Design

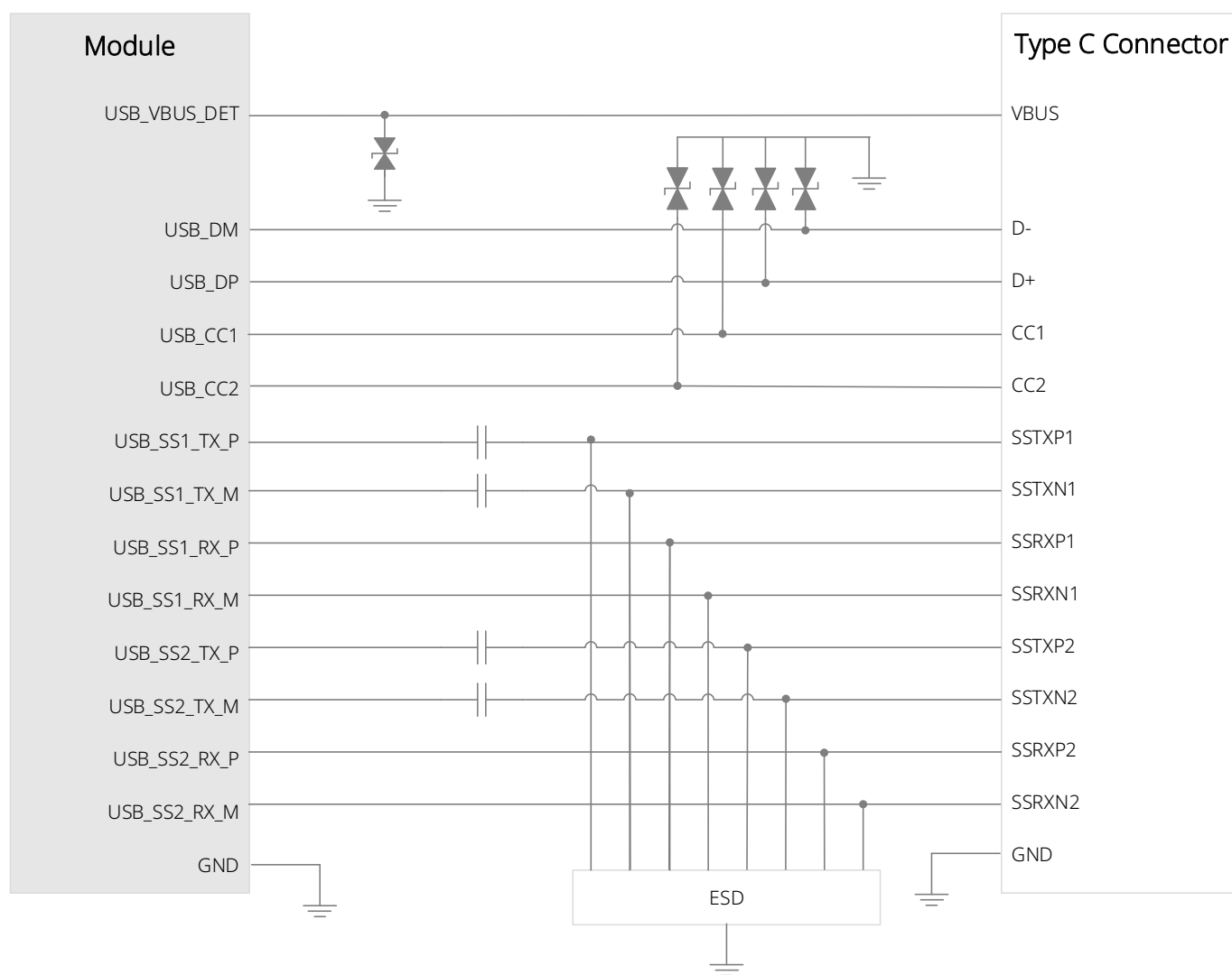


Figure 12. USB3.1 reference circuit design

4.3.2 USB Design Considerations

USB are high-speed signal lines, and the following points should be noted during PCB layout:

- The ESD protection device for USB_DP/DM should have a junction capacitance of less than 2pF.
- USB_DP and USB_DM are high-speed differential signal lines. The following requirements must be observed during PCB layout:

- The signal lines of USB_DP and USB_DM should be of equal length, with the length difference between the differential lines controlled within 2mm. They should be routed parallel to each other, avoiding right-angle routing, and the differential impedance of 90Ω should be well controlled.
- The USB2.0 differential signal lines should be surrounded by a ground plane in three dimensions (3D ground).
- OTG function support: The VBUS_USB_DET module does not support outputting 5V for OTG power supply. An external OTG power supply must be added.

USB3.1 Design Notes:

- USB3.1 is a high-speed signal line and requires proper shielding (3D ground for differential lines). The principles of high-speed differential routing must be followed.
- The spacing between USB3.1 signal Rx and Tx lines is recommended to be 3 times the line width. The spacing between differential lines and other routing lines should be maintained at 4 times the line width.
- Differential impedance control should be well maintained at $90\Omega \pm 10\%$. The length difference between differential lines should be controlled within 0.7mm, and the length difference between groups should be controlled within 10mm.
- The parasitic capacitance of the ESD device must be less than 0.2pF.

4.4 UART Interfaces

The module supports 2 UART interfaces, namely the DEBUG debugging interface and the UART1 interface, both with a voltage domain of 1.8V.

4.4.1 UART Pin Definition

Table 31. UART pin definition

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
DBG_UART_TX	94	DO	PD	Debug UART data transmission	1.8V
DBG_UART_RX	93	DI	PD	Debug UART data reception	1.8V
UART1_TX	226	DO	PD	UART1 transmitting signal	1.8V
UART1_RX	225	DI	PD	UART1 receiving signal	1.8V

4.4.2 UART Interface Circuit

The UART interface of the module operates at 1.8V voltage level. If the customer's host system operates at 3.3V or other voltage levels, an additional level shifting circuit is required.

The following figure shows the reference circuit of level shifting chip.

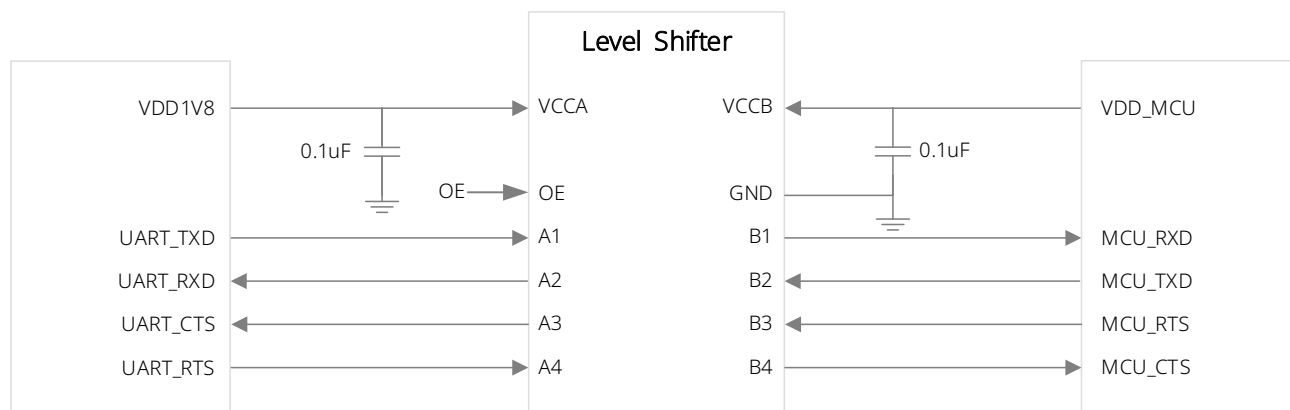


Figure 13. Reference circuit of level shifting chip

4.5 SPI Interfaces

Table 32. SPI pin definition

Pin Name	Pin NO.	I/O	Reset Value	Pin Description	DC Feature
SPI_CLK	116	DI	PD	SPI clock	1.8V
SPI_CS	117	DO	PD	SPI chip select	1.8V
SPI_MISO	118,253	DI	PD	SPI master in slave out	1.8V
SPI_MOSI	119,254	DO	PD	SPI master out slave in	1.8V

4.6 SDIO Interfaces

4.6.1 SDIO Pin Definition

Table 33. SDIO pin definition

Pin Name	Pin NO.	I/O	Reset Value	Pin Description	DC Feature
VREG_L22A	38	PO	--	SD card power supply	2.96V
VREG_L5A	32	PO	--	SD card signal pull-up power supply	1.8V/2.96V
SD_DET	45	DI	--	SD card plug and unplug detection	1.8V
SD_DATA3	44	DI/DO	--	SDIO DATA3	1.8V/2.96V
SD_DATA2	43	DI/DO	--	SDIO DATA2	1.8V/2.96V
SD_DATA1	42	DI/DO	--	SDIO DATA1	1.8V/2.96V
SD_DATA0	41	DI/DO	--	SDIO DATA0	1.8V/2.96V

Pin Name	Pin NO.	I/O	Reset Value	Pin Description	DC Feature
SD_CMD	40	DI/DO	- -	SD card command	1.8V/2.96V
SD_CLK	39	DO	- -	SD card clock	1.8V/2.96V

4.6.2 SDIO Interface Circuit

The reference circuit of SDIO interface circuit is shown in the following figure.

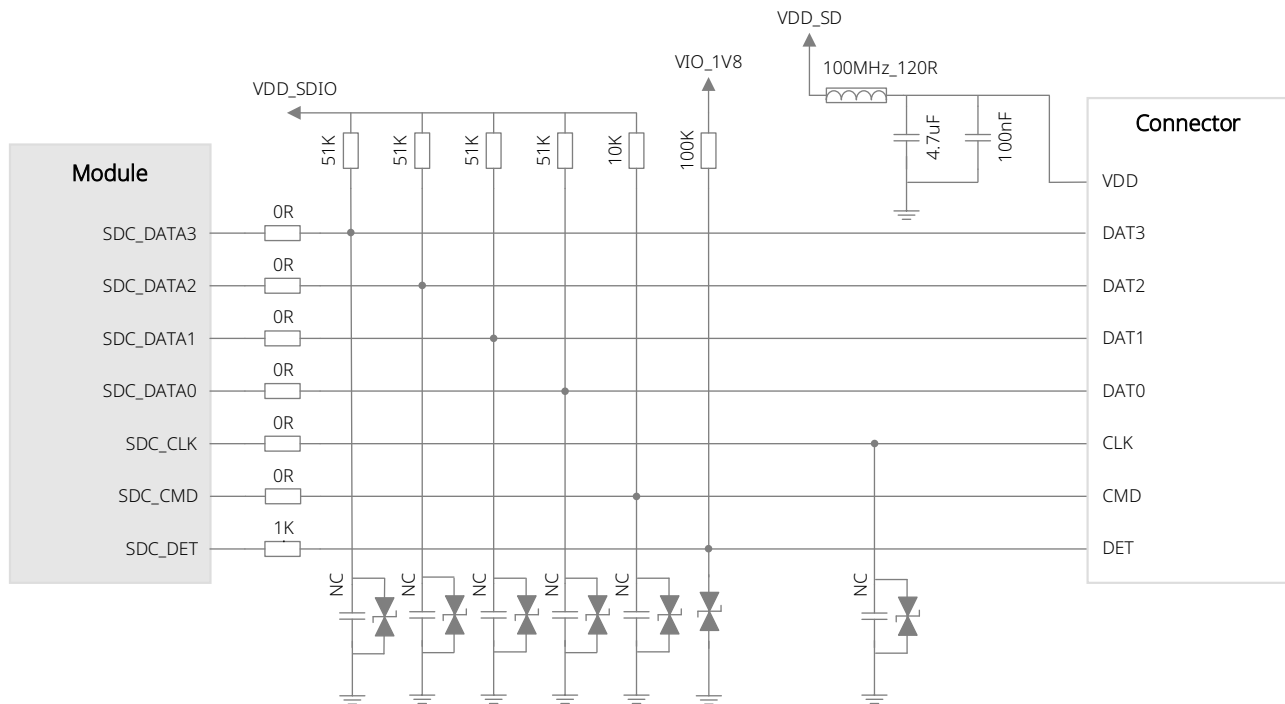


Figure 14. SDIO interface reference circuit

EMC and ESD protection should be considered in the design of SDIO circuit, and the anti-interference ability should be improved to ensure the stable operation of SD card. The following rules should be strictly followed in the design:

- The length of the SDIO trace is ≤ 50 mm, and the length difference between the clock signal and data signal traces is ≤ 2 mm.
- The SDIO signal line must be three-dimensionally grounded and kept away from RF antenna, DCDC power supply, clock signal line, and other strong interference sources.
- The SDIO signals should have a complete reference ground, and the impedance of the data lines should be controlled at $45\Omega (\pm 10\%)$.
- The total capacitance of the load on the SDIO signal lines should be less than 0.5pF.



- VDD_SD is the power supply for the SD card peripheral drive, capable of providing approximately 800 mA of current. Note that the trace width should be greater than 0.8 mm.
- For the pull-up of SD_DET, please use the VREG_L9A_1P8 power supply.

- For the pull-up of SDIO, please use the VREG_L5A power supply.

4.7 USIM Interfaces

The module has two sets of (U)SIM interfaces, supports dual card and dual standby and hot plug detection. Pin definitions can be found in the pin descriptions.

4.7.1 USIM Pin Definition

Table 34. USIM pin definition

Pin Name	Pin NO.	I/O	Reset Value	Pin Description	DC Feature
VREG_L19A	26	PO	--	USIM1 power supply	1.8V/3V
USIM1_DATA	25	DI/D O	--	USIM1 data	1.8V/3V
USIM1_CLK	24	DO	--	USIM1 clock	1.8V/3V
USIM1_RST	23	DO	--	USIM1 reset	1.8V/3V
USIM1_DET	22	DI	--	USIM1 hot-plug detection	1.8V
VREG_L20A	21	PO	--	USIM2 power supply	1.8V/3V
USIM2_DATA	20	DI/D O	--	USIM2 data	1.8V/3V
USIM2_CLK	19	DO	--	USIM2 clock	1.8V/3V
USIM2_RST	18	DO	--	USIM2 reset	1.8V/3V
USIM2_DET	17	DI	--	USIM2 hot-plug detection	1.8V

4.7.2 USIM Interface Circuit

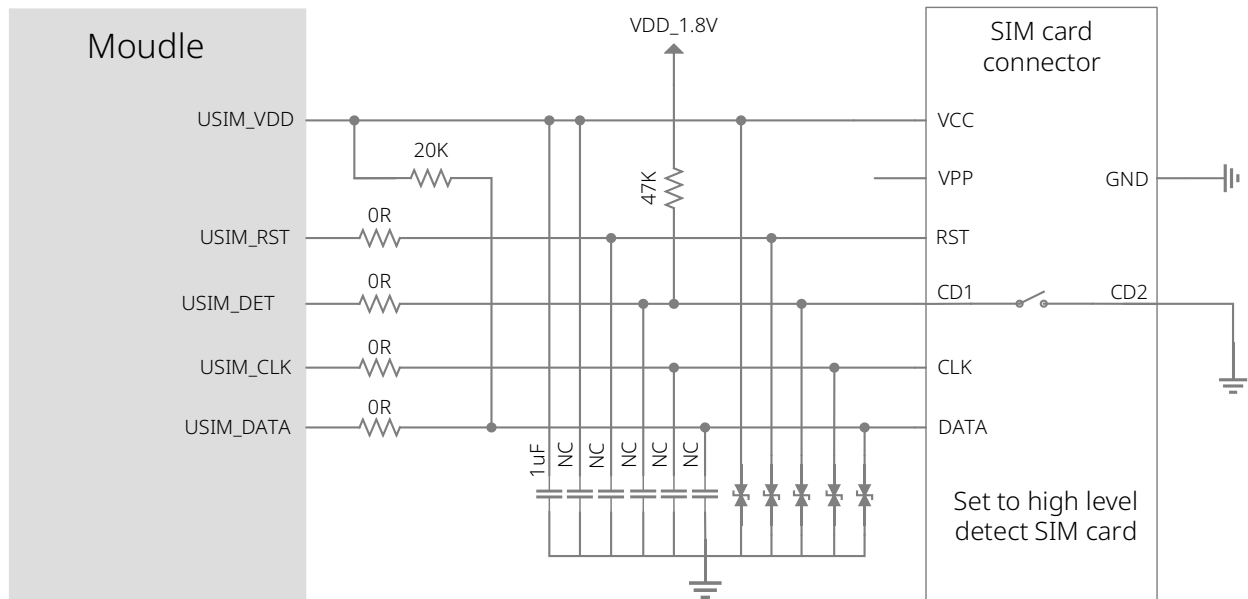


Figure 15. USIM card reference circuit

To ensure the stable operation of USIM cards, the following rules should be strictly followed in the design:

- The equivalent capacitance on the SIM card RST, CLK, and DATA signal lines should be less than 33pF.
- SIM card slot should be located as close to the module as possible, and kept away from the RF antenna, DCDC power, clock signal lines and other strong interference sources.
- SIM card signal lines should be kept away from RF lines, power lines, clock lines, and high-speed data lines as much as possible.
- Test points, filtering capacitors, and ESD devices for USIM card signal lines should be placed near the USIM card slot.
- The PCB surface below the spring contact should be kept clear to prevent the spring contact from scratching the green solder mask, which could lead to short circuit.
- It is recommended to keep the routing length from the module to the USIM card slot within 100 mm. Excessively long routing can degrade signal quality.
- USIM_CLK and USIM_DATA signal lines are isolated by ground to avoid mutual interference.
- Avoid routing signal lines on adjacent layers of the SIM card signal lines. If it is unavoidable, try to intersect them perpendicularly as much as possible to reduce the risk.
- Try to ensure the continuity and integrity of the PCB's GND and connect SIM_GND to the main ground with the shortest path.

4.8 I2C Interfaces

The module has multiple sets of universal I2C interfaces, which can be used to connect peripherals separately. Some I2C interfaces have built-in pull-up resistors, so external pull-up resistors are not required. Please refer to the pin description for the definition of I2C pins:

Table 35. I2C pin definition

Pin Name	Pin NO.	I/O	Reset Value	Pin Description	Remarks
SENSOR_I2C_SCL	91	DO	PD	Sensor I2C clock	Dedicated I2C for sensors
SENSOR_I2C_SDA	92	DI/DO	PD	Sensor I2C data	
I2C_SDA_GPIO_14	37	DI/DO	PU	CC logic I2C data	General I2C, the module internally uses CC logic, occupies I2C bus address 0x60. Not available for general GPIO.
I2C_SCL_GPIO_15	36	DO	PU	CC logic I2C clock	
CCI_I2C_SCL1	83	DO	PU	Camera I2C1 clock	Camera dedicated I2C, the internal flash drive chip occupies I2C bus address 0xc8. Not available for general GPIO.
CCI_I2C_SDA1	84	DI/DO	PU	Camera I2C1 data	
CCI_I2C_SCL0	239	DO	PU	Camera I2C0 clock	Camera dedicated I2C
CCI_I2C_SDA0	240	DI/DO	PU	Camera I2C0 data	
TP_I2C_SCL	47	DO	PU	CTP I2C clock	CTP dedicated I2C
TP_I2C_SDA	48,183	DI/DO	PU	CTP I2C data	



- When multiple peripherals are connected on an I2C bus, ensure the uniqueness of each peripheral's address. When connecting peripherals with high real-time requirements, do not share a single I2C bus among multiple peripherals.
- PIN 36/37 has an I2C device CC Logic internally mounted, with an address of 0x60. Since there are already 2.2KΩ pull-up resistors inside the module, no external pull-ups are needed for this I2C interface. It can only be used as an I2C interface and cannot be configured as other types, such as GPIO.
- PIN 83/84 has an I2C device internally mounted, with an address of 0xc8. Since there are already 2.2KΩ pull-up resistors inside the module, no external pull-ups are needed for this I2C interface. It can only be used for the Camera I2C interface and cannot be configured as other types, such as GPIO.

4.9 ADC Interfaces

Table 36. ADC pin definition

Pin Name	Pin No.	I/O	Reset Value	Pin Description	DC Feature
ADC	128	AI	--	Analog-to-digital input port	1.8V
ADC1	260	AI	--	Analog-to-digital input port	1.8V

The module provides two ADC, the ADC trace need to be surrounded by ground to improve ADC voltage measurement accuracy.

Table 37. ADC electrical characteristics

Pin Name	Input Voltage Range (V)	Accuracy (mv)
ADC	0-1.8	±10

4.10 GPIO Control Interfaces

Table 38. GPIO pin definition

Pin Name	Pin NO.	Reset Value	Pin Description	Interrupt Wakeup	DC Feature
GPIO_31	33	PD	General purpose input/output	YES	1.8V
GPIO_16	34	PD	General purpose input/output	NO	1.8V
GPIO_17	35	PD	General purpose input/output	YES	1.8V
GPIO_112	90	PD	General purpose input/output	YES	1.8V
GPIO_84	97	PD	General purpose input/output	YES	1.8V
GPIO_108	98	PD	General purpose input/output	NO	1.8V
GPIO_85	99	PD	General purpose input/output	YES	1.8V
GPIO_68	100	PD	General purpose input/output	NO	1.8V
GPIO_104	101	PD	General purpose input/output	YES	1.8V
GPIO_105	102	PD	General purpose input/output	YES	1.8V
GPIO_103	103	PD	General purpose input/output	YES	1.8V
GPIO_102	104	PD	General purpose input/output	YES	1.8V
GPIO_99	105	PD	General purpose input/output	YES	1.8V
GPIO_111	106	PD	General purpose input/output	NO	1.8V
GPIO_26	112	PD	General purpose input/output	NO	1.8V
GPIO_25	113	PD	General purpose input/output	YES	1.8V
PM_GPIO_2	115	PD	General purpose input/output	YES	1.8V
GPIO_24	123	PD	General purpose input/output	YES	1.8V
GPIO_86	124	PD	General purpose input/output	YES	1.8V
GPIO_67	127	PD	General purpose input/output	YES	1.8V
GPIO-36	159	PD	General purpose input/output	YES	1.8V

Pin Name	Pin NO.	Reset Value	Pin Description	Interrupt Wakeup	DC Feature
GPIO_101	187	PD	General purpose input/output	NO	1.8V
GPIO_100	205	PD	General purpose input/output	NO	1.8V
GPIO_98	206	PD	General purpose input/output	NO	1.8V
GPIO_107*	207	PD	General purpose input/output	YES	1.8V
GPIO_27	252	PD	General purpose input/output	YES	1.8V
GPIO_83	257	PD	General purpose input/output	YES	1.8V

The module has abundant GPIO resources, and the power domain is 1.8V.



Pins marked with an asterisk "*" are boot configuration pins. They should not be pulled up to the power supply in the design. Because doing so may cause the device to fail to power on.

4.11 GRFC Interfaces

Table 39. Pin definition of antenna tuner control interface

Pin Name	Pin No.	I/O	Reset Value	Pin Description	DC Feature
GRFC11_GPIO_48*	247	DO	PD	General RF control 11 or common GPIO	1.8V
GRFC12_GPIO_49	202	DO	PD	General RF control 12 or common GPIO	1.8V
GRFC13_GPIO_50*	203	DO	PD	General RF control 13 or common GPIO	1.8V



- By default, it serves as the RF antenna tuner control interface. If the RF antenna tuner control interface is not needed, it can be used as a GPIO (General Purpose Input/Output).
- Pins marked with an asterisk "*" are boot configuration pins. They should not be pulled up to the power supply in the design. Because doing so may cause the device to fail to power on.

4.12 LCD Interfaces

4.12.1 LCD Pin Definition

The screen interface is based on the MIPI_DSI standard, supporting one group of 4-lane high-speed differential data transmission .

Table 40. LCD pin definition

Pin Name	Pin No.	I/O	Description	Note
PWM	29	DO	PWM output	--
LCD_RST	49	DO	LCD rest	--
LCD_TE	50	DI	LCD tearing effect	--
MIPI_DSI0_CLK_N	52	AO	LCD MIPI clock (-)	--
MIPI_DSI0_CLK_P	53	AO	LCD MIPI clock (+)	--
MIPI_DSI0_LN0_N	54	AO	LCD MIPI data0 (-)	--
MIPI_DSI0_LN0_P	55	AO	LCD MIPI data0 (+)	--
MIPI_DSI0_LN1_N	56	AO	LCD MIPI data1 (-)	--
MIPI_DSI0_LN1_P	57	AO	LCD MIPI data1 (+)	--
MIPI_DSI0_LN2_N	58	AO	LCD MIPI data2 (-)	--
MIPI_DSI0_LN2_P	59	AO	LCD MIPI data2 (+)	--
MIPI_DSI0_LN3_N	60	AO	LCD MIPI data3 (-)	--
MIPI_DSI0_LN3_P	61	AO	LCD MIPI data3 (+)	--

4.12.2 LCD Interface Circuit

The reference circuit of LCD interface is as follows.

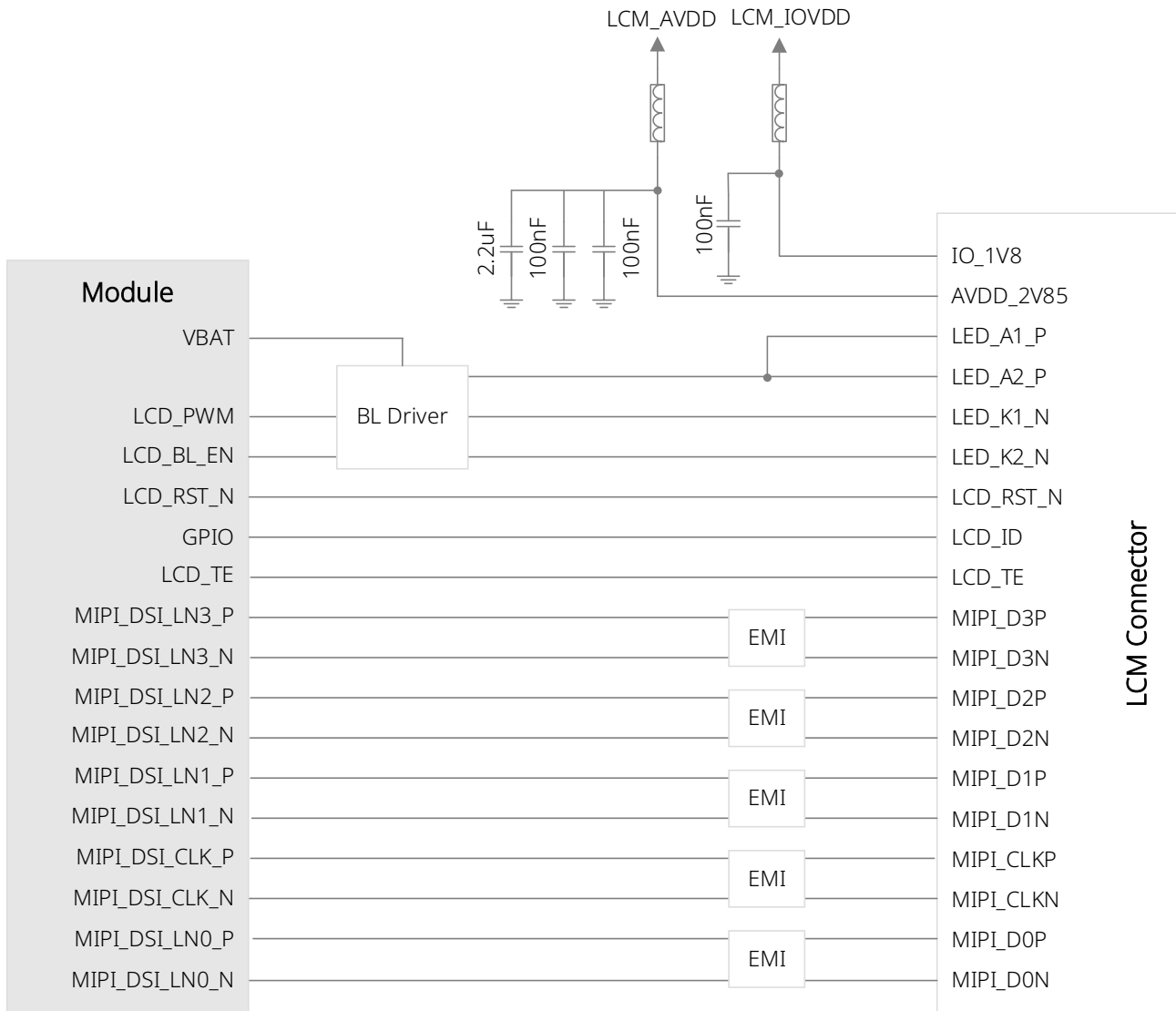


Figure 16. Reference schematic of LCD circuit

LCD design considerations are as follows:

- It is recommended to connect a common-mode inductor in series on the MIPI high-speed signal line near the LCD connector end to reduce EMI.
- MIPI routing is recommended to be designed in the inner layer, and surrounded with GND in three dimensions.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance $\pm 10\%$.
- The length difference of the differential line within the group is controlled within 0.7 mm, and the length difference between groups is controlled within 1.4 mm.
- EMI components can be selected, and the parasitic capacitance of the entire trace should be controlled within 1pF.
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

4.13 Touch Panel Interfaces

4.13.1 TP Pin Definition

The module provides one set of dedicated I2C interfaces for the touch panel. It also provides the required interrupt, and reset pins for the touch panel. The pin definitions are as follows:

Table 41. TP pin definition

Pin Name	Pin No.	I/O	Description	Note
TP_RST	31	DO	CTP interrupt	--
TP_INT	30	DI	CTP rest	--
TP_I2C_SDA	48, 183	DI/DO	CTP I2C clock	--
TP_I2C_SCL	47	DO	CTP I2C data	--

4.13.2 Touch Panel Interface Circuit

TP reference circuit design is as follows.

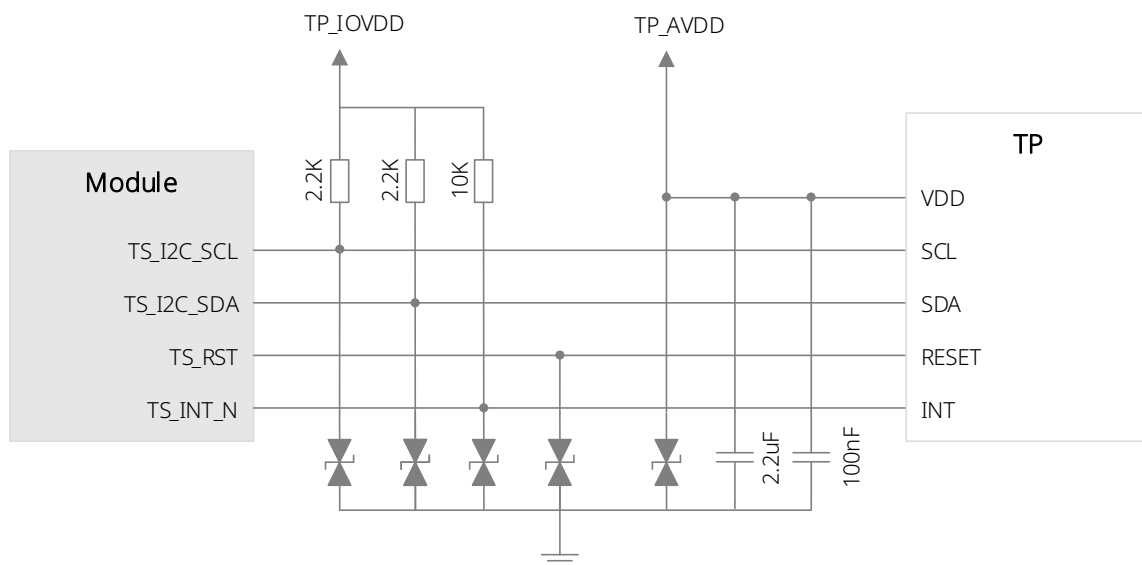


Figure 17. Reference schematic of TP circuit

4.14 Camera Interfaces

4.14.1 Camera Pin Definition

The camera interface of the module is based on the MIPI_CSI standard and can support 3 (4-lane + 2-lane + 1-lane) camera combinations. The pin definition of camera interface is as follows.

Table 42. Camera power supply

Pin Name	Pin No.	I/O	Description	Note
ELDO_IOVDD_1V8	125	PO	Camera IO power	--
ELDO_VDD_2V8	129	PO	Camera analog power	--

Table 43. Camera interface pin definition

Pin Name	Pin No.	I/O	Description	Note
MCAM_PWDN	80	DO	MCAM PWDN	--
MCAM_RST	79	DO	MCAM reset	--
MCAM_MCLK	74	DO	MCAM clock	--
MIPI_CSI1_CLK_N	230	AI	MIPI CSI1 clock 0 (-)	--
MIPI_CSI1_CLK_P	229	AI	MIPI CSI1 clock 0 (+)	--
MIPI_CSI1_LN0_N	231	AI	MIPI CSI1 data 0 (-)	--
MIPI_CSI1_LN0_P	155	AI	MIPI CSI1 data 0 (+)	--
MIPI_CSI1_LN1_N	232	AI	MIPI CSI1 data 1 (-)	--
MIPI_CSI1_LN1_P	156	AI	MIPI CSI1 data 1 (+)	--
MIPI_CSI1_LN2_N	233	AI	MIPI CSI1 data 2 (-)	--
MIPI_CSI1_LN2_P	157	AI	MIPI CSI1 data 2 (+)	--
MIPI_CSI1_LN3_N	234	AI	MIPI CSI1 data 3 (-)	--
MIPI_CSI1_LN3_P	158	AI	MIPI CSI1 data 3 (+)	--
SCAM_PWDN	82	DO	SCAM PWDN	--
SCAM_RST	81	DO	SCAM reset	--
SCAM_MCLK	75	DO	SCAM clock	--
MIPI_CSI0_CLK_N	63	AI	MIPI CSI0 clock 0 (-)	--
MIPI_CSI0_CLK_P	64	AI	MIPI CSI0 clock 0 (+)	--
MIPI_CSI0_LN0_N	65	AI	MIPI CSI0 data 0 (-)	--
MIPI_CSI0_LN0_P	66	AI	MIPI CSI0 data 0 (+)	--
MIPI_CSI0_LN1_N	67	AI	MIPI CSI0 data 1 (-)	--
MIPI_CSI0_LN1_P	68	AI	MIPI CSI0 data 1 (+)	--
MIPI_CSI0_LN2_N	72	AI	MIPI CSI0 data 2 (-)	--
MIPI_CSI0_LN2_P	73	AI	MIPI CSI0 data 2 (+)	--

Pin Name	Pin No.	I/O	Description	Note
MIPI_CSI0_LN3_N	70	AI	MIPI CSI0 data 3 (-)	--
MIPI_CSI0_LN3_P	71	AI	MIPI CSI0 data 3 (+)	--
DCAM_PWDN	236	DO	DCAM PWDN	--
DCAM_RST	237	DO	DCAM reset	--
DCAM_MCLK	238	DO	DCAM clock	--



The module does not have DVDD_1V2 and VDDAF_2V8 power supplies internally. They need to be provided by an external LDO (Low Dropout Regulator) with a high power supply noise rejection ratio.

4.14.2 Camera Interface Circuit

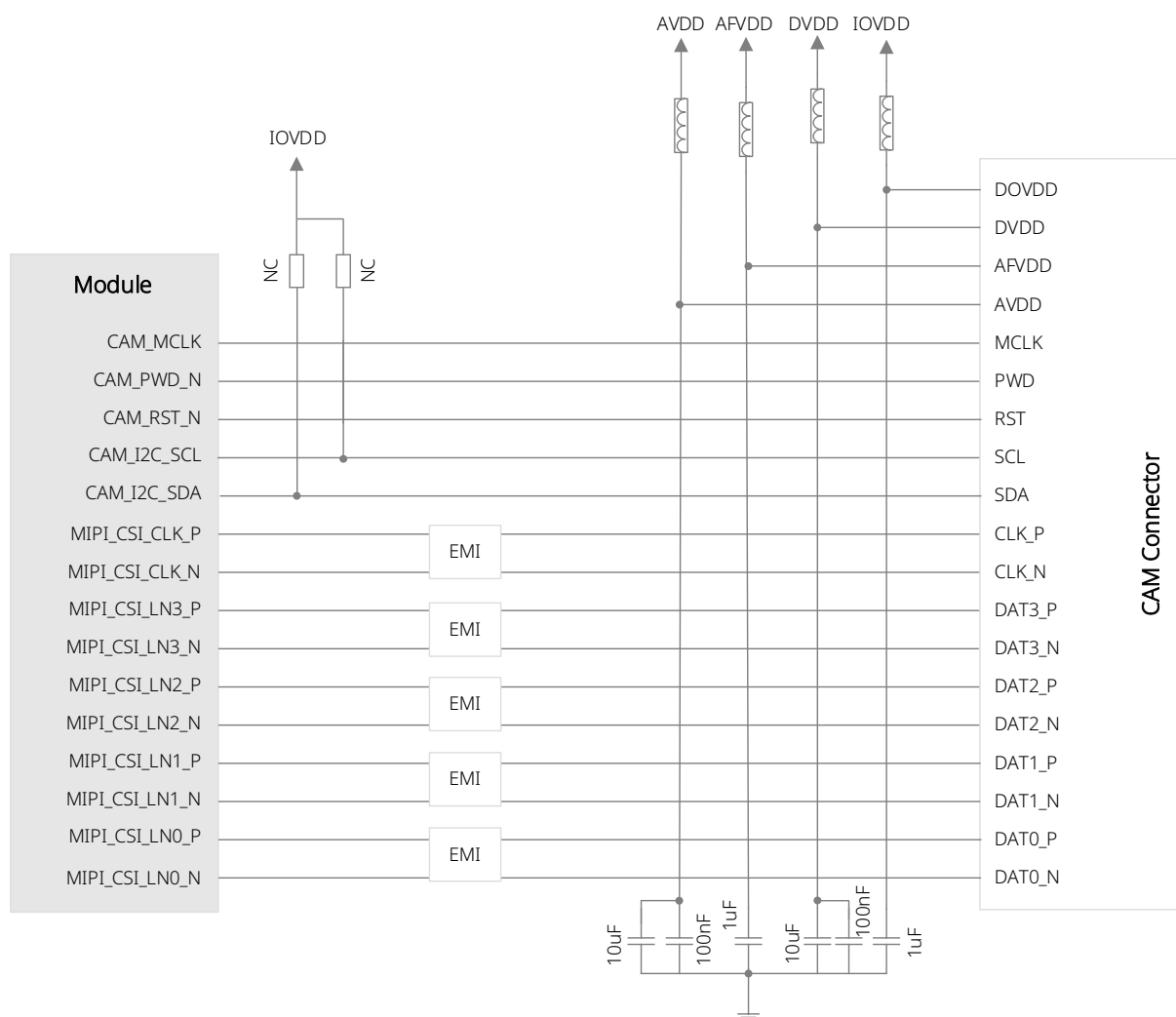


Figure 18. Reference schematic of camera circuit

MIPI_CSI is a high-speed signal line. Pay attention to the following points during PCB layout.

- It is recommended to connect a common-mode inductor in series on the MIPI high-speed signal line near the camera connector end to reduce EMI.
- MIPI routing is recommended to be designed in the inner layer, and surrounded with GND in three dimensions.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance $\pm 10\%$.
- The length difference of differential lines in MIPI signal line groups should be controlled within 0.7 mm, and the length difference between groups should be controlled within 1.4 mm.
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

Design considerations for other signal cables:

- CAM_MCLK is a high-speed clock signal and needs to be surrounded with GND in three dimensions.
- AVDD and DVDD of camera power supply should be routed away from interference sources to avoid introducing power supply noise. It is recommended to add LDO with high power supply noise rejection ratio.
- VDD_1V2 and VDDAF_2V8 must be supplied by an external LDO with a high power supply noise rejection ratio.
- If the cameras need to share an I2C, select two cameras that do not work at the same time, and make sure that the two cameras have different addresses.

4.15 Audio Interfaces

4.15.1 Analog Audio Pin Definition

The module supports three input and three output analog audio interfaces. The pin definition is as follows:

Table 44. Definition of analog audio interfaces

Pin Name	Pin No.	I/O	Description	Note
MIC1_P	4	AI	Main MIC input (+)	MIC2 and MIC3 cannot be used simultaneously.
MIC1_M	5	AI	Main MIC input (-)	
MIC2_P	6	AI	Headphone MIC input (+)	
MIC3_P	220	AI	Auxiliary microphone input (+)	
MIC3_M	221	AI	Auxiliary microphone input (-)	
EAR_P	8	AO	Receiver output(+)	--
EAR_M	9	AO	Receiver output (-)	
LINEOUT_P	10	AO	Differential Lineout	--

Pin Name	Pin No.	I/O	Description	Note
			output (+)	
LINEOUT_M	11	AO	Differential Lineout output (-)	--
HPH_R	136	AO	Headphone right channel	--
HPH_GND	137	AO	Headphone reference ground	Ground required
HPH_L	138	AO	Headphone left channel	--
HS_DET	139	AI	Headphone Plug and unplug detection	--
MIC_BIAS1	219	PO	MIC bias voltage 1	--
MIC_BIAS3	227	PO	MIC bias voltage 3	--

4.15.2 Analog Audio Interface Circuit

The MEMS type microphone differential input reference circuit is as follows:

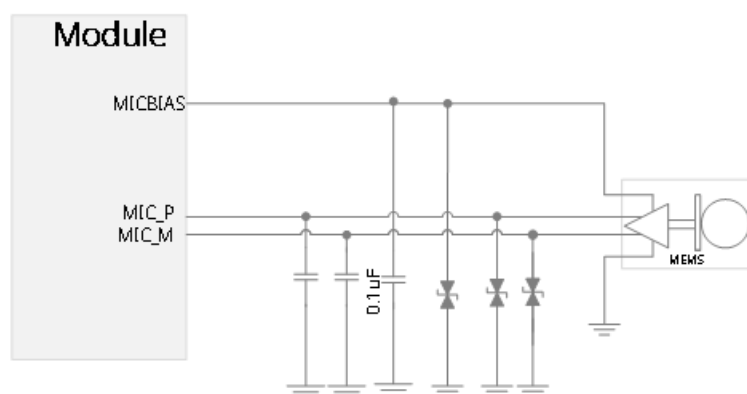


Figure 19. Reference schematic of MIC circuit

The reference circuit of receiver is as follows:

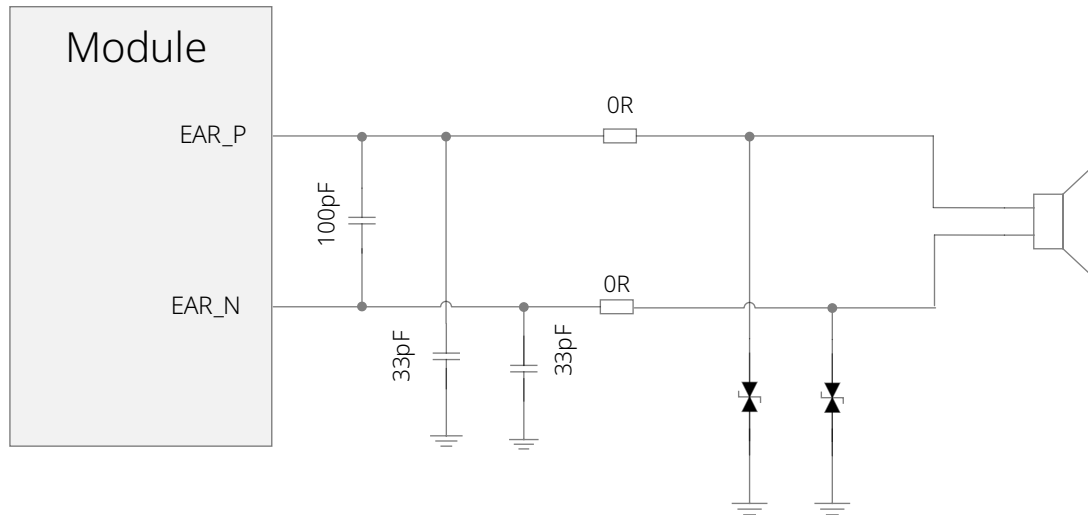


Figure 20. Reference schematic of receiver circuit

The reference circuit of headphone is as follows:

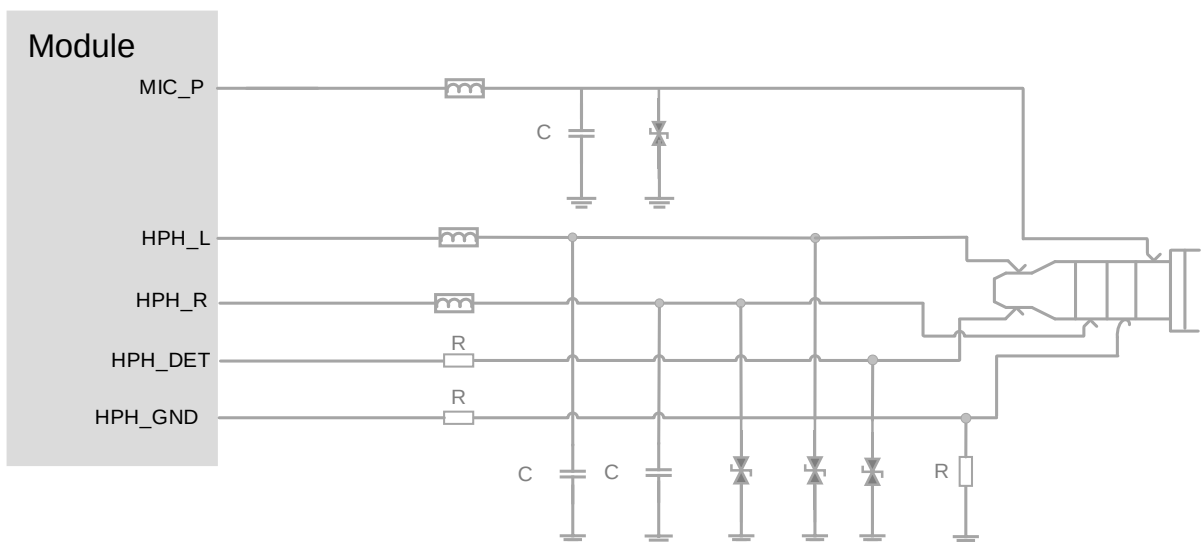


Figure 21. Reference schematic of headphone circuit

Audio interface design considerations:

- The module requires external components; a secondary MIC with a MIC_BIAS bias circuit should be added. The headphone MIC has internal biasing and does not need external addition.
- The headphone reference ground should be connected close to the connector.
- It is recommended to use a 32Ω impedance device for the earpiece.
- To reduce noise and improve audio quality, the following suggestions are made:
 - Audio PCB traces should be kept as far away as possible from antennas and high-frequency digital signals.
 - An LC filter circuit should be reserved in the audio circuit to reduce EMI.

- Audio traces require shielding treatment.

4.16 FLASH_LED Interface

4.16.1 FLASH_LED Pin Definition

Table 45. FLASH_LED interface definition

Pin Name	Pin No.	I/O	Description	Note
FLASH_LED	255	PO	Flashlight/Torch Drive Output	Flashlight: I _{max} = 1.5 A. Torch: I _{max} = 388 mA.



Supports torch and flashlight modes. The built-in flash driver chip needs to be used in conjunction with CCI_I2C1.

4.16.2 FLASH_LED Interface Circuit

The reference circuit for the FLASH_LED interface is as follows.

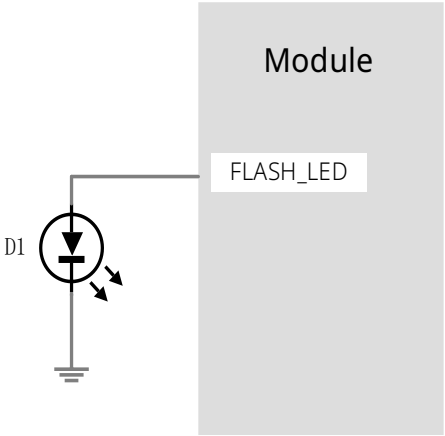


Figure 22. Reference schematic diagram for FLASH_LED

5 Antenna Interfaces

5.1 Definition of Antenna Interfaces

The following table contains all the frequency bands of the whole series of modules. Please read the antenna interface definition carefully and select the correct antenna interface for connection. For assistance, please contact the Fibocom technical personnel.

Table 46. Definition of antenna interfaces

Pin Name	Pin No.	I/O	Description	Note
ANT_MAIN	87	AI/AO	2G/3G/4G main antenna	-
ANT_DRX	131	AI	4G diversity Antenna	-
ANT_WIFI/BT	77	AI/AO	WIFI/BT antenna	-
ANT_GNSS	121	AI	GNSS antenna	-

5.2 Operating Frequency

Tables 47. Cellular frequency reference table

Operating Band	Frequency	Tx (MHz)	Rx (MHz)
LTE FDD	Band 2	1850-1910	1930-1990
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 12	699-716	729-746
	Band 13	777-787	746-756
	Band 17	704-716	734-746
	Band 25	1850-1915	1930-1995
	Band 26	814-849	859-894
	Band 66	1710-1780	2110-2180
	Band 71	663-698	617-652
LE TDD	Band 41	2496-2690	2496-2690

Table 48. Wi-Fi/BT frequency reference table

Mode	Frequency	Unit
WIFI	2402 - 2482	MHz
	5170 - 5835	MHz
BT	2402 - 2480	MHz

Table 49. GNSS frequency reference table

Satellite Type	Center Frequency Point (MHz)	Modulation
GPS	1575.42	CDMA
GLONASS	1597.5~1605.8	FDMA
BeiDou	1561.098	CDMA
Galileo	1575.42±2.02	CBOC
QZSS	1575.42±1.023	QPSK/BPSK

5.3 Antenna Design Circuit

The following figure shows an antenna circuit for a cellular network.

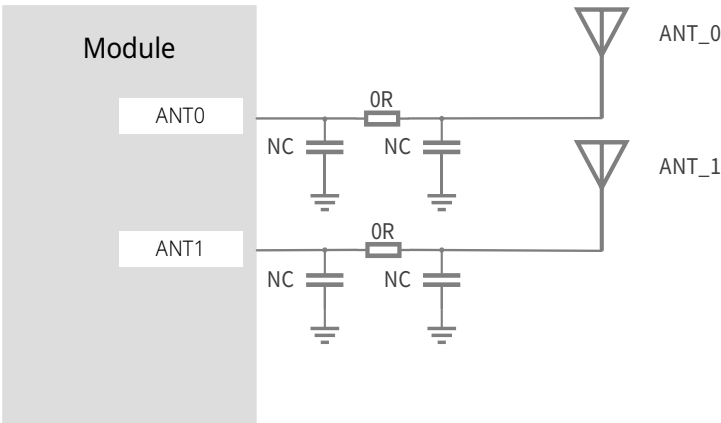


Figure 23. Cellular network antenna reference circuit

The following figure shows the GNSS active antenna. If the active antenna is not required, the dotted line part can be deleted. The circuit diagram of GNSS antenna is as follows.

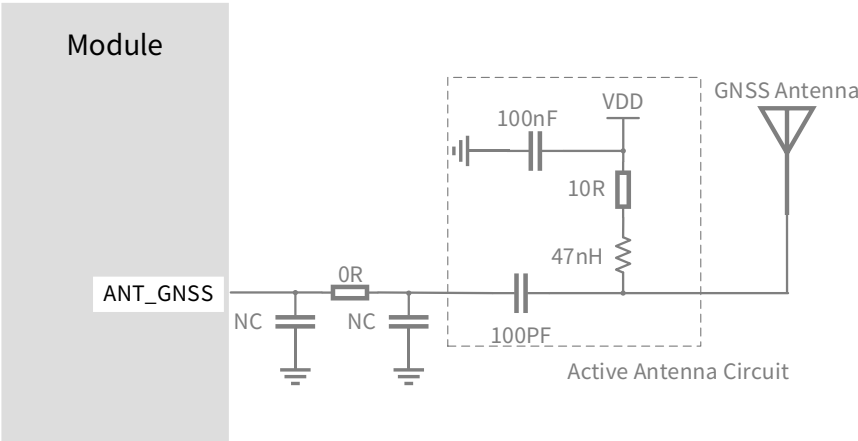


Figure 24. GNSS antenna reference circuit

5.4 Antenna Performance Requirements

Standard	Antenna Performance Requirement
WCDMA/LTE/NR	VSWR: ≤ 2
	Gain (dBi): 1
	Max input power (W): 5
	Input impedance (Ω): 50
	Polarization type: vertical direction
	Insertion loss: $< 1\text{dB}$ (0.7GHz to 1GHz)
	Insertion loss: $< 1.5\text{dB}$ (1.4GHz to 2.2GHz)
Wi-Fi/BT	Insertion loss: $< 2\text{dB}$ (2.3GHz to 5GHz)
	VSWR: ≤ 2
	Gain (dBi): 1
	Max input power (W): 5
	Input impedance (Ω): 50
GNSS	Polarization type: vertical direction
	Insertion loss: $< 2\text{dB}$
	Frequency range: 1559MHz to 1607MHz
	Polarization type: right-circular or linear polarization
	VSWR: < 2 (typical value)
	Passive antenna gain: $> 0\text{ dBi}$
Isolation between GPS and MAIN	Active antenna NF: $< 1.5\text{ dB}$ (typical value)
	Active antenna gain: $> -2\text{ dBi}$

Standard	Antenna Performance Requirement
antennas:	
Isolation between Wi-Fi and MAIN antennas:	> 20 dB

5.5 PCB Layout Reference Design

In practical applications, the shorter the RF microstrip trace, the better. Impedance is usually closely related to the width (W) and thickness of the trace, the height (H) of the reference layer, the spacing (S) between the trace and the left and right sides of the ground, and the dielectric constant of the material. The impedance control model of RF microstrip line is divided into planar reference model and coplanar impedance model. Generally, if the planar reference model can meet the requirements, the coplanar impedance model should not be used.

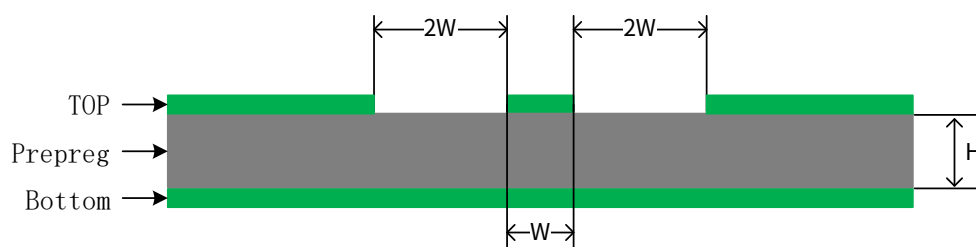


Figure 25. Planar reference model for a two-layer board

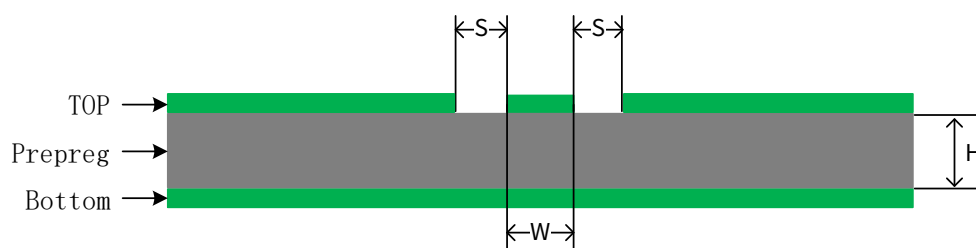


Figure 26. Coplanar impedance model for a two-layer board

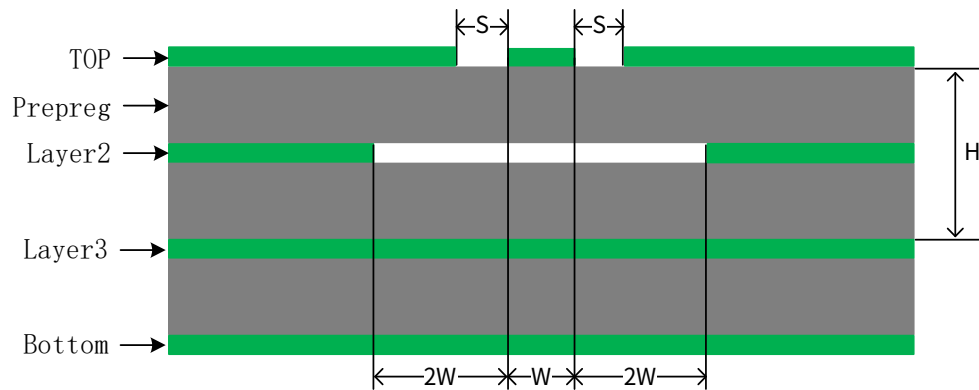


Figure 27. Coplanar impedance model for a four-layer board

The design rules are as follows:

- The RF trace impedance is controlled to 50Ω , and the reference ground must be kept intact.
- The RF routing should be curved as far as possible, and both sides of the routing should be protected by vias. The distance between vias and traces should be greater than 2 times the line width.
- There should be clearance below the RF connector, and the RF routing should be far away from the interference source to avoid crossing and paralleling with the interference source.

6 Wi-Fi&Bluetooth

6.1 Wi-Fi Overview

The module supports 2.4G and 5G WLAN wireless communication, and supports standards such as 802.11a, 802.11b, 802.11g, 802.11n, and 802.11ac, with a maximum speed of 433Mbps. Its characteristics are as follows:

- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 Wi-Fi Performance Index

Test conditions: Supply voltage of 3.8V, ambient temperature of 25°C.

Table 50. Wi-Fi TX Power

Frequency	Standard	Speed	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17±3
		11Mbps	20	17±3
	802.11g	6Mbps	20	16±3
		54Mbps	20	13±3
	802.11n	MCS0	20	15±3
		MCS7	20	13±3
		MCS0	40	14±3
		MCS7	40	12±3
5G	802.11a	6Mbs	20	16±3
		54Mbps	20	14±3
	802.11n	MCS0	20	15±3
		MCS7	20	12±3
		MCS0	40	14±3
		MCS7	40	12±3
	802.11ac	MCS0	20	15±3
		MCS8	20	12±3
		MCS0	40	14±3

Frequency	Standard	Speed	Bandwidth (MHz)	TX Power (dBm)
		MCS9	40	11±3
		MCS0	80	13±3
		MCS9	80	9±3

Table 51. Wi-Fi receiver sensitivity

Frequency	Standard	Speed	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-88
		11Mbps	20	-83
	802.11g	6Mbps	20	-88
		54Mbps	20	-71
	802.11n	MCS0	20	-88
		MCS7	20	-70
		MCS0	40	-85
		MCS7	40	-68
5G	802.11a	6Mbps	20	-89
		54Mbps	20	-74
	802.11n	MCS0	20	-89
		MCS7	20	-69
		MCS0	40	-85
		MCS7	40	-65
	802.11ac	MCS0	20	-89
		MCS8	20	-66
		MCS0	40	-86
		MCS9	40	-62
		MCS0	80	-82
		MCS9	80	-57

6.3 Bluetooth Overview

The module supports the BT5.0 (BR/ADR+BLE) specification, with modulation methods supporting GFSK, 8-DPSK, and $\pi/4$ -DQPSK. The BR/EDR channel bandwidth is 1MHz and can accommodate 79 channels; The BLE channel has a bandwidth of 2MHz and can accommodate 40 channels. Its main characteristics are as follows:

- BT 5.0 + BR/EDR + BLE

- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave, and page scanning)

Table 52. BT speed and version information

Version	Speed	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	--
BT2.0+EDR	3Mbit/s	> 80Kbit/s	--
BT3.0+HS	24Mbit/s	Please refer to 3.0+HS	--
BT4.2 LE	24Mbit/s	Please refer to 4.2 LE	--
BT5.0	24Mbit/s	Please refer to 5.0	--

6.4 Bluetooth Performance Index

Test conditions: Supply voltage of 3.8V, ambient temperature of 25°C.

Table 53. BT performance index

Type	DH-5	2-DH5	3-DH5	BLE	Unit
TX Power	10±3	9±3	9±3	6±3	dBm
Sensitivity	-84	-82	-80	-88	dBm



The sensitivity here is a typical value.

7 GNSS

7.1 Overview

The intelligent module supports GPS/ GLONASS /BeiDou positioning systems. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS.

7.2 Performance Index

Test conditions: Supply voltage of 3.8V, ambient temperature of 25°C.

Table 54. GNSS positioning performance

Parameter	Description	Measurement value	Unit
RX Sensitivity	Acquisition	-144	dBm
	Tracking	-157	dBm
SNR	-130 dBm	39	dB-Hz
First positioning time	Cold Start	44	s
	Warm Start	44	s
	Hot Start	3	s
Positioning accuracy	Static accuracy (95% @-130dbm)	5	m

8 Electrical Characteristics

8.1 Operating Voltage

The following table shows the normal operating voltage range of the module, and all performance indicators of the module are guaranteed within this operating voltage range.

Table 55. Operating Voltage

Power	Min.	Typical	Max.	Unit
VBAT	3.5	3.8	4.4	V
VBUS_USB_DET	3	5.0	18	V

8.2 Maximum Voltage

The following table shows the absolute maximum rated parameters of the module. Exceeding the absolute maximum parameter range may cause permanent damage to the equipment.

Table 56. Maximum voltage

Power	Min.	Max.	Unit
VBAT	-0.3	5	V

8.3 Working and Storage Temperature

Table 57. Working and storage temperature

Item	Min.	Max.	Unit
Working ambient temperature	-30	75	°C
Storage temperature	-40	85	°C

8.4 Power Consumption

The power consumption measurement is closely related to the operating state of the module, and the test conditions are as follows:

The ambient temperature is 25°C, the power supply voltage is 3.8V.

Table 58. Power consumption (mA)

Parameter	Description	Condition	Typical Result	Unit
I _{off}	Static leakage current	Leakage current before power on	110	uA
	Software power-off	The module is powered on,	100	

Parameter	Description	Condition	Typical Result	Unit
	leakage current	and then powered off by AT commands or selecting an option from the pop-up box.		
I_{sleep}	Radio Off	Airplane mode standby status	4.5	mA
	LTE FDD	DPC (Default Paging Cycle)=#256	8	
	LTE TDD	DPC (Default Paging Cycle)=#256	8	
$I_{\text{LTE-RMS}}$	LTE FDD RMS Current	Band 2@max power(10MHz,1RB)	720	mA
		Band 4 @max power(10MHz,1RB)	720	
		Band 5 @max power(10MHz,1RB)	700	
		Band 7 @max power(10MHz,1RB)	870	
		Band 12 @max power(10MHz,1RB)	710	
		Band 13 @max power(10MHz,1RB)	700	
		Band 17 @max power(10MHz,1RB)	710	
		Band 25 @max power(10MHz,1RB)	720	
		Band 26 @max power(10MHz,1RB)	700	
		Band 66 @max power(10MHz,1RB)	720	
		Band 71 @max power(10MHz,1RB)	650	
	LTE TDD RMS Current	Band 41 @max power(10MHz,1RB)	460	mA

8.5 Maximum Transmit Power

The maximum transmit power is the transmit power measured at the antenna pin at an ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when designing, so as to avoid excessive insertion loss affecting TRP indicators. The maximum transmit power of the module

is as follows:

Test condition: 3.8V power supply, environment temperature 25°C, LTE power test performed with 10 MHz, 12RB bandwidth.

Table 59. Maximum transmit power (dBm)

Mode	Band	Maximum Power (dBm)	Minimum Power (dBm)
LTE FDD	Band 2	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39
	Band 7	23.0±2	<-39
	Band 12	23.0±2	<-39
	Band 13	23.0±2	<-39
	Band 17	23.0±2	<-39
	Band 25	23.0±2	<-39
	Band 26	23.0±2	<-39
	Band 66	23.0±2	<-39
	Band 71	23.0±2	<-39
LTE TDD (10MHz)	Band 41	23.0±2	<-39

8.6 Receiver Sensitivity

Receiver sensitivity is the receiver sensitivity of the module measured at the antenna pin at an ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when designing, so as to avoid excessive insertion loss affecting TIS indicators. The receiver sensitivity of the module is as follows:

Test condition: 3.8V power supply, environment temperature 25°C, LTE power test performed with 10 MHz bandwidth. For RB configuration, see 3GPP standard.

Table 60. RF receiver sensitivity (dBm)

Mode	Band	Main Antenna	Diversity Antenna	Main+Diversity Antenna	3GPP Standard	Unit
LTE FDD (10MHz)	Band 2	-98	-98.5	-100.5	-94.3	dBm
	Band 4	-97	-98.5	-99.5	-96.3	dBm
	Band 5	-98	-98.5	-100.5	-94.3	dBm
	Band 7	-95.5	-97.5	-98	-94.3	dBm
	Band 12	-98	-98.5	-100	-93.3	dBm

Mode	Band	Main Antenna	Diversity Antenna	Main+Diversity Antenna	3GPP Standard	Unit
	Band 13	-97.5	-98.5	-100	-93.3	dBm
	Band 17	-98	-98.5	-100	-93.3	dBm
	Band 25	-98	-98.5	-100	-92.8	dBm
	Band 26	-98	-98	-100	-93.8	dBm
	Band 66	-97	-98	-99.5	-95.8	dBm
	Band 71	-98	-98.5	-100	-93.5	dBm
LTE TDD	Band 41	-96.5	-97.5	-99	-94.3	dBm

8.7 Electrostatic Protection

The module is a precise electronic product. If electrostatic protection measures are not taken, permanent damage may be caused to the module. In the process of R&D, debugging, production, assembly, testing and other links, ESD protection measures should be taken. The ESD protection level at 25°C ambient temperature and 45% humidity is described in the following table.

Table 61. ESD protection level

Location	Air Discharge	Contact Discharge
VBAT, GND	±10KV	±5KV
Antenna interface	±10KV	±5KV



1. The data is tested based on the development board of Fibocom.
2. ESD performance is strongly related to PCB design, and key control signals should be protected.
3. When designing the whole machine, pay attention to maintaining the integrity and connectivity of GND.

8.8 Reliability

The reliability test of Fibocom is carried out at industrial level, please refer to *Fibocom_SC206_Reliability Test Report* for the reliability test results.

8.9 Thermal Design

For more thermal design guidance, see *Fibocom_Module General Thermal Design Guide*.

9 Structural Specifications

9.1 Product Appearance



Figure 28. Product appearance

9.2 Structural Dimensions

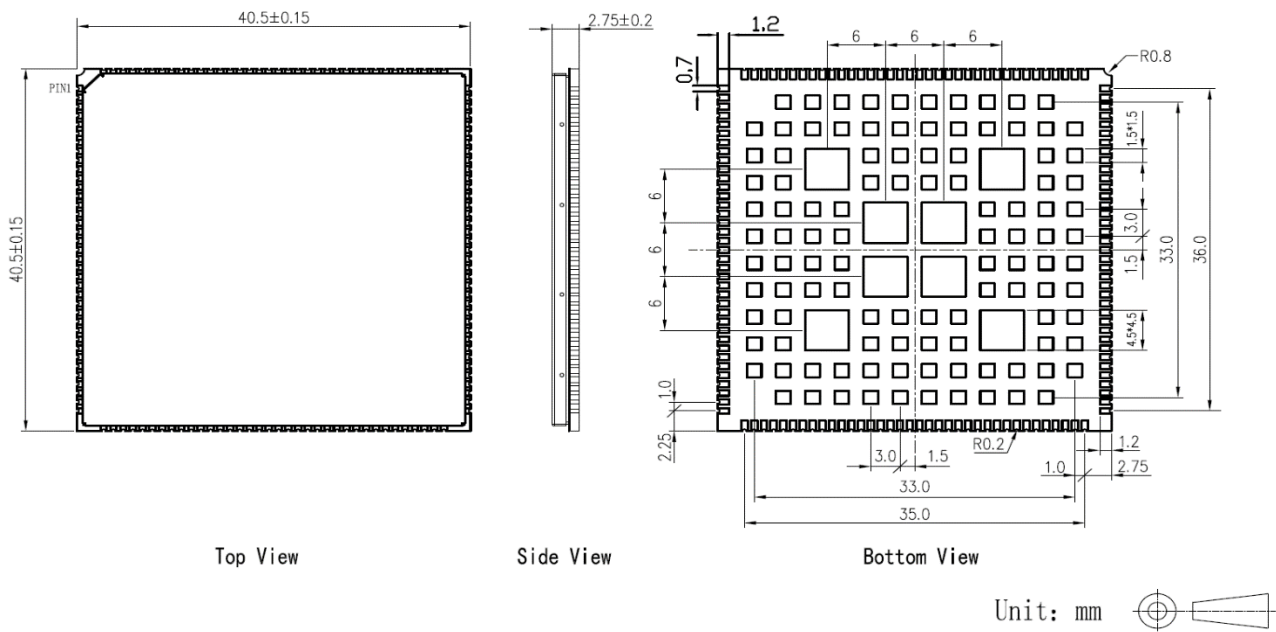


Figure 29. Structural Dimensions (unit: mm)

9.3 PCB Package

Fibocom provides users with a designed *Fibocom_SC206_Package*, which can be found in the package.

10 Storage, Production and Packaging

For storage, production, and packaging, see *Fibocom_SC206_SMT Design Guide*.

Appendix A Reference Documents

Category	Document Name
Reference Design	Fibocom_SC206_Package
	Fibocom_SC206_ADP User Guide
Development kit	Fibocom_EVKB-SOC_User Guide
	Fibocom_SC206_SMT Design Guide
	Fibocom_Module General Thermal Design Guide

Appendix B Acronyms and Abbreviations

Acronyms and Abbreviations	Description
AR	Augmented Reality
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Down Link
DLCA	Down Link Carrier Aggregation
ECC	Envelope Correlation Coefficient
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	Multiple-input and multiple-output
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board

Acronyms and Abbreviations	Description
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VSWR	Voltage Standing Wave Ratio
VR	Virtual Reality
WCDMA	Wideband Code Division Multiple Access