PERFECT WIRELESS EXPERIENCE

FIBOCOM SQ806-W Series Hardware Guide

Version: V1.0.3

Date: 2021-06-02

Applicability Type

No.	Product Model	Description
1	SQ806-W	1 GB +8 GB eMCP, WIFI version

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Change History

Version	Author	Reviewer	Approver	Date	Description
V1.0.3	GaoTianhuan He Ruzhi	Tu Min Li Xiyi	Chen Guojiang	2021-06-02	● Change FTM power consumption and BLE parameters ● Add product model of SQ806-W-10
V1.0.2	Ma Menghan	Ma Menghan	Luo Qin	2020-12-30	Standardized the document format, corrected errors found in the document, including grammar, spelling, etc., and optimized the sentence structure.
V1.0.1	Gao Tianhuan He Ruzhi	Tu Min Li Xiyi	Chen Guojiang	2020-08-25	Supplement product appearance drawings and TBD data
V1.0.0	Gao Tianhuan He Ruzhi	Tu Min Li Xiyi	Chen Guojiang	2020-04-14	Initial version

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1 Introduction

1.1 Instruction

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SQ806-W series module (hereinafter referred to as module). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

This product has been designed with the following standards.

- *IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11ac, IEEE Std 802.11i*
- *IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007*
- *IEEE 802.11-2007 WLAN MAC and PHY, June 2007*
- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 +*
- *HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*

1.3 Related Document

FIBOCOM SQ806 Series SMT Design Guide

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2 Product Overview

2.1 General Description

SQ806-W-00 module integrates core components such as Baseband, eMCP, PMU, etc; it supports WIFI/BT short-distance radio transmission technology. The module is embedded with Android operating system and supports various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 2-1 SQ806-W supported bands

Mode	Band
WIFI 802.11 a/b/g/n/ac	2402 - 2482 MHz; 5125 - 5835MHz
BT4.2	2402 - 2480 MHz

2.2 Main Performance

The module is available in 262 LCC + LGA package that includes 146 LCC pins and 116 LGA pins. The dimension is 40.5mm × 40.5mm × 2.8mm. It can provide a stable and reliable connection between the industrial, consumer and automotive sectors. The following table describes the detailed performance parameters of the module.

Table 2-2 Performance parameter

Performance	Description
Power	DC 3.5~4.2V, typical voltage: 3.8V
Application CPU	Arm Cortex-A53 microprocessor, 64-bit, Quad-core (1.3 GHz)
Memory	SQ806-W-00: 1GB LPDDR3+ 8 GB eMMC Flash SQ806-W-10: 2GB LPDDR3+ 16 GB eMMC Flash

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Performance	Description
WLAN features	Support 2.4G and 5G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, maximum rate up to 433Mbps
Bluetooth features	BT4.2 (BR/EDR + BLE)
LCD interface	4 Lane MIPI_DSI interface Support maximum HD+ (1440 * 720) 60 fps
Camera interface	Two 4 Lane MIPI_CSI interface, up to 2.1Gbps per lane, support 2 or 3 cameras Up to 13 MP, using dual ISP
Audio interface	Audio Input: 3 analog microphone inputs Integrated internal bias Audio output: Class AB stereo headphone output Class AB differential receiver output Class D differential speaker amplifier output
USB interface	USB2.0 HS interface, with data transfer rate up to 480 Mbps Support USB OTG (external 5V power supply)
UART interface	Three UART serial interfaces, with maximum rate up to 4Mbps One 4-line serial interface supporting RTS and CTS hardware flow control One 2-line serial interface One 2-line debug serial interface
SD interface	Support SD 3.0, 4bit SD; SD card supports hot plug
I2C interface	Multiple I2C interfaces, and can be used for peripherals such as TP, Camera, and Sensor
ADC interface	Universal ADC
RTC clock	Support

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Performance	Description
Antenna interface	WIFI/BT antenna
Physical characteristics	Dimension: 40.5mm × 40.5mm × 2.8mm Encapsulation: 146 LCC pins + 116 LGA pins Weight: 9.6 ± 0.1g
Temperature range	Operating temperature: -30°C - 75°C [1)] Storage temperature: -40°C - 85°C
Software update	USB/OTA/SD
RoHS	RoHS Compliant

Note:

1) When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the IEEE standard.

2.3 Function Block Diagram

Function diagram shows the main hardware features of the SQ806-W-00 module, including:

- Baseband
- Wireless transceiver
- PMU
- Memory
- Peripheral interface
  - Communication expansion interface (USB/UART/I2C/SD/SPI)
  - MIPI DSI interface
  - MIPI CSI Interface
  - Analog audio interface

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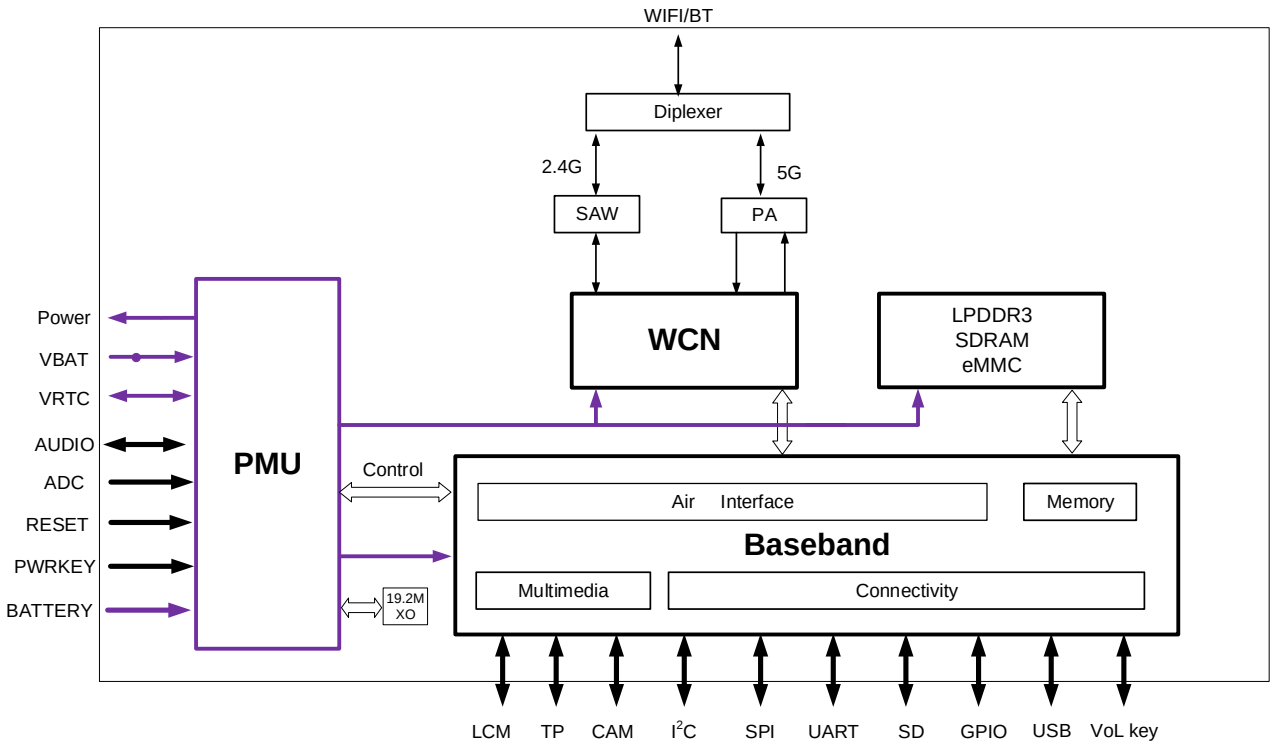

Figure 2-1 Function block diagram

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2.4 Pin Definitions

2.4.1 Pin Assignment

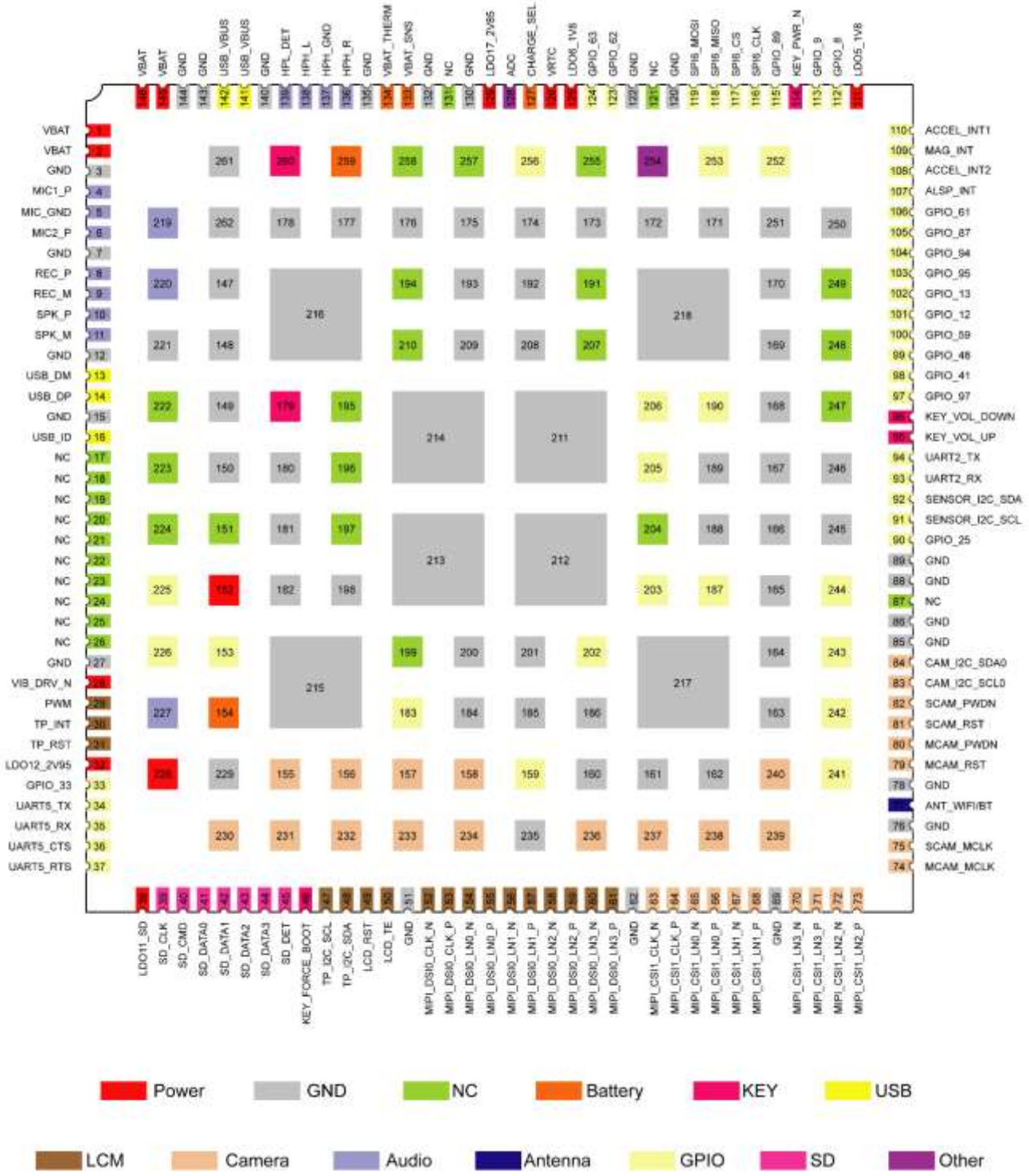

Figure 2-2 Pin assignment

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Note:

"NC" stands for "No Connect", that is, the pin does not have network to be connected.

2.4.2 Pin Description

Table 2-3 I/O parameters description

Type	Description
IO	Input/Output
DI	Digital Input
DO	Digital Output
PI	Power Input
PO	Power Output
AI	Analog Input
AO	Analog Output
OD	Open Drain

Module pins are described in the following table:

Table 2-4 Pin description

Pin Name	Pin #	I/O	Pin Description	Note
Power				
VBAT	1, 2, 145, 146	PI	Main power input	-
VRTC	126	PI/PO	RTC clock power supply	-
LDO5_1V8	111	PO	1.8V voltage output	-
LDO6_1V8	125	PO	1.8V voltage output	-
LDO10_2V85	228	PO	2.85V voltage output	-
LDO11_SD	38	PO	SD card power supply, 2.95V	-

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Pin Name	Pin #	I/O	Pin Description	Note
LDO12_2V95	32	PO	2.95V voltage output	-
LDO16_2V8	152	PO	2.8V voltage output	-
LDO17_2V85	129	PO	2.85V voltage output	-
VIB_DRV_N	28	PO	Motor driver output control	-
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 147, 148, 149, 150, 160~178, 180~182, 184~186, 188, 189, 192, 193, 198, 200, 201, 208, 209, 211~218, 221, 235, 245, 246, 250, 251, 262			ground
Battery Supply Interface				
BAT_ID	260	AI	Battery ID pin	-
CHARGE_SEL	127	DI	Charging path select	External charge: please connect this pin to ground; Internal charge: keeps it suspending
VBAT_SNS	133	AI	Battery voltage detection	-
VBAT_THERM	134	AI	Battery temperature detection	-
CHG_LED_SINK_N	154	AO	Charge LED	-
Key				
KEY_FORCE_BOOT	46	DI	Forced download pin	High level effective,1.8V
KEY_VOL_UP	95	DI	Volume + key	Low level effective, cannot pull up before module power on
KEY_VOL_DOWN	96	DI	Volume - key	Low level effective. Used as a volume

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Pin Name	Pin #	I/O	Pin Description	Note
				down key by default and can be configured for low-level shutdown and restart
KEY_PWR_N	114	DI	Power key	Low level effective
KEY_RESET_N	179	DI	Reset Key	Low level effective
KEY_CBL_PWR_N	261	DI	CBL Power key	Low level effective
SD Card Interface				
SD_DET	45	DI	SD card detection	Low level effective by default
SD_DATA3	44	I/O	SD card data interface	-
SD_DATA2	43	I/O	SD card data interface	-
SD_DATA1	42	I/O	SD card data interface	-
SD_DATA0	41	I/O	SD card data interface	-
SD_CMD	40	I/O	SD card command interface	-
SD_CLK	39	DO	SD card clock	-
I2C Interface				
SENSOR_I2C_SCL	91	OD	Sensor I2C clock	-
SENSOR_I2C_SDA	92	OD	Sensor I2C data cable	-
TP_I2C_SCL	47	OD	TP I2C clock	-
TP_I2C_SDA	48	OD	TP I2C data cable	-
CAM_I2C_SCL0	83	OD	Camera I2C clock	Cannot be used as I2C and GPIO for other devices
CAM_I2C_SDA0	84	OD	Camera I2C data cable	
CAM_I2C_SCL1	239	OD	Camera I2C clock	
CAM_I2C_SDA1	240	OD	Camera I2C data cable	
USB Interface				
USB_VBUS	141, 142	PI	5V input	-

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Pin Name	Pin #	I/O	Pin Description	Note
USB_DP	14	AI/AO	USB 2.0 differential data signal +	-
USB_DM	13	AI/AO	USB 2.0 differential data signal -	-
USB_ID	16	DI	USB OTG detection pin	-
UART Interface				
UART5_TX	34	DO	UART5 data transmission	-
UART5_RX	35	DI	UART5 data reception	-
UART5_CTS	36	DI	UART5 clear to send	-
UART5_RTS	37	DO	UART5 request to send	-
UART2_TX	94	DO	UART2 data transmission	Use as debug serial port by default
UART2_RX	93	DI	UART2 data reception	
UART4_TX	226	DO	UART4 data transmission	-
UART4_RX	225	DI	UART4 data reception	-
SPI Interface				
SPI6_CLK	116	DO	SPI clock	-
SPI6_CS	117	DO	SPI chip select	-
SPI6_MISO	118	DI	SPI Master input Slave output	-
SPI6_MOSI	119	DO	SPI Master output Slave input	-
LCD Interface				
MIPI_DSI0_CLK_N	52	AO	LCD MIPI differential clock signal	-
MIPI_DSI0_CLK_P	53	AO		-
MIPI_DSI0_LN0_N	54	AO	LCD MIPI differential data signal	-
MIPI_DSI0_LN0_P	55	AO		-
MIPI_DSI0_LN1_N	56	AO		-
MIPI_DSI0_LN1_P	57	AO		-
MIPI_DSI0_LN2_N	58	AO		-

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Pin Name	Pin #	I/O	Pin Description	Note
MIPI_DSI0_LN2_P	59	AO		-
MIPI_DSI0_LN3_N	60	AO		-
MIPI_DSI0_LN3_P	61	AO		-
LCD_RST_N	49	DO	LCD reset signal	-
PWM	29	DO	LCD backlight PWM control signal	-
LCD_TE	50	DI	LCD swipe synchronization signal	Keep it suspending when not in use
Touch Panel Interface				
TP_INT	30	DI	Main touch panel TP interrupt signal	-
TP_RST	31	DO	Main touch panel TP reset signal	-
Camera Interface				
MIPI_CSI0_CLK_P	229	AI	Rear camera MIPI differential clock signal +	-
MIPI_CSI0_CLK_N	230	AI	Rear camera MIPI differential clock signal -	-
MIPI_CSI0_LN0_P	155	AI	Rear camera MIPI differential data signal +	-
MIPI_CSI0_LN0_N	231	AI	Rear camera MIPI differential data signal -	-
MIPI_CSI0_LN1_P	156	AI	Rear camera MIPI differential data signal +	-
MIPI_CSI0_LN1_N	232	AI	Rear camera MIPI differential data signal -	-
MIPI_CSI0_LN2_P	157	AI	Rear camera MIPI differential	-

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Pin Name	Pin #	I/O	Pin Description	Note
			data signal +	
MIPI_CSI0_LN2_N	233	AI	Rear camera MIPI differential data signal -	-
MIPI_CSI0_LN3_P	158	AI	Rear camera MIPI differential data signal +	-
MIPI_CSI0_LN3_N	234	AI	Rear camera MIPI differential data signal -	-
MCAM_MCLK	74	DO	Rear camera main clock signal	-
MCAM_RST	79	DO	Rear camera reset signal	-
MCAM_PWDN	80	DO	Rear camera shutdown signal	-
MIPI_CSI1_CLK_P	64	AI	Front camera MIPI differential clock signal +	CSI1's 4 Lane can be configured as 2 Lane camera + 1 Lane camera
MIPI_CSI1_CLK_N	63	AI	Front camera MIPI differential clock signal -	
MIPI_CSI1_LN0_P	66	AI	Front camera MIPI differential data signal +	
MIPI_CSI1_LN0_N	65	AI	Front camera MIPI differential data signal -	
MIPI_CSI1_LN1_P	68	AI	Front camera MIPI differential data signal +	
MIPI_CSI1_LN1_N	67	AI	Front camera MIPI differential data signal -	
MIPI_CSI1_LN2_P	73	AI	Front camera MIPI differential data signal +	
MIPI_CSI1_LN2_N	72	AI	Front camera MIPI differential data signal -	

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Pin Name	Pin #	I/O	Pin Description	Note
MIPI_CSI1_LN3_P	71	AI	Front camera MIPI differential data signal +	
MIPI_CSI1_LN3_N	70	AI	Front camera MIPI differential data signal -	
SCAM_MCLK	75	DO	Front camera main clock signal	-
SCAM _RST	81	DO	Front camera reset signal	-
SCAM _PWDN	82	DO	Front camera shutdown signal	-
DCAM_MCLK	238	DO	Depth of field camera MCLK signal	-
DCAM _RST	237	DO	Depth of field camera reset signal	-
DCAM _PWDN	236	DO	Depth of field camera shutdown signal	-
Audio Interface				
SPK_P	10	AO	Loudspeaker differential output +	-
SPK_M	11	AO	Loudspeaker differential output -	-
REC_P	8	AO	Receiver differential output +	-
REC_M	9	AO	Receiver differential output -	-
HPH_L	138	AO	Earphone left channel output	-
HPH_GND	137	-	Earphone reference ground	-
HPH_R	136	AO	Earphone right channel output	-
HPH_DET	139	AI	Earphone plug detection	-

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Pin Name	Pin #	I/O	Pin Description	Note
MIC2_P	6	AI	Earphone MIC input	-
MIC_GND	5	-	MIC ground	-
MIC1_P	4	AI	Main MIC input	-
MIC_BIAS1	219	AO	MIC bias 1	-
MIC3_P	220	AI	Secondary MIC input	-
MIC_BIAS2	227	AO	MIC bias 2	-
Antenna Interface				
ANT-WIFI/BT	77	I/O	WIFI/BT antenna	-
INT Interface				
ALSP_INT	107	DI	Ambient light sensor interrupt	-
ACCEL_INT2	108	DI	Accelerometer sensor interrupt 2	-
MAG_INT	109	DI	Magnetic sensor interrupt	-
ACCEL_INT1	110	DI	Accelerometer sensor interrupt 1	-
Other Interfaces				
ADC	128	AI	ADC detect pin	-
NFC_CLK	256	DO	NFC clock signal	-
NFC_DWL_REQ	257	DI	NFC power reset control pin	-
GPIO Interface				
GPIO_33	33	I/O	General GPIO. 1.8V power domain	B-PD: nppukp
GPIO_25	90	I/O		B-PD: nppukp
GPIO_97	97	I/O		B-PD: nppukp
GPIO_41	98	I/O		B-PD: nppukp
GPIO_48	99	I/O		B-PD: nppukp
GPIO_59	100	I/O		B-PD: nppukp
GPIO_12	101	I/O		B-PD: nppukp

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Pin Name	Pin #	I/O	Pin Description	Note
GPIO_13	102	I/O		B-PD: nppukp
GPIO_95	103	I/O		B-PD: nppukp
GPIO_94	104	I/O		B-PD: nppukp
GPIO_87	105	I/O		B-PD: nppukp
GPIO_61	106	I/O		B-PD: nppukp
GPIO_8	112	I/O		B-PD: nppukp, Boot configuration
GPIO_9	113	I/O		B-PD: nppukp, Boot configuration
GPIO_89	115	I/O		B-PD: nppukp
GPIO_62	123	I/O		B-PD: nppukp
GPIO_63	124	I/O		B-PD: nppukp, Boot configuration
GPIO_2	153	I/O		B-PD: nppukp
GPIO_46	159	I/O		B-PD: nppukp
GPIO_50	183	I/O		B-PD: nppukp
GPIO_86	187	I/O		B-PD: nppukp
GPIO_93	190	I/O		B-PD: nppukp
GPIO_81	202	I/O		B-PD: nppukp
GPIO_82	203	I/O		B-PD: nppukp
GPIO_88	205	I/O		B-PD: nppukp, Boot configuration
GPIO_66	206	I/O		B-PD: nppukp
GPIO_6	241	I/O		B-PD: nppukp
GPIO_7	242	I/O		B-PD: nppukp
GPIO_127	243	I/O		B-PD: nppukp
GPIO_34	244	I/O		B-PD: nppukp

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Pin Name	Pin #	I/O	Pin Description	Note
GPIO_90	252	I/O		B-PD: nppukp
GPIO_106	253	I/O		B-PD: nppukp, Boot configuration
GPIO_104	254	I/O		B-PD: nppukp
NC Interface				
NC	17~26, 87, 121, 131, 151, 191, 194~197, 199, 204, 207, 210, 222~224, 247~249, 255, 258, 259	NC		Keep it suspending

Note:

Note that GPIOs with Boot configuration disable hardware pull-ups.

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3 Application Interface

3.1 Power Supply

The module provides four VBAT pins for connecting to external power supply source. The input range of power is 3.5V~4.2V and the recommended value is 3.8V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. In extreme cases, the peak current of the module can reach 2A and if the power supply capacity is insufficient that VBAT voltage instantaneous drops below 3V, the module may be powered off or restarted. The VBAT voltage drop is as follows:

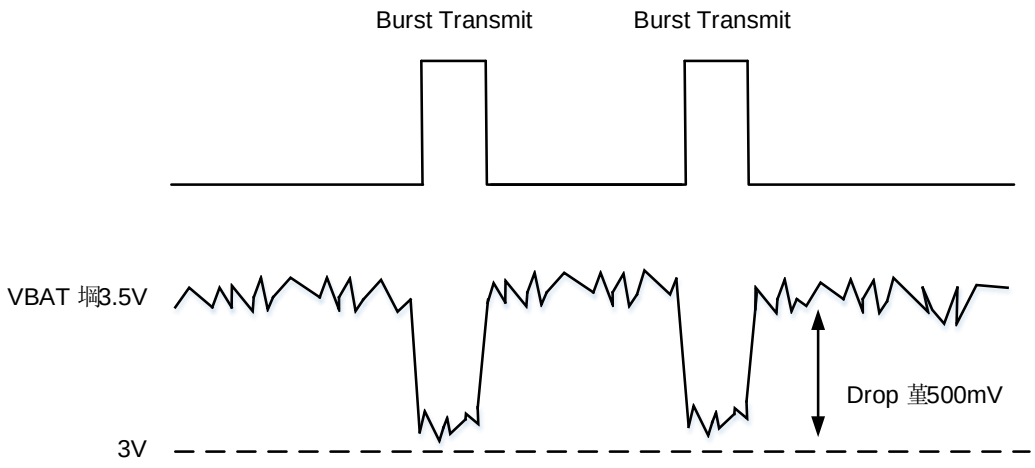

Figure 3-1 VBAT voltage drop

3.1.1 Power Input

External power source supplies the module by VBAT pins. To ensure the instantaneous voltage is no less than 3V, it is recommended to connect two 220μF tantalum capacitors with low ESR and filter capacitors of 1uF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides, the PCB cable of VBAT should be as short and wide as possible (no narrow than 3mm) and the ground plane of the power section should be flat. That can reduce the equivalent impedance of the VBAT cable and ensure at maximum transmit power, significant voltage drop will not occur at high currents.

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Table 3-1 Power supply

Parameter	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.2	V

The reference design of power supply circuit is as follows:

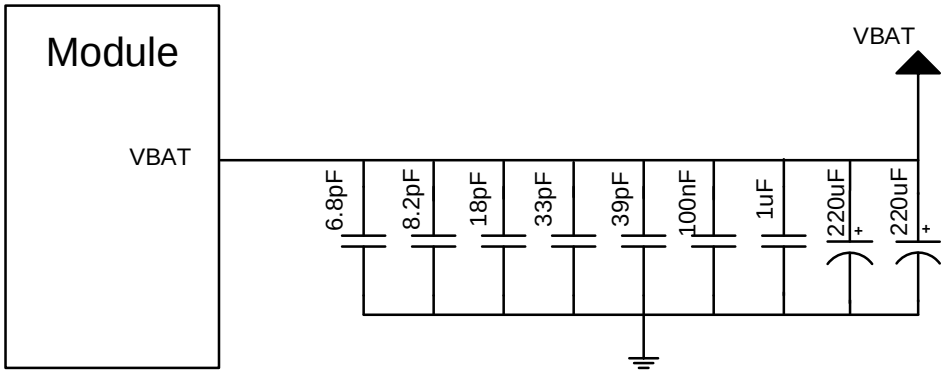

Figure 3-2 Power supply circuit reference design

The filter capacitor design for the power supply is shown in the table below:

Table 3-2 Power supply filter capacitor design

Recommended Capacitor	Application	Description
220uF x 2	Voltage stabilizing capacitor	To reduce power fluctuations during module operation, it is required to adopt low ESR capacitor LDO or DCDC power requires no less than 440uF capacitor Battery power can be properly reduced to 100 ~ 220uF capacitor
1uF, 100nF	Filter capacitor	Filter clock and digital signal interference
39pF, 33pF, 18pF, 8.2pF, 6.8pF	Decoupling capacitor	Filter high frequency interference

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3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When powered on VBAT pin, the VRTC pin will output voltage. When VBAT is disconnected, if the real-time clock needs to be maintained, it needs to be powered by an external power source (such as a coin battery). The VRTC parameters are as follows:

Table 3-3 VRTC parameters

Parameter	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.5	3.1	3.2	V
VRTC input voltage (clock works well)	2.0	3.0	3.25	V
VRTC input current (clock works well)	-	6	-	μA

The VRTC power supply uses the following reference circuit when powered by an external power source:

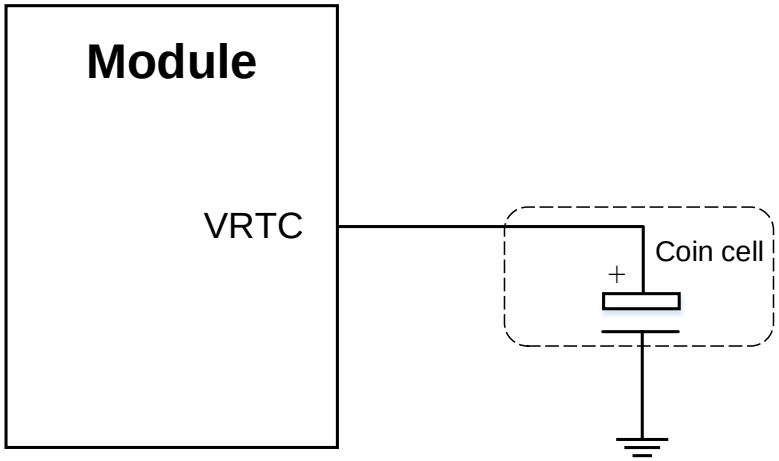

Figure 3-3 VRTC power reference circuit

3.1.3 Power Output

The module provides multiple power outputs for peripheral circuits. For applications, 33pF and 10pF capacitors can be connected in parallel to effectively remove high frequency interference.

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Table 3-4 Power output

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
LDO5_1V8	1.75~3.337	1.8	200
LDO6_1V8	1.75~3.337	1.8	150
LDO10_2V85	1.75~3.337	2.85	150
LDO11_SD	1.75~3.337	2.95	600
LDO12_2V95	1.75~3.337	2.95	50
LDO14_UIM1	1.75~3.337	1.8/3	55
LDO15_UIM2	1.75~3.337	1.8/3	55
LDO16_2V8	1.75~3.337	2.8	55
LDO17_2V85	1.75~3.337	2.85	450

3.2 Control Signal

3.2.1 Power On/Off

The module has two power-on control signals, which can power on/off, reboot, sleep/wake the module.

Table 3-5 Power on/off control signal

Pin Name	Pin #	I/O	Description	Note
KEY_PWR_N	114	DI	Low level effective, can be used to power on/off, restart, sleep/wakeup the module	-
KEY_CBL_PWR_N	261	DI	Low level effective, can be used to power on the module	Auto power on when grounded

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3.2.1.1 Power On

After module's VBAT pin is powered, pull down KEY_PWR_N pin 0.5s - 10s can trigger the module to power on. The keystroke power-up circuit and the OC drive power-up reference circuit are designed as follows:

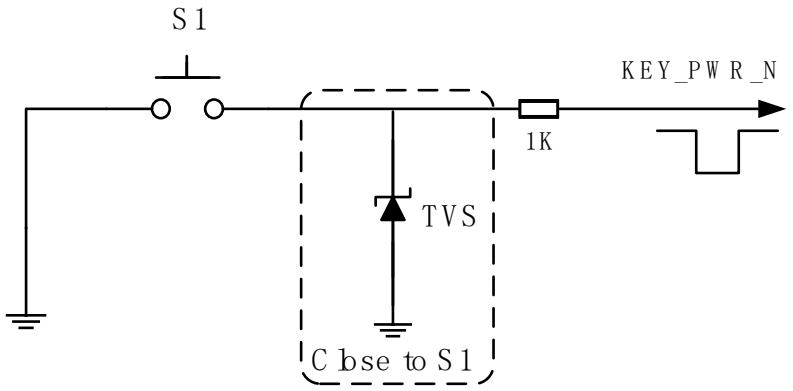

Figure 3-4 Keystroke power-up circuit

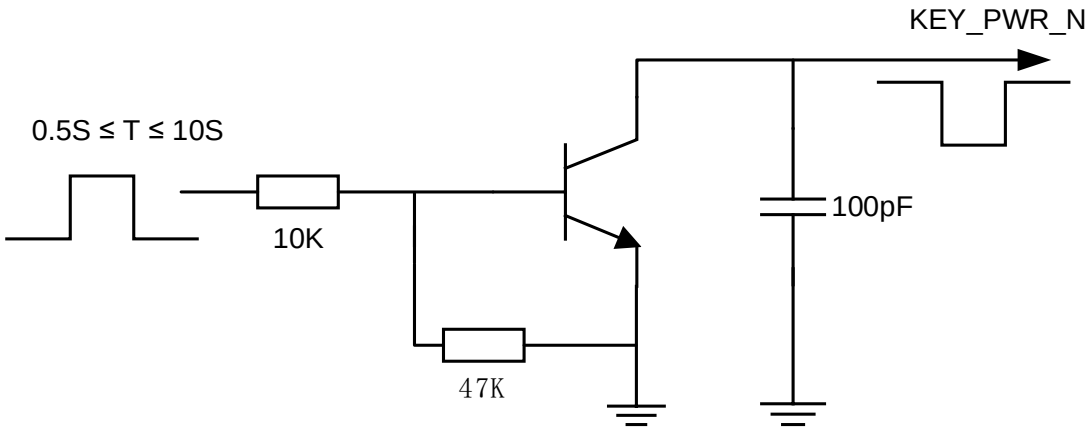

Figure 3-5 OC drive power-up circuit

The power on timing is as follows:

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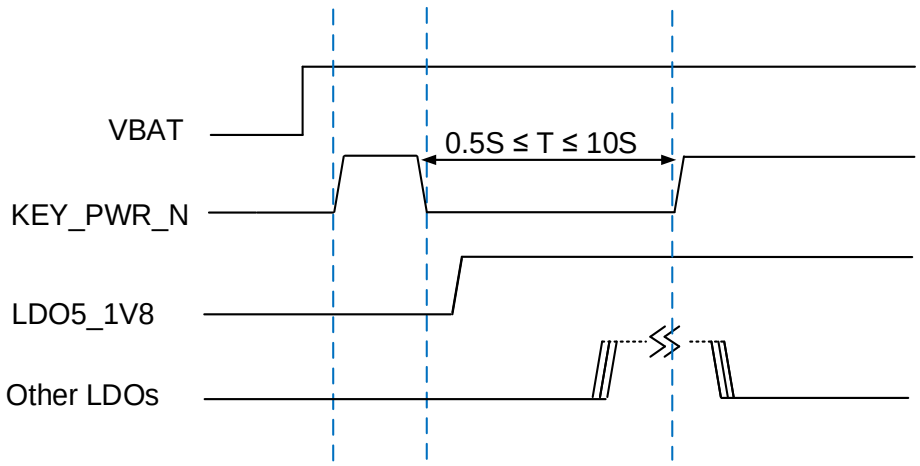

Figure 3-6 Power on timing

3.2.1.2 Power Off

Normal power off: when module is in operating mode, pull down KEY_PWR_N pin 0.6s and then release it, user interface will display selection box (select power off or restart).

Force power off: pull down KEY_PWR_N pin 9s - 15s, and the module will be forced power off. The forced power off timing is as follows:

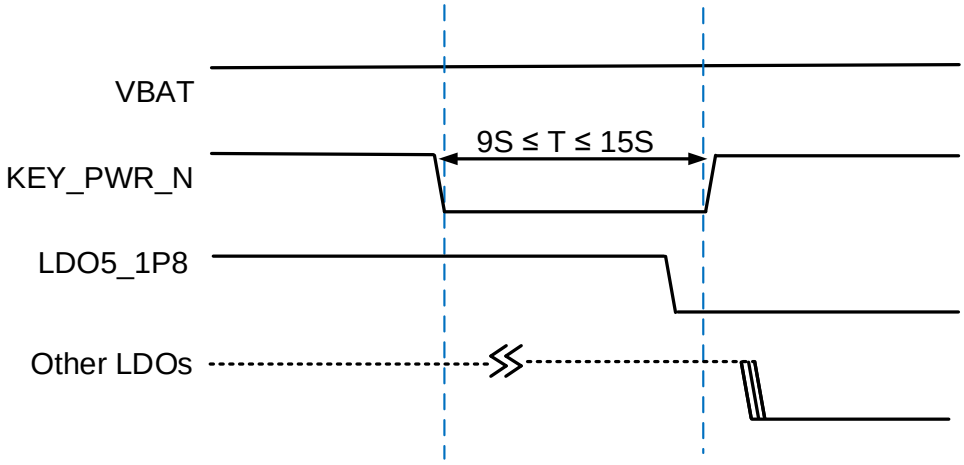

Figure 3-7 Power off timing

Note:

When the system is abnormal or shutdown, can use forced power off method to power off the module. In general, please use the normal shutdown method to power off, otherwise may cause data loss and other anomalies.

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3.2.1.3 Sleep/Wake up

When module is in standby mode, pull down KEY_PWR_N pin 0.1s and then release it, and the module will enter sleep mode. When module is in sleep mode, pull down KEY_PWR_N pin 0.1s and then release it, and the module can be woke up.

3.2.2 Volume Control

KEY_VOL_DOWN_N pin and KEY_VOL_UP_N pin are the volume down key and volume up key; the volume key circuit design can be referred to the power-on circuit design.

3.2.3 Reset

KEY_RESET_N is the reset input of the module PMIC. When the system crashes or other abnormalities occur, pull down KEY_ RESET _N pin 9s - 15s and then release it, the system will be forced to restart.

3.3 USB

The module supports one USB 2.0 interface; USB2.0 supports HS (480Mbps) mode and compatible USB1.1 FS (12Mbps). USB supports OTG function and HUB expansion interface; its pin definition is shown in the following table:

Table 3-6 USB2.0 pin definition

Pin Name	Pin #	I/O	Description	Note
USB_VBUS	141, 142	PI	5V input	-
USB_DP	14	I/O	USB differential signal +	-
USB_DM	13	I/O	USB differential signal -	-
USB_ID	16	AI	USB OTG detection	-

The USB 2.0 interface circuit reference design is shown in the following figure:

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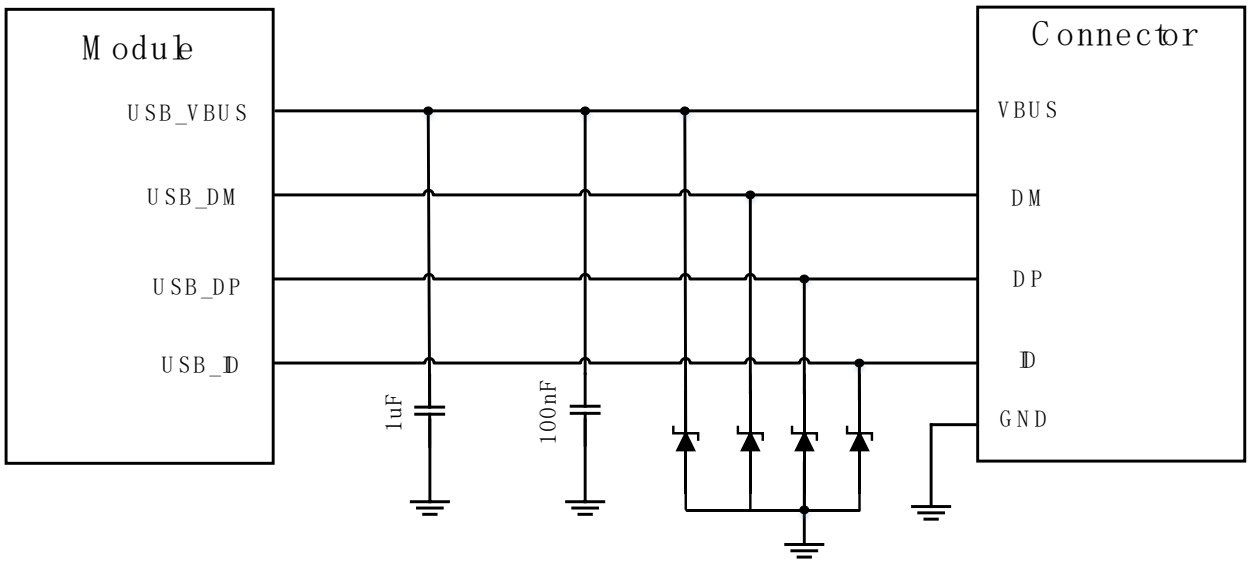

Figure 3-8 USB2.0 reference circuit design

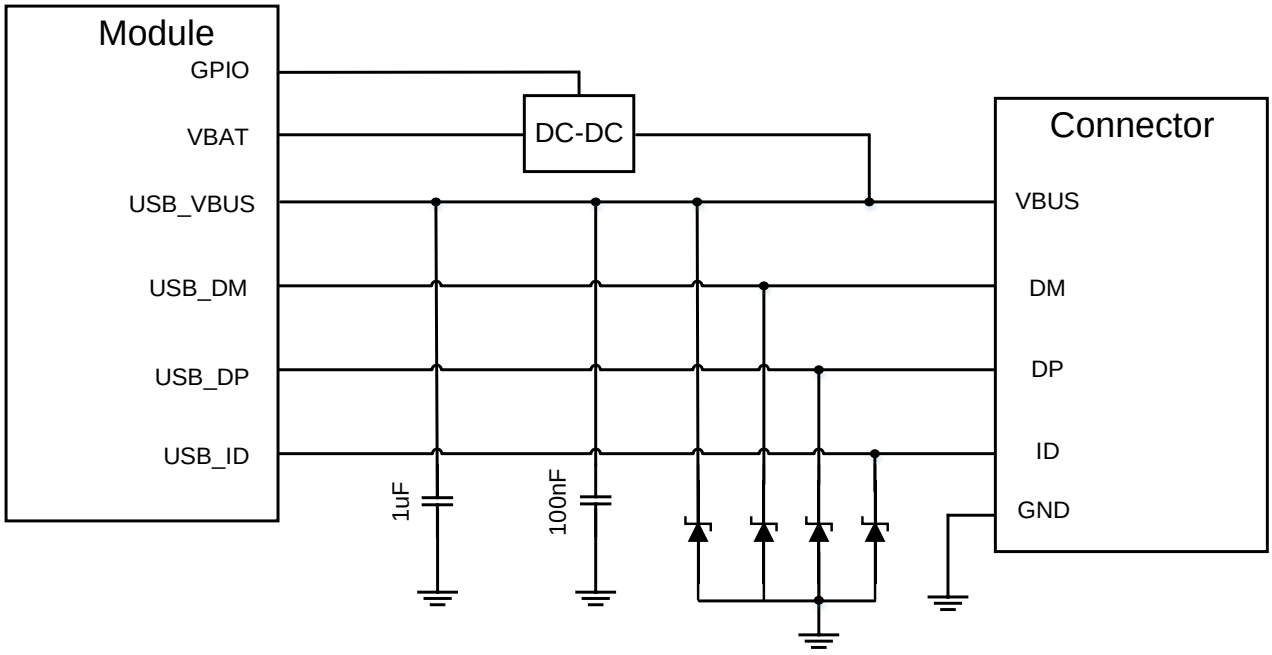

Figure 3-9 USB2.0 reference circuit design (support OTG function)

Note:

1) The total component parasitic capacitance on the USB2.0 differential signal line cannot exceed 2.0pF;

2) USB_DP and USB_DM are high-speed differential signal cables. The highest transmission rate is 480Mbps. Please pay attention to the following requirements in PCB layout:

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- USB_DP and USB_DM signal cables are required to be parallel and equal in length (differential cable length controlled within 2mm), while the right-angle route shall be avoided, and differential 90Ω impedance shall be controlled.
- USB2.0 differential signal cable is laid on the signal layer nearest to the ground, with well grounded.

3) For the reference circuit design DC-DC that supports the OTG function, please use the 5V output.

Table 3-7 Module's internal USB cable length

Pin Name	Pin #	Length (mm)	Length Error (DP-DM)
USB_DP	14	29.37	-0.53
USB_DM	13	30.00	

3.4 UART

The module defines three UART ports, all are 1.8V voltage domain. Its pin definition is as follows:

Table 3-8 UART pin definition

Pin Name	Pin #	I/O	Description	Note
UART5_TX	34	DO	UART5 data transmission	-
UART5_RX	35	DI	UART5 data reception	-
UART5_CTS	36	DI	UART5 clear to send	-
UART5_RTS	37	DO	UART5 request to send	-
UART2_RX	93	DI	UART2 data reception	Debug serial port
UART2_TX	94	DO	UART2 data transmission	
UART4_RX	225	DI	UART4 data reception	-
UART4_TX	226	DO	UART4 data transmission	-

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The voltage domain of each serial port is 1.8V; when communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip with the following reference circuit design:

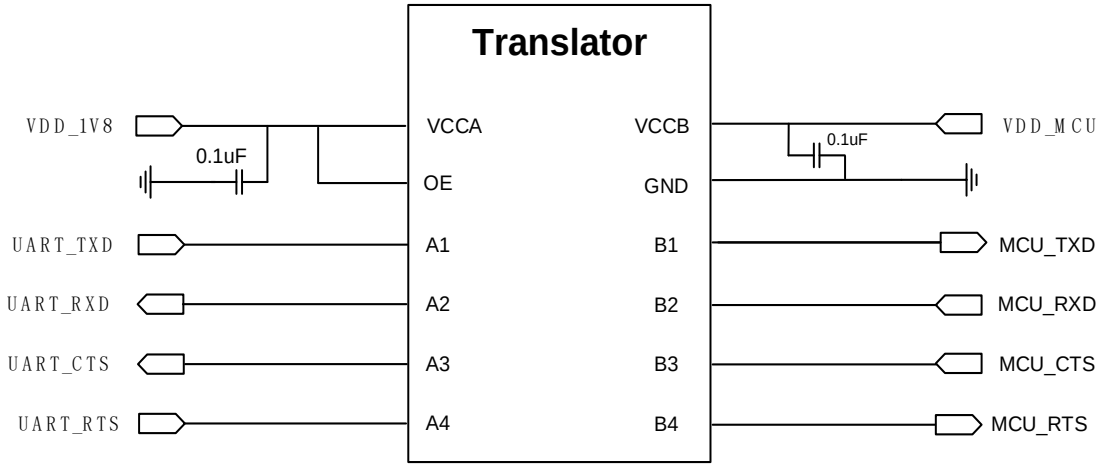

Figure 3-10 Level shift reference circuit

3.5 SPI

The module has one set of SPI interfaces, but only supports master device mode, and does not support DMA mode. The pin definition is as follows:

Table 3-9 SPI pin definition

Pin Name	Pin #	I/O	Description	Note
SPI7_CLK	116	DO	SPI clock	-
SPI7_CS	117	DO	SPI device select	-
SPI7_MISO	118	DI	SPI Master input Slave output	-
SPI7_MOSI	119	DO	SPI Master output Slave input	-

3.6 SD

The module supports one SD interface. The pin definition is as follows:

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Table 3-10 SD interface pin definition

Pin Name	Pin #	I/O	Description	Note
SD_DET	45	DI	SD card detection	-
SD_DATA3	44	I/O	SD card data interface	-
SD_DATA2	43	I/O	SD card data interface	-
SD_DATA1	42	I/O	SD card data interface	-
SD_DATA0	41	I/O	SD card data interface	-
SD_CMD	40	I/O	SD card command interface	-
SD_CLK	39	DO	SD card clock	-
LDO11_SD	38	PO	SD card power supply	-
LDO12_2V95	32	PO	2.95V voltage output	-

SD reference circuit design is as follows:

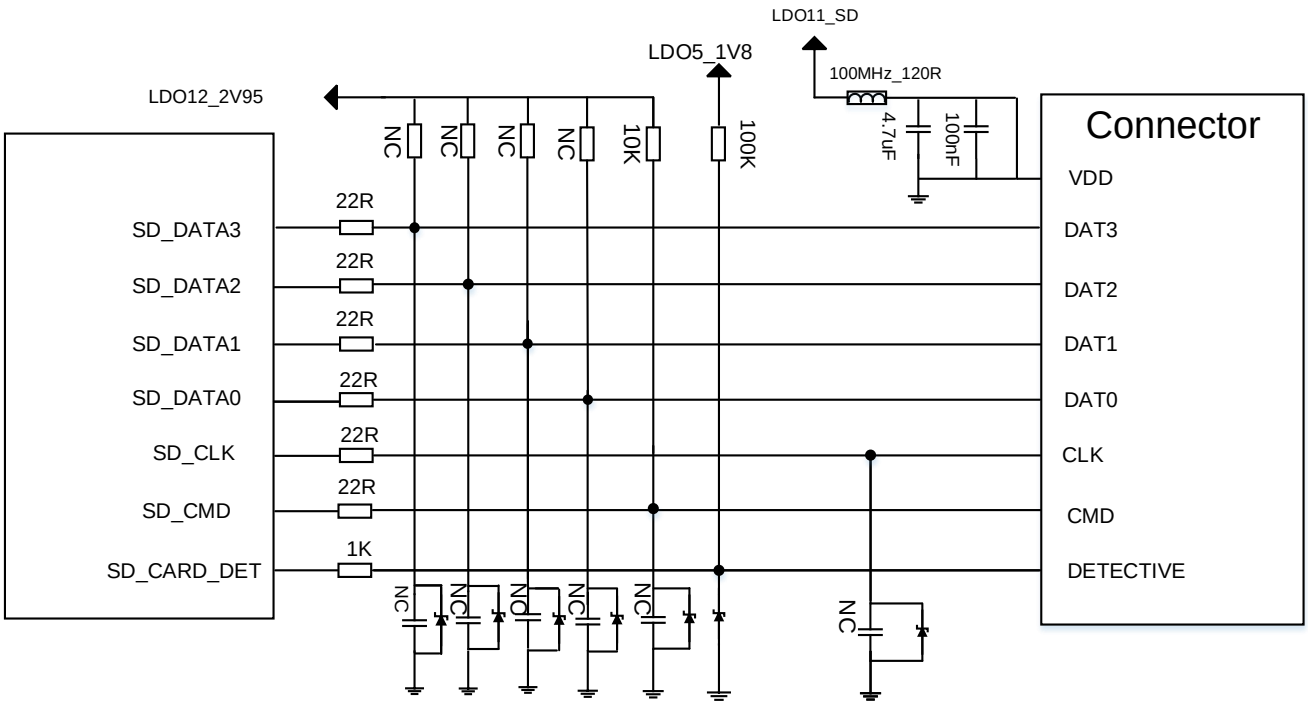

Figure 3-11 SDIO reference circuit

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SD interface design consideration:

1. LDO11_SD is the SD card peripheral driving power and can provide about 800mA current. Pay attention to control the width of cable to 1mm.
2. Pull up SD_DET with LDO5_1V8 power supply.
3. SD is a high-speed digital signal cable, which needs to be shielded.
4. SD cable must be of equal length; the equivalent capacitor must be less than 2pF.

3.7 GPIO

The module has rich GPIO resources and the interface level is 1.8V. The pin definition is as follows:

Table 3-11 GPIO list

Pin Name	Pin #	Reset State	Interrupt Function
GPIO_2	153	B-PD :nppukp	NO
GPIO_6	241	B-PD :nppukp	NO
GPIO_7	242	B-PD :nppukp	NO
GPIO_8	112	B-PD :nppukp	NO
GPIO_9	113	B-PD :nppukp	YES
GPIO_12	101	B-PD :nppukp	YES
GPIO_13	102	B-PD :nppukp	YES
GPIO_25	90	B-PD :nppukp	YES
GPIO_33	33	B-PD :nppukp	NO
GPIO_34	244	B-PD :nppukp	YES
GPIO_41	98	B-PD :nppukp	YES
GPIO_46	159	B-PD :nppukp	YES
GPIO_48	99	B-PD :nppukp	YES
GPIO_50	183	B-PD :nppukp	YES
GPIO_59	100	B-PD :nppukp	YES
GPIO_61	106	B-PD :nppukp	YES

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Pin Name	Pin #	Reset State	Interrupt Function
GPIO_62	123	B-PD :nppukp	YES
GPIO_63	124	B-PD :nppukp	YES
GPIO_66	206	B-PD :nppukp	NO
GPIO_81	202	B-PD :nppukp	YES
GPIO_82	203	B-PD :nppukp	NO
GPIO_86	187	B-PD :nppukp	YES
GPIO_87	105	B-PD :nppukp	NO
GPIO_88	205	B-PD :nppukp	NO
GPIO_89	115	B-PD :nppukp	NO
GPIO_90	252	B-PD :nppukp	YES
GPIO_93	190	B-PD :nppukp	YES
GPIO_94	104	B-PD :nppukp	NO
GPIO_95	103	B-PD :nppukp	NO
GPIO_97	97	B-PD :nppukp	YES
GPIO_104	254	B-PD :nppukp	NO
GPIO_106	253	B-PD :nppukp	NO
GPIO_127	243	B-PD :nppukp	YES

Note:

B: Bidirectional digital with CMOS input.

H: High-voltage tolerant.

NP: pdpukp = default no-pull with programmable options following the colon (:).

PD: nppukp = default pulldown with programmable options following the colon (:).

PU: nppdkp = default pullup with programmable options following the colon (:).

KP: nppdpu = default keeper with programmable options following the colon (:).

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3.8 I²C

The module provides four I2C interfaces for TP, camera, sensor, etc. And four I2C interfaces are all open-drain outputs, when in use, please pull up to 1.8V power domain through pull-up resistors. The pin definition is as follows:

Table 3-12 I2C interface pin definition

Pin Name	Pin #	I/O	Description	Note
SENSOR_I2C_SCL	91	OD	Sensor I2C clock	-
SENSOR_I2C_SDA	92	OD	Sensor I2C data	-
TP_I2C_SCL	47	OD	Touch panel I2C clock	-
TP_I2C_SDA	48	OD	Touch panel I2C data	-
CAM_I2C_SCL0	83	OD	Camera I2C clock	Cannot be used as I2C and GPIO for other devices
CAM_I2C_SDA0	84	OD	Camera I2C data	
CAM_I2C_SCL1	239	OD	Camera I2C clock	
CAM_I2C_SDA1	240	OD	Camera I2C data	

Note:

When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address. When mounting peripherals with high real-time requirements, please do not share I2C with other peripherals.

3.9 ADC

The module provides one ADC interfaces and its maximum resolution is 15 bits, its pin definition is as follows:

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Table 3-13 ADC pin definition

Pin Name	Pin #	I/O	Description	Note
ADC	128	AI	ADC detection	Configurable as 0.3V~VBAT

3.10 Battery Interface

Table 3-14 Battery interface pin definition

Pin Name	Pin #	I/O	Description	Note
BAT_ID	260	AI	Battery ID	Ground it when not in use
CHARGE_SEL	127	DI	Charging path select	External charge: please connect this pin to ground; Internal charge: keeps it suspending
VBAT_SNS	133	AI	Main battery voltage sense	Connect to VBAT
VBAT_THERM	134	AI	Battery thermistor	The NTC is 47K

3.11 Motor Driver Interface

Table 3-15 Motor interface pin definition

Pin Name	Pin #	I/O	Description	Note
VIB_DRV_N	28	PO	Motor driver	Connects to the negative terminal of the motor

3.12 LCM

The screen interface of module is based on MIPI_DSI standard and supports one 4-lane high-speed differential data transmission. It supports HD+ resolution.

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Table 3-16 LCM pin definition

Pin Name	Pin #	I/O	Description	Note
LDO6_1V8	125	PO	LCD IO voltage	-
LDO17_2V85	129	PO	LCD analog power VDD	-
MIPI_DSI0_CLK_P	53	AO	Main-LCD MIPI clock+	-
MIPI_DSI0_CLK_N	52	AO	Main-LCD MIPI clock-	-
MIPI_DSI0_LN0_P	55	AI/AO	Main LCD MIPI Lane 0+	-
MIPI_DSI0_LN0_N	54	AI/AO	Main LCD MIPI Lane 0-	-
MIPI_DSI0_LN1_P	57	AI/AO	Main LCD MIPI Lane 1+	-
MIPI_DSI0_LN1_N	56	AI/AO	Main LCD MIPI Lane 1-	-
MIPI_DSI0_LN2_P	59	AI/AO	Main LCD MIPI Lane 2+	-
MIPI_DSI0_LN2_N	58	AI/AO	Main LCD MIPI Lane 2-	-
MIPI_DSI0_LN3_P	61	AI/AO	Main LCD MIPI Lane 3+	-
MIPI_DSI0_LN3_N	60	AI/AO	Main LCD MIPI Lane 3-	-
LCD_RST_N	49	DO	Main LCD reset	-
PWM	29	DO	LCD backlight PWM control	-
LCD_TE	50	DI	Swipe Sync	-

The reference design of LCD interface circuit is as follows:

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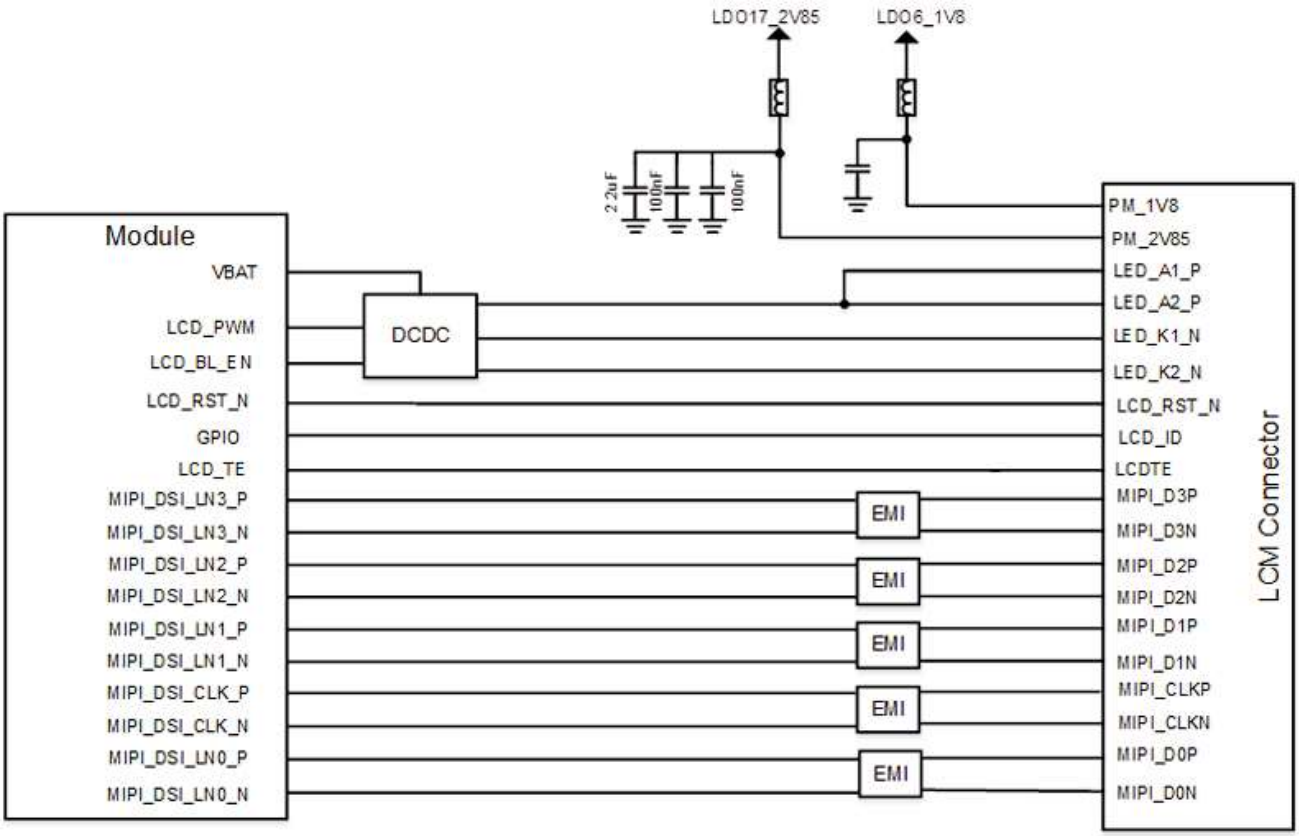

Figure 3-12 LCM reference circuit

3.13 TP

The module provides one I2C interface that can be used to connect the touch panel and it provides power, interrupt, reset pins. The pin definition of the module is shown in the following table:

Table 3-17 TP pin definition

Pin Name	Pin #	I/O	Description	Note
TP_INT_N	30	DI	LCD TP interrupt signal	-
TP_RST_N	31	DO	LCD TP reset signal	-
LDO6_1V8	125	PO	LCD TP I2C pull up power supply	-
LDO17_2V85	129	PO	LCD TP VDD power supply	-
TP_I2C_SCL	47	OD	LCD TP I2C clock	-
TP_I2C_SDA	48	OD	LCD TP I2C data	-

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TP reference circuit is as follows:

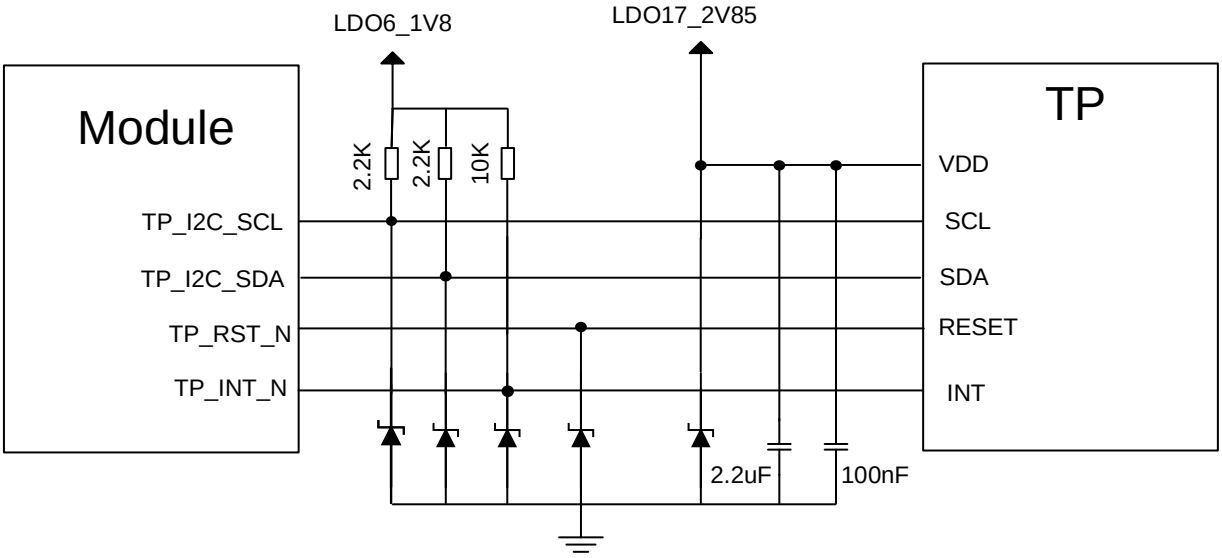

Figure 3-13 TP reference circuit

3.14 Camera

The camera interface of module is based on the MIPI_CSI standard and can support two (4 Lane + 4 Lane) or three (4 Lane + 2 Lane + 1 Lane) cameras (three by default), the maximum camera resolution is 13 MP. The pin definition of camera interface is as follows:

Table 3-18 Camera interface pin definition

Pin Name	Pin #	I/O	4 Lane + 2 Lane + 1 Lane (Default)	4 Lane + 4 Lane (Configurable)
LDO6_1V8	125	PO	DOVDD power supply	DOVDD power supply
LDO16_2V8	152	PO	AVDD power supply	AVDD power supply
LDO10_2V85	228	PO	Camera focus motor driver AFVDD power supply	Camera focus motor driver AFVDD power supply
MIPI_CSI0_CLK_P	229	AI	Rear camera MIPI Clock+	Rear camera MIPI Clock+
MIPI_CSI0_CLK_N	230	AI	Rear camera MIPI Clock-	Rear camera MIPI Clock-
MIPI_CSI0_LN0_P	155	AI	Rear camera MIPI Lane 0+	Rear camera MIPI Lane 0+

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Pin Name	Pin #	I/O	4 Lane + 2 Lane + 1 Lane (Default)	4 Lane + 4 Lane (Configurable)
MIPI_CSI0_LN0_N	231	AI	Rear camera MIPI Lane 0-	Rear camera MIPI Lane 0-
MIPI_CSI0_LN1_P	156	AI	Rear camera MIPI Lane 1+	Rear camera MIPI Lane 1+
MIPI_CSI0_LN1_N	232	AI	Rear camera MIPI Lane 1-	Rear camera MIPI Lane 1-
MIPI_CSI0_LN2_P	157	AI	Rear camera MIPI Lane 2+	Rear camera MIPI Lane 2+
MIPI_CSI0_LN2_N	233	AI	Rear camera MIPI Lane 2-	Rear camera MIPI Lane 2-
MIPI_CSI0_LN3_P	158	AI	Rear camera MIPI Lane 3+	Rear camera MIPI Lane 3+
MIPI_CSI0_LN3_N	234	AI	Rear camera MIPI Lane 3-	Rear camera MIPI Lane 3-
MCAM_MCLK	74	DO	Rear camera master clock	Rear camera master clock
MCAM_RST	79	DO	Rear camera reset signal	Rear camera reset signal
MCAM_PWDN	80	DO	Rear camera power down signal	Rear camera power down signal
CAM_I2C_SCL0	83	OD	Rear Camera I2C clock signal	Rear Camera I2C clock signal
CAM_I2C_SDA0	84	OD	Rear Camera I2C data signal	Rear Camera I2C data signal
MIPI_CSI1_CLK_P	64	AI	Front camera MIPI Clock+	Front camera MIPI Clock+
MIPI_CSI1_CLK_N	63	AI	Front camera MIPI Clock-	Front camera MIPI Clock-
MIPI_CSI1_LN0_P	66	AI	Front camera MIPI Lane 0+	Front camera MIPI Lane 0+
MIPI_CSI1_LN0_N	65	AI	Front camera MIPI Lane 0-	Front camera MIPI Lane 0-
MIPI_CSI1_LN1_P	68	AI	Front camera MIPI Lane 1+	Front camera MIPI Lane 1+
MIPI_CSI1_LN1_N	67	AI	Front camera MIPI Lane 1-	Front camera MIPI Lane 1-
MIPI_CSI1_LN2_P	73	AI	Depth of field camera MIPI Lane 0+	Front camera MIPI Lane 2+
MIPI_CSI1_LN2_N	72	AI	Depth of field camera MIPI Lane 0-	Front camera MIPI Lane 2-
MIPI_CSI1_LN3_P	71	AI	Depth of field camera MIPI Clock+	Front camera MIPI Lane 3+
MIPI_CSI1_LN3_N	70	AI	Depth of field camera MIPI	Front camera MIPI Lane 3-

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Pin Name	Pin #	I/O	4 Lane + 2 Lane + 1 Lane (Default)	4 Lane + 4 Lane (Configurable)
			Clock -	
SCAM_MCLK	75	DO	Front camera master clock	Front camera master clock
SCAM_RST	81	DO	Front camera reset signal	Front camera reset signal
SCAM_PWDN	82	DO	Front camera power down signal	Front camera power down signal
CAM2_I2C_SCL1	239	OD	Front /Depth of field camera I2C clock signal	Front Camera I2C clock signal
CAM2_I2C_SDA1	240	OD	Front /Depth of field camera I2C data signal	Front Camera I2C data signal
DCAM_MCLK	238	DO	Depth of field camera master clock	Reserved
DCAM _RST	237	DO	Depth of field camera reset signal	Reserved
DCAM _PWDN	236	DO	Depth of field camera power down signal	Reserved

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3.14.1 Rear Camera

Reference circuit design of rear camera is as follows:

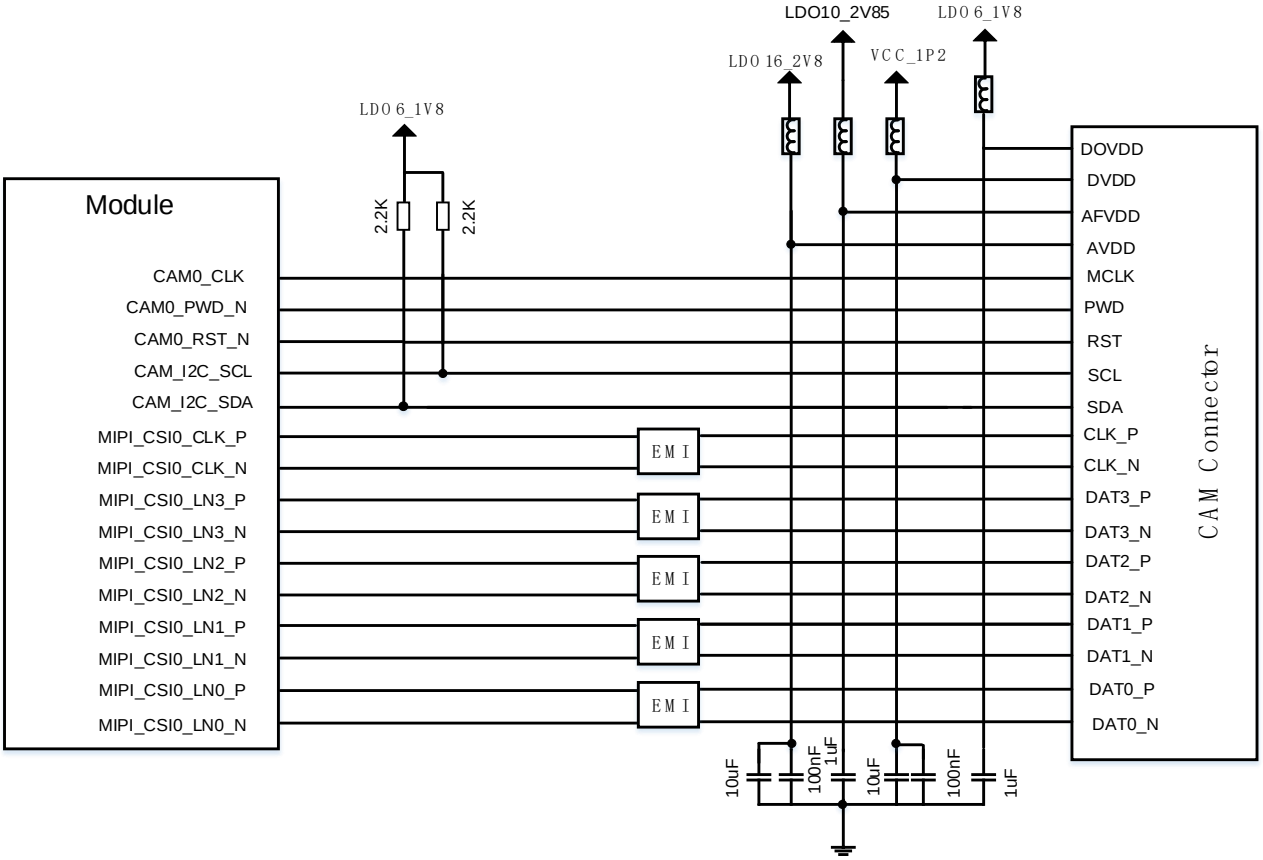

Figure 3-14 Rear camera reference circuit

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3.14.2 Front Camera

Reference circuit design of 4 Lane front camera is as follows:

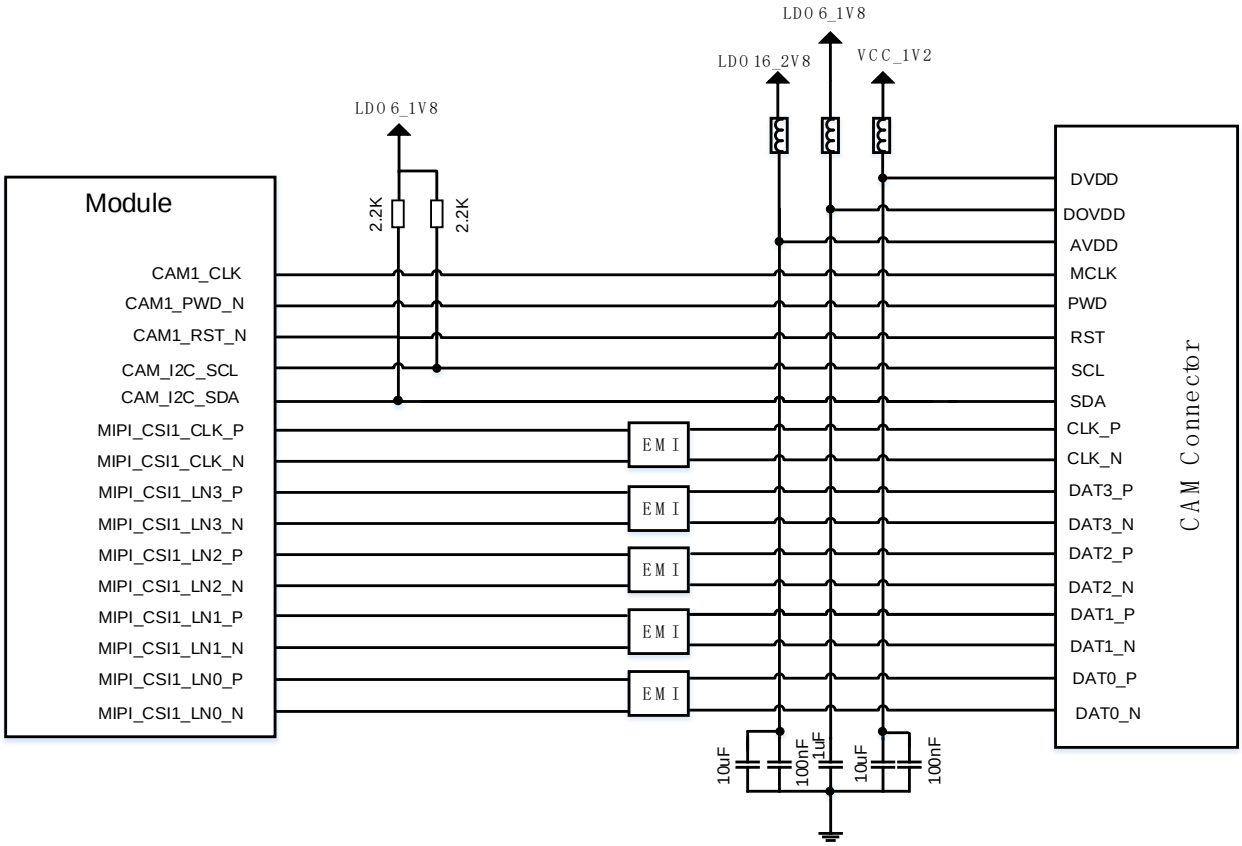

Figure 3-15 4 Lane front camera reference circuit

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Reference circuit design of 2 Lane front camera is as follows:

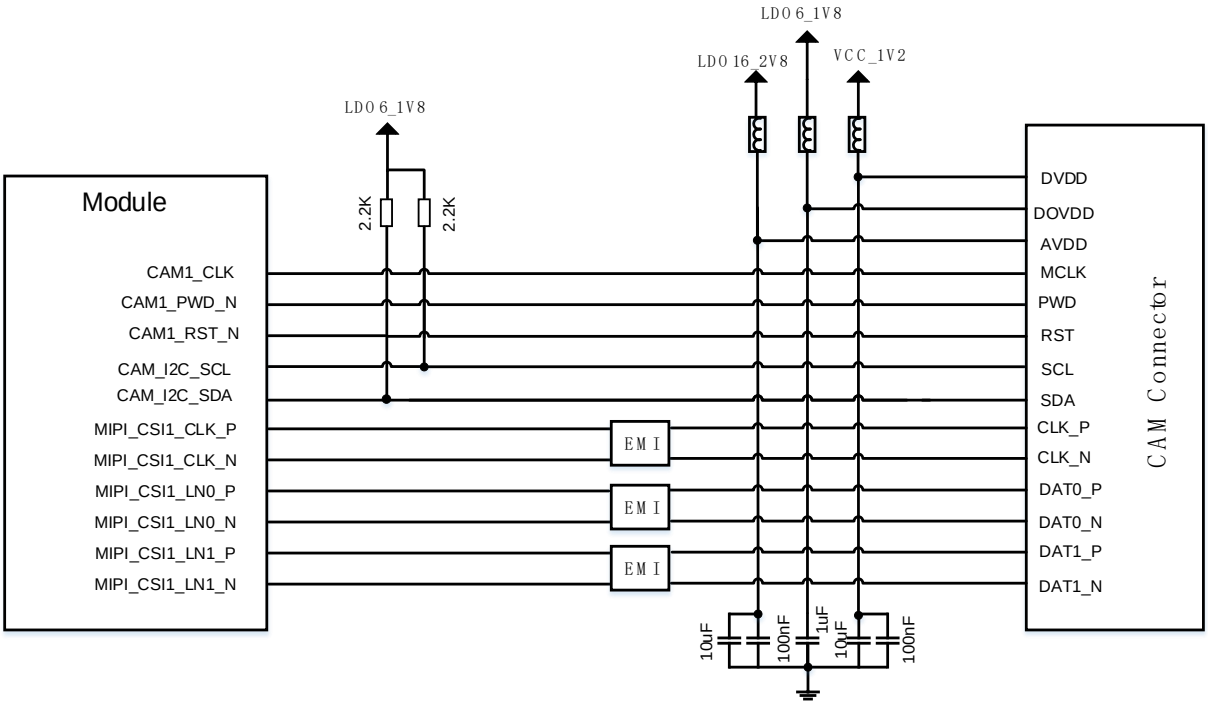

Figure 3-16 2 Lane front camera reference circuit

3.14.3 Depth of Field Camera

Reference circuit of depth of field camera is as follows:

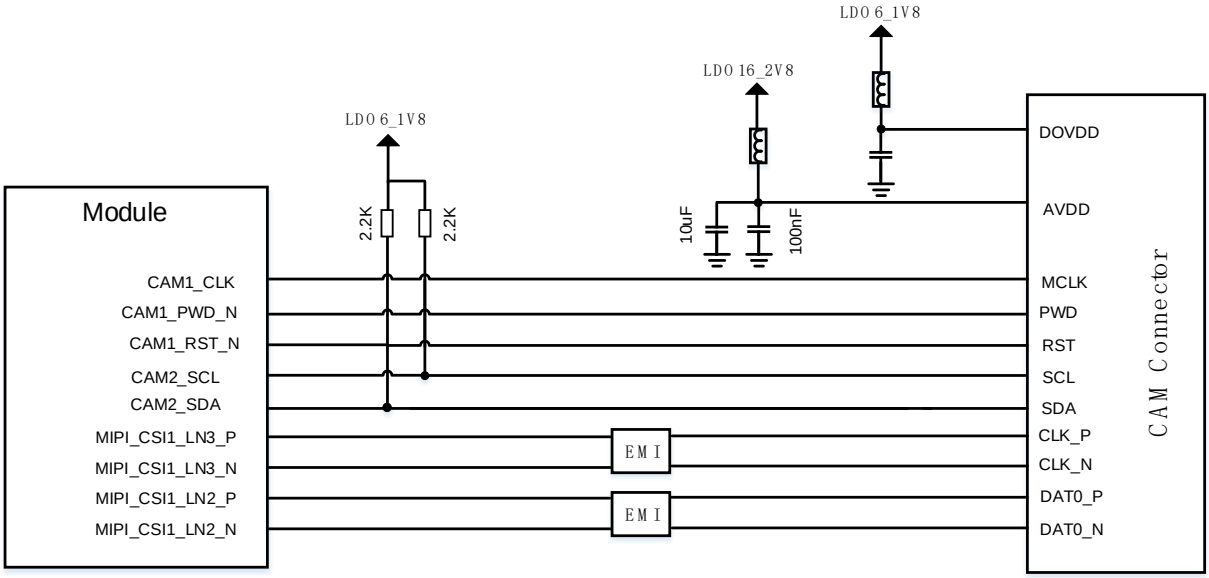

Figure 3-17 1 Lane depth of field camera reference circuit

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3.14.4 MIPI Design Considerations

1. MIPI is a high-speed signal cable. It is recommended to connect the common mode inductor in series near the camera connector to reduce the electromagnetic interference of the circuit;
2. MIPI routing is recommended to be in the inner layer, with three-dimensional grounding;
3. The MIPI signal needs to be controlled with a differential impedance of 100Ω and with an error of ±10%;
4. The total length of the cable shall not exceed 300mm;
5. The intra lane match of MIPI signal must be controlled within 0.7mm;
6. The inter lane match of MIPI signal must be controlled within 1.4mm;
7. It is recommended that the space of intra lane should be 1x line width and the space of inter lane should be 2x line width;
8. The total component parasitic capacitance on the MIPI differential signal line cannot exceed 1.0pF;

Other Considerations:

9. CAM_CLK is a high-speed clock signal and requires three-dimensional grounding;
10. The analog voltage AVDD routing should be away from interference sources, otherwise it is easy to bring interference of power noise;
11. If the front and rear cameras share the I2C, you need to confirm that the I2C addresses of the two cameras do not conflict;
12. Camera analog power supply is suggested to add LDO with high PSRR ability.

Table 3-19 Module's internal MIPI cable length

Pin Name	Pin #	Length (mm)	Length Error (P-N)
MIPI_DSI0_CLK_P	53	11.29	-0.48
MIPI_DSI0_CLK_N	52	11.77	
MIPI_DSI0_LN0_P	55	10.10	-0.56
MIPI_DSI0_LN0_N	54	10.66	
MIPI_DSI0_LN1_P	57	10.32	-0.24
MIPI_DSI0_LN1_N	56	10.56	

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Pin Name	Pin #	Length (mm)	Length Error (P-N)
MIPI_DSI0_LN2_P	59	9.99	-0.56
MIPI_DSI0_LN2_N	58	10.55	
MIPI_DSI0_LN3_P	61	10.43	0.12
MIPI_DSI0_LN3_N	60	10.67	
MIPI_CSI0_CLK_P	229	19.21	-0.41
MIPI_CSI0_CLK_N	230	19.62	
MIPI_CSI0_LN0_P	155	19.62	0.42
MIPI_CSI0_LN0_N	231	19.20	
MIPI_CSI0_LN1_P	156	18.12	-0.61
MIPI_CSI0_LN1_N	232	18.81	
MIPI_CSI0_LN2_P	157	18.92	-0.85
MIPI_CSI0_LN2_N	233	19.05	
MIPI_CSI0_LN3_P	158	19.17	-0.09
MIPI_CSI0_LN3_N	234	19.26	
MIPI_CSI1_CLK_P	64	17.79	0.01
MIPI_CSI1_CLK_N	63	17.78	
MIPI_CSI1_LN0_P	66	17.72	0.18
MIPI_CSI1_LN0_N	65	17.54	
MIPI_CSI1_LN0_P	68	17.61	-0.31
MIPI_CSI1_LN0_N	67	17.92	
MIPI_CSI1_LN1_P	73	18.27	-0.14
MIPI_CSI1_LN1_N	72	18.41	
MIPI_CSI1_LN2_P	71	17.96	0.36
MIPI_CSI1_LN2_N	70	17.60	

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3.15 Sensor

The module uses I2C to communicate with sensors on the EVK, and supports various types of sensors, such as accelerometer sensor, ambient light sensor, magnetic sensor and gyroscopes, etc.

Table 3-20 Sensor interface pin definition

Pin Name	Pin #	I/O	Description	Note
SENSOR_I2C_SCL	91	OD	I2C clock	-
SENSOR_I2C_SDA	92	OD	I2C data cable	-
ALSP_INT	107	DI	Ambient light sensor interrupt signal	-
MAG_INT	109	DI	Magnetic sensor interrupt signal	-
ACCEL_INT2	108	DI	G-Sensor interrupt signal 2	-
ACCEL_INT1	110	DI	G-Sensor interrupt signal 1	-

3.16 Audio

3.16.1 Audio Interface Definition

The module supports analog audio interface, and has 3 inputs and 3 outputs. Pin definition is as follows:

Table 3-21 Audio interface definition

Pin Name	Pin #	I/O	Description	Note
SPK _P	10	AO	Loudspeaker driver output+	-
SPK _M	11	AO	Loudspeaker driver output-	-
REC_P	8	AO	Receiver output+	-
REC_M	9	AO	Receiver output-	-
HPH_L	138	AO	Headphone left channel output	-
HPH_GND	137	-	Headphone reference ground	-
HPH_R	136	AO	Headphone right channel output	-

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Pin Name	Pin #	I/O	Description	Note
HPH_DET	139	AI	Headphone plug detection	-
MIC2_P	6	AI	Headphone MIC input	-
MIC_GND	5	AI	MIC ground	-
MIC3_P	220	AI	Secondary MICinput	-
MIC1_P	4	AI	Main MICinput	-
MIC_BIAS1	219	AO	MIC bias 1	-
MIC_BIAS2	227	AO	MIC bias 2	-

Audio Interface Design Consideration:

1. The module has MIC bias circuit internally, and no external circuit is required.
2. The SPK is configured to have class D amplifier and cannot be connected to an external amplifier. It is recommended to connect 8Ω speakers. Note that the route width must meet the power rating requirements. If an external audio amplifier is required, please use the output of headphone as the input of external audio amplifier.
3. The reference ground of the headphone has already grounded in the module. The external circuit is recommended not to be grounded and resistor can be reserved.
4. It is recommended to use receiver with 32Ω impendence.
5. To reduce noise and improve audio quality, the following approaches are recommended:
   - Keep audio PCB routing away from the antenna and high-frequency digital signal.
   - Reserve LC filter circuit in audio circuit to reduce EMI.
   - Audio routing needs to be shielded.

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3.16.2 Microphone Circuit Design

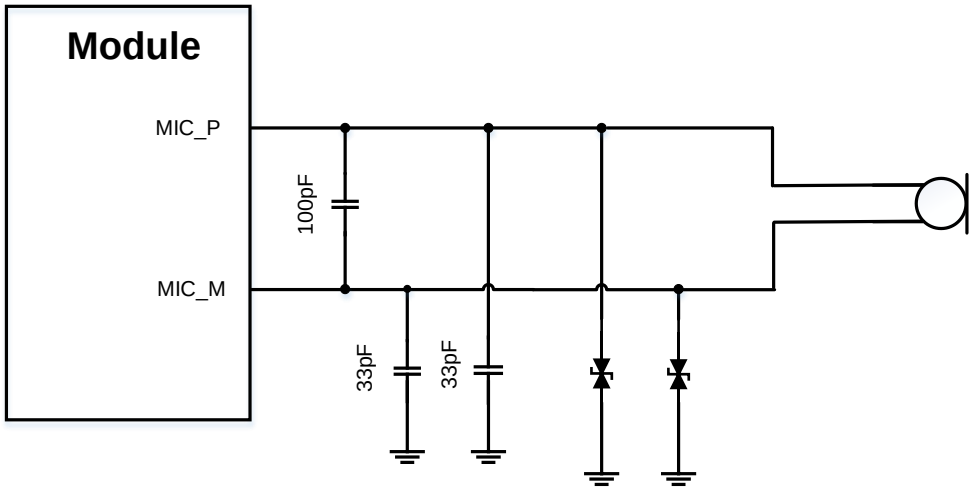

Figure 3-18 Microphone circuit design

3.16.3 Receiver Circuit Design

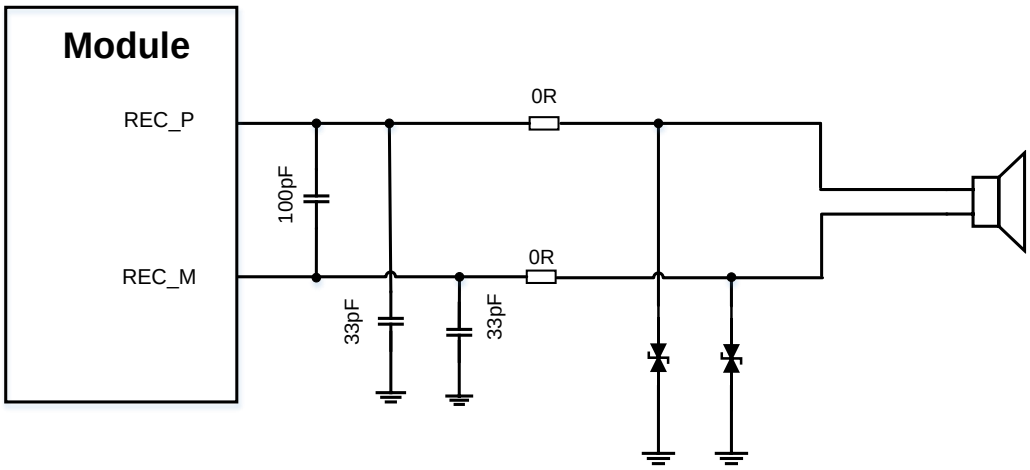

Figure 3-19 Receiver circuit design

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3.16.4 Headphone Interface Circuit Design

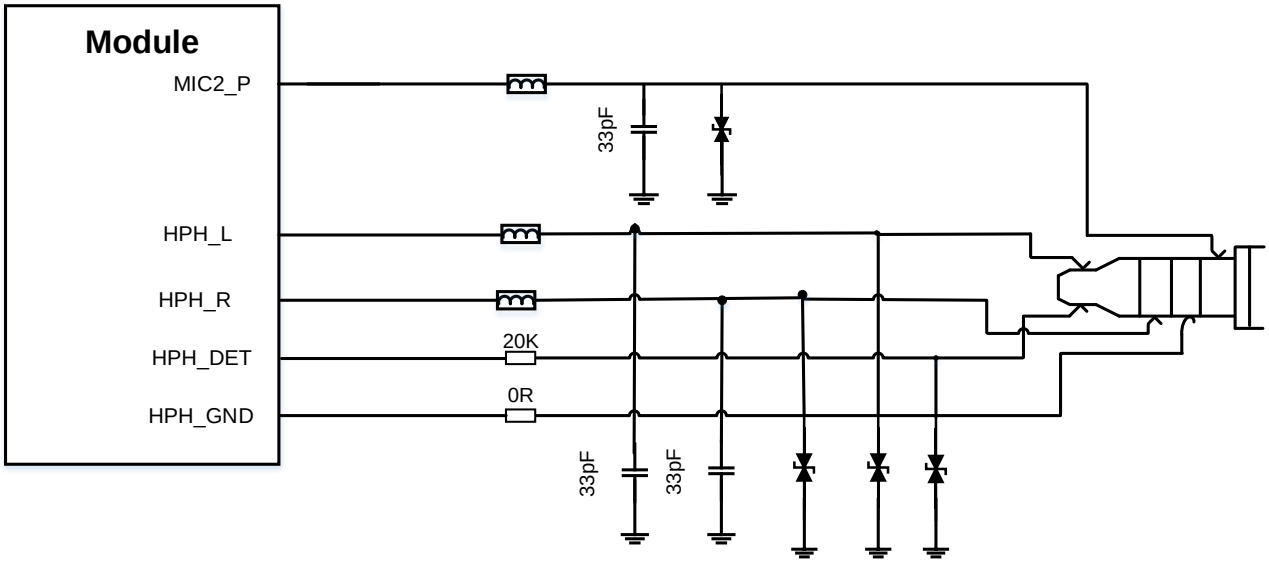

Figure 3-20 Headphone interface circuit design

Note:

Use a bi-directional TVS tube for the ESD protection device of the headphone interface.

3.16.5 Speaker Circuit Design

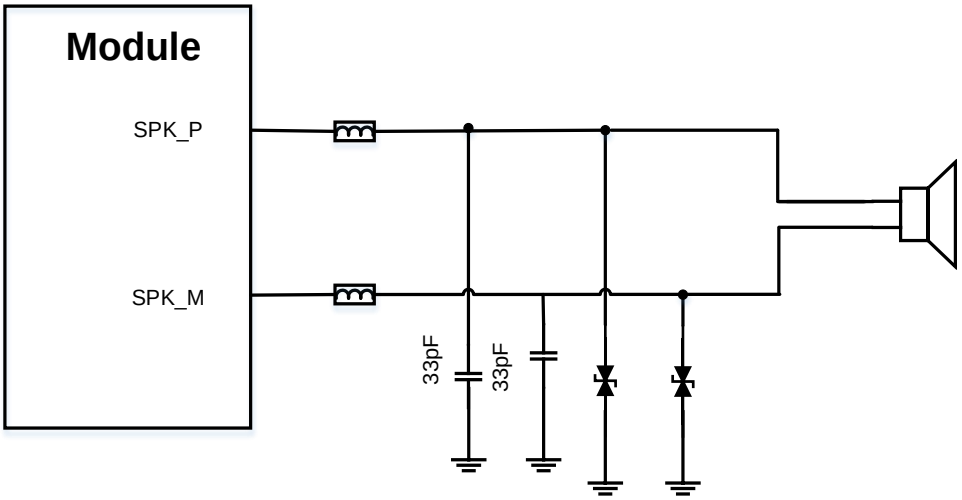

Figure 3-21 Speaker circuit design

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3.17 Forced Download Interface Design

The module provides KEY_FORCE_BOOT pin as an emergency download interface. Connect the KEY_FORCE_BOOT pin with LDO5_1V8 pin when powering on, and the module can enter the emergency download mode, which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin. Reference circuit is as follows:

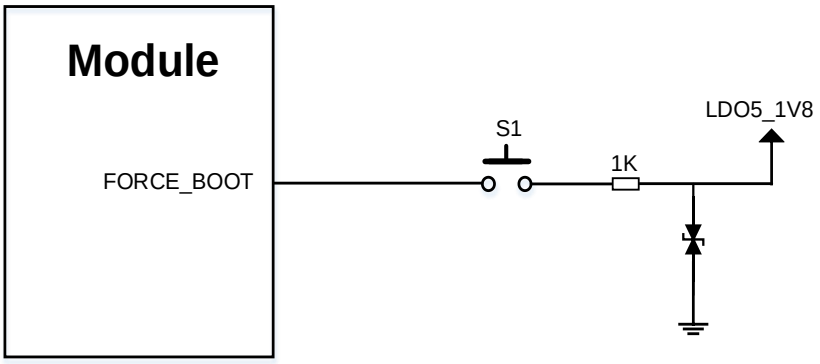

Figure 3-22 Forced download interface design

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4 Antenna Interface

The module supports WIFI/BT antenna.

4.1 WIFI/BT Antenna

Microstrip cable is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50Ω.

Table 4-1 WIFI/BT antenna interface definition

Pin Name	Pin #	I/O	Description	Note
ANT-WIFI/BT	77	I/O	WIFI/BT antenna interface	-

4.1.1 WIFI/BT Operating Frequency

Table 4-2 WIFI/BT operating frequency

Mode	Frequency	Unit
WIFI	2402 - 2482	MHz
	5180 - 5835	MHz
BT4.2	2402 - 2480	MHz

4.1.2 Circuit Reference Design

WIFI/BT antenna reference circuit is as follows:

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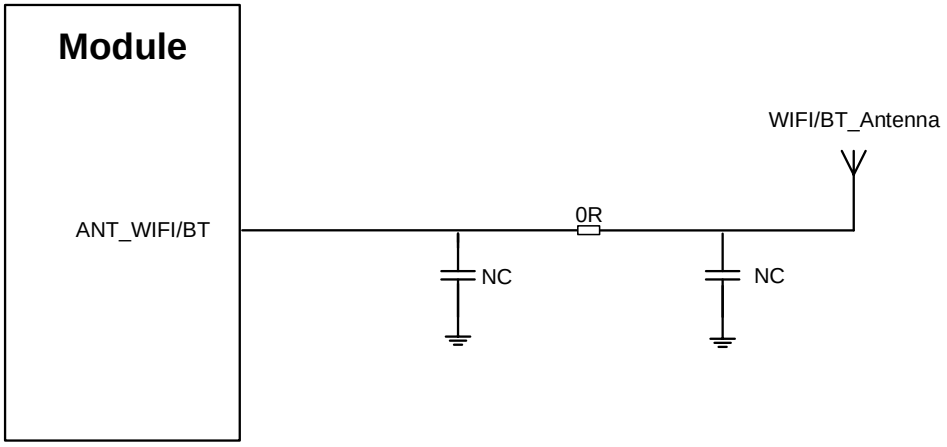

Figure 4-1 WIFI/BT reference circuit

4.2 Antenna Requirements

The module provides WIFI/BT antenna interfaces. The antenna requirements are as follows:

Table 4-3 Antenna requirements

Module Antenna Requirements	
Standard	**Antenna Requirements**
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 50 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB

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5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal cables should be within 50Ω. In general, the impedance of the RF signal cable is determined by the dielectric constant of the material, the cable width (W), the ground clearance (S) and the height of the reference ground plane (H). PCB characteristic impedance is usually controlled using both microstrip cable and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip cable and coplanar waveguide when the impedance cable is at 50Ω.

- Microstrip cable complete structure

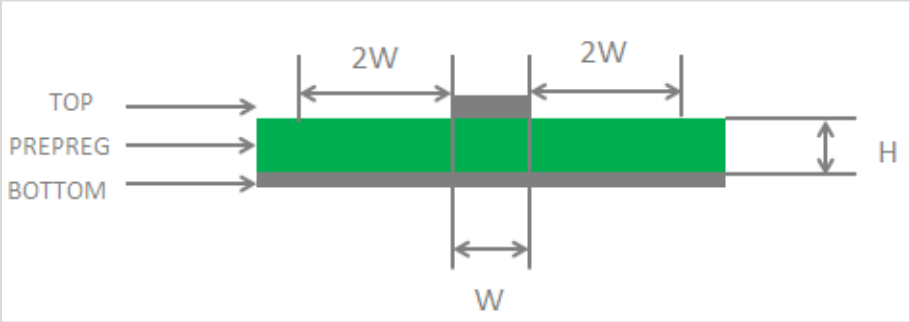

Figure 5-1 Two-layer PCB microstrip cable structure

- Coplanar waveguide complete structure

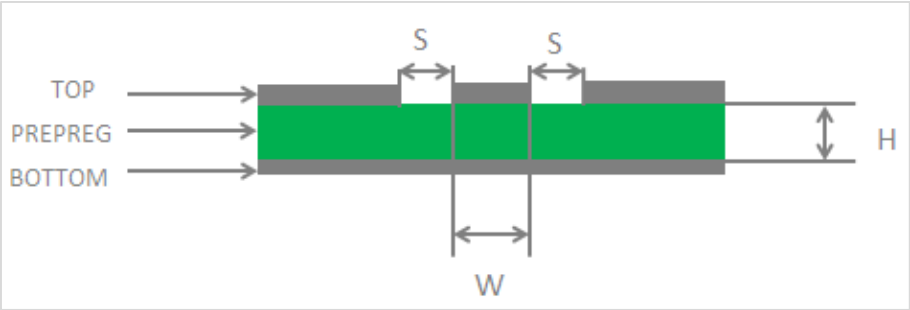

Figure 5-2 Two-layer PCB coplanar waveguide structure

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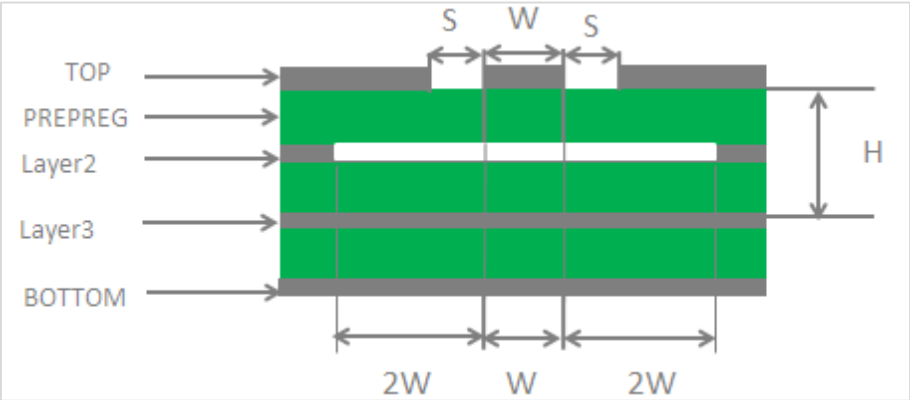

Figure 5-3 Four-layer PCB coplanar waveguide structure (reference ground layer 3)

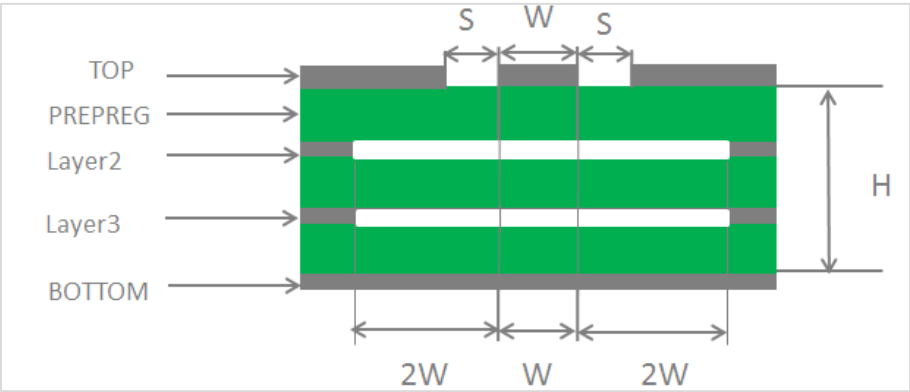

Figure 5-4 Four-layer PCB coplanar waveguide structure (reference ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following design principles:

- The impedance simulation tool should be used to accurately control the RF signal cable at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.
- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degrees.
- Attention should be paid to the encapsulation of the component package and the signal pin should be kept at a certain distance from the ground.
- The reference ground plane of the RF signal cable should be kept intact; adding a certain amount of ground holes around the signal and the reference ground can improve the RF performance; the

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distance between the ground hole and the signal cable should be at least 2 times the cable width (2*W).

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6 WIFI and Bluetooth

6.1 WIFI Overview

The module supports 2.4G and 5G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum rate up to 433Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance

Test condition: VBAT: 3.8V, temperature: 25°C.

Table 6-1 WIFI transmit power

Frequency	Mode	Data Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17.5 ± 2.5
		11Mbps	20	17.5 ± 2.5
	802.11g	6Mbps	20	16.0 ± 3
		54Mbps	20	13.0 ± 3
	802.11n	MCS0	20	15.0 ± 3
		MCS7	20	12.0 ± 3
		MCS0	40	15.0 ± 3
		MCS7	40	12.0 ± 3

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Frequency	Mode	Data Rate	Bandwidth (MHz)	TX Power (dBm)
5G	802.11a	6Mbs	20	19.0 ± 3
		54Mbps	20	16.0 ± 3
	802.11n	MCS0	20	18.0 ± 3
		MCS7	20	15.0 ± 3
	802.11n	MCS0	40	18.0 ± 3
		MCS7	40	15.0 ± 3
	802.11ac	MCS0	20	18.0 ± 3
		MCS8	20	13.0 ± 3
		MCS0	40	18.0 ± 3
		MCS9	40	13.0 ± 3
		MCS0	80	18.0 ± 3
		MCS9	80	13.0 ± 3

Table 6-2 WIFI RX sensitivity

Frequency	Mode	Data Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-90.0
		11Mbps	20	-87.0
	802.11g	6Mbps	20	-89.0
		54Mbps	20	-73.0
	802.11n	MCS0	20	-88.0
		MCS7	20	-70.0
		MCS0	40	-85.0
		MCS7	40	-67.0
5G	802.11a	6Mbps	20	-89.0
		54Mbps	20	-73.0
	802.11n	MCS0	20	-89.0

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Frequency	Mode	Data Rate	Bandwidth (MHz)	Sensitivity (dBm)
		MCS7	20	-71.0
		MCS0	40	-89.0
		MCS7	40	-70.0
	802.11ac	MCS0	20	-88.0
		MCS8	20	-65.0
		MCS0	40	-86.0
		MCS9	40	-61.0
		MCS0	80	-84.0
		MCS9	80	-56.0

6.3 Bluetooth Overview

The module supports BT4.2 (BR/EDR + BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1MHz and can accommodate 79 channels. The BLE channel bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 6-3 BT rate and version information

Version	Data Rate	Throughput	Note
BT1.2	1Mb/s	> 80Kbit/s	-
BT2.0 + EDR	2Mb/s	> 80Kbit/s	-
BT3.0 + HS	24Mbps	Refer to 3.0 + HS	-
BT4.2 LE	24Mbps	Refer to 4.2 LE	-

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6.4 Bluetooth Performance

Test condition: VBAT: 3.8V, temperature: 25°C.

Table 6-4 BT performance index

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitter	9±2.5	7±2.5	7±2.5	1±2.5	dBm
Sensitivity	-89	-88	-84	-93	dBm

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7 Electricity, Reliability and RF Performance

7.1 Recommended Parameters

Table 7-1 Recommended parameters

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.2	V
USB_VBUS	4.75	5	5.25	V
VRTC	2.0	3.0	3.25	V
Operating Temperature	-30	25	75	°C
Storage Temperature	-40	25	85	°C

7.2 Operating Current

Test condition: VBAT: 3.8V, temperature: 25℃.

Table 7-2 Operating current

Parameter	Description	Condition	Type	Unit
I_{off}	Power Off	Power Off	25	μA

7.3 Electrostatic Protection

In the application of the module, due to static electricity generated by human body and charged friction between micro-electronics, etc. discharging to the module through various channels that may cause damage, ESD protection should be taken seriously attention. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added at the designed circuit interface and the points susceptible to

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electrostatic discharge or impact. Anti-static gloves should be worn during production.

ESD performance parameters table (Temperature: 25°C, Humidity: 45%).

Table 7-3 ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	± 5	± 10	KV
Antenna interface	± 4	± 8	KV
Other interface	± 0.5	± 1	KV

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8 Structural Specification

8.1 Product Appearance

The module product appearance is shown in the following figure, and the appearance is subject to the actual product.

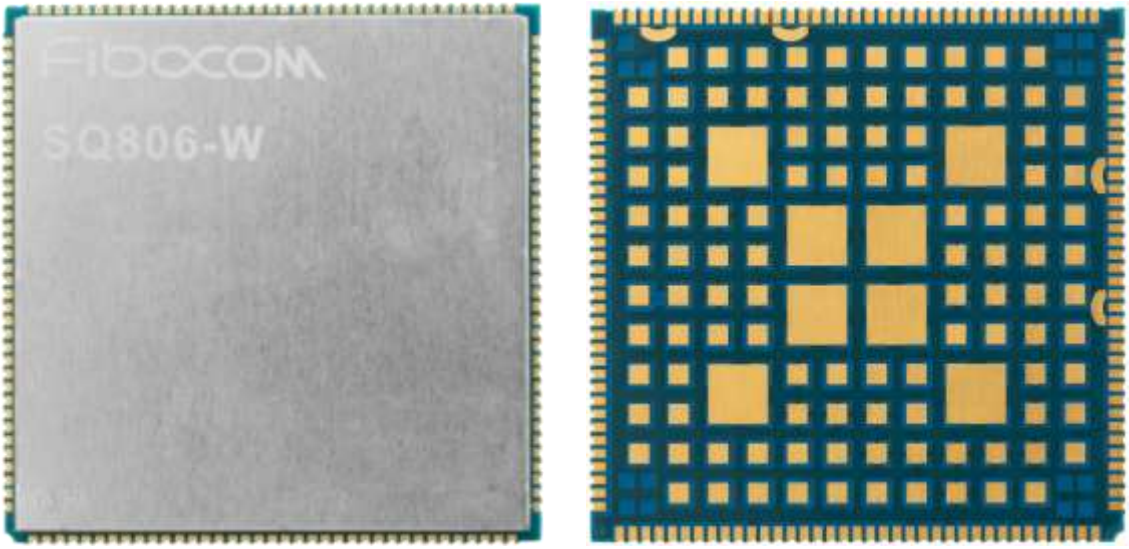

Figure 8-1 Module product appearance

8.2 Structural Dimension

The structural dimension of the module is shown in the following figure:

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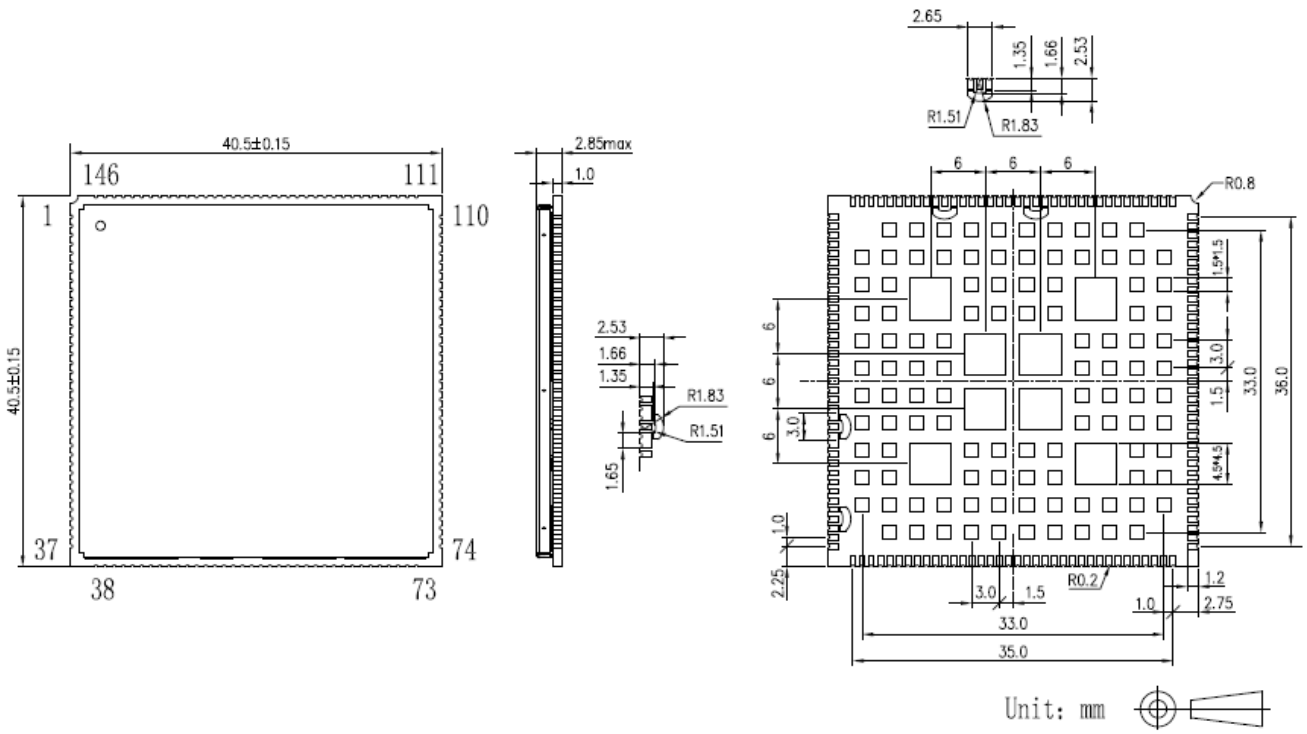

Figure 8-2 Structural dimension

8.3 Recommended PCB Soldering Pad Design

For PCB soldering pad and stencil design, please refer to *FIBOCOM SQ806 Series SMT Design Guide*.

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9 Production and Storage

9.1 SMT

For SMT production process parameters and related requirements, please refer to *FIBOCOM SQ806 Series SMT Design Guide*.

9.2 Package and Storage

For package and storage requirements, please refer to *FIBOCOM SQ806 Series SMT Design Guide*.

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A Acronyms

Table A-1 Acronyms

Acronyms	Definition
bps	Bits Per Second
LED	Light Emitting Diode
PCB	Printed Circuit Board
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RTC	Real Time Clock
Rx	Receive
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter

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10 CE Conformance information

The device could be used with a separation distance of 20cm to the human body.

Hereby, [Fibocom Wireless Inc.] declares that the radio equipment type [SQ806-W] is in compliance with Directive 2014/53/EU.

	AT	BE	BG	CH	CY	CZ	DE	DK
	EE	EL	ES	FI	FR	HR	HU	IE
	IS	IT	LI	LT	LU	LV	MT	NL
	NO	PL	PT	RO	SE	SI	SK	UK(NI)

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11 FCC Conformance information

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom Wireless Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID:ZMOSQ806W”

“Contains IC: 21374-SQ806W“

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

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Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90,part 96, part 15 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

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This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

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12 ISED Conformance information

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

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As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

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This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC:21374-SW806W”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 21374-SW806W".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

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